THE DATASHEET OF

SN74V3690-15PEU

www.win-source.net 0086-755-83957316

- **Choice of Memory Organizations**
  - **SN74V3640 – 1024 × 36 Bit**
  - **SN74V3650 – 2048 × 36 Bit**
  - **SN74V3660 – 4096 × 36 Bit**
  - **SN74V3670 – 8192 × 36 Bit**
  - **SN74V3680 – 16384 × 36 Bit**
  - **SN74V3690 – 32768 × 36 Bit**
- **166-MHz Operation (6-ns Read/Write Cycle Time)**
- **User-Selectable Input- and Output-Port Bus Sizing**
  - **×36 in to ×36 out**
  - **×36 in to ×18 out**
  - **×36 in to ×9 out**
  - **×18 in to ×36 out**
  - **×9 in to ×36 out**
- **Big-Endian/Little-Endian User-Selectable Byte Representation**
- **5-V-Tolerant Inputs**
- **Fixed, Low, First-Word Latency**
- **Zero-Latency Retransmit**
- **Master Reset Clears Entire FIFO**
- **Partial Reset Clears Data, But Retains Programmable Settings**
- **Empty, Full, and Half-Full Flags Signal FIFO Status**
- **Programmable Almost-Empty and Almost-Full Flags; Each Flag Can Default to One of Eight Preselected Offsets**
- **Selectable Synchronous/Asynchronous Timing Modes for Almost-Empty and Almost-Full Flags**
- **Program Programmable Flags by Either Serial or Parallel Means**
- **Select Standard Timing (Using $\overline{EF}$ and $\overline{FF}$ Flags) or First-Word Fall-Through (FWFT) Timing (Using $\overline{OR}$ and $\overline{IR}$ Flags)**
- **Output Enable Puts Data Outputs in High-Impedance State**
- **Easily Expandable in Depth and Width**
- **Independent Read and Write Clocks Permit Reading and Writing Simultaneously**
- **High-Performance Submicron CMOS Technology**
- **Available in 128-Pin Thin Quad Flat Pack (TQFP)**

description

The SN74V3640, SN74V3650, SN74V3660, SN74V3670, SN74V3680, and SN74V3690 are exceptionally deep, high-speed CMOS, first-in first-out (FIFO) memories, with clocked read and write controls and a flexible bus-matching ×36/×18/×9 data flow. These FIFOs offer several key user benefits:

- Flexible ×36/×18/×9 bus matching on both read and write ports
- The period required by the retransmit operation is fixed and short.
- The first-word data-latency period, from the time the first word is written to an empty FIFO to the time it can be read, is fixed and short.
- High-density offerings up to 1 Mbit

Bus-matching synchronous FIFOs are particularly appropriate for network, video, signal processing, telecommunications, data communications, and other applications that need to buffer large amounts of data and match buses of unequal sizes.

Each FIFO has a data input port (Dn) and a data output port (Qn), both of which can assume 36-bit, 18-bit, or 9-bit width, as determined by the state of external control pins' input width (IW), output width (OW), and bus matching (BM) during the master-reset cycle.

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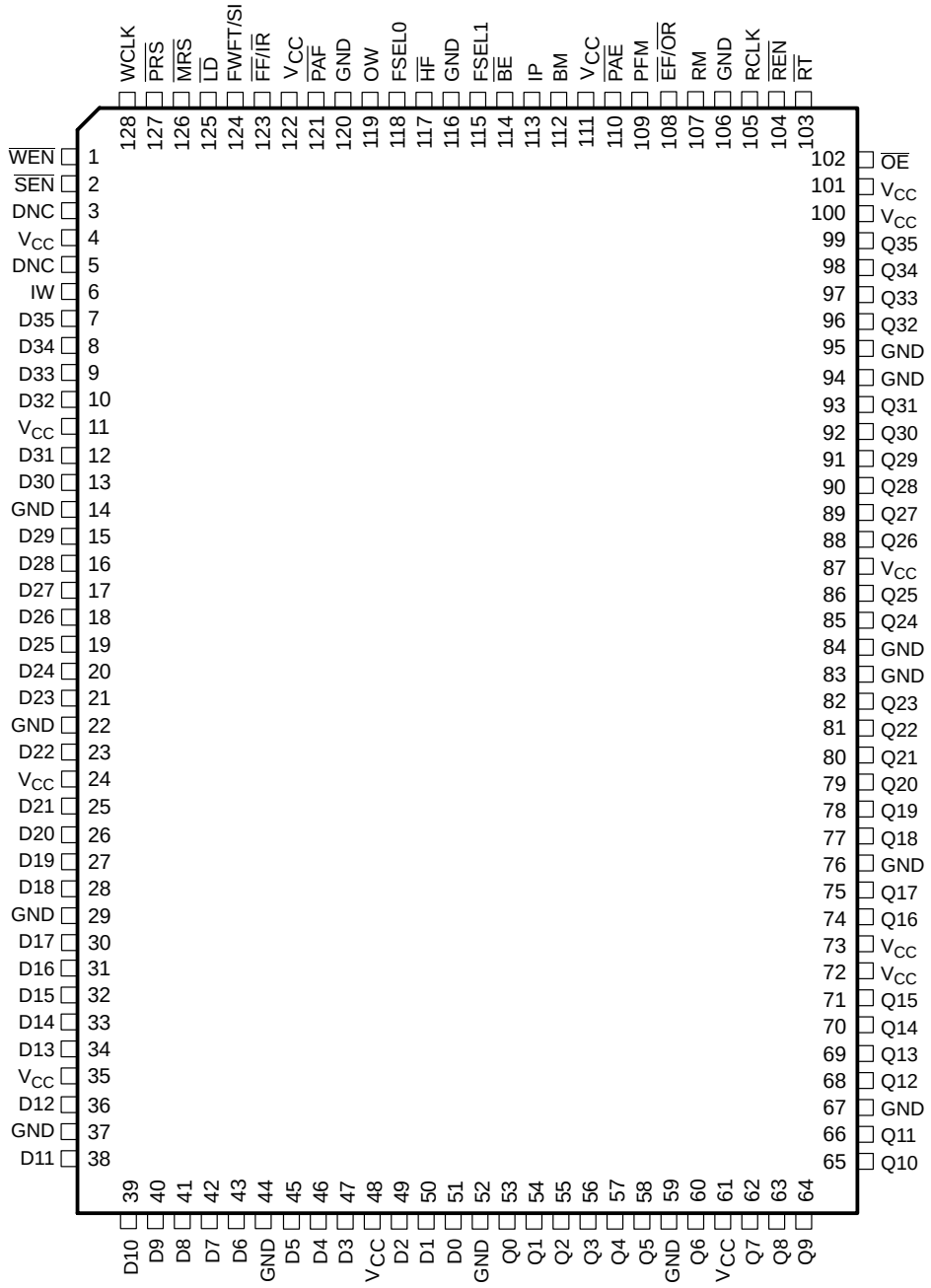
PEU PACKAGE
(TOP VIEW)

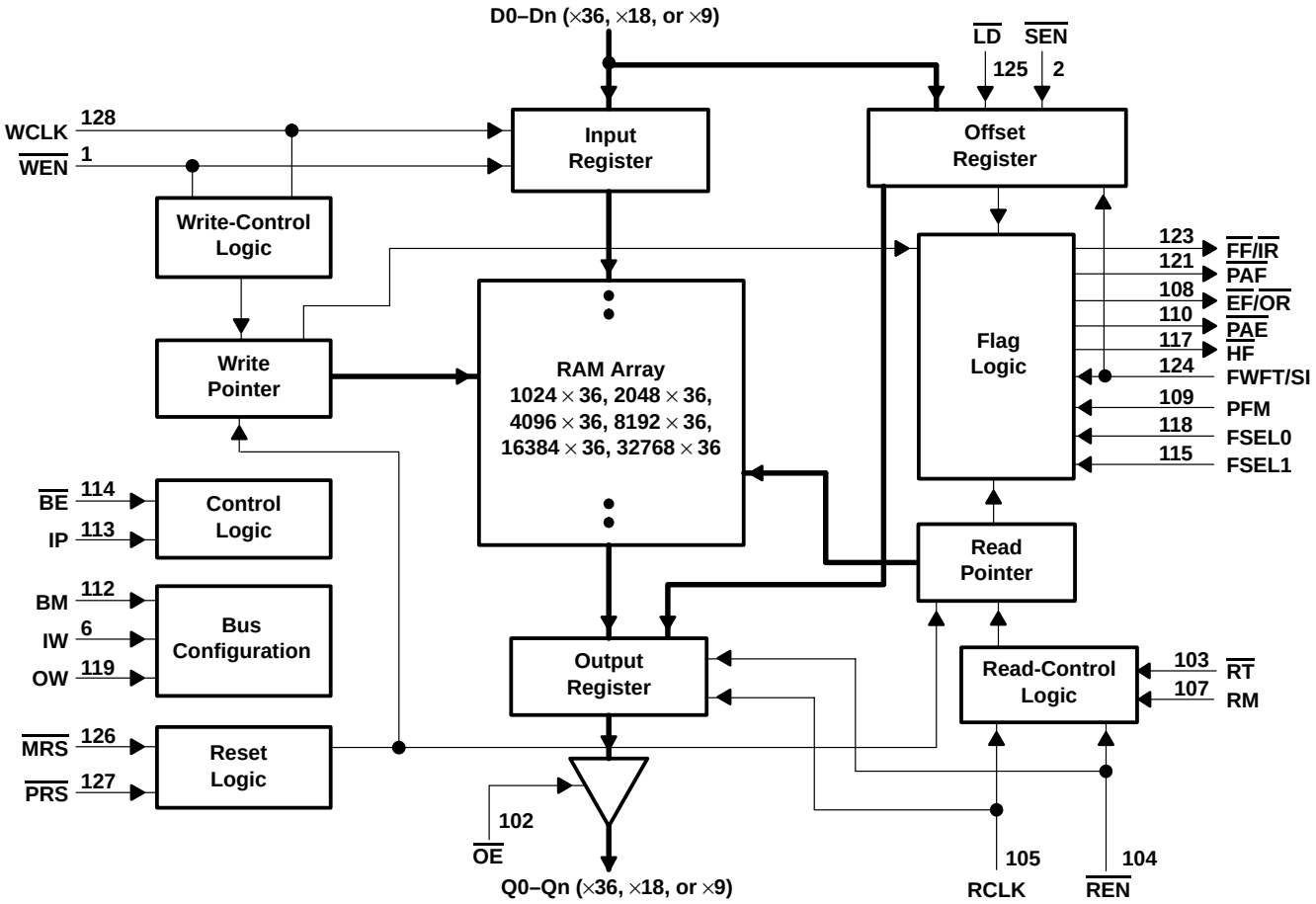


DNC = Do not connect

description (continued)

The input port is controlled by write-clock (WCLK) and write-enable ($\overline{\text{WEN}}$) inputs. Data is written into the FIFO on every rising edge of WCLK when $\overline{\text{WEN}}$ is asserted. The output port is controlled by read-clock (RCLK) and read-enable ($\overline{\text{REN}}$) inputs. Data is read from the FIFO on every rising edge of RCLK when $\overline{\text{REN}}$ is asserted. An output-enable ($\overline{\text{OE}}$) input is provided for 3-state control of the outputs.

functional block diagram



description (continued)

The frequencies of the RCLK and WCLK signals can vary from 0 to f_{MAX}, with complete independence. There are no restrictions on the frequency of one clock input with respect to the other.

There are two possible timing modes of operation with these devices: first-word fall-through (FWFT) mode and standard mode.

In FWFT mode, the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. $\overline{REN}$ need not be asserted for accessing the first word. However, subsequent words written to the FIFO do require a low on $\overline{REN}$ for access. The state of the FWFT/SI input during master reset determines the timing mode.

For applications requiring more data-storage capacity than a single FIFO can provide, the FWFT timing mode permits depth expansion by chaining FIFOs in series (i.e., the data outputs of one FIFO are connected to the corresponding data inputs of the next). No external logic is required.

In standard mode, the first word written to an empty FIFO does not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating $\overline{REN}$ and enabling a rising RCLK edge, shifts the word from internal memory to the data output lines.

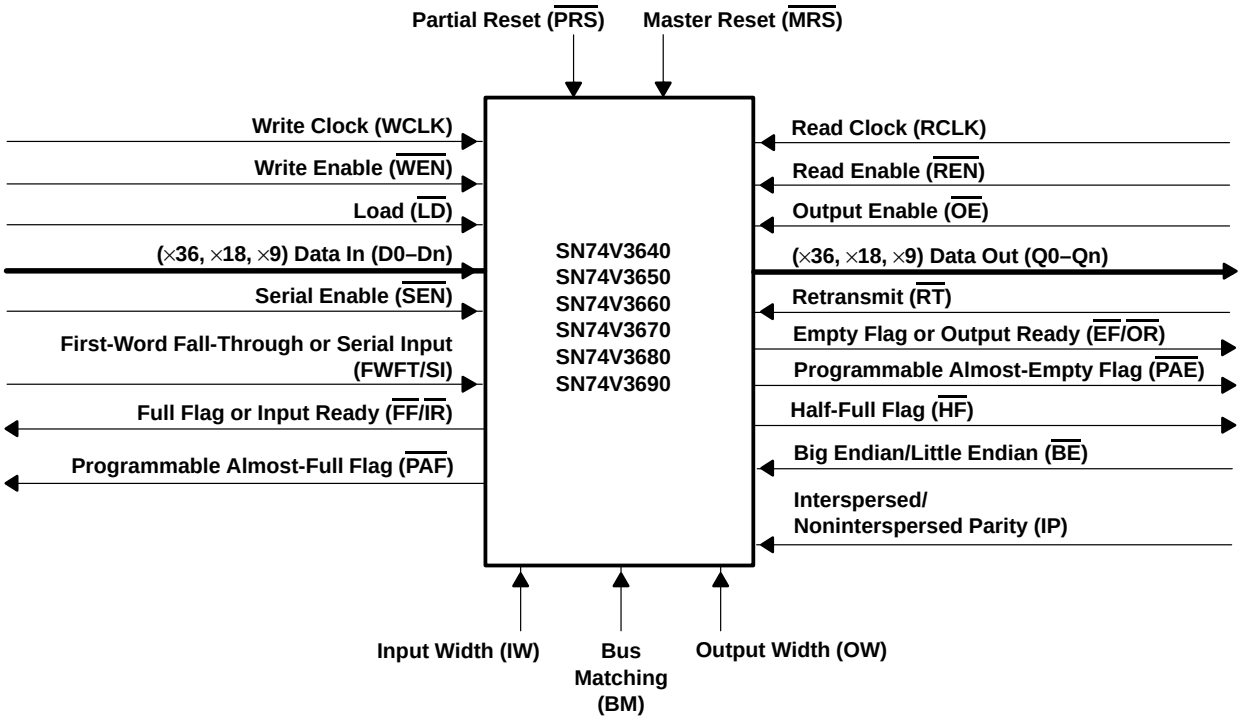


Figure 1. Single-Device-Configuration Signal Flow

description (continued)

These FIFOs have five flag pins: empty flag or output ready ($\overline{EF}$/$\overline{OR}$), full flag or input ready ($\overline{FF}$/$\overline{IR}$), half-full flag ($\overline{HF}$), programmable almost-empty flag ($\overline{PAE}$), and programmable almost-full flag ($\overline{PAF}$). The $\overline{EF}$ and $\overline{FF}$ functions are selected in standard mode. The $\overline{IR}$ and $\overline{OR}$ functions are selected in FWFT mode. $\overline{HF}$, $\overline{PAE}$, and $\overline{PAF}$ always are available for use, regardless of timing mode.

$\overline{PAE}$ and $\overline{PAF}$ can be programmed independently to switch at any point in memory. Programmable offsets determine the flag-switching threshold and can be loaded by parallel or serial methods. Eight default offset settings also are provided, so that $\overline{PAE}$ can be set to switch at a predefined number of locations from the empty boundary. The $\overline{PAF}$ threshold also can be set at similar predefined values from the full boundary. The default offset values are set during master reset by the state of the FSEL0, FSEL1, and $\overline{LD}$.

For serial programming, $\overline{SEN}$, together with $\overline{LD}$, loads the offset registers via the serial input (SI) on each rising edge of WCLK. For parallel programming, $\overline{WEN}$, together with $\overline{LD}$, loads the offset registers via Dn on each rising edge of WCLK. $\overline{REN}$, together with $\overline{LD}$, can read the offsets in parallel from Qn on each rising edge of RCLK, regardless of whether serial parallel offset loading has been selected.

During master reset ($\overline{MRS}$), the read and write pointers are set to the first location of the FIFO. The FWFT pin selects standard mode or FWFT mode.

Partial reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the timing mode, programmable-flag programming method, and default or programmed offset settings existing before partial reset remain unchanged. The flags are updated according to the timing mode and offsets in effect. $\overline{PRS}$ is useful for resetting a device in mid-operation, when reprogramming programmable flags would be undesirable.

Also, the timing modes of $\overline{PAE}$ and $\overline{PAF}$ outputs can be selected. Timing modes can be set as either asynchronous or synchronous for $\overline{PAE}$ and $\overline{PAF}$.

description (continued)

If the asynchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected, $\overline{PAE}$ is asserted low on the low-to-high transition of RCLK. $\overline{PAE}$ is reset to high on the low-to-high transition of WCLK. Similarly, $\overline{PAF}$ is asserted low on the low-to-high transition of WCLK, and $\overline{PAF}$ is reset to high on the low-to-high transition of RCLK.

If the synchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected , the $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only, and not WCLK. Similarly, $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only, and not RCLK. The mode desired is configured during master reset by the state of the programmable flag mode (PFM).

The retransmit function allows data to be reread from the FIFO more than once. A low on the retransmit ($\overline{RT}$) input during a rising RCLK edge initiates a retransmit operation by setting the read pointer to the first location of the memory array. Zero-latency retransmit timing mode can be selected using the retransmit timing mode (RM). During master reset, a low on RM selects zero-latency retransmit. A high on RM during master reset selects normal latency.

If zero-latency retransmit operation is selected, the first data word to be retransmitted is placed on the output register, with respect to the same RCLK edge that initiated the retransmit, if $\overline{RT}$ is low.

See Figures 11 and 12 for normal latency retransmit timing. See Figures 13 and 14 for zero-latency retransmit timing.

The devices can be configured with different input and output bus widths (see Table 1).

Table 1. Bus-Matching Configuration Modes†

BM	IW	OW	WRITE-PORT WIDTH	READ-PORT WIDTH
L	L	L	×36	×36
H	L	L	×36	×18
H	L	H	×36	×9
H	H	L	×18	×36
H	H	H	×9	×36

† Logic levels during master reset

A big-endian/little-endian data word format is provided. This function is useful when data is written into the FIFO in long-word (×36/×18) format and read out of the FIFO in small-word (×18/×9) format. If big-endian mode is selected, the most-significant byte (MSB) (word) of the long word written into the FIFO is read out of the FIFO first, followed by the least-significant byte (LSB). If little-endian format is selected, the LSB of the long word written into the FIFO is read out first, followed by the MSB. The mode desired is configured during master reset by the state of the big-endian/little-endian ($\overline{BE}$) pin (see Figure 4 for the bus-matching byte arrangement).

The interspersed/noninterspersed parity (IP) bit function allows the user to select the parity bit in the word loaded into the parallel port (D0–Dn) when programming the flag offsets. If interspersed-parity mode is selected, the FIFO assumes that the parity bit is located in bit positions D8, D17, D26, and D35 during the parallel programming of the flag offsets. If noninterspersed-parity mode is selected, D8, D17, and D26 are assumed to be valid bits, and D32, D33, D34, and D35 are ignored. Interspersed parity mode is selected during master reset by the state of the IP input. Interspersed parity control has an effect only during parallel programming of the offset registers. It does not affect data written to and read from the FIFO.

The SN74V3640, SN74V3650, SN74V3660, SN74V3670, SN74V3680, and SN74V3690 are fabricated using high-speed submicron CMOS technology, and are characterized for operation from 0°C to 70°C.

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
$\overline{BE}$†	I	Big endian/little endian. During master reset, a low on $\overline{BE}$ selects big-endian operation. A high on $\overline{BE}$ during master reset selects little-endian format.
BM†	I	Bus matching. BM works with IW and OW to select the bus sizes for both write and read ports (see Table 1 for bus-size configuration).
D0–D36	I	Data inputs. Data inputs for a 36-, 18-, or 9-bit bus. When in 18- or 9-bit mode, the unused input pins are in a don't-care state.
$\overline{EF}$/$\overline{OR}$	O	Empty flag/output ready. In standard mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether the FIFO memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether there is valid data available at the outputs.
$\overline{FF}$/$\overline{IR}$	O	Full flag/input ready. In standard mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether the FIFO memory is full. In FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether there is space available for writing to the FIFO memory.
FSEL0†	I	Flag-select bit 0. During master reset, FSEL0, along with FSEL1 and $\overline{LD}$, selects the default offset values for $\overline{PAE}$ and $\overline{PAF}$. Up to eight possible settings are available.
FSEL1†	I	Flag-select bit 1. During master reset, FSEL1, along with FSEL0 and $\overline{LD}$, selects the default offset values for $\overline{PAE}$ and $\overline{PAF}$. Up to eight possible settings are available.
FWFT/SI	I	First-word fall-through/serial in. During master reset, FWFT/SI selects FWFT or standard mode. After master reset, FWFT/SI functions as a serial input for loading offset registers.
$\overline{HF}$	O	Half-full flag. $\overline{HF}$ indicates whether the FIFO memory is more or less than half full.
IP†	I	Interspersed parity. During master reset, a low on IP selects noninterspersed-parity mode. A high selects interspersed-parity mode. Interspersed-parity control has an effect only during parallel programming of the offset registers. It does not effect data written to and read from the FIFO.
IW†	I	Input width. IW, along with OW and BM, selects the bus width of the write port (see Table 1 for bus-size configuration).
$\overline{LD}$	I	Load. This is a dual-purpose pin. During master reset, the state of $\overline{LD}$, along with FSEL0 and FSEL1, determines one of eight default offset values for $\overline{PAE}$ and $\overline{PAF}$, along with the method by which these offset registers can be programmed, parallel or serial (see Table 2). After master reset, $\overline{LD}$ enables writing to and reading from the offset registers.
$\overline{MRS}$	I	Master reset. $\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During master reset, the FIFO is configured for either FWFT or standard mode, bus-matching configurations, one of eight programmable-flag default settings, serial or parallel programming of the offset settings, big-endian/little-endian format, zero-latency timing mode, interspersed parity, and synchronous versus asynchronous programmable-flag timing modes.
$\overline{OE}$	I	Output enable. $\overline{OE}$ controls the output impedance of Qn.
OW†	I	Output width. OW, along with IW and BM, selects the bus width of the read port (see Table 1 for bus-size configuration).
$\overline{PAE}$	O	Programmable almost-empty flag. $\overline{PAE}$ goes low if the number of words in the FIFO memory is less than offset n, which is stored in the empty offset register. $\overline{PAE}$ goes high if the number of words in the FIFO memory is greater than, or equal to, offset n.
$\overline{PAF}$	O	Programmable almost-full flag. $\overline{PAF}$ goes high if the number of free locations in the FIFO memory is more than offset m, which is stored in the full offset register. $\overline{PAF}$ goes low if the number of free locations in the FIFO memory is less than, or equal to, m.
PFM†	I	Programmable-flag mode. During master reset, a low on PFM selects asynchronous programmable-flag timing mode. A high on PFM selects synchronous programmable-flag timing mode.
$\overline{PRS}$	I	Partial reset. $\overline{PRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During partial reset, the existing mode (standard or FWFT), programming method (serial or parallel), and programmable-flag settings are all retained.
Q0–Q35	O	Data outputs. Data outputs for a 36-, 18-, or 9-bit bus. When in 18- or 9-bit mode, the unused output pins are in a don't-care state. Outputs are not 5-V tolerant, regardless of the state of $\overline{OE}$.
RCLK	I	Read clock. When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers.

† Inputs should not change state after master reset.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
$\overline{REN}$	I	Read enable. $\overline{REN}$ enables RCLK for reading data from the FIFO memory and offset registers.
RM†	I	Retransmit latency mode. During master reset, a low on RM selects zero-latency retransmit timing mode. A high on RM selects normal-latency mode.
$\overline{RT}$	I	Retransmit. $\overline{RT}$ asserted on the rising edge of RCLK initializes the READ pointer to zero, sets the $\overline{EF}$ flag to low ($\overline{OR}$ to high in FWFT mode) and does not disturb the write pointer, programming method, existing timing mode, or programmable-flag settings. $\overline{RT}$ is useful to reread data from the first physical location of the FIFO.
$\overline{SEN}$	I	Serial enable. $\overline{SEN}$ enables serial loading of programmable flag offsets.
WCLK	I	Write clock. When enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO and offsets into the programmable registers for parallel programming and, when enabled by $\overline{SEN}$, the rising edge of WCLK writes one bit of data into the programmable register for serial programming.
$\overline{WEN}$	I	Write enable. $\overline{WEN}$ enables WCLK for writing data into the FIFO memory and offset registers.

† Inputs should not change state after master reset.

detailed description

inputs

data in (D0–Dn)

D0–D35 are data inputs for 36-bit-wide data. D0–D17 are data inputs for 18-bit-wide data. D0–D8 are data inputs for 9-bit-wide data.

controls

master reset ($\overline{MRS}$)

A master reset is accomplished when $\overline{MRS}$ is taken low. This operation sets the internal read and write pointers to the first location of the RAM array. $\overline{PAE}$ goes low, $\overline{PAF}$ goes high, and $\overline{HF}$ goes high.

If FWFT/SI is low during master reset, the standard mode, $\overline{EF}$, and $\overline{FF}$ are selected. $\overline{EF}$ goes low and $\overline{FF}$ goes high. If FWFT/SI is high, the FWFT mode, $\overline{IR}$, and $\overline{OR}$ are selected. $\overline{OR}$ goes high and $\overline{IR}$ goes low.

All control settings, such as OW, IW, BM, $\overline{BE}$, RM, PFM, and IP are defined during the master reset cycle.

During a master reset, the output register is initialized to all zeroes. A master reset is required after power up, before a write operation can take place. $\overline{MRS}$ is asynchronous.

See Figure 5 for timing information.

partial reset ($\overline{PRS}$)

A partial reset is accomplished when the $\overline{PRS}$ input is taken to a low state. As in the case of the master reset, the internal read and write pointers are set to the first location of the RAM array, $\overline{PAE}$ goes low, $\overline{PAF}$ goes high, and $\overline{HF}$ goes high.

Whichever mode is active at the time of partial reset remains selected (standard or FWFT mode). If standard mode is active, $\overline{FF}$ goes high and $\overline{EF}$ goes low. If the FWFT mode is active, $\overline{OR}$ goes high and $\overline{IR}$ goes low.

Following partial reset, all values held in the offset registers remain unchanged. The programming method (parallel or serial) active at the time of partial reset also is retained. The output register is initialized to all zeroes. $\overline{PRS}$ is asynchronous.

A partial reset is useful for resetting the device during operation when reprogramming programmable-flag offsets might not be convenient.

See Figure 6 for timing information.

retransmit ($\overline{RT}$)

The retransmit operation allows previously read data to be accessed again. There are two modes of retransmit operation: normal latency and zero latency. There are two stages to retransmit. The first stage is a setup procedure that resets the read pointer to the first location of memory. The second stage is the actual retransmit, which consists of reading out the memory contents, starting at the beginning of the memory.

Retransmit setup is initiated by holding $\overline{RT}$ low during a rising RCLK edge. $\overline{REN}$ and $\overline{WEN}$ must be high before bringing $\overline{RT}$ low. When zero latency is utilized, $\overline{REN}$ need not be high before bringing $\overline{RT}$ low.

If standard mode is selected, the FIFO marks the beginning of the retransmit setup by setting $\overline{EF}$ low. The change in level is noticeable only if $\overline{EF}$ was high before setup. During this period, the internal read pointer is initialized to the first location of the RAM array.

When $\overline{EF}$ goes high, retransmit setup is complete and read operations can begin, starting with the first location in memory. Because standard mode is selected, every word read, including the first word following retransmit setup, requires a low on $\overline{REN}$ to enable the rising edge of RCLK.

See Figure 11 for timing information.

If FWFT mode is selected, the FIFO marks the beginning of the retransmit setup by setting $\overline{OR}$ high. During this period, the internal read pointer is set to the first location of the RAM array.

When $\overline{OR}$ goes low, retransmit setup is complete. At the same time, the contents of the first location appear on the outputs. Because FWFT mode is selected, the first word appears on the outputs and no low on $\overline{REN}$ is necessary. Reading all subsequent words requires a low on $\overline{REN}$ to enable the rising edge of RCLK.

See Figure 12 for timing information.

In retransmit operation, zero-latency mode can be selected using the retransmit latency mode (RM) pin during a master reset. This can be applied to the standard mode and the FWFT mode.

first-word fall-through/serial in (FWFT/SI)

FWFT/SI is a dual-purpose pin. During master reset, the state of the FWFT/SI input determines whether the device operates in standard or FWFT mode.

If, at the time of master reset, FWFT/SI is low, standard mode is selected. This mode uses $\overline{EF}$ to indicate whether any words are present in the FIFO memory. It also uses $\overline{FF}$ to indicate whether the FIFO memory has free space for writing. In standard mode, every word read from the FIFO, including the first, must be requested using $\overline{REN}$ and RCLK.

If, at the time of master reset, FWFT/SI is high, FWFT mode is selected. This mode uses $\overline{OR}$ to indicate whether there is valid data at the data outputs (Qn). It also uses $\overline{IR}$ to indicate whether the FIFO memory has free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Qn after three RCLK rising edges, therefore, $\overline{REN}$ = low is not necessary. Subsequent words must be accessed using $\overline{REN}$ and RCLK.

After master reset, FWFT/SI acts as a serial input for loading $\overline{PAE}$ and $\overline{PAF}$ offsets into the programmable registers. The serial input function can be used only when the serial loading method is selected during master reset. Serial programming using the FWFT/SI pin functions the same way in both standard and FWFT modes.

write clock (WCLK)

A write cycle is initiated on the rising edge of the WCLK input. Data setup and hold times must be met, with respect to the low-to-high transition of the WCLK. It is permissible to stop WCLK. Note that while WCLK is idle, the $\overline{FF}$/$\overline{IR}$, $\overline{PAF}$, and $\overline{HF}$ flags are not updated. WCLK is capable only of updating $\overline{HF}$ flag to low. The write and read clocks can be independent or coincident.

write enable ($\overline{WEN}$)

When $\overline{WEN}$ is low, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When $\overline{WEN}$ is high, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow in the standard mode, $\overline{FF}$ goes low, inhibiting further write operations. After completion of a valid read cycle, $\overline{FF}$ goes high, allowing a write to occur. $\overline{FF}$ is updated by two WCLK cycles + t_{sk} after the RCLK cycle.

To prevent data overflow in the FWFT mode, $\overline{IR}$ goes high, inhibiting further write operations. After completion of a valid read cycle, $\overline{IR}$ goes low, allowing a write to occur. The $\overline{IR}$ flag is updated by two WCLK cycles + t_{sk} after the valid RCLK cycle.

$\overline{WEN}$ is ignored when the FIFO is full in either FWFT or standard mode.

read clock (RCLK)

A read cycle is initiated on the rising edge of the RCLK input. Data can be read on the outputs, on the rising edge of the RCLK input. It is permissible to stop RCLK. While RCLK is idle, the $\overline{EF}$/$\overline{OR}$, $\overline{PAE}$, and $\overline{HF}$ flags are not updated. RCLK is capable only of updating the $\overline{HF}$ flag to high. The write and read clocks can be independent or coincident.

read enable ($\overline{REN}$)

When $\overline{REN}$ is low, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle, if the device is not empty.

When $\overline{REN}$ is high, the output register holds the previous data and no new data is loaded into the output register. The data outputs Q0–Qn maintain the previous data value.

In standard mode, every word accessed at Qn, including the first word written to an empty FIFO, must be requested using $\overline{REN}$. When the last word has been read from the FIFO, the empty flag ($\overline{EF}$) goes low, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}$ goes high, allowing a read to occur. The $\overline{EF}$ flag is updated by two RCLK cycles + t_{sk} after the valid WCLK cycle.

In FWFT mode, the first word written to an empty FIFO automatically goes to the outputs Qn, on the third valid low-to-high transition of RCLK + t_{sk} after the first write. $\overline{REN}$ need not be asserted low. In order to access all other words, a read must be executed using $\overline{REN}$. The RCLK low-to-high transition after the last word has been read from the FIFO and $\overline{OR}$ goes high with a true read (RCLK with $\overline{REN}$ = low), inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

serial enable ($\overline{SEN}$)

The $\overline{SEN}$ input is an enable used only for serial programming of the offset registers. The serial programming method must be selected during master reset. $\overline{SEN}$ always is used with $\overline{LD}$. When these lines are both low, data at the SI input can be loaded into the program register, with one bit for each low-to-high transition of WCLK.

When $\overline{SEN}$ is high, the programmable registers retain the previous settings and no offsets are loaded. $\overline{SEN}$ functions the same way in standard and FWFT modes.

output enable ($\overline{OE}$)

When output enable is asserted (low), the parallel output buffers receive data from the output register. When $\overline{OE}$ is high, the output data bus (Qn) goes into the high-impedance state.

load ($\overline{LD}$)

$\overline{LD}$ is a dual-purpose pin. During master reset, the state of the $\overline{LD}$ input, along with FSEL0 and FSEL1, determines one of eight default offset values for the $\overline{PAE}$ and $\overline{PAF}$ flags, along with the method by which these offset registers can be programmed, parallel or serial (see Table 2). After master reset, $\overline{LD}$ enables write operations to, and read operations from, the offset registers. Only the offset loading method currently selected can be used to write to the registers. Offset registers can be read only in parallel.

After master reset, $\overline{LD}$ activates the programming process of the flag offset values $\overline{PAE}$ and $\overline{PAF}$. Pulling $\overline{LD}$ low begins a serial loading, or a parallel load, or a read of these offset values.

bus matching (BM, IW, OW)

BM, IW, and OW define the input and output bus widths. During master reset, the state of these pins is used to configure the device bus sizes (see Table 1 for control settings). All flags operate on the word/byte-size boundary, as defined by the selection of bus width (see Figure 4 for the bus-matching byte arrangement).

big endian/little endian ($\overline{BE}$)

During master reset, a low on $\overline{BE}$ selects big-endian operation. A high on $\overline{BE}$ during master reset selects little-endian format. This function is useful when the following input-to-output bus widths are implemented: ×36 to ×18, ×36 to ×9, ×18 to ×36, and ×9 to ×36. If big-endian mode is selected, the MSB (word) of the long word written into the FIFO is read out of the FIFO first, followed by the LSB. If little-endian format is selected, the LSB of the long word written into the FIFO is read out first, followed by the MSB. The desired mode is configured during master reset by the state of $\overline{BE}$ (see Figure 4 for bus-matching byte arrangement).

programmable-flag mode (PFM)

During master reset, a low on PFM selects asynchronous programmable-flag timing mode. A high on PFM selects synchronous programmable-flag timing mode. If asynchronous $\overline{PAF}$/$\overline{PAE}$ configuration is selected (PFM low during $\overline{MRS}$), $\overline{PAE}$ is asserted low on the low-to-high transition of RCLK. $\overline{PAE}$ is reset to high on the low-to-high transition of WCLK. Similarly, $\overline{PAF}$ is asserted low on the low-to-high transition of WCLK, and $\overline{PAF}$ is reset to high on the low-to-high transition of RCLK.

If synchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected (PFM high during $\overline{MRS}$), $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only, and not WCLK. Similarly, $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during master reset by the state of the PFM.

interspersed parity (IP)

During master reset, a low on IP selects noninterspersed-parity mode. A high selects interspersed-parity mode. The IP bit function allows the user to select the parity bit in the word loaded into the parallel port (D0–Dn) when programming the flag offsets. If interspersed-parity mode is selected, the FIFO assumes that the parity bits are located in bit positions D8, D17, D26, and D35 during the parallel programming of the flag offsets. If noninterspersed-parity mode is selected, D8, D17, and D28 are assumed to be valid bits and D32, D33, D34, and D35 are ignored. IP mode is selected during master reset by the state of the IP input pin. Interspersed-parity control has an effect only during parallel programming of the offset registers. It does not affect the data written to, and read from, the FIFO.

outputs

full flag/input ready ($\overline{FF}$/$\overline{IR}$)

$\overline{FF}$/$\overline{IR}$ is a dual-purpose pin. In standard mode, the $\overline{FF}$ function is selected. When the FIFO is full, $\overline{FF}$ goes low, inhibiting further write operations. When $\overline{FF}$ is high, the FIFO is not full. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{FF}$ goes low after D writes to the FIFO (D = 1024 for the SN74V3640, D = 2048 for the SN74V3650, D = 4096 for the SN74V3660, D = 8192 for the SN74V3670, D = 16384 for the SN74V3680, and D = 32768 for the SN74V3690).

See Figure 7 for timing information.

In FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ goes low when memory space is available for writing in data. When there is no longer any free space left, $\overline{IR}$ goes high, inhibiting further write operations. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{IR}$ goes high after D writes to the FIFO (D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 4097 for the SN74V3660, D = 8193 for the SN74V3670, D = 16385 for the SN74V3680, and D = 32769 for the SN74V3690).

See Figure 9 for timing information.

The $\overline{IR}$ status not only measures the contents of the FIFO memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to deassert $\overline{IR}$ is one greater than needed to assert $\overline{FF}$ in standard mode.

$\overline{FF}$/$\overline{IR}$ is synchronous and updated on the rising edge of WCLK. $\overline{FF}$/$\overline{IR}$ are double register-buffered outputs.

empty flag/output ready ($\overline{EF}$/$\overline{OR}$)

$\overline{EF}$/$\overline{OR}$ is a dual-purpose pin. In the standard mode, the $\overline{EF}$ function is selected. When the FIFO is empty, $\overline{EF}$ goes low, inhibiting further read operations. When $\overline{EF}$ is high, the FIFO is not empty.

See Figure 8 for timing information.

In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ goes low at the same time the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}$ stays low after the RCLK low-to-high transition that shifts the last word from the FIFO memory to the outputs. $\overline{OR}$ goes high only with a true read (RCLK with $\overline{REN}$ = low). The previous data stays at the outputs, indicating the last word was read. Further data reads are inhibited until $\overline{OR}$ goes low again.

See Figure 10 for timing information.

$\overline{EF}$/$\overline{OR}$ is synchronous and updated on the rising edge of RCLK.

In standard mode, $\overline{EF}$ is a double register-buffered output. In FWFT mode, $\overline{OR}$ is a triple register-buffered output.

programmable almost-full flag ($\overline{PAF}$)

$\overline{PAF}$ goes low when the FIFO reaches the almost-full condition. In standard mode, if no reads are performed after reset ($\overline{MRS}$), $\overline{PAF}$ goes low after (D – m) words are written to the FIFO. The $\overline{PAF}$ goes low after (1024 – m) writes for the SN74V3640, (2048 – m) writes for the SN74V3650, (4096 – m) writes for the SN74V3660, (8192 – m) writes for the SN74V3670, (16384 – m) writes for the SN74V3680, and (32768 – m) writes for the SN74V3690. The offset m is the full offset value. The default setting for this value is shown in Table 2.

In FWFT mode, $\overline{PAF}$ goes low after (1025 – m) writes for the SN74V3640, (2049 – m) writes for the SN74V3650, (4097 – m) writes for the SN74V3660, (8193 – m) writes for the SN74V3670, (16385 – m) writes for the SN74V3680, and (32769 – m) writes for the SN74V3690. The offset m is the full offset value. The default setting for this value is shown in Table 2.

See Figure 18 for timing information.

If the asynchronous $\overline{PAF}$ configuration is selected, $\overline{PAF}$ is asserted low on the low-to-high transition of WCLK. $\overline{PAF}$ is reset to high on the low-to-high transition of RCLK. If the synchronous $\overline{PAF}$ configuration is selected, $\overline{PAF}$ is updated on the rising edge of WCLK.

See Figure 20 for timing information.

programmable almost-empty flag ($\overline{PAE}$)

$\overline{PAE}$ goes low when the FIFO reaches the almost-empty condition. In standard mode, $\overline{PAE}$ goes low when there are n words, or fewer, in the FIFO. The offset n is the empty offset value. The default setting for this value is shown in Table 2.

In FWFT mode, $\overline{PAE}$ goes low when there are n + 1 words, or fewer, in the FIFO. The default setting for this value is shown in Table 2.

See Figure 19 for timing information.

If the asynchronous $\overline{PAE}$ configuration is selected, $\overline{PAE}$ is asserted low on the low-to-high transition of RCLK. $\overline{PAE}$ is reset to high on the low-to-high transition of WCLK. If the synchronous $\overline{PAE}$ configuration is selected, $\overline{PAE}$ is updated on the rising edge of RCLK.

See Figure 21 for timing information.

half-full flag ($\overline{HF}$)

$\overline{HF}$ indicates a half-full FIFO. The rising WCLK edge that fills the FIFO beyond half-full sets $\overline{HF}$ low. The flag remains low until the difference between the write and read pointers becomes less than, or equal to, one-half of the total depth of the device. The rising RCLK edge that accomplishes this condition sets $\overline{HF}$ high.

In standard mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ goes low after (D/2 + 1) writes to the FIFO, where D = 1024 for the SN74V3640, D = 2048 for the SN74V3650, D = 4096 for the SN74V3660, D = 8192 for the SN74V3670, D = 16384 for the SN74V3680, and D = 32768 for the SN74V3690.

In FWFT mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ goes low after [(D – 1)/2] + 2 writes to the FIFO, where D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 4097 for the SN74V3660, D = 8193 for the SN74V3670, D = 16385 for the SN74V3680, and D = 32769 for the SN74V3690.

See Figure 22 for timing information. Because $\overline{HF}$ is updated by both RCLK WCLK, it is considered asynchronous.

data outputs (Q0-Qn)

Q0–Q35 are data outputs for 36-bit-wide data. Q0–Q17 are data outputs for 18-bit-wide data. Q0–Q8 are data outputs for 9-bit-wide data.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.5 V
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Storage temperature range, T_{stg} . . . . . –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	3.15	3.3	3.45	V
GND	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage (see Note 2)	2		5.5	V
V_{IL}	Low-level input voltage (see Note 3)			0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. V_{CC} = 3.3 V ± 0.15 V, JEDEC JESD8-A compliant
2. Outputs are not 5-V tolerant.
3. 1.5-V undershoots are allowed for 10 ns once per cycle.

electrical characteristics over recommended operating conditions, t_{CLK} = 6 ns, 7.5 ns, 10 ns, and 15 ns (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –2 mA	2.4			V
V_{OL}	I_{OL} = 8 mA			0.4	V
I_I	V_I = V_{CC} to 0.4 V			±1	µA
I_{OZ}	$\overline{OE} \geq V_{IH}$, V_O = V_{CC} to 0.4 V			±10	µA
I_{CC1}	See Notes 4, 5, and 6			40	mA
I_{CC2}	See Notes 4 and 7			15	mA
C_{IN}	V_I = 0, T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	V_O = 0, T_A = 25°C, f = 1 MHz, Output deselected ($\overline{OE} \geq V_{IH}$)			10	pF

NOTES: 4. Tested with outputs open (I_{OUT} = 0)
5. RCLK and WCLK switch at 20 MHz and data inputs switch at 10 MHz.
6. Typical $I_{CC1} = 4.2 + 1.4 \times f_S + 0.02 \times C_L \times f_S$ (in mA), with V_{CC} = 3.3 V, T_A = 25°C, f_S = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at $f_S/2$, C_L = capacitive load (in pF)
7. All inputs = (V_{CC} – 0.2 V) or (GND + 0.2 V), except RCLK and WCLK, T_A = 25°C, which switch at 20 MHz.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 2 through Figure 22)†

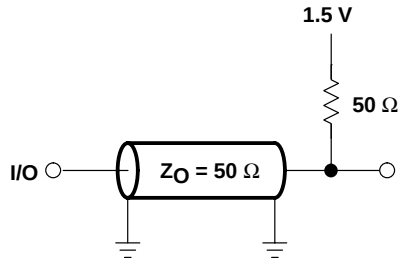
		SN74V3640-6 SN74V3650-6 SN74V3660-6 SN74V3670-6 SN74V3680-6 SN74V3690-6		SN74V3640-7 SN74V3650-7 SN74V3660-7 SN74V3670-7 SN74V3680-7 SN74V3690-7		SN74V3640-10 SN74V3650-10 SN74V3660-10 SN74V3670-10 SN74V3680-10 SN74V3690-10		SN74V3640-15 SN74V3650-15 SN74V3660-15 SN74V3670-15 SN74V3680-15 SN74V3690-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock cycle frequency		166		133.3		100		66.7	MHz
t_A	Data access time	2	4.5	2	5	2	6.5	2	10	ns
t_{CLK}	Clock cycle time	6		7.5		10		15		ns
t_{CLKH}	Clock high time	2.5		3.5		4.5		6		ns
t_{CLKL}	Clock low time	2.5		3.5		4.5		6		ns
t_{DS}	Data setup time	1.5		2.5		3.5		4		ns
t_{DH}	Data hold time	0.5		0.5		0.5		1		ns
t_{ENS}	Enable setup time	1.5		2.5		3.5		4		ns
t_{ENH}	Enable hold time	0.5		0.5		0.5		1		ns
t_{LDS}	Load setup time	2		3.5		3.5		4		ns
t_{LDH}	Load hold time	0		0.5		0.5		1		ns
t_{RS}	Reset pulse duration‡	10		10		10		15		ns
t_{RSS}	Reset setup time	15		15		15		15		ns
t_{RSR}	Reset recovery time	10		10		10		15		ns
t_{RSF}	Reset to flag and output time		15		15		15		15	ns
t_{RTS}	Retransmit setup time	2		3.5		3.5		4		ns
t_{OLZ}	Output enable to output in low impedance	0		0		0		0		ns
t_{OE}	Output enable to output valid	2	4.5	2	6	2	6	2	8	ns
t_{OHZ}	Output enable to output in high impedance	2	4.5	2	6	2	6	2	8	ns
t_{WFF}	Write clock to $\overline{FF}$ or $\overline{IR}$		4.5		5		6.5		10	ns
t_{REF}	Read clock to $\overline{EF}$ or $\overline{OR}$		4.5		5		6.5		10	ns
t_{PAFA}	Clock to asynchronous $\overline{PAF}$		8.5		12.5		16		20	ns
t_{PAFS}	Write clock to synchronous $\overline{PAF}$		4.5		5		6.5		10	ns
t_{PAEA}	Clock to asynchronous $\overline{PAE}$		8.5		12.5		16		20	ns
t_{PAES}	Read clock to synchronous $\overline{PAE}$		4.5		5		6.5		10	ns
t_{HF}	Clock to $\overline{HF}$		9		12.5		16		20	ns
t_{sk1}	Skew time between read clock and write clock for $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$	4.5		5		7		9		ns
t_{sk2}	Skew time between read clock and write clock for $\overline{PAE}$ and $\overline{PAF}$	4.5		7		10		14		ns

† All ac timings apply to standard mode and FWFT mode.
‡ Pulse durations less than minimum values are not allowed.

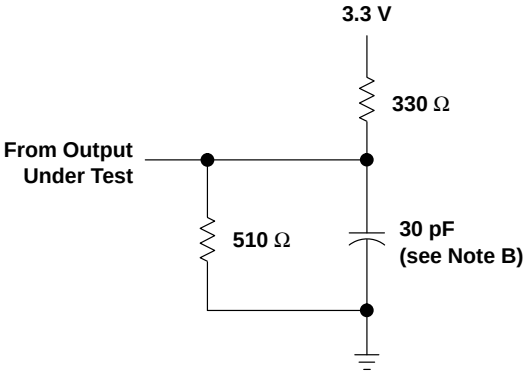
PARAMETER MEASUREMENT INFORMATION

AC TEST CONDITIONS

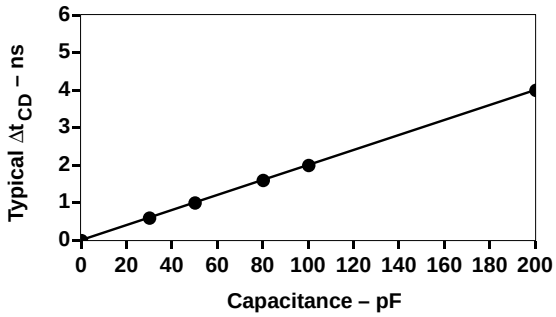
Input Pulse Levels	GND to 3.0 V
Input Rise/Fall Times	3 ns (see Note A)
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load for t_{CLK} = 10 ns, 15 ns	See B
Output Load for t_{CLK} = 6 ns, 7.5 ns	See A and C



A. AC TEST LOAD
FOR 6-ns AND 7.5-ns SPEED GRADES



B. OUTPUT LOAD CIRCUIT
FOR 10-ns AND 15-ns SPEED GRADES



C. LUMPED CAPACITIVE LOAD, TYPICAL DERATING

NOTES: A. For 133-MHz operation, input rise/fall times are 1.5 ns.
B. Includes probe and jig capacitance

Figure 2. Load Circuits

functional description

timing modes: FWFT mode vs standard mode

The SN74V3640, SN74V3650, SN74V3660, SN74V3670, SN74V3680, and SN74V3690 support two different timing modes of operation: standard mode or FWFT mode. The mode is selected during master reset by the state of the FWFT/SI input.

If, at the time of master reset, FWFT/SI is low, standard mode is selected. This mode uses $\overline{EF}$ to indicate whether any words are present in the FIFO. It also uses $\overline{FF}$ to indicate whether the FIFO has any free space for writing. In standard mode, every word read from the FIFO, including the first word, must be requested using $\overline{REN}$ and RCLK.

If, at the time of master reset, FWFT/SI is high, FWFT mode is selected. This mode uses $\overline{OR}$ to indicate whether valid data is at the data outputs (Qn). It also uses $\overline{IR}$ to indicate whether the FIFO has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Qn after three RCLK rising edges; $\overline{REN}$ = low is not necessary. Subsequent words must be accessed using $\overline{REN}$ and RCLK.

Various signals (both input and output) operate differently, depending on which timing mode is in effect.

FWFT mode

In FWFT mode, status flags $\overline{IR}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{OR}$ operate as outlined in Table 4. To write data into the FIFO, $\overline{WEN}$ must be low. Data presented to the DATA IN lines is clocked into the FIFO on subsequent transitions of WCLK. After the first write is performed, the $\overline{OR}$ flag goes low. Subsequent writes continue to fill the FIFO. $\overline{PAE}$ goes high after n + 2 words have been loaded into the FIFO, where n is the empty offset value. The default settings for these values are shown in Table 2, and are user programmable.

If one continues to write data into the FIFO and assumes no read operations are taking place, $\overline{HF}$ switches to low once the 514th word for the SN74V3640, 1026th word for the SN74V3650, 2050th word for the SN74V3660, 4098th word for the SN74V3670, 8194th word for the SN74V3680, and 16386th word for the SN74V3690, are written into the FIFO. Continuing to write data into the FIFO causes $\overline{PAF}$ to go low. If no reads are performed, $\overline{PAF}$ goes low after (1025 – m) writes for the SN74V3640, (2049 – m) writes for the SN74V3650, (4097 – m) writes for the SN74V3660, (8193 – m) writes for the SN74V3670, (16385 – m) writes for the SN74V3680, and (32769 – m) writes for the SN74V3690, where m is the full offset value. The default setting for these values is shown in Table 2.

When the FIFO is full, the $\overline{IR}$ flag goes high, inhibiting further write operations. If no reads are performed after a reset, $\overline{IR}$ goes high after D writes to the FIFO. D = 1025 writes for the SN74V3640, D = 2049 writes for the SN74V3650, D = 4097 writes for the SN74V3660, D = 8193 writes for the SN74V3670, D = 16385 writes for the SN74V3680, and D = 32769 writes for the SN74V3690. Note that the additional word in FWFT mode is due to the capacity of the memory plus output register.

If the FIFO is full, the first read operation causes the $\overline{IR}$ flag to go low. Subsequent read operations cause $\overline{PAF}$ and $\overline{HF}$ to go high at the conditions described in Table 4. If further read operations occur without write operations, $\overline{PAE}$ goes low when there are n + 1 words in the FIFO, where n is the empty offset value. Continuing read operations causes the FIFO to become empty. When the last word has been read from the FIFO, $\overline{OR}$ goes high, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

When configured in FWFT mode, the $\overline{OR}$ flag output is triple register buffered, and the $\overline{IR}$ flag output is double register buffered.

See Figures 9, 10, 12, and 14 for timing information.

standard mode

In standard mode, status flags $\overline{FF}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{EF}$ operate as outlined in Table 3. To write data into the FIFO, $\overline{WEN}$ must be low. Data presented to the DATA IN lines is clocked into the FIFO on subsequent transitions of WCLK. After the first write is performed, $\overline{EF}$ goes high. Subsequent writes continue to fill the FIFO. $\overline{PAE}$ goes high after n + 1 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values is shown in Table 2. This parameter is also user programmable.

If one continues to write data into the FIFO and assumes no read operations are taking place, $\overline{HF}$ switches to low after the 513rd word for SN74V3640, 1025th word for SN74V3650, 2049th word for SN74V3660, 4097th word for SN74V3670, 8193th word for the SN74V3680, and 16385th word for the SN74V3690 are written into the FIFO. Continuing to write data into the FIFO causes $\overline{PAF}$ to go low. If no reads are performed, $\overline{PAF}$ goes low after (1024 – m) writes for the SN74V3640, (2048 – m) writes for the SN74V3650, (4096 – m) writes for the SN74V3660, (8192 – m) writes for the SN74V3670, (16384 – m) writes for the SN74V3680, and (32768 – m) writes for the SN74V3690. Offset m is the full offset value. The default setting for these values is in the footnote of Table 2. This parameter is also user programmable.

When the FIFO is full, $\overline{FF}$ goes low, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}$ goes low after D writes to the FIFO. D = 1024 writes for the SN74V3640, D = 2048 writes for the SN74V3650, D = 4096 writes for the SN74V3660, D = 8192 writes for the SN74V3670, D = 16384 writes for the SN74V3680, and D = 32768 writes for the SN74V3690.

standard mode (continued)

If the FIFO is full, the first read operation causes $\overline{FF}$ to go high. Subsequent read operations cause $\overline{PAF}$ and $\overline{HF}$ to go high at the conditions described in Table 3. If further read operations occur without write operations, $\overline{PAE}$ goes low when there are n words in the FIFO, where n is the empty offset value. Continuing read operations causes the FIFO to become empty. When the last word has been read from the FIFO, $\overline{EF}$ goes low, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

When configured in standard mode, the $\overline{EF}$ and $\overline{FF}$ outputs are register-buffered outputs.

See Figures 7, 8, 11, and 13 for timing information.

Table 2. Default Programmable Flag Offsets

SN74V3640, SN74V3650				SN74V3660, SN74V3670, SN74V3680, SN74V3690			
$\overline{LD}$	FSEL1	FSEL0	OFFSETS (n, m)†	$\overline{LD}$	FSEL1	FSEL0	OFFSETS (n, m)†
L	H	L	511	H	L	L	1,023
L	L	H	255	L	H	L	511
L	L	L	127	L	L	H	255
L	H	H	63	L	L	L	127
H	L	L	31	L	H	H	63
H	H	L	15	H	H	L	31
H	L	H	7	H	L	H	15
H	H	H	3	H	H	H	7
			PROGRAM MODE				**PROGRAM MODE**
H	X	X	Serial‡	H	X	X	Serial‡
L	X	X	Parallel§	L	X	X	Parallel§

† n = empty offset for $\overline{PAE}$, m = full offset for $\overline{PAF}$
‡ As well as selecting serial programming mode, one of the default values also is loaded, depending on the state of FSEL0 and FSEL1.
§ As well as selecting parallel programming mode, one of the default values also is loaded, depending on the state of FSEL0 and FSEL1.

programming flag offsets

Full and empty flag offset values are user programmable. The SN74V3640, SN74V3650, SN74V3660, SN74V3670, SN74V3680, and SN74V3690 have internal registers for these offsets. Eight default offset values are selectable during master reset. These offset values are shown in Table 2. Offset values can also be programmed into the FIFO by serial or parallel loading. The loading method is selected using $\overline{LD}$. During master reset, the state of the $\overline{LD}$ input determines whether serial or parallel flag offset programming is enabled. A high on $\overline{LD}$ during master reset selects serial loading of offset values. A low on $\overline{LD}$ during master reset selects parallel loading of offset values.

In addition to loading offset values into the FIFO, it is also possible to read the current offset values. Offset values can be read via the parallel output port Q0–Qn, regardless of the programming mode selected (serial or parallel). It is not possible to read the offset values in serial fashion.

Figure 3 summarizes the control pins and sequence for both serial and parallel programming modes. A more detailed description is given in the following paragraphs.

The offset registers may be programmed (and reprogrammed) any time after master reset, regardless of whether serial or parallel programming has been selected. Valid programming ranges are from 0 to D – 1.

synchronous vs asynchronous programmable flag timing selection

The SN74V3640, SN74V3650, SN74V3660, SN74V3670, SN74V3680, and SN74V3690 can be configured during the master reset cycle, with either synchronous or asynchronous timing for $\overline{PAF}$ and $\overline{PAE}$, by use of the PFM pin.

If synchronous $\overline{PAF}$/$\overline{PAE}$ configuration is selected (PFM high during $\overline{MRS}$), $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only and not RCLK. Similarly, $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only, and not WCLK (see Figure 17 for synchronous $\overline{PAF}$ timing and Figure 18 for synchronous $\overline{PAE}$ timing).

If asynchronous $\overline{PAF}$/$\overline{PAE}$ configuration is selected (PFM low during $\overline{MRS}$), $\overline{PAF}$ is asserted low on the low-to-high transition of WCLK, and $\overline{PAF}$ is reset to high on the low-to-high transition of RCLK. Similarly, $\overline{PAE}$ is asserted low on the low-to-high transition of RCLK. $\overline{PAE}$ is reset to high on the low-to-high transition of WCLK.

See Figure 19 for asynchronous $\overline{PAF}$ timing and Figure 20 for asynchronous $\overline{PAE}$ timing.

Table 3. Status Flags for Standard Mode

	SN74V3640	SN74V3650	SN74V3660	SN74V3670	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in FIFO (see Note 8)	0	0	0	0	H	H	H	L	L
	1 to n	1 to n	1 to n	1 to n	H	H	H	L	H
	(n + 1) to 512	(n + 1) to 1024	(n + 1) to 2048	(n + 1) to 4096	H	H	H	H	H
	513 to [1024 – (m + 1)]	1025 to [2048 – (m + 1)]	2049 to [4096 – (m + 1)]	4097 to [8192 – (m + 1)]	H	H	L	H	H
	(1024 – m) to 1023	(2048 – m) to 2047	(4096 – m) to 4095	(8192 – m) to 8191	H	L	L	H	H
	1024	2048	4096	8192	L	L	L	H	H

	SN74V3680	SN74V3690	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in FIFO (see Note 8)	0	0	H	H	H	L	L
	1 to n	1 to n	H	H	H	L	H
	(n + 1) to 8192	(n + 1) to 16384	H	H	H	H	H
	8193 to [16384 – (m + 1)]	16385 to [32768 – (m + 1)]	H	H	L	H	H
	(16384 – m) to 16383	(32768 – m) to 32767	H	L	L	H	H
	16384	32768	L	L	L	H	H

NOTE 8: See Table 2 for values for n, m.

Table 4. Status Flags for FWFT Mode

	SN74V3640	SN74V3650	SN74V3660	SN74V3670	$\overline{IR}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{OR}$
Number of Words in FIFO (see Note 8)	0	0	0	0	L	H	H	L	H
	1 to (n + 1)	1 to (n + 1)	1 to (n + 1)	1 to (n + 1)	L	H	H	L	L
	(n + 2) to 513	(n + 2) to 1025	(n + 2) to 2049	(n + 2) to 4097	L	H	H	H	L
	514 to [1025 – (m + 1)]	1026 to [2049 – (m + 1)]	2050 to [4097 – (m + 1)]	4098 to [8193 – (m + 1)]	L	H	L	H	L
	(1025 – m) to 1024	(2049 – m) to 2048	(4097 – m) to 4096	(8193 – m) to 8192	L	L	L	H	L
	1025	2049	4097	8193	H	L	L	H	L

	SN74V3680	SN74V3690	$\overline{IR}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{OR}$
Number of Words in FIFO (see Note 8)	0	0	L	H	H	L	H
	1 to (n + 1)	1 to (n + 1)	L	H	H	L	L
	(n + 2) to 8193	(n + 2) to 16385	L	H	H	H	L
	8194 to [16385 – (m + 1)]	16386 to [32769 – (m + 1)]	L	H	L	H	L
	(16385 – m) to 16384	(32769 – m) to 32768	L	L	L	H	L
	16385	32769	H	L	L	H	L

NOTE 8: See Table 2 for values for n, m.

$\overline{LD}$	$\overline{WEN}$	$\overline{REN}$	$\overline{SEN}$	WCLK	RCLK	SN74V3640, SN74V3650, SN74V3660, SN74V3670, SN74V3680, SN74V3690
0	0	1	1	↑	X	Parallel write to registers: Empty offset (LSB) Empty offset (MSB) Full offset (LSB) Full offset (MSB)
0	1	0	1	X	↑	Parallel read from registers: Empty offset (LSB) Empty offset (MSB) Full offset (LSB) Full offset (MSB)
0	1	1	0	↑	X	Serial shift into registers: 20 bits for the SN74V3640 22 bits for the SN74V3650 24 bits for the SN74V3660 26 bits for the SN74V3670 28 bits for the SN74V3680 30 bits for the SN74V3690 1 bit for each rising WCLK edge, starting with empty offset (LSB) ending with full offset (MSB)
X	1	1	1	X	X	No operation
1	0	X	X	↑	X	Write memory
1	X	0	X	X	↑	Read memory
1	1	1	X	X	X	No operation

NOTES: A. The programming method can be selected only at master reset.
B. Parallel reading of the offset registers is always permitted, regardless of which programming method has been selected.
C. The programming sequence applies to FWFT and standard modes.

Figure 3. Programmable Flag Offset Programming Sequence

1st Parallel Offset Write/Read Cycle

Data Inputs/Outputs

D/Q35						D/Q15							D/Q8								D/Q0	
EMPTY OFFSET REGISTER ($\overline{PAE}$) BIT LOCATIONS																						
X		X	X	X	X	X	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	**Noninterspersed Parity**
X		X	X	X	X	15	14	13	12	11	10	9	X	8	7	6	5	4	3	2	1	**Interspersed Parity**

2nd Parallel Offset Write/Read Cycle

Data Inputs/Outputs

D/Q35					D/Q17								D/Q8								D/Q0	
FULL OFFSET REGISTER ($\overline{PAF}$) BIT LOCATIONS																						
X		X	X	X	X	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	**Noninterspersed Parity**
X		X	X	X	16	15	14	13	12	11	10	9	X	8	7	6	5	4	3	2	1	**Interspersed Parity**

×36 Bus Width

1st Parallel Offset Write/Read Cycle

D/Q17 **D/Q15** **Data Inputs/Outputs** **D/Q0**

	EMPTY OFFSET (LSB) REGISTER ($\overline{PAE}$) BIT LOCATIONS																
X	X	X	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	X	15	14	13	12	11	10	9	X	8	7	6	5	4	3	2	1

D/Q8

Noninterspersed Parity
Interspersed Parity

2nd Parallel Offset Write/Read Cycle

D/Q17 **D/Q15** **Data Inputs/Outputs** **D/Q0**

	FULL OFFSET (LSB) REGISTER ($\overline{PAF}$) BIT LOCATIONS																
X	X	X	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	X	15	14	13	12	11	10	9	X	8	7	6	5	4	3	2	1

D/Q8

Noninterspersed Parity
Interspersed Parity

×18 Bus Width

Number of bits used:
10 bits for the SN74V3640
11 bits for the SN74V3650
12 bits for the SN74V3660
13 bits for the SN74V3670
14 bits for the SN74V3680
15 bits for the SN74V3690
Note: All unused bits of the LSB and MSB are don't care.

Figure 3. Programmable Flag Offset Programming Sequence (Continued)

1st Parallel Offset Write/Read Cycle

D/Q8								D/Q0
EMPTY OFFSET REGISTER ($\overline{PAE}$) BIT LOCATIONS								
X	8	7	6	5	4	3	2	1

2nd Parallel Offset Write/Read Cycle

D/Q8								D/Q0
EMPTY OFFSET REGISTER ($\overline{PAE}$) BIT LOCATIONS								
X	16	15	14	13	12	11	10	9

3rd Parallel Offset Write/Read Cycle

D/Q8								D/Q0
FULL OFFSET REGISTER ($\overline{PAF}$) BIT LOCATIONS								
X	8	7	6	5	4	3	2	1

4th Parallel Offset Write/Read Cycle

D/Q8								D/Q0
FULL OFFSET REGISTER ($\overline{PAF}$) BIT LOCATIONS								
X	16	15	14	13	12	11	10	9

×9 Bus Width

Number of bits used:
10 bits for the SN74V3640
11 bits for the SN74V3650
12 bits for the SN74V3660
13 bits for the SN74V3670
14 bits for the SN74V3680
15 bits for the SN74V3690
Note: All unused bits of the LSB and MSB are don't care.

Figure 3. Programmable Flag Offset Programming Sequence (Continued)

serial programming mode

If the serial programming mode has been selected as described previously, programming of $\overline{PAE}$ and $\overline{PAF}$ values can be achieved by using a combination of the $\overline{LD}$, $\overline{SEN}$, WCLK, and SI inputs. Programming $\overline{PAE}$ and $\overline{PAF}$ proceeds as follows. When $\overline{LD}$ and $\overline{SEN}$ are set low, data on the SI input are written, one bit for each WCLK rising edge, starting with the empty offset LSB and ending with the full offset MSB. This makes a total of 20 bits for the SN74V3640, 22 bits for the SN74V3650, 24 bits for the SN74V3660, 26 bits for the SN74V3670, 28 bits for the SN74V3680, and 30 bits for the SN74V3690.

See Figure 15 for the timing information.

Using the serial method, individual registers cannot be programmed selectively. $\overline{PAE}$ and $\overline{PAF}$ can show a valid status only after the complete set of bits (for all offset registers) has been entered. The registers can be reprogrammed, as long as the complete set of new offset bits is entered. When $\overline{LD}$ is low and $\overline{SEN}$ is high, no serial write to the registers can occur.

serial programming mode (continued)

Write operations to the FIFO are allowed before and during the serial programming sequence. In this case, the programming of all offset bits need not occur at once. A select number of bits can be written to the SI input and then, by bringing $\overline{LD}$ and $\overline{SEN}$ high, data can be written to FIFO memory via Dn by switching $\overline{WEN}$. When $\overline{WEN}$ is brought high with $\overline{LD}$ and $\overline{SEN}$ restored to a low, the next offset bit in sequence is written to the registers via SI. If an interruption of serial programming is desired, it is sufficient either to set $\overline{LD}$ low and deactivate $\overline{SEN}$, or to set $\overline{SEN}$ low and deactivate $\overline{LD}$. When $\overline{LD}$ and $\overline{SEN}$ are restored to a low level, serial offset programming continues.

From the time serial programming begins, neither programmable flag is valid until the full set of bits required to fill all the offset registers is written. Measuring from the rising WCLK edge that achieves the previous criteria, $\overline{PAF}$ is valid after two more rising WCLK edges + t_{PAF}. $\overline{PAE}$ is valid after the next two rising RCLK edges + t_{PAE} + t_{sk2}.

Flag offset values can be read only via parallel output port Qn.

parallel programming mode

If the parallel programming mode has been selected as described previously, programming of $\overline{PAE}$ and $\overline{PAF}$ values can be achieved by using a combination of the $\overline{LD}$, WCLK , $\overline{WEN}$ and Dn inputs. Programming $\overline{PAE}$ and $\overline{PAF}$ proceeds as follows. $\overline{LD}$ and $\overline{WEN}$ must be set low. For ×36-bit input bus width, data on the inputs Dn are written into the Empty Offset register on the first low-to-high transition of WCLK. On the second low-to-high transition of WCLK, data are written into the Full Offset register. The third transition of WCLK writes, once again, to the Empty Offset register. For ×18-bit input bus width, data on the inputs Dn are written into the Empty Offset register (LSB) on the first low-to-high transition of WCLK. On the second low-to-high transition of WCLK, data are written into the Empty Offset (MSB) register. The third transition of WCLK writes to the Full Offset register (LSB). The fourth transition of WCLK writes to the Full Offset register (MSB). The fifth transition of WCLK writes, once again, to the Empty Offset register (LSB). A total of four writes to the offset registers is required to load values using a ×18 input bus width. For an input bus width of ×9 bits, a total of six write cycles to the offset registers is required to load values.

See Figures 3 and 16 for timing information.

Writing offsets in parallel employs a dedicated Write Offset register pointer. Reading offsets employs a dedicated Read Offset register pointer. The two pointers operate independently; however, a read and a write should not be performed simultaneously to the offset registers. A master reset initializes both pointers to the Empty Offset register (LSB). A partial reset has no effect on the position of these pointers.

Write operations to the FIFO are allowed before and during the parallel programming sequence. In this case, the programming of all offset registers need not occur at one time. One, two, or more offset registers can be written to and then, by bringing $\overline{LD}$ high, write operations can be redirected to the FIFO memory. When $\overline{LD}$ is set low again and $\overline{WEN}$ is low, the next offset register in sequence is written to. As an alternative to holding $\overline{WEN}$ low and switching $\overline{LD}$, parallel programming can also be interrupted by setting $\overline{LD}$ low and switching $\overline{WEN}$.

Note that the status of a programmable-flag ($\overline{PAE}$ or $\overline{PAF}$) output is invalid during the programming process. From the time parallel programming has begun, a programmable-flag output is not valid until the appropriate offset word has been written to the register(s) pertaining to that flag. Measuring from the rising WCLK edge that achieves the previous criteria, $\overline{PAF}$ is valid after two more rising WCLK edges + t_{PAF}. $\overline{PAE}$ is valid after the next two rising RCLK edges + t_{PAE} + t_{sk2}.

Reading the offset registers employs a dedicated read offset register pointer. The contents of the offset registers can be read on the Q0–Qn pins when $\overline{LD}$ is set low and $\overline{REN}$ is set low. For ×36 output bus width, data are read via Qn from the Empty Offset register on the first low-to-high transition of RCLK. On the second low-to-high transition of RCLK, data are read from the Full Offset register. The third transition of RCLK reads, once again, from the Empty Offset register. For ×18 output bus width, a total of four read cycles is required to obtain the values of the offset registers, starting with the Empty Offset register (LSB) and finishing with the Full Offset register (MSB). For ×9 output bus width, a total of six read cycles must be performed on the offset registers.

parallel programming mode (continued)

See Figures 3 and 17 for timing information.

It is permissible to interrupt the offset register read sequence with reads or writes to the FIFO. The interruption is accomplished by deasserting $\overline{REN}$, $\overline{LD}$, or both together. When $\overline{REN}$ and $\overline{LD}$ are restored to a low level, reading of the offset registers continues where it left off. It should be noted (and care should be taken from the fact) that when a parallel read of the flag offsets is performed, the data word that was present on output lines Qn is overwritten.

Parallel reading of the offset registers always is permitted, regardless of which timing mode (Standard or FWFT modes) has been selected.

retransmit operation

The retransmit operation allows data that has been read to be accessed again. There are two modes of retransmit operation: normal latency and zero latency. There are two stages to retransmit. The first stage is a setup procedure that resets the read pointer to the first location of memory. The second stage is the actual retransmit, which consists of reading out the memory contents, starting at the beginning of memory.

Retransmit setup is initiated by holding $\overline{RT}$ low during a rising RCLK edge. $\overline{REN}$ and $\overline{WEN}$ must be high before bringing $\overline{RT}$ low. When zero latency is utilized, $\overline{REN}$ need not be high before bringing $\overline{RT}$ low. At least two words, but no more than D – 2 words should have been written into the FIFO, and read from the FIFO, between reset (master or partial) and the time of retransmit setup, D = 1024 for the SN74V3640, D = 2048 for the SN74V3650, D = 4096 for the SN74V3660, D = 8192 for the SN74V3670, D = 16384 for the SN74V3680, and D = 32768 for the SN74V3690. In FWFT mode, D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 4097 for the SN74V3660, D = 8193 for the SN74V3670, D = 16385 for the SN74V3680, and D = 32769 for the SN74V3690.

If standard mode is selected, the FIFO marks the beginning of the retransmit setup by setting $\overline{EF}$ low. The change in level is noticeable only if $\overline{EF}$ was high before setup. During this period, the internal read pointer is initialized to the first location of the RAM array.

When $\overline{EF}$ goes high, retransmit setup is complete and read operations can begin, starting with the first location in memory. Because standard mode is selected, every word read, including the first word following retransmit setup, requires a low on $\overline{REN}$ to enable the rising edge of RCLK.

See Figure 11 for timing information.

If FWFT mode is selected, the FIFO marks the beginning of the retransmit setup by setting $\overline{OR}$ high. During this period, the internal read pointer is set to the first location of the RAM array.

When $\overline{OR}$ goes low, retransmit setup is complete. At the same time, the contents of the first location appear on the outputs. Because FWFT mode is selected, the first word appears on the outputs and no low on $\overline{REN}$ is necessary. Reading all subsequent words requires a low on $\overline{REN}$ to enable the rising edge of RCLK.

See Figure 12 for timing information.

For either standard mode or FWFT mode, updating of $\overline{PAE}$, $\overline{HF}$, and $\overline{PAF}$ begins with the rising edge of RCLK that $\overline{RT}$ is set up on. $\overline{PAE}$ is synchronized to RCLK, thus, on the second rising edge of RCLK after $\overline{RT}$ is set up, $\overline{PAE}$ is updated. $\overline{HF}$ is asynchronous, thus, the rising edge of RCLK that $\overline{RT}$ is set up on updates $\overline{HF}$. $\overline{PAF}$ is synchronized to WCLK, thus, the second rising edge of WCLK that occurs t_{sk} after the rising edge of RCLK that $\overline{RT}$ is set up on updates $\overline{PAF}$. $\overline{RT}$ is synchronized to RCLK.

The retransmit function has the option of two modes of operation, either normal latency or zero latency. Figures 11 and 12 show normal latency. Figures 13 and 14 show the zero-latency retransmit operation. Zero latency means, basically, that the first data word to be retransmitted is placed in the output register, with respect to the RCLK pulse that initiated the retransmit.

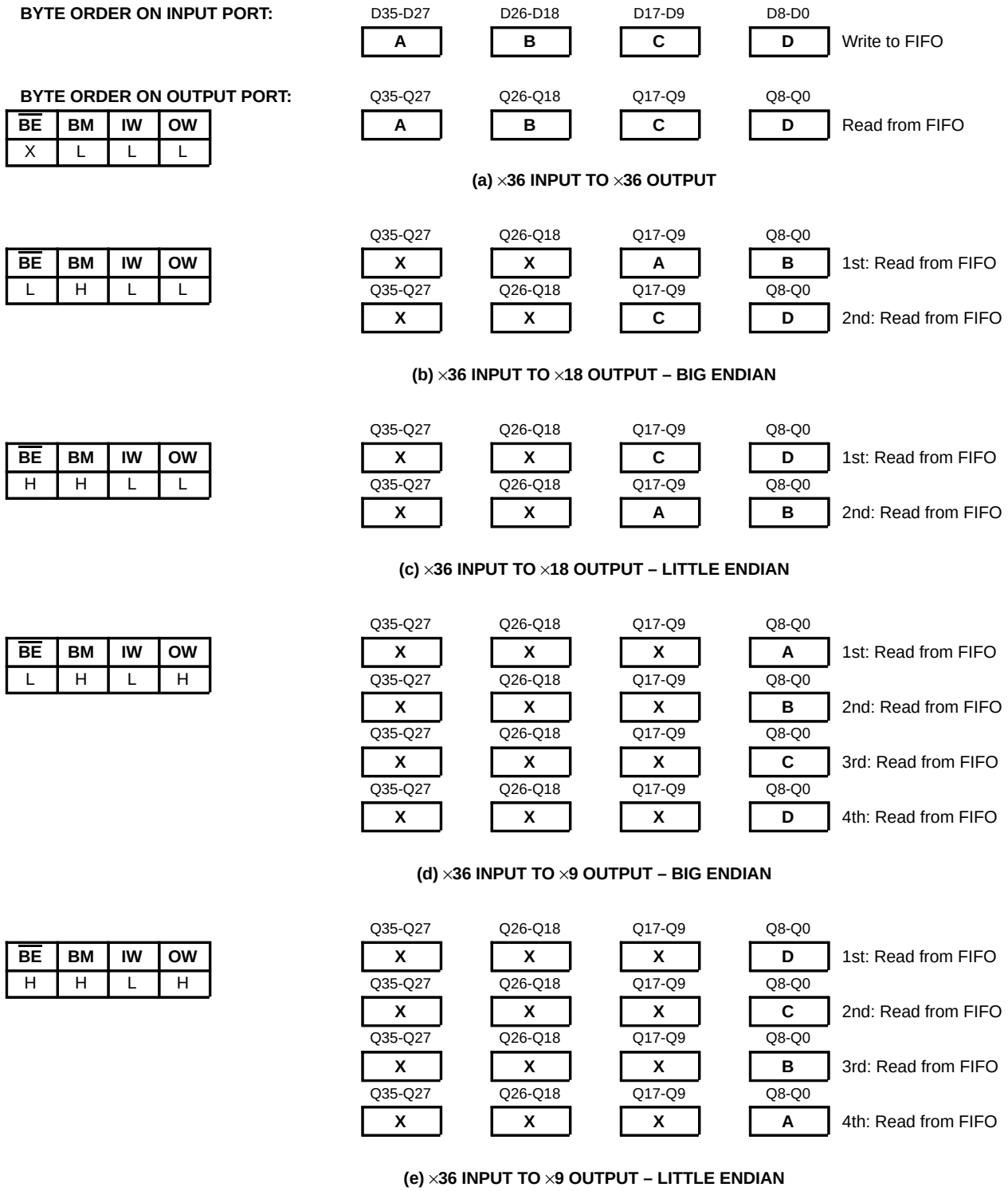


Figure 4. Bus-Matching Byte Arrangement

BYTE ORDER ON INPUT PORT:

	D35-D27	D26-D18	D17-D9	D8-D0	
	X	X	A	B	1st: Write to FIFO
	Q35-Q27	Q26-Q18	Q17-Q9	Q8-Q0	
	X	X	C	D	2nd: Write to FIFO

BYTE ORDER ON OUTPUT PORT:

$\overline{BE}$	BM	IW	OW
L	H	H	L

Q35-Q27	Q26-Q18	Q17-Q9	Q8-Q0	
A	B	C	D	Read from FIFO

(a) ×18 INPUT TO ×36 OUTPUT – BIG ENDIAN

$\overline{BE}$	BM	IW	OW
H	H	H	L

Q35-Q27	Q26-Q18	Q17-Q9	Q8-Q0	
C	D	A	B	Read from FIFO

(b) ×18 INPUT TO ×36 OUTPUT – LITTLE ENDIAN

BYTE ORDER ON INPUT PORT:

Q35-Q27	Q26-Q18	Q17-Q9	Q8-Q0	
X	X	X	A	1st: Write to FIFO
X	X	X	B	2nd: Write to FIFO
X	X	X	C	3rd: Write to FIFO
X	X	X	D	4th: Write to FIFO

BYTE ORDER ON OUTPUT PORT:

$\overline{BE}$	BM	IW	OW
L	H	H	H

Q35-Q27	Q26-Q18	Q17-Q9	Q8-Q0	
A	B	C	D	Read from FIFO

(a) ×9 INPUT TO ×36 OUTPUT – BIG ENDIAN

$\overline{BE}$	BM	IW	OW
H	H	H	H

Q35-Q27	Q26-Q18	Q17-Q9	Q8-Q0	
D	C	B	A	Read from FIFO

(b) ×9 INPUT TO ×36 OUTPUT – LITTLE ENDIAN

Figure 1. Bus-Matching Byte Arrangement (Continued)

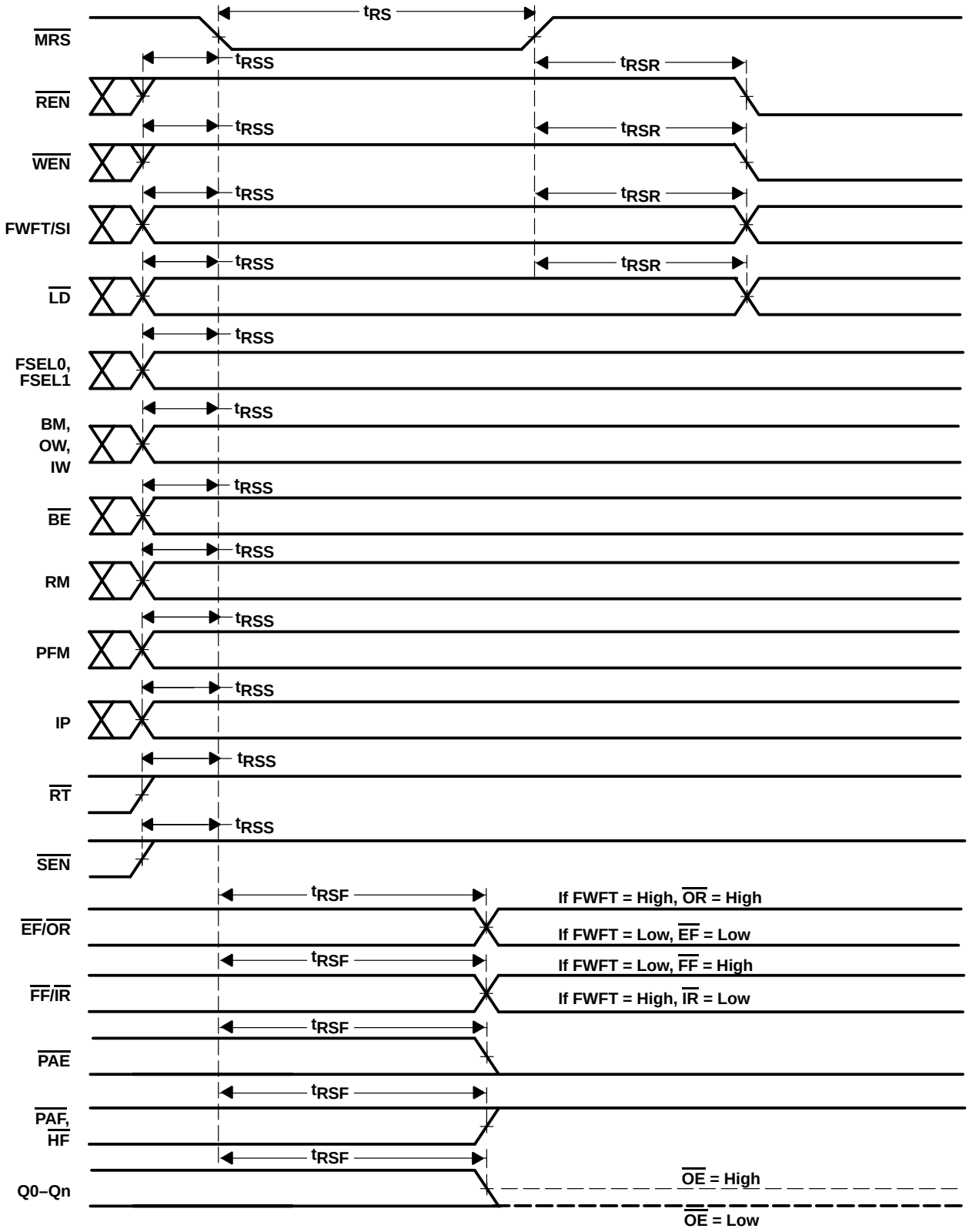


Figure 2. Master Reset Timing

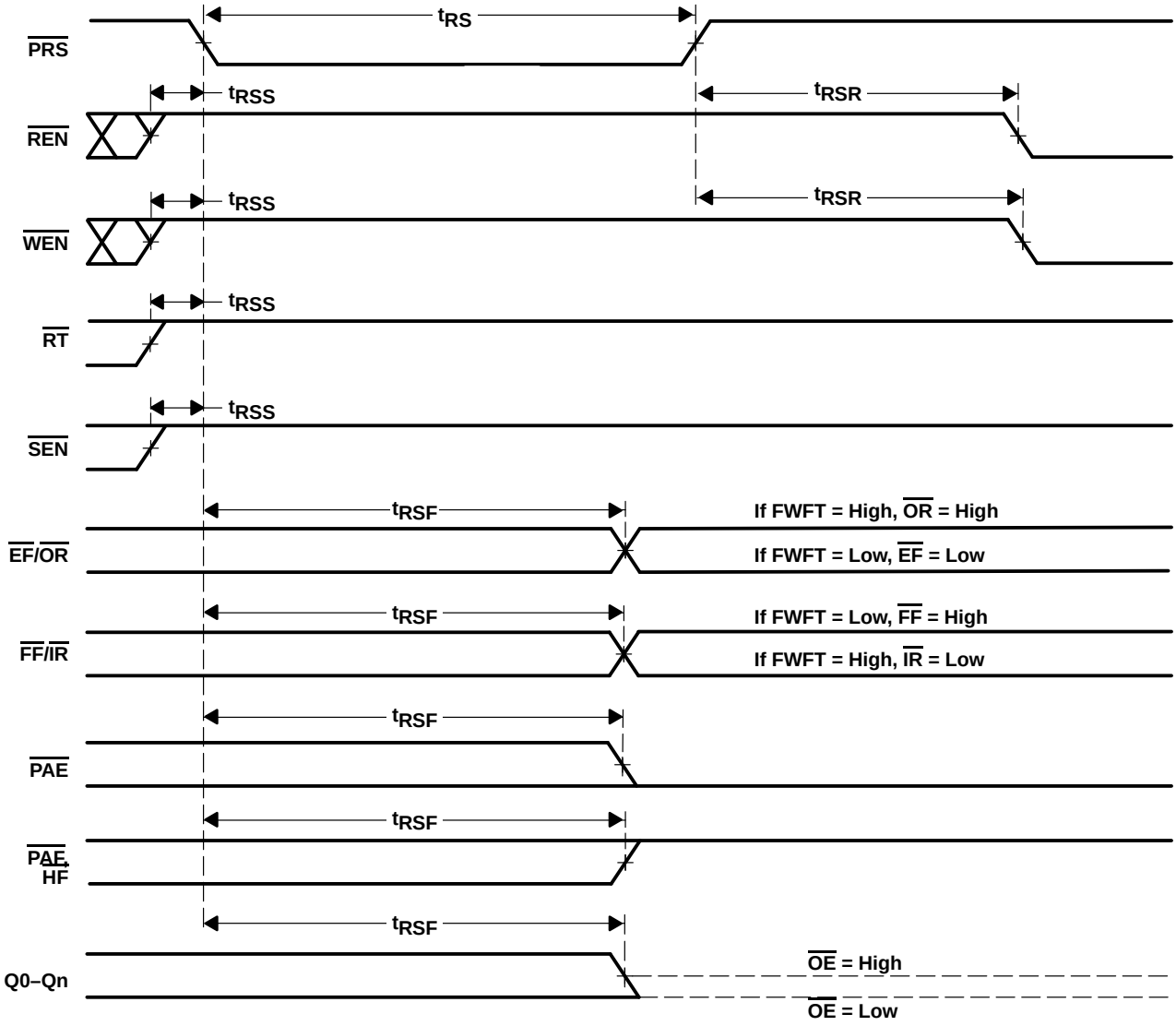
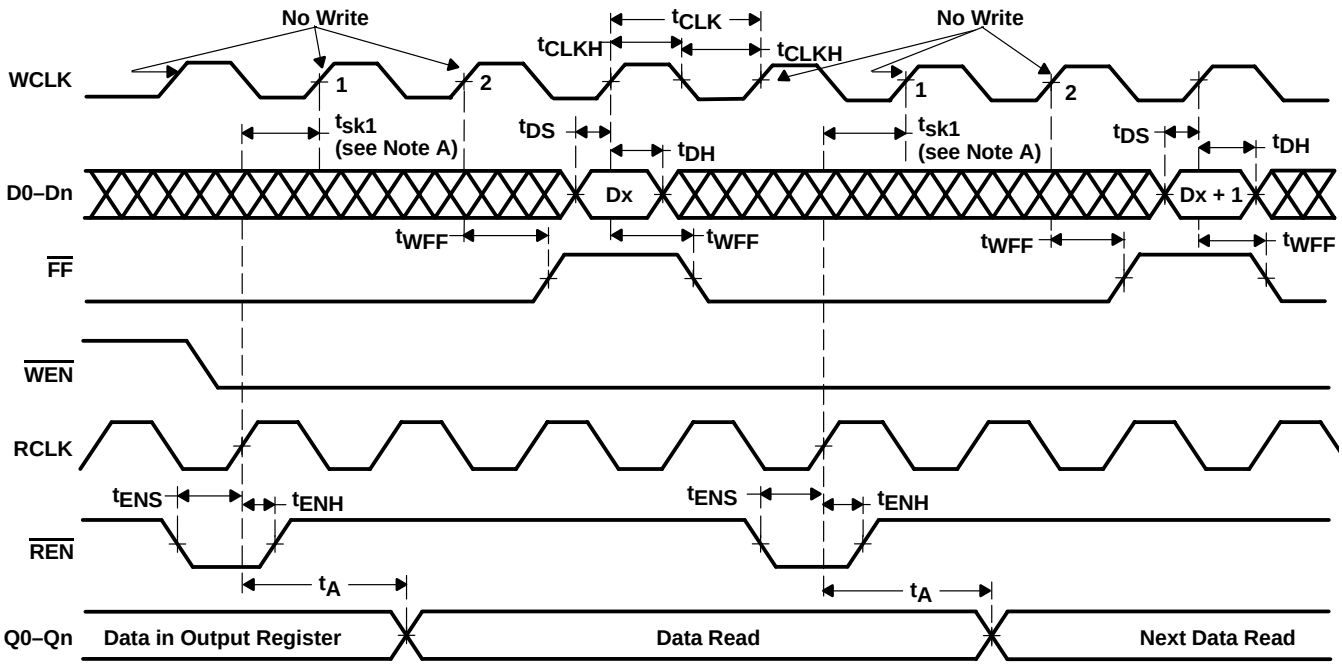


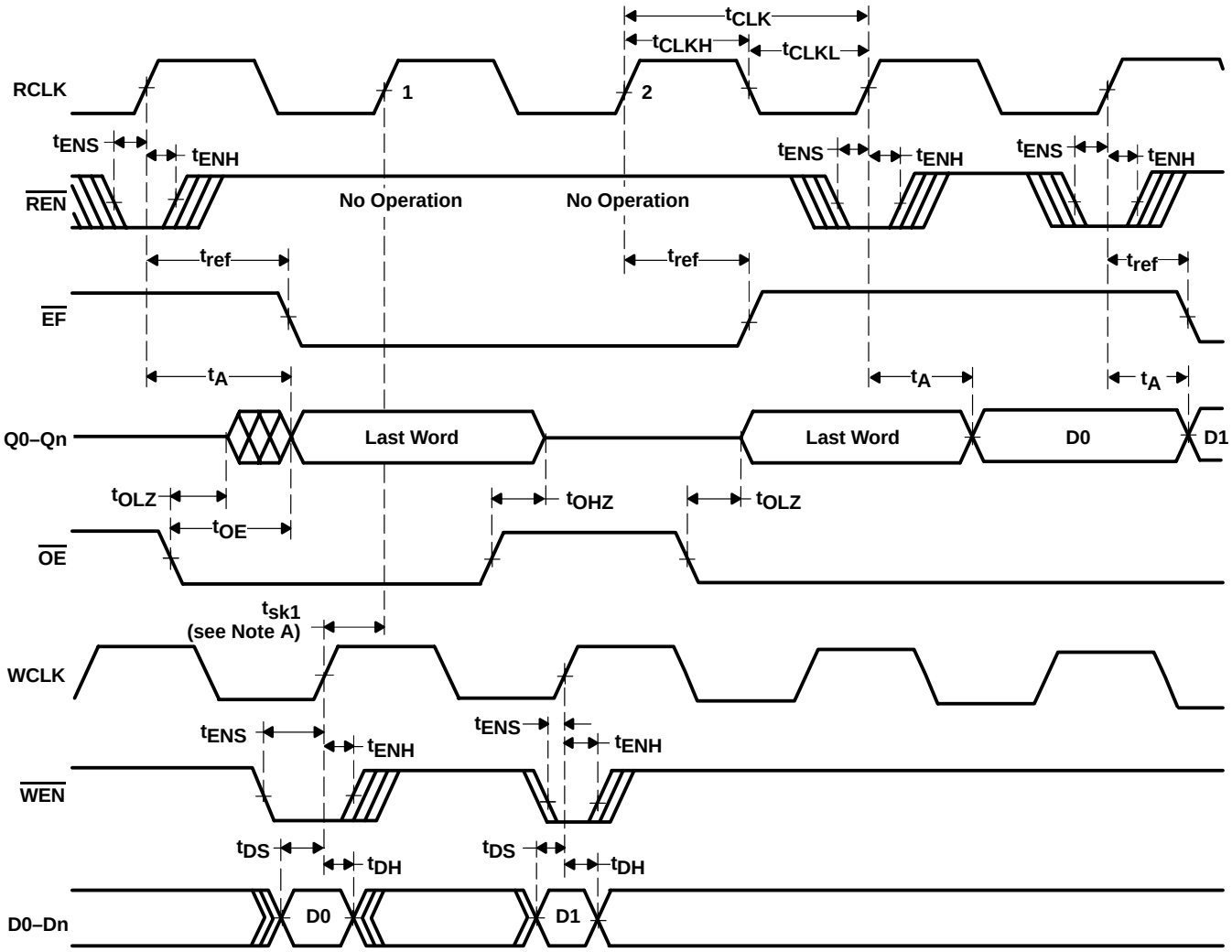
Figure 3. Partial Reset Timing



NOTES: A. t_{sk1} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{FF}$ goes high (after one WCLK cycle + t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{sk1}, $\overline{FF}$ deassertion can be delayed one additional WCLK cycle.

B. $\overline{LD}$ = high, $\overline{OE}$ = low, $\overline{EF}$ = high

Figure 4. Write Cycle and Full Flag Timing (Standard Mode)

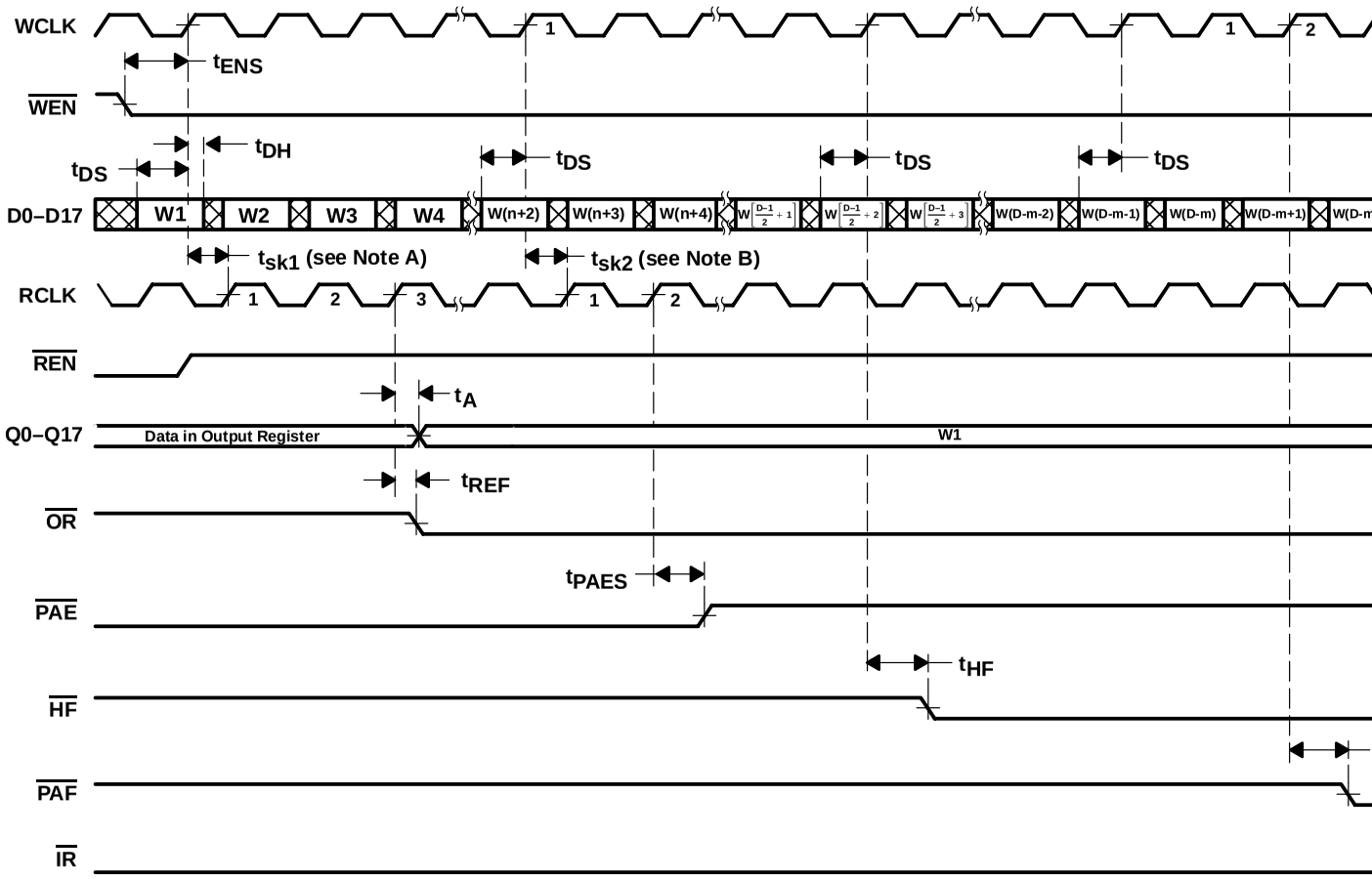


NOTES: A. t_{sk1} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{EF}$ goes high (after one RCLK cycle + t_{ref}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{sk1}, $\overline{EF}$ deassertion can be delayed one additional RCLK cycle.

B. $\overline{LD}$ = high

C. First-data-word latency: $t_{sk1} + 1T_{RCLK} + t_{REF}$

Figure 5. Read Cycle, Empty Flag, and First-Data-Word Latency Timing (Standard Mode)



NOTES: A. t_{sk1} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{OR}$ goes low after two RCLK cycles + t_{REF} edge of WLCK and the rising edge of RCLK is less than t_{sk1}, $\overline{OR}$ assertion can be delayed one additional RCLK cycle.

B. t_{sk2} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{PAE}$ goes high after one RCLK cycle + t_{PA} rising edge of WCLK and the rising edge of RCLK is less than t_{sk2}, $\overline{PAE}$ deassertion can be delayed one additional RCLK cycle.

C. $\overline{LD}$ = high, $\overline{OE}$ = low

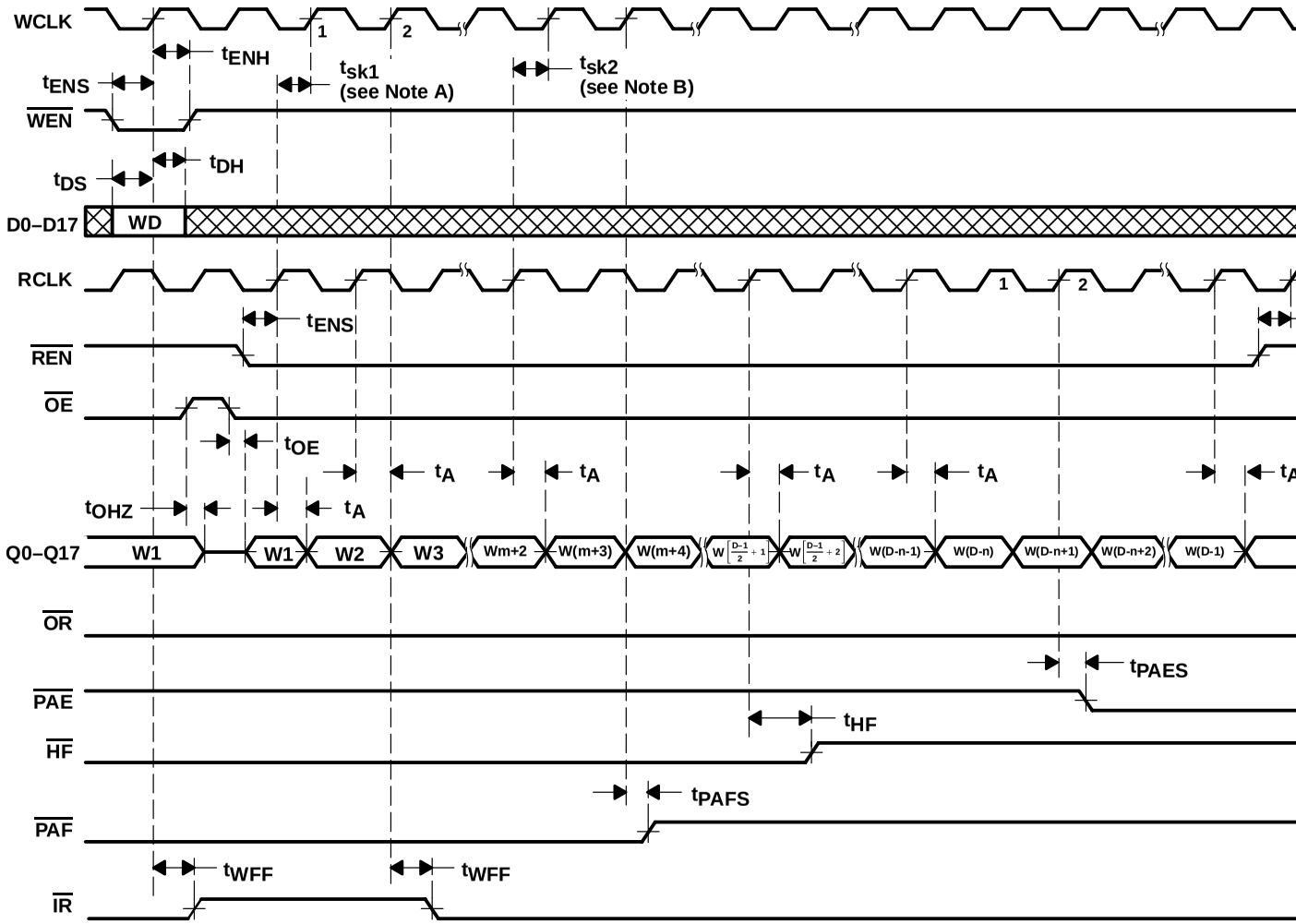
D. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset, D = maximum FIFO depth

E. D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 4097 for the SN74V3660, D = 8193 for the SN74V3670, D = 16385 for the for the SN74V3690

F. First-data-word latency: $t_{sk1} + 2t_{RCLK} + t_{REF}$

Figure 6. Write Timing (FWFT Mode)

PRODUCT PREVIEW



NOTES: A. t_{sk1} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{IR}$ goes low after one WCLK cycle + t_{WFF}. I
edge of RLCK and the rising edge of WCLK is less than t_{sk1}, $\overline{IR}$ assertion may be delayed an additional WCLK cycle.

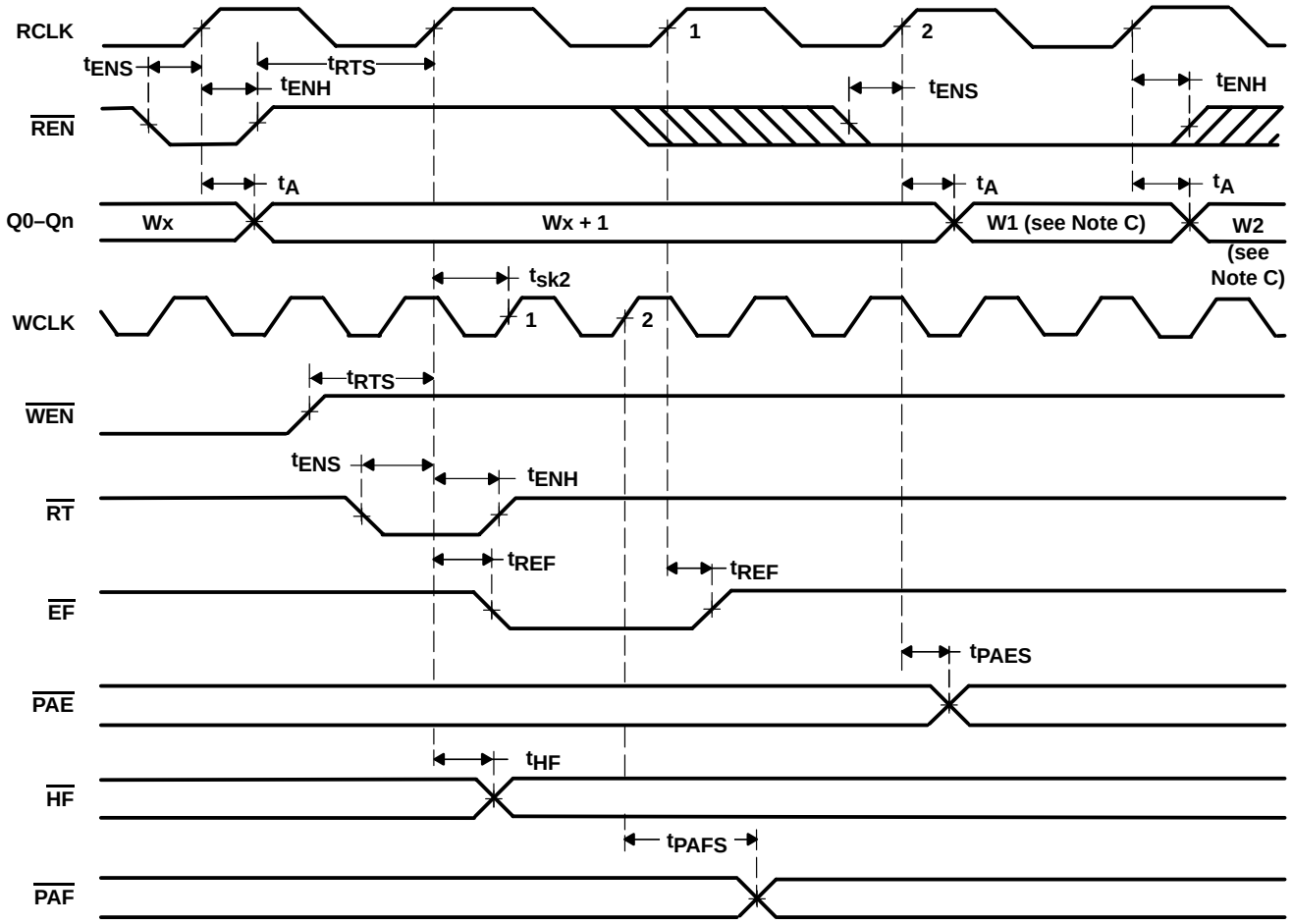
B. t_{sk2} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{PAF}$ to goes high after one WCLK cycle + t_P
rising edge of RCLK and the rising edge of WCLK is less than t_{sk2}, $\overline{PAF}$ deassertion may be delayed an additional WCLK cycle.

C. $\overline{LD}$ = high

D. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset, D = maximum FIFO depth

E. D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 8193 for the SN74V3670, D = 16385 for the SN74V3680, and D = 327

Figure 7. Read Timing (FWFT Mode)

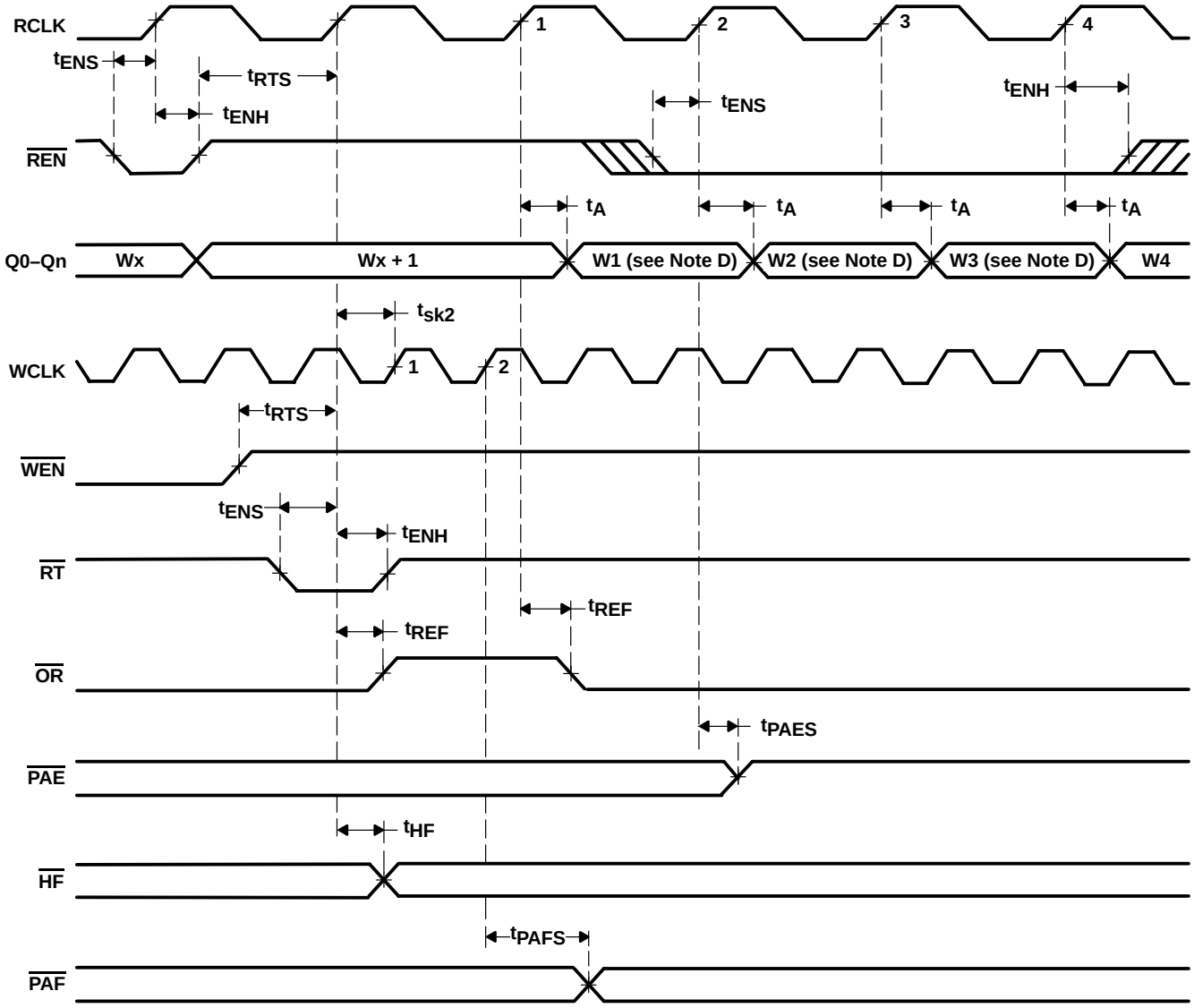


NOTES: A. Retransmit setup is complete after $\overline{EF}$ returns high; only then can a read operation begin.
B. $\overline{OE}$ = low
C. W1 = first word written to the FIFO after master reset, W2 = second word written to the FIFO after master reset
D. No more than (D – 2) words may be written to the FIFO between reset (master or partial) and retransmit setup. Therefore, $\overline{FF}$ is high throughout the retransmit setup procedure.
D = 1024 for the SN74V3640, D = 2048 for the SN74V3650, D = 4096 for the SN74V3660, D = 8192 for the SN74V3670, D = 16384 for the SN74V3680, and D = 32768 for the SN74V3690.
E. There must be at least two words written to and two words read from the FIFO before a retransmit operation can be invoked.
F. RM is set high during $\overline{MRS}$.

Figure 8. Retransmit Timing (Standard Mode)

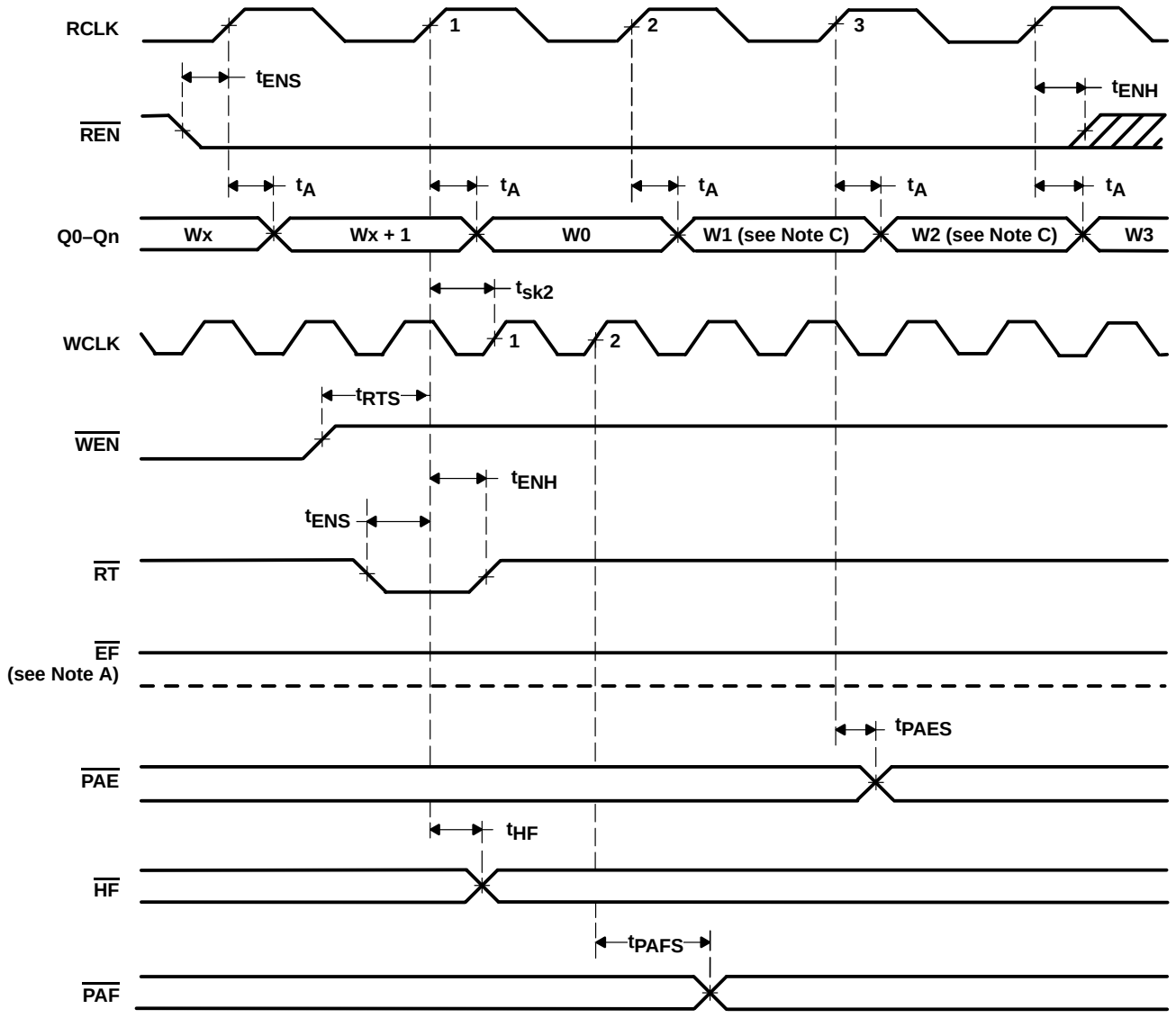
PRODUCT PREVIEW

PRODUCT PREVIEW



NOTES: A. Retransmit setup is complete after $\overline{OR}$ returns low.
B. No more than (D – 2) words can be written to the FIFO between reset (master or partial) and retransmit setup. Therefore, $\overline{IR}$ is low throughout the retransmit setup procedure.
D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 4097 for the SN74V3660, D = 8193 for the SN74V3670, D = 16385 for the SN74V3680, and D = 32769 for the SN74V3690.
C. $\overline{OE}$ = low
D. W1, W2, W3 = first, second, and third words written to the FIFO after master reset
E. There must be at least two words written to the FIFO before a retransmit operation can be invoked.
F. RM is set high during $\overline{MRS}$.

Figure 9. Retransmit Timing (FWFT Mode)



NOTES: A. If the FIFO is empty at the point of retransmit, $\overline{EF}$ is updated, based on RCLK (retransmit clock cycle). Valid data appears on the output.

B. $\overline{OE}$ = low, enables data to be read on outputs Q0–Qn

C. W1 = first word written to the FIFO after master reset, W2 = second word written to the FIFO after master reset

D. No more than (D – 2) words may be written to the FIFO between reset (master or partial) and retransmit setup. Therefore, $\overline{FF}$ is high throughout the retransmit setup procedure.
D = 1024 for the SN74V3640, D = 2048 for the SN74V3650, D = 4096 for the SN74V3660, D = 8192 for the SN74V3670, D = 16384 for the SN74V3680, D = 32768 for the SN74V3690.

E. At least two words must be written to and read from the FIFO before a retransmit operation can be invoked.

F. RM is set low during $\overline{MRS}$.

Figure 10. Zero-Latency Retransmit Timing (Standard Mode)

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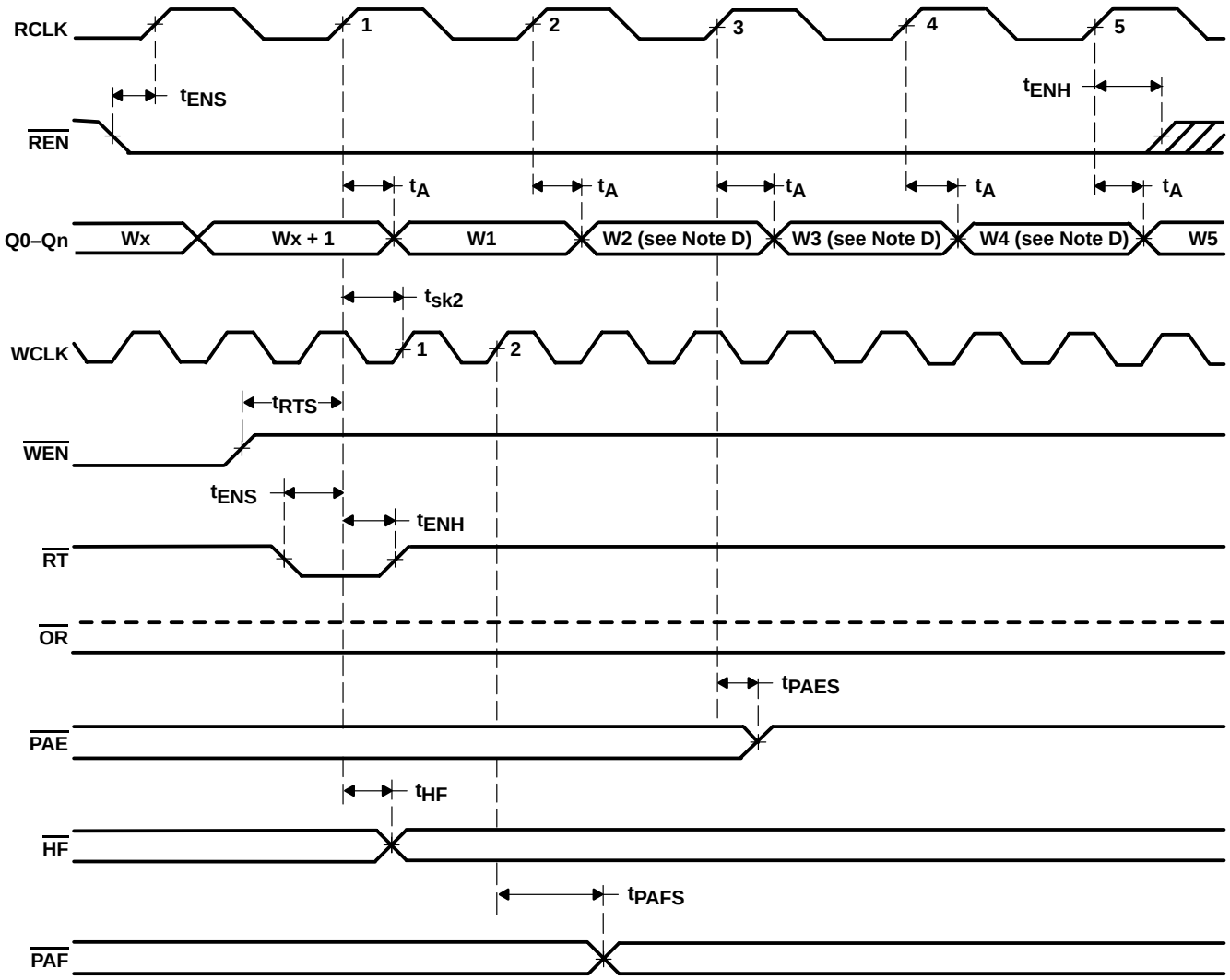


NOTES: A. If the FIFO is empty at the point of retransmit, $\overline{OR}$ is updated, based on RCLK (retransmit clock cycle). Valid data also appears on the output.

B. No more than (D – 2) words may be written to the FIFO between reset (master or partial) and retransmit setup. Therefore, $\overline{IR}$ is low throughout the retransmit setup procedure.
D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 4097 for the SN74V3660, and D = 8193 for the SN74V3670, D = 16385 for the SN74V3680, and D = 32769 for the SN74V3690.

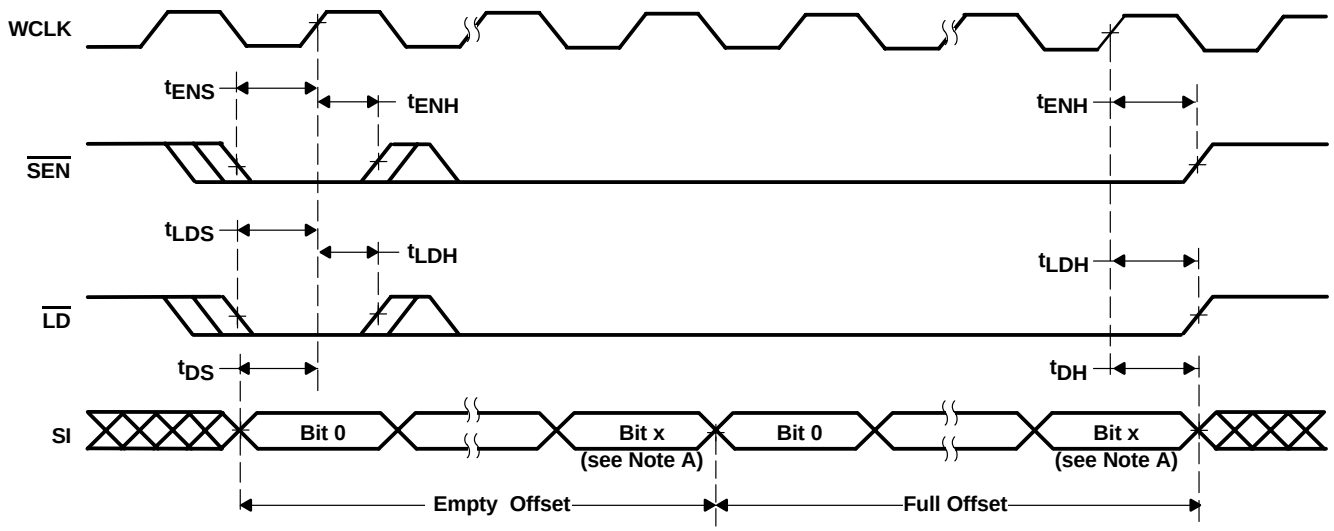
C. $\overline{OE}$ = low

D. W1, W2, W3 = first, second, and third words written to the FIFO after master reset.

E. There must be at least two words written to the FIFO before a retransmit operation can be invoked.

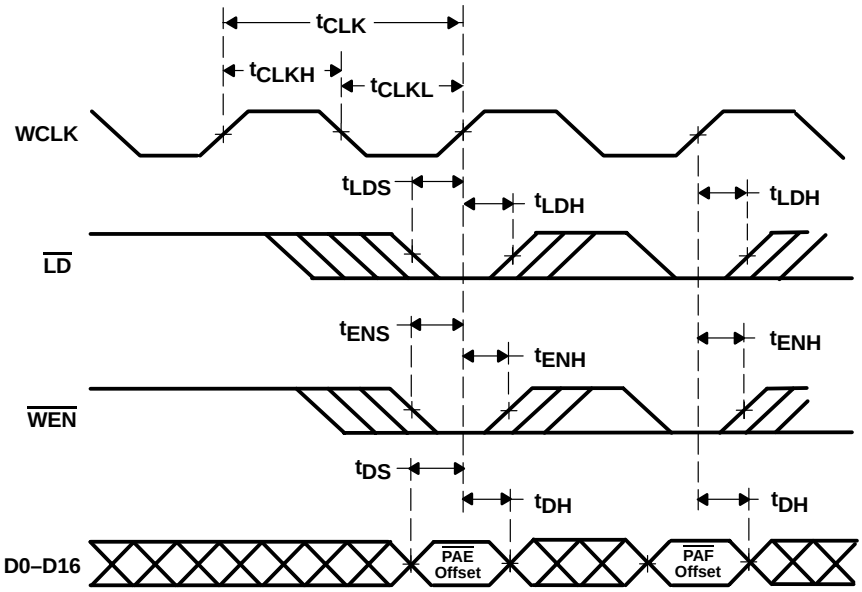
F. RM is set low during $\overline{MRS}$.

Figure 11. Zero-Latency Retransmit Timing (FWFT Mode)



NOTE A: x = 9 for the SN74V3640, x = 10 for the SN74V3650, x = 11 for the SN74V3660, x = 12 for the SN74V3670, x = 13 for the SN74V3680, x = 14 for the SN74V3690.

Figure 12. Serial Loading of Programmable Flag Registers (FWFT Mode)



NOTE A: This diagram shows programming with an input bus width of 36 bits.

Figure 13. Parallel Loading of Programmable Flag Registers (Standard and FWFT Modes)

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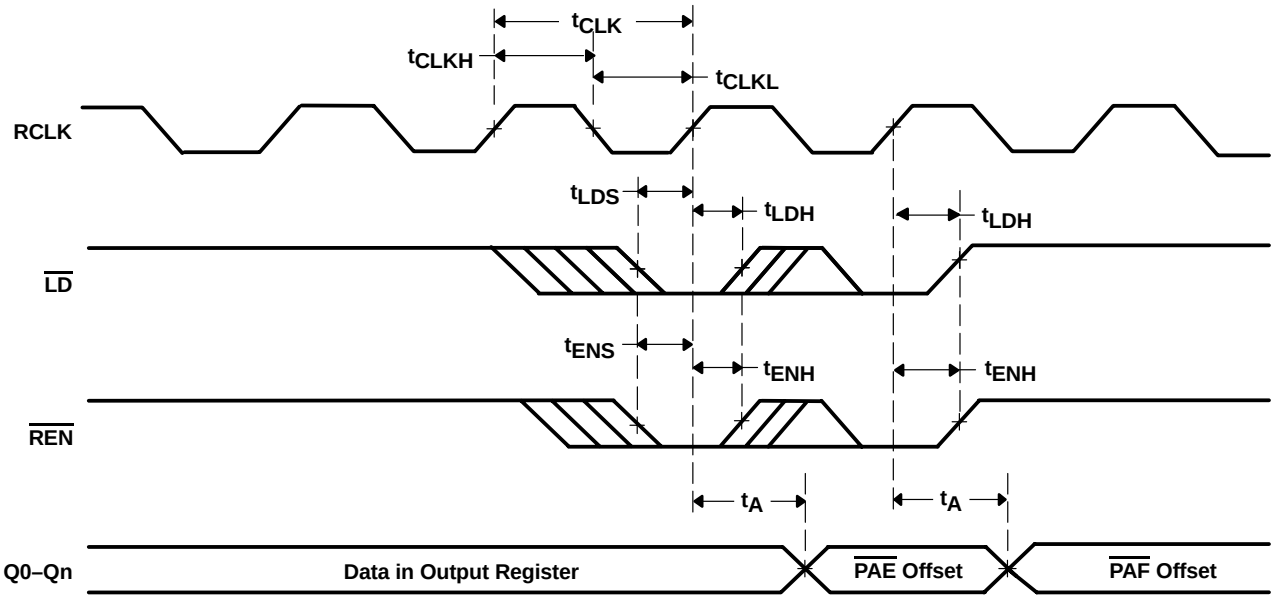

NOTES: A. OE = low
B. This diagram shows reading of offset registers with an output bus width of 36 bits.

Figure 14. Parallel Read of Programmable Flag Registers (Standard and FWFT Modes)

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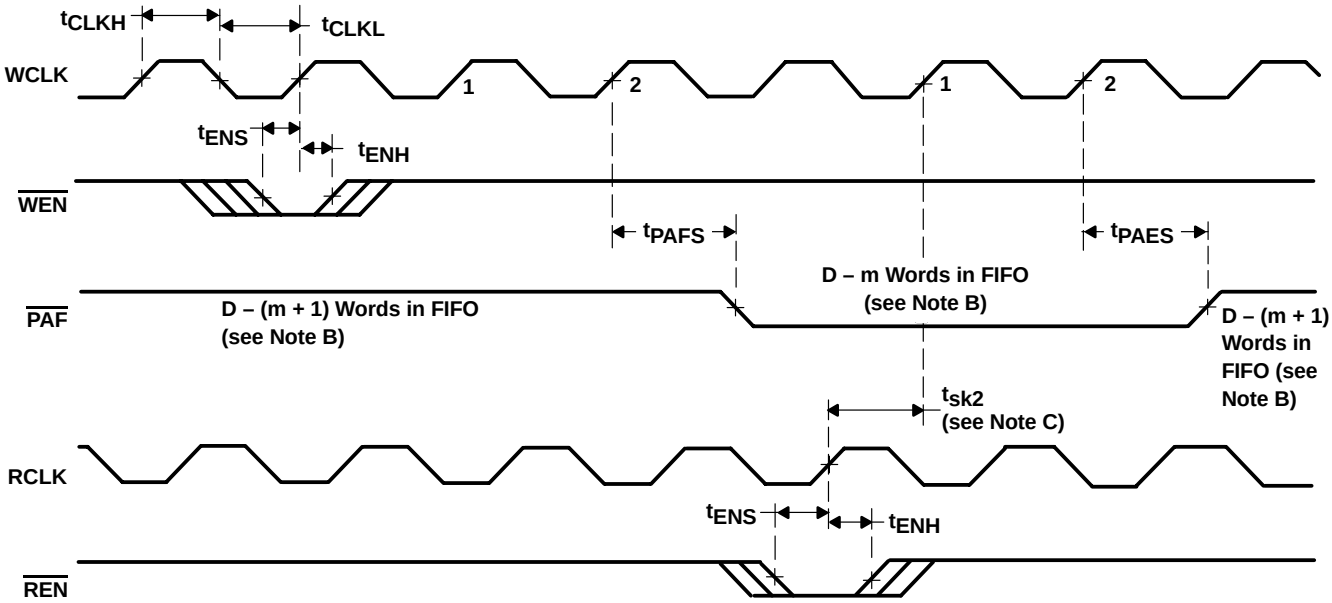

NOTES: A. m = $\overline{\text{PAF}}$ offset

B. D = maximum FIFO depth
In FWFT mode: D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 4097 for the SN74V3660, and D = 8193 for the SN74V3670, D = 16385 for the SN74V3680, and D = 32769 for the SN74V3690.
In standard mode: D = 1024 for the SN74V3640, D = 2048 for the SN74V3650, D = 4096 for the SN74V3660, D = 8192 for the SN74V3670, D = 16384 for the SN74V3680, D = 32768 for the SN74V3690.

C. t_{sk2} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{\text{PAF}}$ goes high (after one WCLK cycle + t_{PAFS}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{sk2}, $\overline{\text{PAF}}$ deassertion time may be delayed one additional WCLK cycle.

D. $\overline{\text{PAF}}$ is asserted and updated on the rising edge of WCLK only.

E. Select this mode by setting PFM high during master reset.

Figure 15. Synchronous Programmable Almost-Full Flag Timing (Standard and FWFT Modes)

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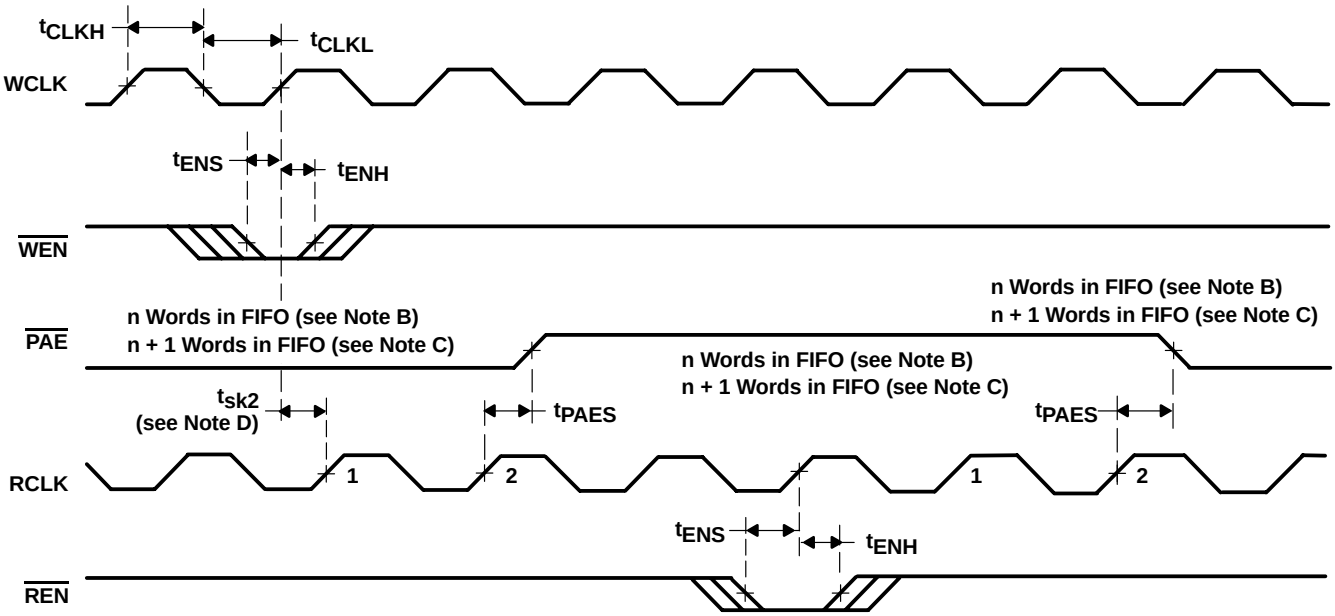

NOTES: A. n = $\overline{PAE}$ offset
B. For standard mode
C. For FWFT mode
D. t_{sk2} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{PAE}$ goes high (after one RCLK cycle + t_{PAES}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{sk2}, $\overline{PAE}$ deassertion can be delayed one additional RCLK cycle.
E. $\overline{PAE}$ is asserted and updated on the rising edge of WCLK only.
F. Select this mode by setting PFM high during master reset.

Figure 16. Synchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Modes)

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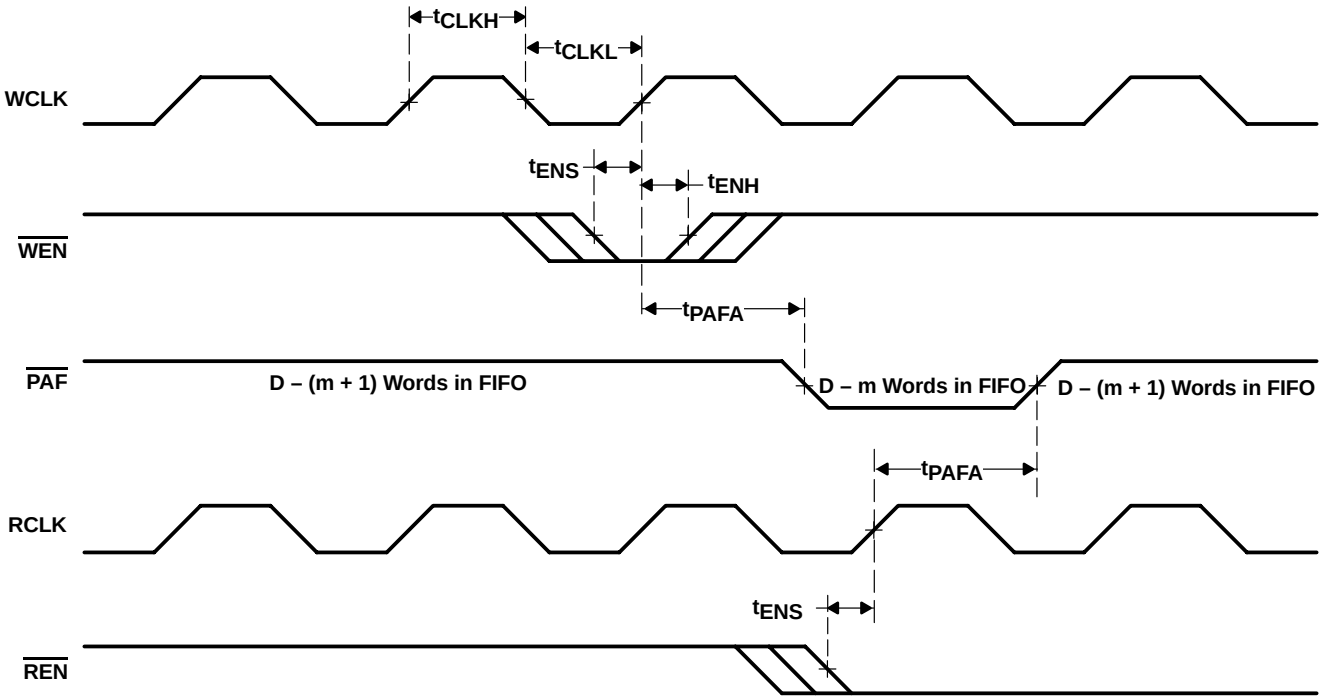
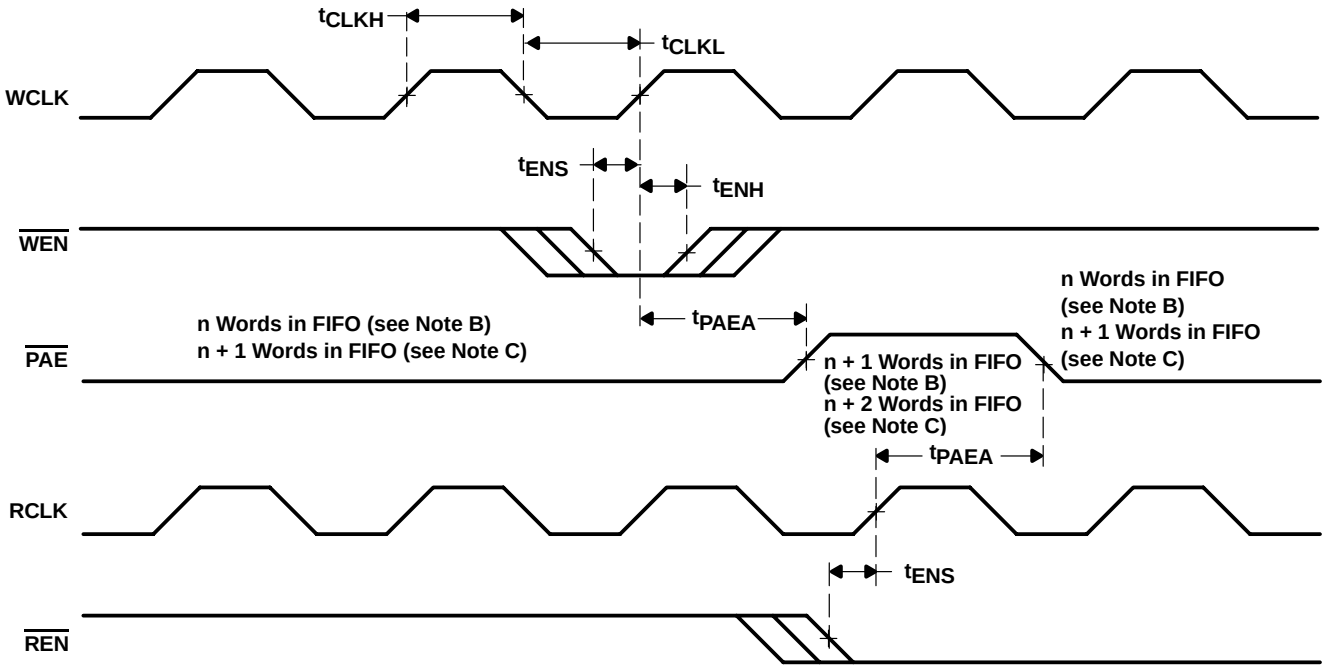


NOTES: A. m = $\overline{\text{PAF}}$ offset
B. D = maximum FIFO depth
In FWFT mode: D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 4097 for the SN74V3660, D = 8193 for the SN74V3670, D = 16385 for the SN74V3680, and D = 32769 for the SN74V3690.
In standard mode: D = 1024 for the SN74V3640, D = 2048 for the SN74V3650, D = 4096 for the SN74V3660, D = 8192 for the SN74V3670, D = 16384 for the SN74V3680, and D = 32768 for the SN74V3690.
C. $\overline{\text{PAF}}$ is asserted to low on WCLK transition and reset to high on RCLK transition.
D. Select this mode by setting PFM low during master reset.

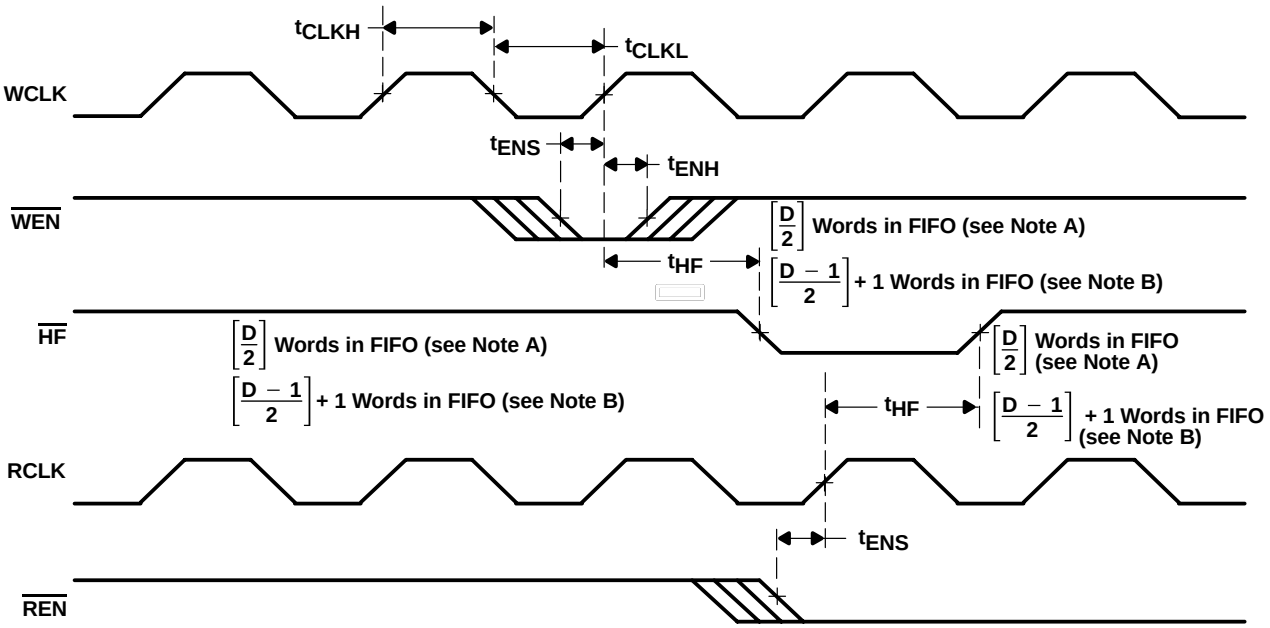
Figure 17. Asynchronous Programmable Almost-Full Flag Timing (Standard and FWFT Modes)

PRODUCT PREVIEW



NOTES: A. n = $\overline{\text{PAE}}$ offset
B. For standard mode
C. For FWFT mode
D. $\overline{\text{PAE}}$ is asserted low on RCLK transition and reset to high on WCLK transition.
E. Select this mode by setting PFM low during master reset.

Figure 18. Asynchronous Programmable Almost-Empty Flag Timing (Standard and FWFT Modes)



NOTES: A. In standard mode: D = maximum FIFO depth. D = 1024 for the SN74V3640, D = 2048 for the SN74V3650, D = 4096 for the SN74V3660, D = 8192 for the SN74V3670, D = 16384 for the SN74V3680, and D = 32768 for the SN74V3690.

B. In FWFT mode: D = maximum FIFO depth. D = 1025 for the SN74V3640, D = 2049 for the SN74V3650, D = 4097 for the SN74V3660, D = 8193 for the SN74V3670, D = 16385 for the SN74V3680, and D = 32769 for the SN74V3690.

Figure 19. Half-Full Flag Timing (Standard and FWFT Modes)

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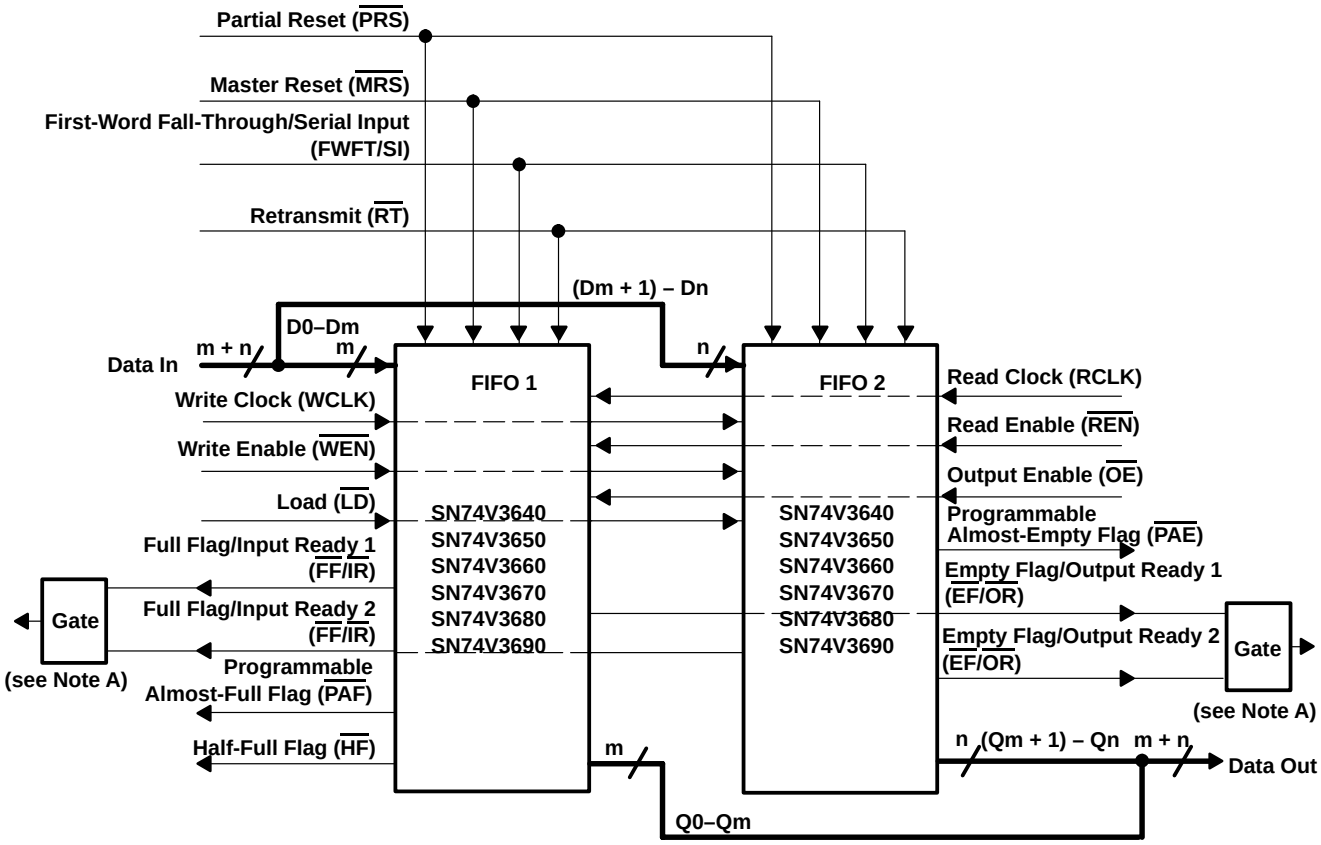
operating configurations

width-expansion configuration

Word width can be increased by connecting the control signals of multiple devices together. Status flags can be detected from any one device. The exceptions are the $\overline{EF}$ and $\overline{FF}$ functions in standard mode and the $\overline{IR}$ and $\overline{OR}$ functions in FWFT mode. Because of variations in skew between RCLK and WCLK, it is possible for $\overline{EF}$/$\overline{FF}$ deassertion and $\overline{IR}$/$\overline{OR}$ assertion to vary by one cycle between FIFOs. In standard mode, such problems can be avoided by creating composite flags, that is, ANDing $\overline{EF}$ of every FIFO and separately ANDing $\overline{FF}$ of every FIFO. In FWFT mode, composite flags can be created by ORing $\overline{OR}$ of every FIFO and separately ORing $\overline{IR}$ of every FIFO.

Figure 23 demonstrates a width expansion using two SN74V3640, SN74V3650, SN74V3660, SN74V3670, SN74V3680, and SN74V3690 devices. D0–D35 from each device form a 72-bit-wide input bus and Q0–Q35 from each device form a 72-bit-wide output bus. Any word width can be attained by adding additional SN74V3640, SN74V3650, SN74V3660, SN74V3670, SN74V3680, and SN74V3690 devices.



NOTES: A. Use an $\overline{OR}$ gate in FWFT mode and an AND gate in standard mode.
B. Do not connect any output control signals together directly.
C. FIFO 1 and FIFO 2 must be the same depth, but can be different word widths.

Figure 20. 1024 × 72, 2048 × 72, 4096 × 72, 8192 × 72, 16384 × 72, 32768 × 72 Width-Expansion Block Diagram

depth-expansion configuration (FWFT mode only)

The SN74V3640 easily can be adapted to applications requiring depths greater than 1024 for the SN74V3640, 2048 for the SN74V3650, 4096 for the SN74V3660, 8192 for the SN74V3670, 16384 for the SN74V3680, and 32768 for the SN74V3690, with an 18-bit bus width. In FWFT mode, the FIFOs can be connected in series (the data outputs of one FIFO connected to the data inputs of the next), with no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. Figure 24 shows a depth expansion using two SN74V3640, SN74V3650, SN74V3660, SN74V3670, SN74V3680, and SN74V3690 devices.

Care should be taken to select FWFT mode during master reset for all FIFOs in the depth-expansion configuration. The first word written to an empty configuration passes from one FIFO to the next (ripple down) until it finally appears at the outputs of the last FIFO in the chain. No read operation is necessary, but the RCLK of each FIFO must be free running. Each time the data word appears at the outputs of one FIFO, that device's $\overline{OR}$ line goes low, enabling a write to the next FIFO in line.

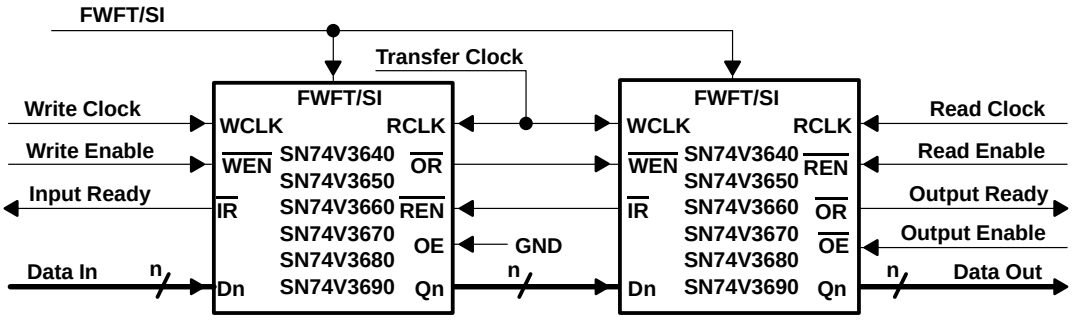


Figure 21. 2048 × 36, 4096 × 36, 8192 × 36, 16384 × 36, 32768 × 36, 65536 × 36 Depth-Expansion Block Diagram

For an empty-expansion configuration, the amount of time it takes for $\overline{OR}$ of the last FIFO in the chain to go low (i.e., valid data to appear on the last FIFO's outputs) after a word has been written to the first FIFO is the sum of the delays for each FIFO:

$$(n-1) \times (4 \times \text{transfer clock}) + 3t_{RCLK} \quad (1)$$

Where:

n = number of FIFOs in the expansion
t_{RCLK} = RCLK period

Note that extra cycles should be added for the possibility that the t_{sk1} specification is not met between WCLK and the transfer clock, or RCLK and the transfer clock, for the $\overline{OR}$ flag.

The ripple-down delay is noticeable only for the first word written to an empty-depth-expansion configuration. There will be no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full-depth-expansion configuration will bubble up from the last FIFO to the previous one until, finally, it moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's $\overline{IR}$ line goes low, enabling the preceding FIFO to write a word to fill it.

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depth-expansion configuration (FWFT mode only) (continued)

For a full expansion configuration, the amount of time it takes for $\overline{IR}$ of the first FIFO in the chain to go low after a word has been read from the last FIFO is the sum of the delays for each individual FIFO:

$$(n-1) \times (3 \times \text{transfer clock}) + 2t_{WCLK} \quad (2)$$

Where:

n = number of FIFOs in the expansion
t_{WCLK} = WCLK period

Note that extra cycles should be added for the possibility that the t_{sk1} specification is not met between RCLK and the transfer clock, or WCLK and the transfer clock, for the $\overline{IR}$ flag.

The transfer-clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in data moving as quickly as possible to the end of the chain and moving free locations to the beginning of the chain.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74V3680-15PEU	ACTIVE	LQFP	PEU	128	72	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	V3680-15	Samples
SN74V3680-6PEU	ACTIVE	LQFP	PEU	128	72	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	V3680-6	Samples
SN74V3690-6PEU	ACTIVE	LQFP	PEU	128	72	RoHS & Green	NIPDAU	Level-3-220C-168 HR	0 to 70	V3690-6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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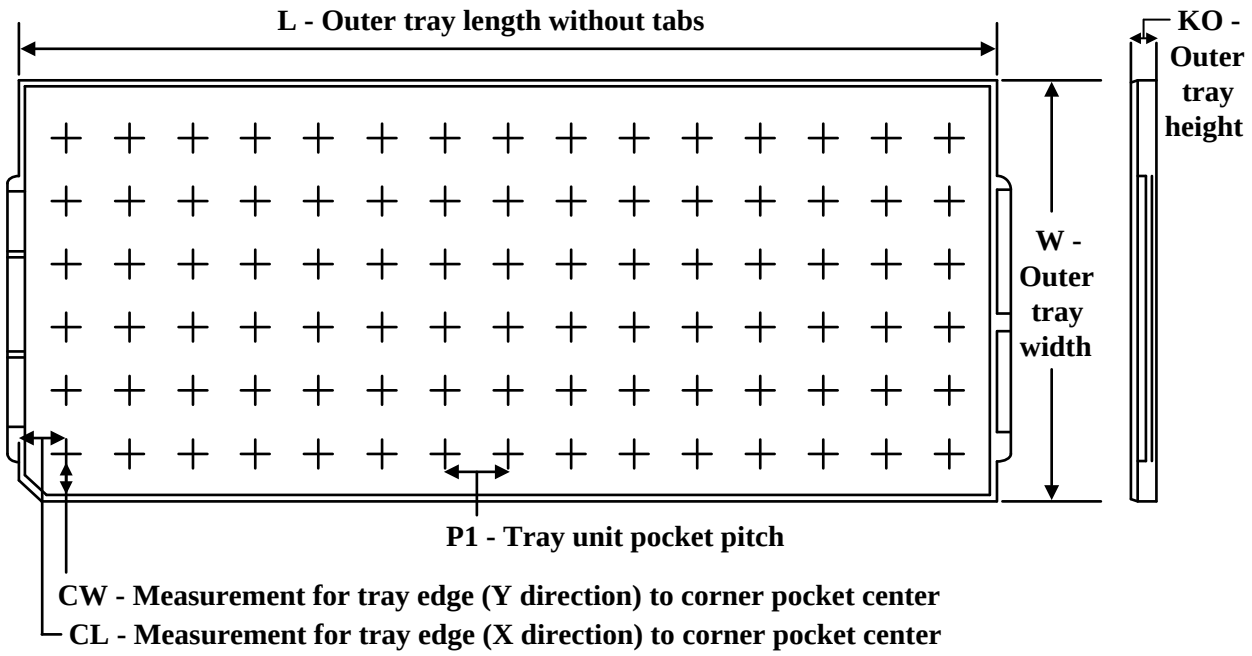
TRAY

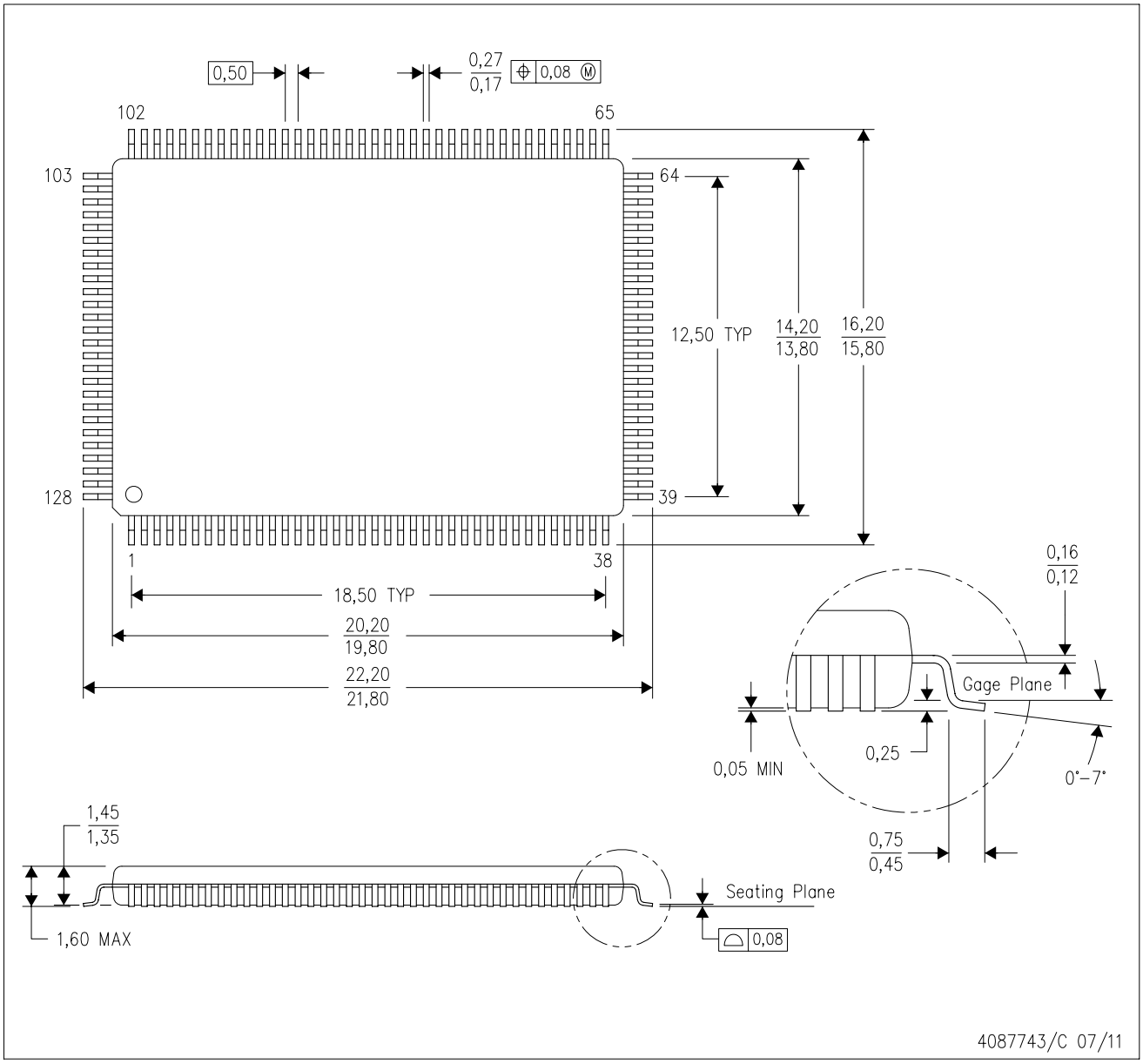


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN74V3680-15PEU	PEU	LQFP	128	72	6X12	150	315	135.9	7620	25.4	17.8	15.45
SN74V3680-6PEU	PEU	LQFP	128	72	6X12	150	315	135.9	7620	25.4	17.8	15.45
SN74V3690-6PEU	PEU	LQFP	128	72	6X12	150	315	135.9	7620	25.4	17.8	15.45

PEU (R–PQFP–G128) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–026

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