



**THE DATASHEET OF
SN74AHCT174DGVRG4**



SN54AHCT174, SN74AHCT174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS419F – JUNE 1998 – REVISED APRIL 2002

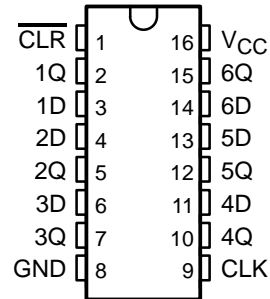
- **Inputs Are TTL-Voltage Compatible**
- **Contain Six Flip-Flops With Single-Rail Outputs**
- **Applications Include:**
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description

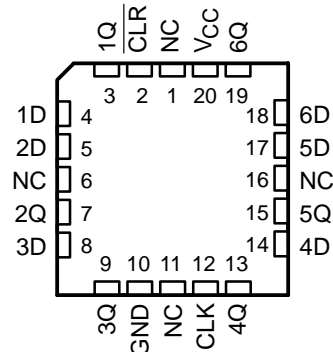
These positive-edge-triggered D-type flip-flops have a direct clear (CLR) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

SN54AHCT174 . . . J OR W PACKAGE
SN74AHCT174 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHCT174 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHCT174N	SN74AHCT174N
	SOIC – D	Tube	SN74AHCT174D	AHCT174
		Tape and reel	SN74AHCT174DR	
	SOP – NS	Tape and reel	SN74AHCT174NSR	AHCT174
	SSOP – DB	Tape and reel	SN74AHCT174DBR	HB174
	TSSOP – PW	Tape and reel	SN74AHCT174PWR	HB174
TVSOP – DGV	Tape and reel	SN74AHCT174DGV	HB174	
–55°C to 125°C	CDIP – J	Tube	SNJ54AHCT174J	SNJ54AHCT174J
	CFP – W	Tube	SNJ54AHCT174W	SNJ54AHCT174W
	LCCC – FK	Tube	SNJ54AHCT174FK	SNJ54AHCT174FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated

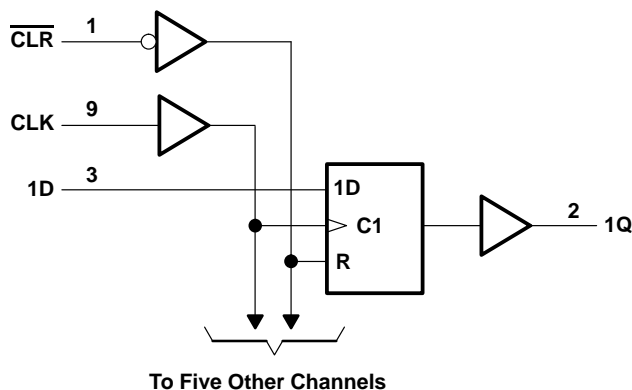
SN54AHCT174, SN74AHCT174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS419F – JUNE 1998 – REVISED APRIL 2002

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54AHCT174, SN74AHCT174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS419F – JUNE 1998 – REVISED APRIL 2002

recommended operating conditions (see Note 3)

		SN54AHCT174		SN74AHCT174		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-8		-8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall time		20		20	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT174		SN74AHCT174		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1			0.1	V	
	I _{OL} = 8 mA				0.36		0.44	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1			±1*	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V				4		40	μA	
ΔI _{CC} †	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5	1.5	mA	
C _i	V _I = V _{CC} or GND	5 V		2	10			10	pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

		T _A = 25°C		SN54AHCT174		SN74AHCT174		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low	5		5		5	ns
		CLK high or low	5		5		5	
t _{su}	Setup time before CLK↑	Data	5		5		5	ns
		CLR inactive	3.5		3.5		3.5	
t _h	Hold time, data after CLK↑		0		0		0	ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54AHCT174, SN74AHCT174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS419F – JUNE 1998 – REVISED APRIL 2002

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT174		SN74AHCT174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	100**	135**		80**		80		MHz
			$C_L = 50\text{ pF}$	80	115		65		65		
t_{PHL}	$\overline{\text{CLR}}$	Any Q	$C_L = 15\text{ pF}$		7.6**	10.4**	1**	13**	1	13	ns
t_{PLH}	CLK	Any Q	$C_L = 15\text{ pF}$		5.8**	7.8**	1**	9**	1	9	ns
t_{PHL}					5.8**	7.8**	1**	9**	1	9	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	$C_L = 50\text{ pF}$		8.1	11.4	1	13	1	13	ns
t_{PLH}	CLK	Any Q	$C_L = 50\text{ pF}$		6.3	8.8	1	10	1	10	ns
t_{PHL}					6.3	8.8	1	10	1	10	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1**				1	ns

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

*** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHCT174			UNIT
		MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic V_{OL}		0.8		V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic V_{OL}		-0.8		V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic V_{OH}		4		V
$V_{\text{IH(D)}}$	High-level dynamic input voltage		2		V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

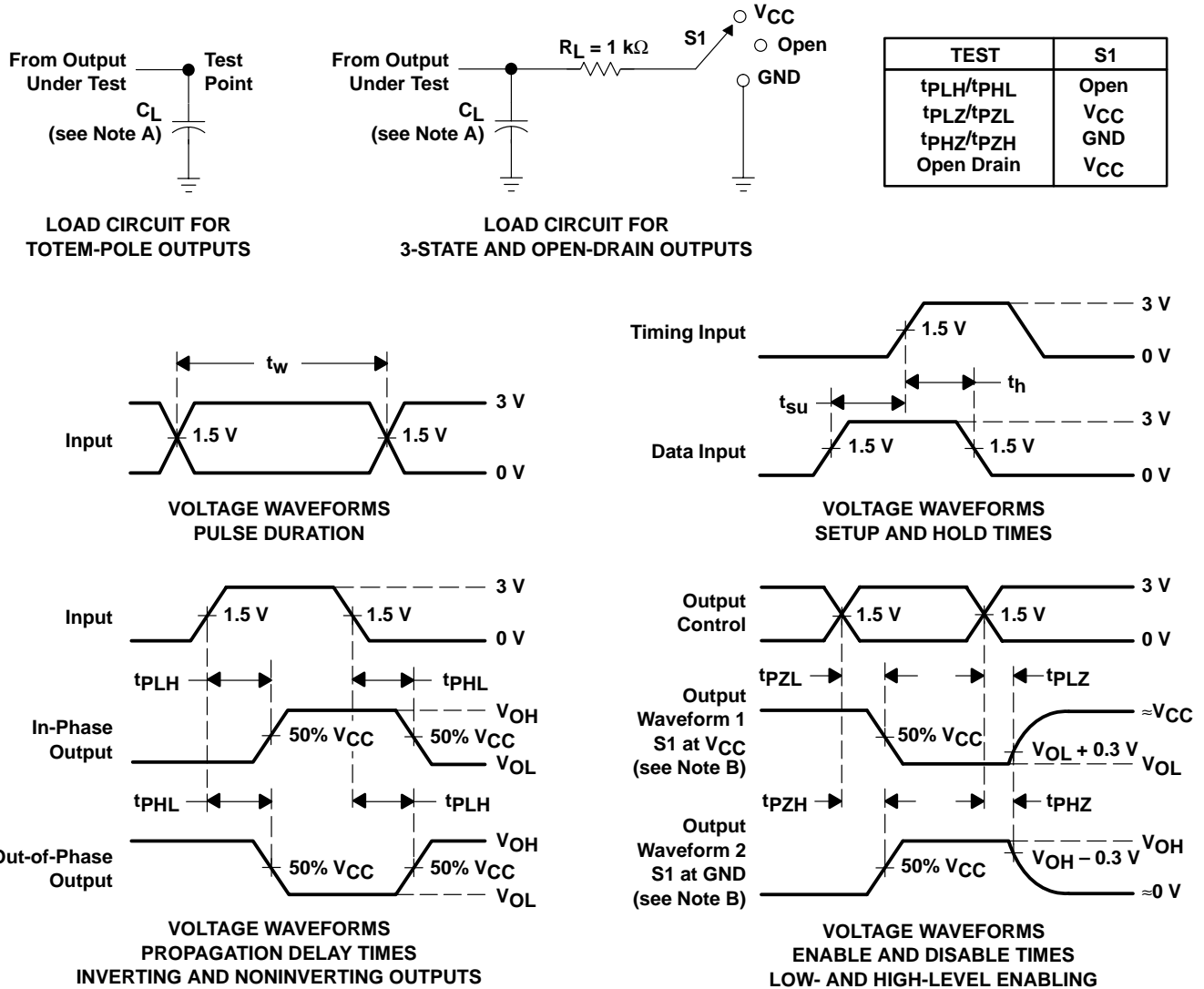
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	28	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN74AHCT174DGVRG4 on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management