



**THE DATASHEET OF
SN74BCT574DW**



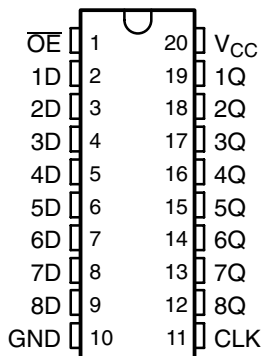
SN54BCT574, SN74BCT574 OCTAL TRANSPARENT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS074C – SEPTEMBER 1991 – REVISED MARCH 2003

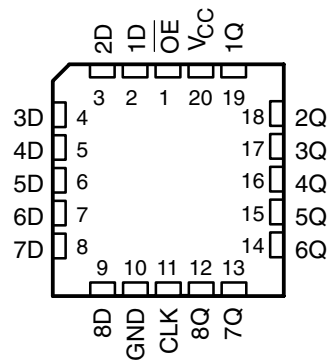
- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- Full Parallel Access for Loading

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54BCT574 . . . J OR W PACKAGE
SN74BCT574 . . . DB, DW, N, OR NS PACKAGE
(TOP VIEW)



SN54BCT574 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'BCT574 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT574N	SN74BCT574N
	SOIC – DW	Tube	SN74BCT574DW	BCT574
		Tape and reel	SN74BCT574DWR	
	SOP – NS	Tape and reel	SN74BCT574NSR	BCT574
SSOP – DB	Tape and reel	SN74BCT574DBR	BT574	
–55°C to 125°C	CDIP – J	Tube	SNJ54BCT574J	SNJ54BCT574J
	CFP – W	Tube	SNJ54BCT574W	SNJ54BCT574W
	LCCC – FK	Tube	SNJ54BCT574FK	SNJ54BCT574FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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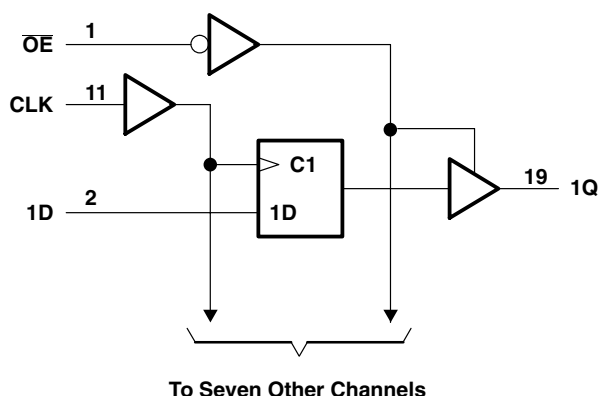
description/ordering information (continued)

\overline{OE} does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_{OH}	–0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$)	–30 mA
Current into any output in the low state: SN54BCT574	96 mA
SN74BCT574	128 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

		SN54BCT574			SN74BCT574			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT574		SN74BCT574		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2		-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3	2.4	3.3	V	
		$I_{OH} = -12\text{ mA}$	2	3.2				
		$I_{OH} = -15\text{ mA}$			2	3.1		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.38	0.55		V	
		$I_{OL} = 64\text{ mA}$				0.42		0.55
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$			0.4		0.4	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			20		20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-0.6		-0.6	mA
I_{OS}^\ddagger	$V_{CC} = 5.5\text{ V}$,	$V_O = 0$	-100		-225	-100	-225	mA
I_{OZH}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$			50		50	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.5\text{ V}$			-50		-50	μA
I_{CCL}	$V_{CC} = 5.5\text{ V}$,	Outputs open		38.1	62	38.1	62	mA
I_{CCH}	$V_{CC} = 5.5\text{ V}$,	Outputs open		4.9	8	4.9	8	mA
I_{CCZ}	$V_{CC} = 5.5\text{ V}$,	Outputs open		4.5	8	4.9	8	mA
C_i	$V_{CC} = 5\text{ V}$,	$V_I = 2.5\text{ V}$ or 0.5 V				5.5		pF
C_o	$V_{CC} = 5\text{ V}$,	$V_O = 2.5\text{ V}$ or 0.5 V				7.5		pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54BCT574		SN74BCT574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		77		77		77	MHz
t_w	Pulse duration, CLK high or low	6.5		6.5		6.5		ns
t_{su}	Setup time, data before CLK↑	High	4.5	4.5	4.5			ns
		Low	6	6	6			
t_h	Hold time, data after CLK↑		0	1	0			ns



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

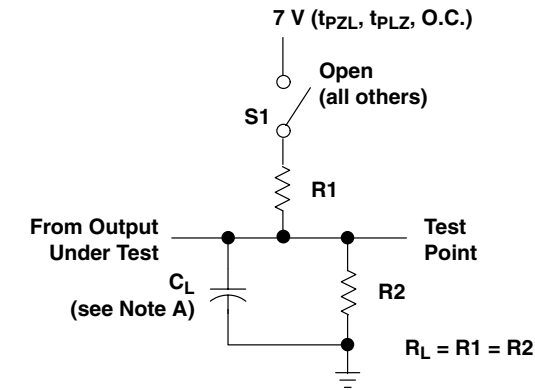
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54BCT574		SN74BCT574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			77			77		77		MHz
t_{PLH}	CLK	Q	2.2	6.5	8.6	2.2	11.2	2.2	10	ns
t_{PHL}			2.8	6.1	8	2.8	9.7	2.8	8.9	
t_{PZH}	\overline{OE}	Q	2.5	6.4	8.1	2.5	10.9	2.5	10.4	ns
t_{PZL}			3.7	7.3	9.2	3.7	11.3	3.7	10.9	
t_{PHZ}	\overline{OE}	Q	1	4.4	7.4	1	8	1	7.5	ns
t_{PLZ}			1.3	4.2	5.8	1.3	7.1	1.3	6.4	



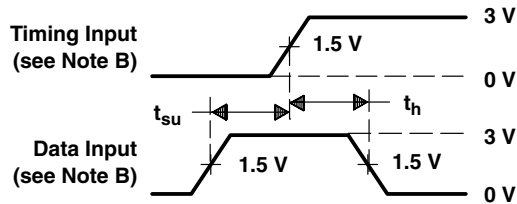
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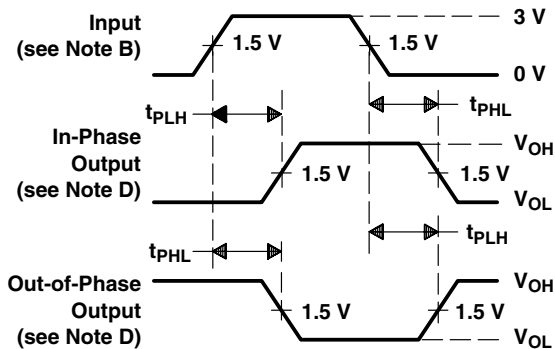
PARAMETER MEASUREMENT INFORMATION



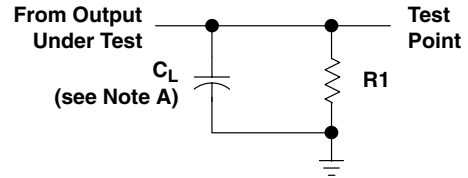
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



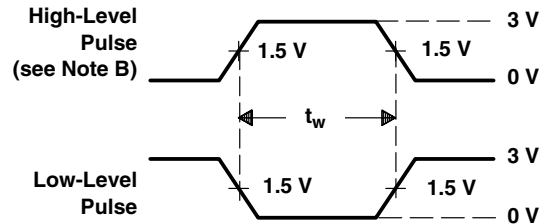
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



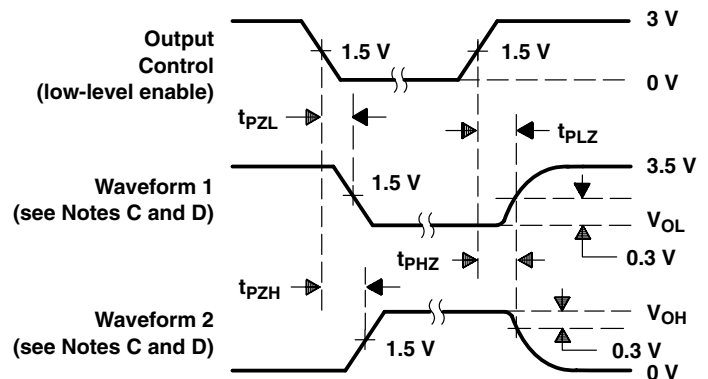
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.
 - When measuring propagation delay times of 3-state outputs, switch S1 is open.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9583601QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9583601QR A SNJ54BCT574J	Samples
SN74BCT574DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT574	Samples
SN74BCT574N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74BCT574N	Samples
SNJ54BCT574J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9583601QR A SNJ54BCT574J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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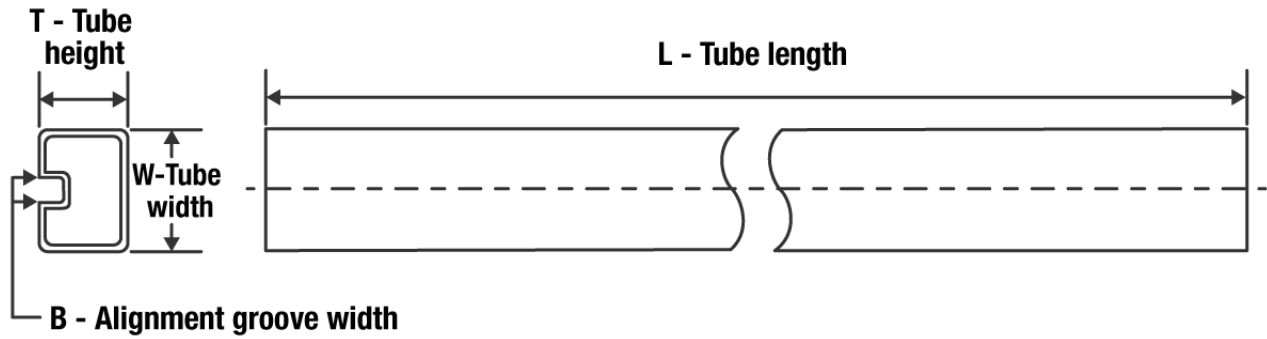
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OTHER QUALIFIED VERSIONS OF SN54BCT574, SN74BCT574 :

- Catalog : [SN74BCT574](#)
- Military : [SN54BCT574](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74BCT574DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT574N	N	PDIP	20	20	506	13.97	11230	4.32

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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