THE DATASHEET OF

CY8C201A0-LDX2I

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CY8C201A0

CapSense® Express™ Slider Capacitive Controllers

Features

- Capacitive slider and button input
  - Choice of configurations:
    - 10-segment slider
    - 5-segment slider with remaining five pins configurable as CapSense® or GPIO
  - Robust sensing algorithm
  - High sensitivity, low noise
  - Immunity to RF and AC noise.
  - Low radiated EMC noise
  - Supports wide range of input capacitance, sensor shapes, and sizes
- Target applications
  - Printers
  - Cellular handsets
  - LCD monitors
  - Portable DVD players
- Low operating current
  - Active current: continuous sensor scan: 1.5 mA
  - Deep sleep current: 4 µA
- Industry's best configurability
  - Custom sensor tuning, one optional capacitor
  - Output supports strong drive for LED
  - Output state can be controlled through I^2C or directly from CapSense input state
  - Run time reconfigurable over I^2C
- Advanced features
  - Interrupt outputs
  - User defined Inputs
  - Wake on interrupt input
  - Sleep control pin
  - Nonvolatile storage of custom settings
  - Easy integration into existing products – configure output to match system
  - No external components required
  - World-class free configuration tool
- Wide range of operating voltages
  - 2.4 V to 2.9 V
  - 3.10 V to 3.6 V
  - 4.75 V to 5.25 V
- I^2C communication
  - Supported from 1.8 V
  - Internal pull-up resistor support option
  - Data rate up to 400 kbps
  - Configurable I^2C addressing
- Industrial temperature range: –40 °C to +85 °C
- Available in 16-pin QFN and 16-pin SOIC Package

Overview

These CapSense Express™ controllers support four to ten capacitive sensing CapSense buttons. The device functionality is configured through an I^2C port and can be stored in the onboard nonvolatile memory for automatic loading at power on. The CapSense Express controller enables the control of 10 I/Os configurable as one capacitive sensing slider (10 segments)[1] or one slider (5 segments) with the rest of the pins as buttons or GPIOs (for driving LEDs or interrupt signals based on various button conditions).

The four key blocks that make up these devices are: a robust capacitive sensing core with high immunity against radiated and conductive noise, control registers with nonvolatile storage, configurable outputs, and I^2C communications. The user can configure registers with parameters needed to adjust the operation and sensitivity of the CapSense buttons and outputs and permanently store the settings. The standard I^2C serial communication interface enables the host to configure the device and to read sensor information in real time. The I^2C address is fully configurable without any external hardware strapping.

Note
1. This part should be selected only if the design requires a slider. This part cannot be configured to work without a slider. For 10 I/O requirements use CY8C20110.

Errata: For information on silicon errata, see "Errata" on page 35. Details include trigger conditions, devices affected, and proposed workaround.

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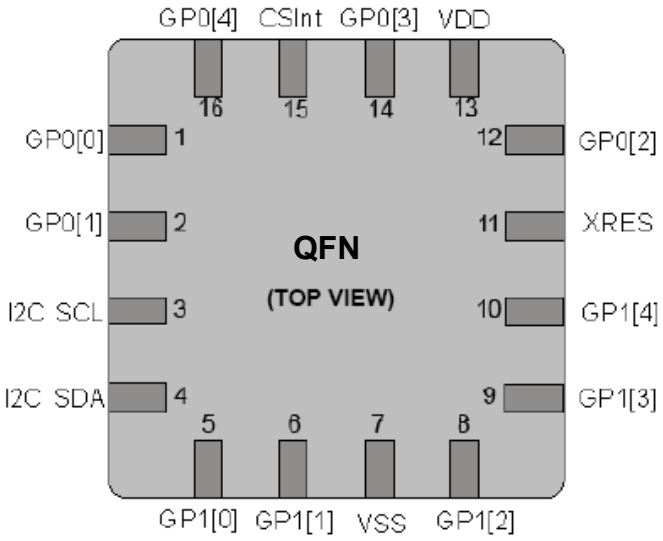
Pinouts

Figure 1. 16-pin QFN (3 × 3 × 0.6 mm) (no e-pad) Pinout – 5/10 Segment Slider



Pin Definitions

16-pin QFN (no e-pad) – 5/10 Segment Slider

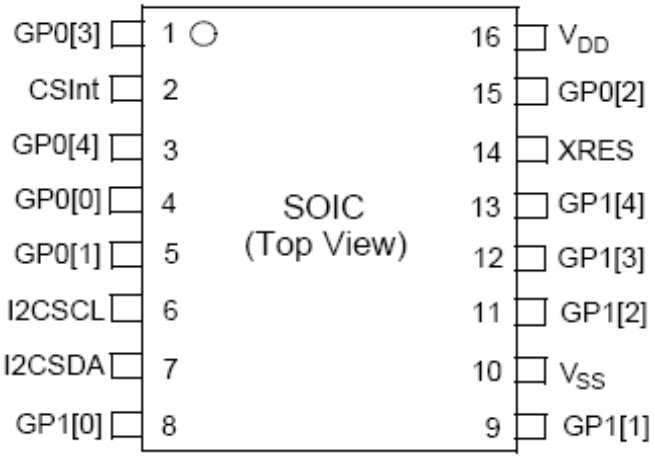
Pin No.	Name	Description
1	GP0[0]	Configurable as CapSense or GPIO
2	GP0[1]	Configurable as CapSense or GPIO
3	I^2C SCL	I^2C clock
4	I^2C SDA	I^2C data
5	GP1[0]	Configurable as CapSense or GPIO
6	GP1[1][2]	Configurable as CapSense or GPIO
7	VSS	Ground connection
8	GP1[2][2]	Configurable as CapSense or GPIO
9	GP1[3]	Configurable as CapSense or GPIO
10	GP1[4]	Configurable as CapSense or GPIO
11	XRES	Active high external reset with internal pull-down
12	GP0[2]	Configurable as CapSense or GPIO
13	VDD	Supply voltage
14	GP0[3]	Configurable as CapSense or GPIO
15	CSInt	Integrating capacitor input. The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 1 nF to 4.7 nF
16	GP0[4]	Configurable as CapSense or GPIO

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at http://www.amkor.com.

Note
2. Avoid using GP1[1] and GP1[2] for driving LEDs. These two pins have special functions during power-up, which is used at factory. LEDs connected to these two pins blink during device power-up.

Pinouts

Figure 2. 16-pin SOIC (150 Mils) pinout – 5/10 Segment Slider



Pin Definitions

16-pin SOIC – 5/10 Segment Slider

Pin No.	Name	Description
1	GP0[3]	Configurable as CapSense or GPIO
2	CSint	Integrating capacitor input. The external capacitance is required only if 5:1 SNR cannot be achieved. Typical range is 1 nF to 4.7 nF.
3	GP0[4]	Configurable as CapSense or GPIO
4	GP0[0]	Configurable as CapSense or GPIO
5	GP0[1]	Configurable as CapSense or GPIO
6	I^2C SCL	I^2C clock
7	I^2C SDA	I^2C data
8	GP1[0]	Configurable as CapSense or GPIO
9	GP1[1][3]	Configurable as CapSense or GPIO
10	V_{SS}	Ground connection
11	GP1[2][3]	Configurable as V_{SS} CapSense or GPIO
12	GP1[3]	Configurable as CapSense or GPIO
13	GP1[4]	Configurable as CapSense or GPIO
14	XRES	Active high external reset with internal pull-down
15	GP0[2]	Configurable as CapSense or GPIO
16	V_{DD}	Supply voltage

Note
3. Avoid using GP1[1] and GP1[2] for driving LEDs. These two pins have special functions during power-up which is used at factory. LEDs connected to these two pins blink during the device power-up.

Typical Circuits

Figure 3. Circuit 1 – Five-Segment Slider with Status LED and Two Buttons with Backlighting LEDs

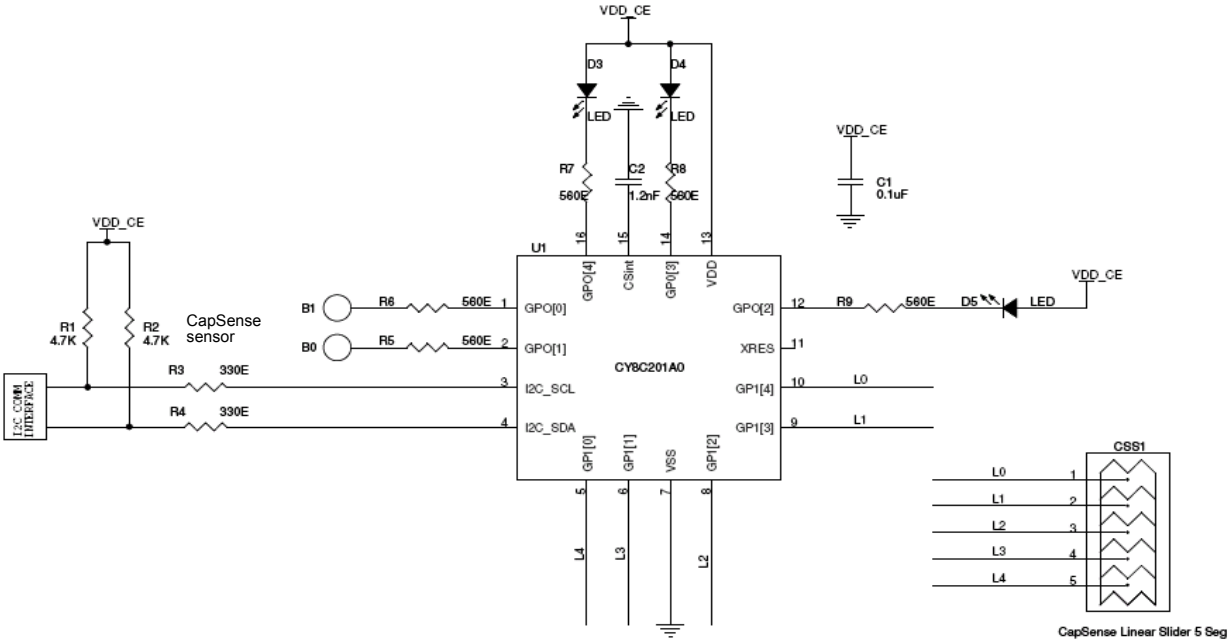
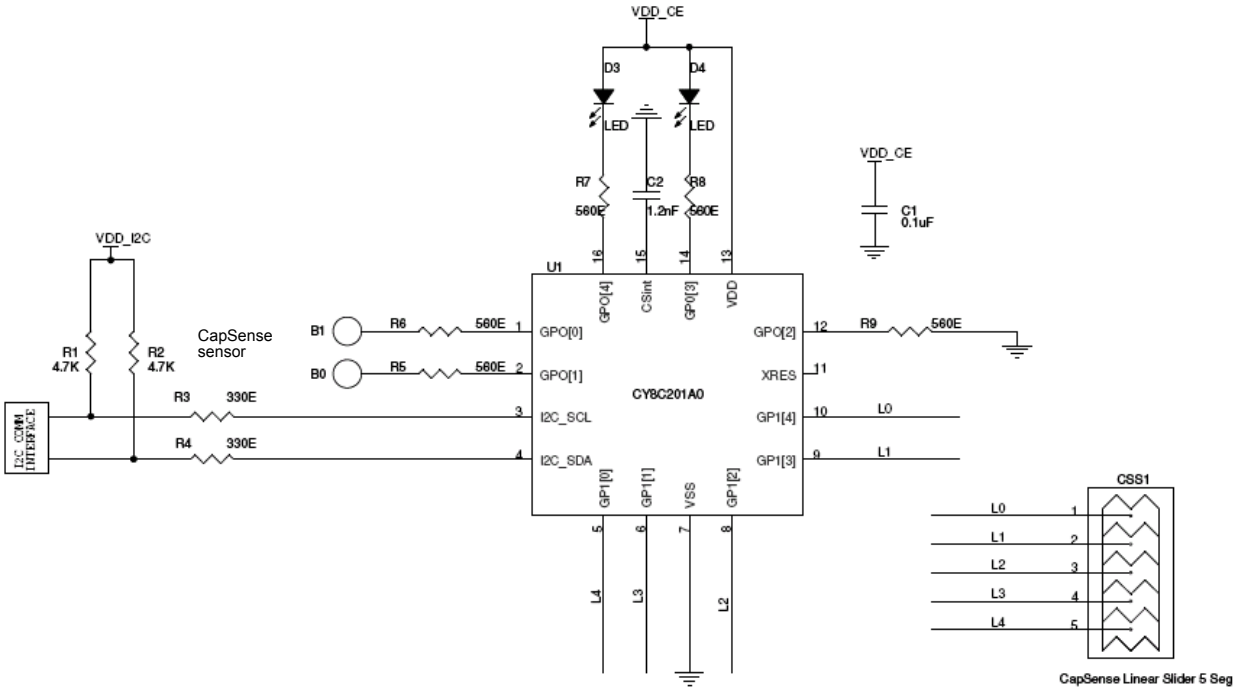


Figure 4. Circuit 2 – Compatibility with 1.8 V I²C Signaling[4, 5]

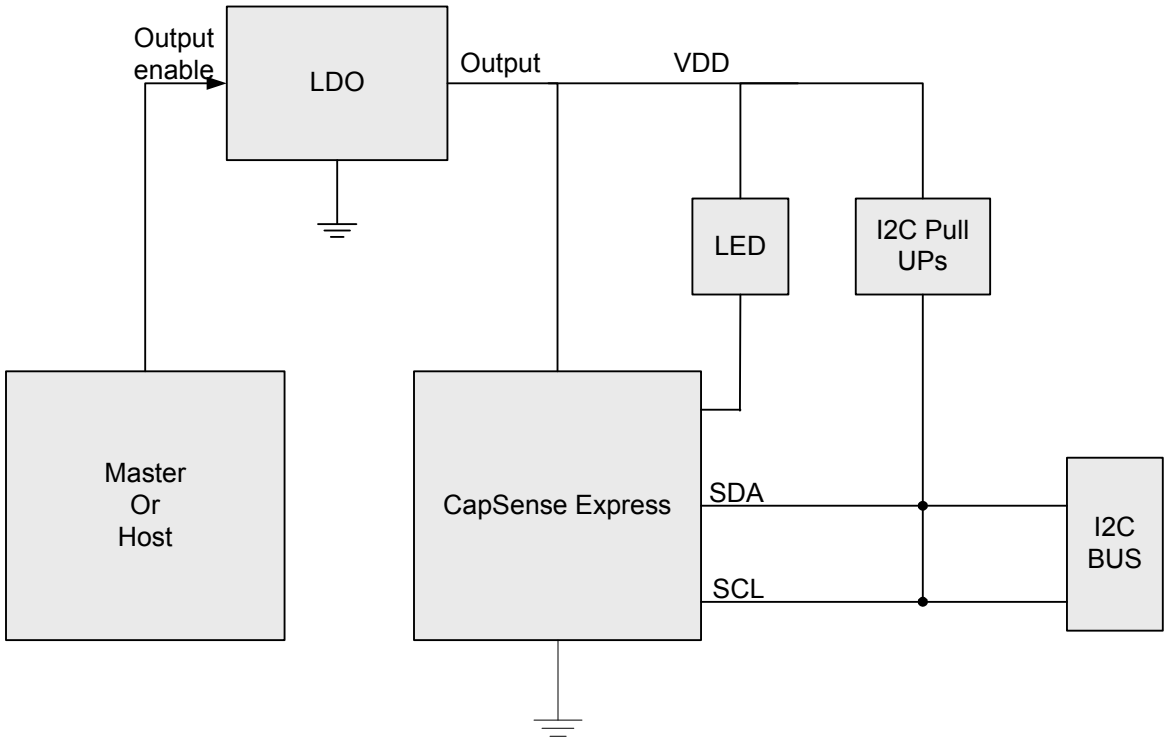


Notes

4. 1.8 V ≤ VDD_I2C ≤ VDD_CE and 2.4 V ≤ VDD_CE ≤ 5.25 V.
5. The I2C drive mode of the CapSense device should be configured properly before using in an I2C environment with external pull-ups. Please refer to I2C_ADDR_DM register and its factory setting.

Typical Circuits (continued)

Figure 5. Circuit 3 – Powering Down CapSense Express Device for Low Power Requirements [6]



Note

6. For low power requirements, if V_{DD} is to be turned off, the concept mentioned in this section can be used. The requirement is that the V_{DD}s of CapSense Express, I^2C pull-ups, and LEDs should be from same source such that turning off the V_{DD} ensures that no signal is applied to the device while it is unpowered. The I^2C signals should not be driven high by the master in this situation. If a port pin or group of port pins of the master can cater to the power supply requirements of the circuit, the LDO can be avoided.

I²C Interface

The CapSense Express devices support the industry standard I²C protocol, which can be used for:

- Configuring the device
- Reading the status and data registers of the device
- To control the device operation
- Executing commands

The I²C address can be modified during configuration.

I²C Device Addressing

The device uses a seven bit addressing protocol. The I²C data transfer is always initiated by the master sending one byte address; the first 7 bit contains address and the last LSB indicates the data transfer direction. Zero in the LSB bit indicates the write transaction form master and one indicates read transfer by the master. The following table shows the example for different I²C addresses.

Table 1. I²C Address Examples

7 Bit Slave Address	D7	D6	D5	D4	D3	D2	D1	D0	8 Bit Slave Address
1	0	0	0	0	0	0	1	0(W)	02
1	0	0	0	0	0	0	1	1(R)	03
75	1	0	0	1	0	1	1	0(W)	96
75	1	0	0	1	0	1	1	1(W)	97

I²C Clock Stretching

'Clock stretching' or 'bus stalling' in I²C communication protocol is a state in which the slave holds the SCL line low to indicate that it is busy. In this condition, the master is expected to wait till the SCL is released by the slave.

When an I²C master communicates with the CapSense Express device, the CapSense Express stalls the I²C bus after the reception of each byte (that is, just before the ACK/NAK bit) until processing of the byte is complete and critical internal functions are executed. It is recommended to use a fully I²C compliant master to communicate with CapSense Express device.

If an I²C master does not support clock stretching (a bit banged software I²C master), the master must wait for a specific amount of time (specified in Format for Register Write and Read on page 8) for each register write and read operation before the next bit is transmitted. Check the SCL status (should be high) before I²C master initiates any data transfer with CapSense Express. If the master fails to do so and continues to communicate, the communication is incorrect.

Also note that, while using CapSense Express Devices on an I²C bus, I²C master should not generate a start or stop condition in the I²C bus before CapSense Express device generates an acknowledgement (ACK/NCK) for the previous transaction. An acknowledgement state produced by the CapSense Express Device for the previous data transfer after start condition for new data transfer by the master may produce unexpected behavior from CapSense Express I²C slave interface.

The following diagrams represent the ACK time delays shown in Format for Register Write and Read on page 8 for write and read.

Also note that, while using CapSense Express Devices on an I²C bus, I²C master should not generate a start or stop condition in the I²C bus before CapSense Express device generating acknowledgement (ACK/NCK) for the previous transaction. An acknowledgement state produced by the CapSense Express Device for the previous data transfer after the master generates a start condition, may produce unexpected behavior from CapSense Express I²C slave interface.

Figure 6. Write ACK Time Representation[7]

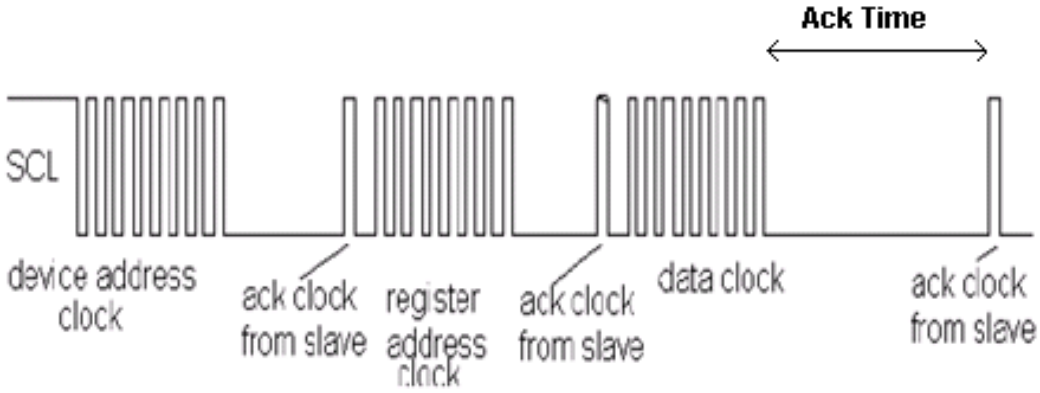
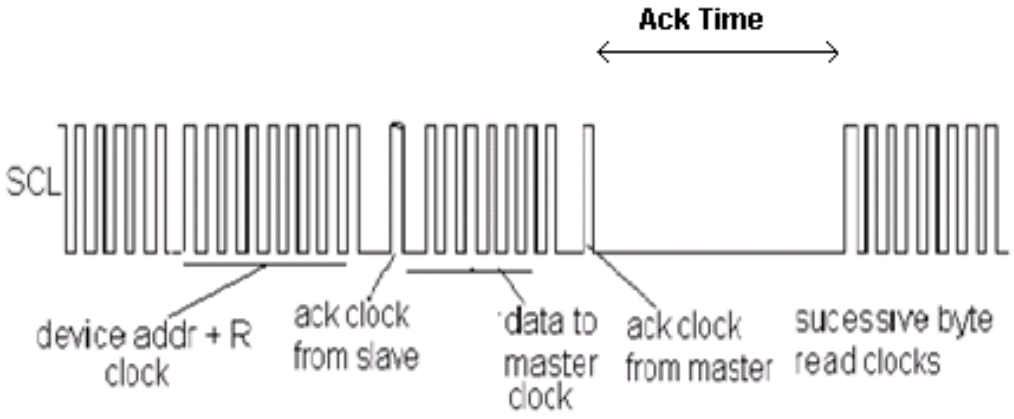


Figure 7. Read ACK Time Representation[8]



Format for Register Write and Read

Register write format

Start	Slave Addr + W	A	Reg Addr	A	Data	A	Data	A	. . . . .	Data	A	Stop

Register read format

Start	Slave Addr + W	A	Reg Addr	A	Stop							
Start	Slave Addr + R	A	Data	A	Data	A	. . . . .	Data	N	Stop		

Legends

Master
Slave

A – ACK
N – NAK

Notes
7. Time to process the received data.
8. Time taken for the device to send next byte.

Operating Modes of I²C Commands

Normal Mode

In normal mode of operation, the acknowledgment time [9] is optimized. The timings remain approximately the same for different configurations of the slave. To reduce the acknowledgment times in normal mode, the registers 0x06–0x09, 0x0C, 0x0D, 0x10–0x17, 0x50, 0x51, 0x57–0x60, 0x7E are given only read access. Write to these registers can be done only in setup mode.

Setup Mode

All registers have read and write access (except those which are read only) in this mode. The acknowledgment times [10] are longer compared to normal mode. When CapSense scanning is disabled (command code 0x0A in command register 0xA0), the acknowledgment times can be improved to values similar to the normal mode of operation.

Device Operation Modes

CapSense Express devices are configured to operate in any of the following three modes to meet different power consumption requirements

- Active Mode
- Periodic Sleep Mode
- Deep Sleep Mode

Active Mode

In the active mode, all the device blocks including the CapSense sub system are powered. Typical active current consumption of the device across the operating voltage range is 1.5 mA.

Periodic Sleep Mode

Sleep mode provides an intermediate power operation mode. It is enabled by configuring the corresponding device registers (0x7E, 0x7F). The device goes into sleep after there is no event for stay awake counter (Reg 0x80) number of sleep intervals. The device wakes up on sleep interval and It scans the capacitive sensors before going back to sleep again. If any sensor is active then the device wakes up. The device can also wake up from sleep mode with a GPIO interrupt. The sleep interval is configured through registers. The following sleep intervals are supported in CapSense Express:

- 1.95 ms (512 Hz)
- 15.6 ms (64 Hz)
- 125 ms (8 Hz)
- 1s (1 Hz)

The sleep interval should be 8 Hz or 1 Hz when using save to flash command. The configuration sequence should be:

1. Write configuration data to registers with sleep interval being 8 Hz or 1 Hz.
2. Save the settings to FLASH.
3. Change the sleep interval as per design.

Deep Sleep Mode

Deep sleep mode provides the lowest power consumption because there is no operation running. All CapSense scanning is disabled during this mode. In this mode, the device is woken up only using an external GPIO interrupt. A sleep timer interrupt cannot wake up a device from deep sleep mode. This is treated as a continuous sleep mode without periodic wakeups. Refer to the application note CapSense Express Power and Sleep Considerations – AN44209 for details on different sleep modes. To get the lowest power during this mode the sleep timer frequency should be set to 1 Hz.

Sleep Control Pin

The devices require a dedicated sleep control pin to enable reliable I²C communication in case any sleep mode is enabled. This is achieved by pulling the sleep control pin Low to wake up the device and start I²C communication. The sleep control pin can be configured on any of the GPIO.

Interrupt Pin to Master

To inform the master of any button press, a GPIO can be configured as interrupt output and all CapSense buttons can be connected to this GPIO with OR logic operator. This can be configured using the software tool.

Notes

9. Errata: The worst case Acknowledgment time for all critical registers is 140 µs. For more information, see “Errata” on page 35.
10. Errata: The CY8C20110 device acknowledges to host within 100 µs, but is not accessible for any other operation until configuration is successfully stored into flash memory and the device is ready to execute the next command. For more information, see “Errata” on page 35.

Registers

Register Map

Name	Register Address (in Hex)	Access	Writable Only in SETUP Mode[11]	Factory Default Values of Registers (in Hex)	I2C Max ACK Time in Normal Mode (ms)[12, 13]	I2C Max ACK Time in Setup Mode (ms)[12, 13]
INPUT_PORT0	00	R	–	00	0.1	–
INPUT_PORT1	01	R	–	00	0.1	–
STATUS_POR0	02	R	–	00	0.1	–
STATUS_POR1	03	R	–	00	0.1	–
OUTPUT_PORT0	04	W	–	00	0.1	–
OUTPUT_PORT1	05	W	–	00	0.1	–
CS_ENABL0	06	RW	YES	00	–	11
CS_ENABLE	07	RW	YES	00	–	11
GPIO_ENABLE0	08	RW	YES	00	–	11
GPIO_ENABLE1	09	RW	YES	00	–	11
INVERSION_MASK0	0A	RW	–	00	0.11	–
INVERSION_MASK1	0B	RW	–	00	0.11	–
INT_MASK0	0C	RW	YES	00	–	11
INT_MASK1	0D	RW	YES	00	–	11
STATUS_HOLD_MSK0	0E	RW	–	1F	0.11	–
STATUS_HOLD_MSK1	0F	RW	–	1F	0.11	–
DM_PULL_UP0	10	RW	YES	00	–	11
DM_STRONG0	11	RW	YES	00	–	11
DM_HIGHZ0	12	RW	YES	00	–	11
DM_OD_LOW0	13	RW	YES	00	–	11
DM_PULL_UP1	14	RW	YES	00	–	11
DM_STRONG1	15	RW	YES	00	–	11
DM_HIGHZ1	16	RW	YES	00	–	11
DM_OD_LOW1	17	RW	YES	00	–	11
	18[14]					
	19[14]					
	1A[14]					
	1B[14]					
OP_SEL_00	1C	RW	–	00	0.12	11
OPR1_PRT0_00	1D	RW	–	00	0.12	11
OPR1_PRT1_00	1E	RW	–	00	0.12	11
OPR2_PRT0_00	1F	RW	–	00	0.12	11
OPR2_PRT1_00	20	RW	–	00	0.12	11
OP_SEL_01	21	RW	–	00	0.12	11
OPR1_PRT0_01	22	RW	–	00	0.12	11
OPR1_PRT1_01	23	RW	–	00	0.12	11

Notes
11. These registers are writable only after entering into setup mode. All the other registers available for read and write in Normal and in Setup mode.
12. All the Ack times specified are max values with all buttons enabled and filer enabled with maximum order.
13. The "I2C Max ACK Time" values mentioned in this table are for 3.3-V and 5-V operation; the timing values for 2.7-V operation are 4x the values provided in this table. Refer to Operating Voltages on page 19.
14. The registers 0x18–0x1B, 0x76, and 0x7D are reserved.

Register Map (continued)

Name	Register Address (in Hex)	Access	Writable Only in SETUP Mode[11]	Factory Default Values of Registers (in Hex)	I2C Max ACK Time in Normal Mode (ms)[12, 13]	I2C Max ACK Time in Setup Mode (ms)[12, 13]
OPR2_PRT0_01	24	RW	–	00	0.12	11
OPR2_PRT1_01	25	RW	–	00	0.12	11
OP_SEL_02	26	RW	–	00	0.12	11
OPR1_PRT0_02	27	RW	–	00	0.12	11
OPR1_PRT1_02	28	RW	–	00	0.12	11
OPR2_PRT0_02	29	RW	–	00	0.12	11
OPR2_PRT1_02	2A	RW	–	00	0.12	11
OP_SEL_03	2B	RW	–	00	0.12	11
OPR1_PRT0_03	2C	RW	–	00	0.12	11
OPR1_PRT1_03	2D	RW	–	00	0.12	11
OPR2_PRT0_03	2E	RW	–	00	0.12	11
OPR2_PRT1_03	2F	RW	–	00	0.12	11
OP_SEL_04	30	RW	–	00	0.12	11
OPR1_PRT0_04	31	RW	–	00	0.12	11
OPR1_PRT1_04	32	RW	–	00	0.12	11
OPR2_PRT0_04	33	RW	–	00	0.12	11
OPR2_PRT1_04	34	RW	–	00	0.12	11
OP_SEL_10	35	RW	–	00	0.12	11
OPR1_PRT0_10	36	RW	–	00	0.12	11
OPR1_PRT1_10	37	RW	–	00	0.12	11
OPR2_PRT0_10	38	RW	–	00	0.12	11
OPR2_PRT1_10	39	RW	–	00	0.12	11
OP_SEL_11	3A	RW	–	00	0.12	11
OPR1_PRT0_11	3B	RW	–	00	0.12	11
OPR1_PRT1_11	3C	RW	–	00	0.12	11
OPR2_PRT0_11	3D	RW	–	00	0.12	11
OPR2_PRT1_11	3E	RW	–	00	0.12	11
OP_SEL_12	3F	RW	–	00	0.12	11
OPR1_PRT0_12	40	RW	–	00	0.12	11
OPR1_PRT1_12	41	RW	–	00	0.12	11
OPR2_PRT0_12	42	RW	–	00	0.12	11
OPR2_PRT1_12	43	RW	–	00	0.12	11
OP_SEL_13	44	RW	–	00	0.12	11
OPR1_PRT0_13	45	RW	–	00	0.12	11
OPR1_PRT1_13	46	RW	–	00	0.12	11
OPR2_PRT0_13	47	RW	–	00	0.12	11
OPR2_PRT1_13	48	RW	–	00	0.12	11
OP_SEL_14	49	RW	–	00	0.12	11
OPR1_PRT0_14	4A	RW	–	00	0.12	11
OPR1_PRT1_14	4B	RW	–	00	0.12	11
OPR2_PRT0_14	4C	RW	–	00	0.12	11

Register Map (continued)

Name	Register Address (in Hex)	Access	Writable Only in SETUP Mode[11]	Factory Default Values of Registers (in Hex)	I2C Max ACK Time in Normal Mode (ms)[12, 13]	I2C Max ACK Time in Setup Mode (ms)[12, 13]
OPR2_PRT1_14	4D	RW	–	00	0.12	11
CS_NOISE_TH	4E	RW	–	28	0.11	11
CS_BL_UPD_TH	4F	RW	–	64	0.11	11
CS_SETL_TIME	50	RW	YES	A0	–	35
CS_OTH_SET	51	RW	YES	00	–	35
CS_HYSTERISIS	52	RW	–	0A	0.11	11
CS_DEBOUNCE	53	RW	–	03	0.11	11
CS_NEG_NOISE_TH	54	RW	–	14	0.11	11
CS_LOW_BL_RST	55	RW	–	14	0.11	11
CS_FILTERING [15, 16]	56	RW	–	20	0.11	11
CS_SCAN_POS_00	57	RW	YES	FF	–	11
CS_SCAN_POS_01	58	RW	YES	FF	–	11
CS_SCAN_POS_02	59	RW	YES	FF	–	11
CS_SCAN_POS_03	5A	RW	YES	FF	–	11
CS_SCAN_POS_04	5B	RW	YES	FF	–	11
CS_SCAN_POS_10	5C	RW	YES	FF	–	11
CS_SCAN_POS_11	5D	RW	YES	FF	–	11
CS_SCAN_POS_12	5E	RW	YES	FF	–	11
CS_SCAN_POS_13	5F	RW	YES	FF	–	11
CS_SCAN_POS_14	60	RW	YES	FF	–	11
CS_FINGER_TH_00	61	RW	–	64	0.14	11
CS_FINGER_TH_01	62	RW	–	64	0.14	11
CS_FINGER_TH_02	63	RW	–	64	0.14	11
CS_FINGER_TH_03	64	RW	–	64	0.14	11
CS_FINGER_TH_04	65	RW	–	64	0.14	11
CS_FINGER_TH_10	66	RW	–	64	0.14	11
CS_FINGER_TH_11	67	RW	–	64	0.14	11
CS_FINGER_TH_12	68	RW	–	64	0.14	11
CS_FINGER_TH_13	69	RW	–	64	0.14	11
CS_FINGER_TH_14	6A	RW	–	64	0.14	11
CS_IDAC_00	6B	RW	–	0A	0.14	11
CS_IDAC_01	6C	RW	–	0A	0.14	11
CS_IDAC_02	6D	RW	–	0A	0.14	11
CS_IDAC_03	6E	RW	–	0A	0.14	11
CS_IDAC_04	6F	RW	–	0A	0.14	11

Notes
15. Errata: Added two on-chip filtering algorithms for improved CapSense performance and better noise immunity.
16. Errata: If a finger is on the sensor, during power-up the sensor triggers and the baseline gets stuck. Baseline is stuck only when Averaging Filter is enabled. For more information, see "Errata" on page 35.

Register Map (continued)

Name	Register Address (in Hex)	Access	Writable Only in SETUP Mode[11]	Factory Default Values of Registers (in Hex)	I2C Max ACK Time in Normal Mode (ms)[12, 13]	I2C Max ACK Time in Setup Mode (ms)[12, 13]
CS_IDAC_10	70	RW	–	0A	0.14	11
CS_IDAC_11	71	RW	–	0A	0.14	11
CS_IDAC_12	72	RW	–	0A	0.14	11
CS_IDAC_13	73	RW	–	0A	0.14	11
CS_IDAC_14	74	RW	–	0A	0.14	11
CS_SLID_CONFIG	75	RW	–	00	0.1	11
	76 [17]					
CS_SLID_MULM	77	RW	–	00	0.1	11
CS_SLID_MULL	78	RW	–	00	0.1	11
I2C_ADDR_LOCK	79	RW	–	01	0.11	11
DEVICE_ID	7A	R	–	A0	0.11	11
DEVICE_STATUS	7B	R	–	03	0.11	11
I2C_ADDR_DM	7C	RW	–	00	0.11	11
	7D [18]					
SLEEP_PIN	7E	RW	YES	00	0.1	11
SLEEP_CTRL	7F	RW	–	00	0.1	11
SLEEP_SA_CNTR	80	RW	–	00	0.1	11
CS_READ_BUTTON	81	RW	–	00	0.12	11
CS_READ_BLM	82	R	–	00	0.12	11
CS_READ_BLL	83	R	–	00	0.12	11
CS_READ_DIFFM	84	R	–	00	0.12	11
CS_READ_DIFFL	85	R	–	00	0.12	11
CS_READ_RAWM	86	R	–	00	0.12	11
CS_READ_RAWL	87	R	–	00	0.12	11
CS_READ_STATUSM	88	R	–	00	0.12	11
CS_READ_STATUSL	89	R	–	00	0.12	11
CS_READ_CEN_POSM	8A	R	–	00	0.12	11
CS_READ_CEN_POSL	8B	R	–	00	0.12	11
CS_READ_CEN_PEAKM	8C	R	–	00	0.12	11
CS_READ_CEN_PEAKL	8D	R	–	00	0.12	11
COMMAND_REG	A0	W	–	00	0.1	11

Notes
17. The registers 0x18–0x1B, 0x76, and 0x7D are reserved.
18. The registers 0x18–0x1B, 0x76, and 0x7D are reserved.

CapSense Express Commands

Command[19]	Description	Executable Mode	Duration the Device is not accessible after ACK (in ms)[20]
W 00 A0 00	Get firmware revision	Setup/Normal	0
W 00 A0 01 [21]	Store current configuration to NVM	Setup/Normal	120
W 00 A0 02	Restore factory configuration	Setup/Normal	120
W 00 A0 03	Write NVM POR defaults	Setup/Normal	120
W 00 A0 04	Read NVM POR defaults	Setup/Normal	5
W 00 A0 05	Read current configurations (RAM)	Setup/Normal	5
W 00 A0 06	Reconfigure device (POR)	Setup	5
W 00 A0 07	Set Normal mode of operation	Setup/Normal	0
W 00 A0 08	Set Setup mode of operation	Setup/Normal	1.2*(loop time[22] + 1 ms)
W 00 A0 09	Start scan	Setup/Normal	10
W 00 A0 0A	Stop scan	Setup/Normal	5
W 00 A0 0B	Get CapSense scan status	Setup/Normal	0

Register Conventions

This table lists the register conventions that are specific to this section.

Convention	Description
RW	Register has both read and write access
R	Register has only read access

Notes

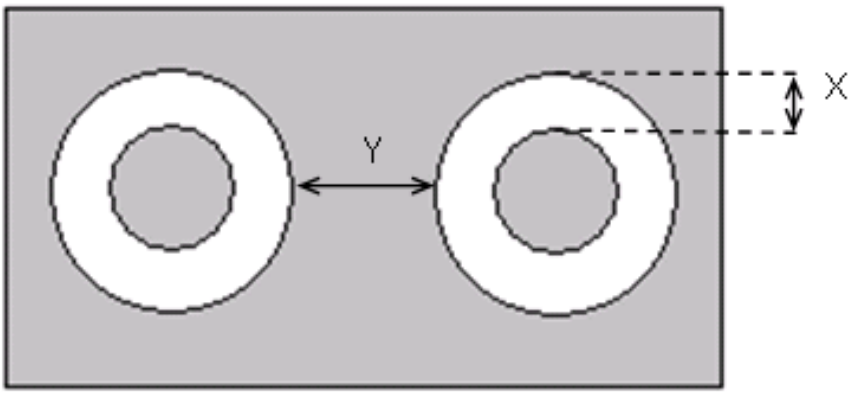
19. The ‘W’ indicates the write transfer. The next byte of data represents the 7-bit I^2C address.
20. The "not accessible after ACK" timing values are the maximum values for 5-V and 3.3-V operation. The timing values for 2.7-V operation will be 4x these values. Refer to Operating Voltages on page 19.
21. Errata: Save to flash command fails when the sleep interval is set to 512 or 64 Hz. For more information, see “Errata” on page 35.
22. # loop time can be measured by probing any sensor using an oscilloscope and measuring the time between two consecutive scans.

Layout Guidelines and Best Practices

This section provides a set of high level rules for board design. Cypress also provides an extensive set of design guidelines for CapSense board designs. Refer to the *"Getting Started with CapSense Design Guide"* for complete system guidelines.

CapSense Button Shapes

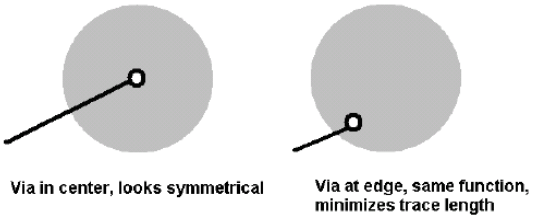
Button Layout Design



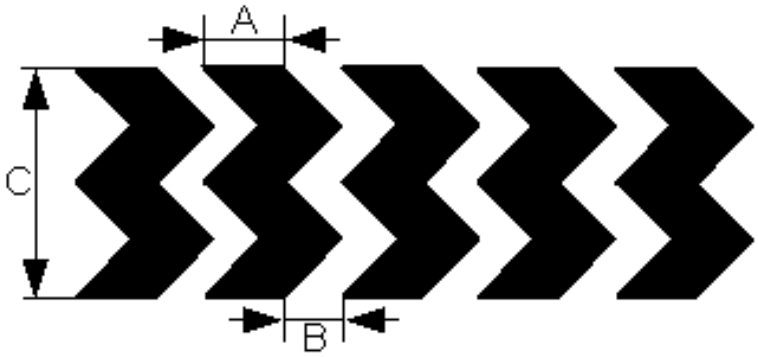
X: Button to ground clearance (Refer to Table 2 on page 17)

Y: Button to button clearance (Refer to Table 2 on page 17)

Recommended via Hole Placement



Slider Shapes



Dimensions for Slider Design

Parameter[23]	Min	Max	Recommended
Width of the Segment (A)	2 mm	–	8 mm[24]
Clearance between Segments (B)	0.5 mm	2 mm	0.5 mm
Height of the segment (C)	7 mm[25]	15 mm	12 mm

The recommended slider-segment width is based on an average human finger diameter of 9 mm. Refer to section “Slider-Segment Shape, Width, and Air Gap” in *“Getting Started with CapSense Design Guide”* for more details.

Notes
23. The end segments of sliders should be grounded.
24. The recommended slider-segment width is based on an average human finger diameter of 9 mm. Refer to section “Slider-Segment Shape, Width, and Air Gap” in *“Getting Started with CapSense Design Guide”* for more details.
25. The minimum slider segment height of 7 mm is recommended based on a minimum human finger diameter of 7 mm. Slider height may be kept lower than 7 mm, provided the overlay thickness and CapSense tuning is such that an SNR ≥ 5:1 is achieved when the finger is placed in the middle of any segment.

Table 2. Layout Guidelines and Best Practices

S. No.	Category	Min	Max	Recommendations/Remarks
1	Button shape	–	–	Solid round pattern, round with LED hole, rectangle with round corners
2	Button size	5 mm	15 mm	10 mm
3	Button-button spacing	Equal to button ground clearance	–	8 mm [X]
4	Button ground clearance	0.5 mm	2 mm	Button ground clearance = overlay thicknesses
5	Slider segment pattern Saw tooth pattern	–	–	–
6	Number of slider segments	5	10	Design can have one 5 segment slider or one 10 segment slider
7	Slider segment width	2 mm	–	8 mm[26]
8	Slider segment spacing	0.5 mm	2 mm	0.5 mm
9	Ground flood - top layer	–	–	Hatched ground 7 mil trace and 45 mil grid (15% filling)
10	Ground flood - bottom layer	–	–	Hatched ground 7 mil trace and 70 mil grid (10% filling)
11	Trace length from sensor to PSoC buttons	–	200 mm	< 100 mm.
12	Trace width	0.17 mm	0.20 mm	0.17 mm (7 mil)
13	Trace routing	–	–	Traces should be routed on the non sensor side. If any non CapSense trace crosses CapSense trace, ensure that intersection is orthogonal.
14	Via position for the sensors	–	–	Via should be placed near the edge of the button/slider to reduce trace length thereby increasing sensitivity.
15	Via hole size for sensor traces	–	–	10 mil
16	Number of vias on sensor trace	1	2	1
17	CapSense series resistor placement	–	10 mm	Place CapSense series resistors close to the device for noise suppression.CapSense resistors have highest priority place them first.
18	Distance between any CapSense trace to ground flood	10 mil	20 mil	20 mil
19	Device placement	–	–	Mount the device on the layer opposite to sensor. The CapSense trace length between the device and sensors should be minimum.
20	Placement of components in 2 layer PCB	–	–	Top layer sensor pads and bottom layer PSoC, other components and traces.
21	Placement of components in 4 layer PCB	–	–	Top layer – sensor pads, second layer – CapSense traces, third layer-hatched ground, bottom layer – PSoC, other components and non CapSense traces
22	Overlay material	–	–	Should be non-conductive material (glass, ABS plastic, formica)
23	Overlay adhesives	–	–	Adhesive should be non conductive and dielectrically homogenous. 467 MP and 468 MP adhesives made by 3M are recommended.
25	LED back lighting	–	–	Cut a hole in the sensor pad and use rear mountable LEDs. Refer to the PCB layout in the following diagrams.
26	Board thickness	–	–	Standard board thickness for CapSense FR4 based designs is 1.6 mm.

Note
26. The recommended slider-segment width is based on an average human finger diameter of 9 mm. Refer to section “Slider-Segment Shape, Width, and Air Gap” in *“Getting Started with CapSense Design Guide”* for more details.

The Recommended maximum overlay thickness is 5 mm (with external CSInt)/ 2 mm (without external CSInt). For more details, refer to the section “The Integrating Capacitor (Cint)” in AN53490.

Example PCB Layout Design with 5 Segment Slider, 2 Buttons with LED Backlighting

Figure 8. Top Layer

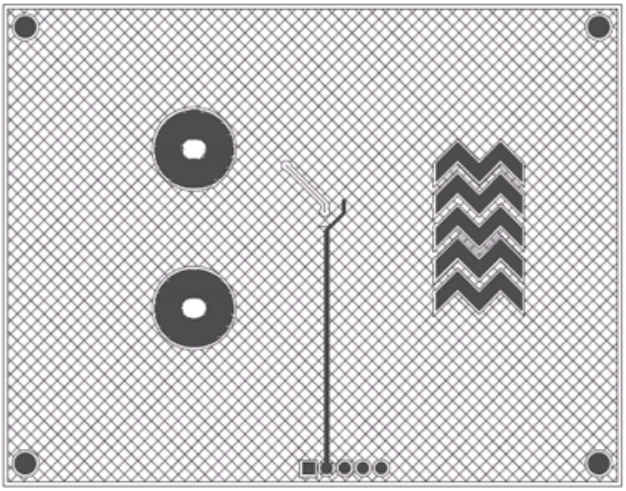
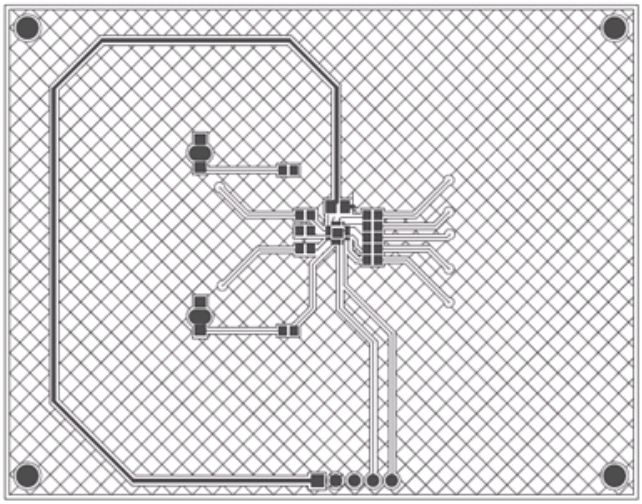
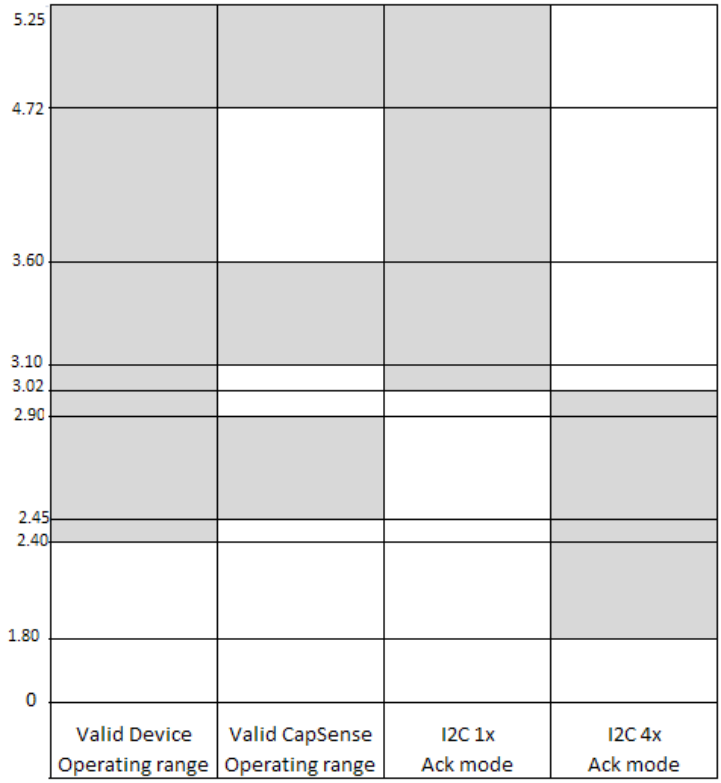


Figure 9. Bottom Layer



Operating Voltages



For details on I^2C 1x Ack time, refer to Register Map on page 10 and CapSense Express Commands on page 14. I2C 4x Ack time is approximately four times the values mentioned in these tables.

CapSense Constraints

Parameter	Min	Typ	Max	Units	Notes
Parasitic capacitance (C_P) of the CapSense sensor	–	–	30	pF	–
Supply voltage variation (V_{DD})	–	–	± 5%	–	–

Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C (0 °C to 50 °C). Extended duration storage temperatures above 65 °C degrade reliability
$T_{BAKETEMP}$	Bake temperature	–	125	See Package label	°C	–
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	–
T_A	Ambient temperature with power applied	–40	–	+85	°C	–
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	–
V_{IO}	DC voltage on CapSense inputs and digital output pins	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
I_{MIC}	Maximum current into any Digs pin	–25	–	+50	mA	–
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch-up current	–	–	200	mA	–

Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	–
T_J	Junction temperature	–40	–	+100	°C	–

Electrical Specifications

DC Electrical Specifications

DC Chip-Level Specifications

Table 3. DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	–
I_{DD}	Supply current	–	1.5	2.5	mA	Conditions are V_{DD} = 3.10 V, T_A = 25 °C
I_{SB}	Deep sleep mode current with POR and LVD active	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C < T_A < 40 °C
I_{SB}	Deep sleep mode current with POR and LVD active	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C < T_A < 85 °C
I_{SB}	Deep sleep mode current with POR and LVD active	–	5.2	6.4	µA	V_{DD} = 5.25 V, –40 °C < T_A < 85 °C

DC GPIO Specifications

Table 4 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.10 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 4. 5-V and 3.3-V DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on Port 0 pins	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} > 3.10 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage on Port 0 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, V_{DD} > 3.10 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage on Port 1 pins	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} > 3.10 V, maximum of 20 mA source current in all I/Os.
V_{OH4}	High output voltage on Port 1 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, V_{DD} > 3.10 V, maximum of 20 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 20 mA/pin, V_{DD} > 3.10, maximum of 60 mA sink current on even port pins and of 60 mA sink current on odd port pins.
I_{OH1}	High output current on Port 0 pins	0.01	–	1	mA	V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os
I_{OH2}	High output current on Port 1 pins	0.01	–	5	mA	V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os
I_{OL}	Low output current	–	–	20	mA	V_{DD} ≥ 3.1 V, maximum of 60 mA sink current on pins P0_2, P1_2, P1_3, P1_4 and 60 mA sink current on pins P0_0, P0_1, P0_3, P0_4, P1_0, P1_1
V_{IL}	Input low voltage	–	–	0.75	V	V_{DD} = 3.10 V to 3.6 V
V_{IH}	Input High voltage	1.6	–	–	V	V_{DD} = 3.10 V to 3.6 V
V_{IL}	Input low voltage	–	–	0.8	V	V_{DD} = 4.75 V to 5.25 V
V_{IH}	Input High voltage	2.0	–	–	V	V_{DD} = 4.75 V to 5.25 V
V_H	Input hysteresis voltage	–	140	–	mV	–
I_{IL}	Input leakage	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25 °C.

Table 5 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 2.90 V and –40 °C < T_A < 85 °C, respectively. Typical parameters apply to 2.7 V at 25 °C and are for design guidance only.

Table 5. 2.7-V DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on Port 0 pins	V_{DD} – 0.2	–	–	V	I_{OH} <10 µA, maximum of 10 mA source current in all I/Os.
V_{OH2}	High output voltage on Port 0 pins	V_{DD} – 0.5	–	–	V	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os.
V_{OH3}	High output voltage on Port 1 pins	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage on Port 1 pins	V_{DD} – 0.5	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA/pin, V_{DD} > 3.10, maximum of 30 mA sink current on even port pins and of 30 mA sink current on odd port pins[27].
I_{OH}	High output current	0.01	–	2	mA	V_{DD} ≤ 2.9 V, maximum of 10 mA source current in all I/Os
I_{OL1}	Low output current on Port 0 pins	–	–	10	mA	V_{DD} ≤ 2.9 V, maximum of 30 mA sink current on pins P0_2, P1_2, P1_3, P1_4 and 30 mA sink current on pins P0_0, P0_1, P0_3, P0_4, P1_0, P1_1
I_{OL2}	Low output current	–	–	20	mA	V_{DD} ≤ 2.9 V, maximum of 50 mA sink current on pins P0_2, P1_2, P1_3, P1_4 and 50 mA sink current on pins P0_0, P0_1, P0_3, P0_4, P1_0, P1_1
V_{IL}	Input low voltage	–	–	0.75	V	V_{DD} = 2.4 to 2.90 V and 3.10 V to 3.6 V
V_{IH1}	Input High voltage	1.4	–	–	V	V_{DD} = 2.4 to 2.7 V
V_{IH2}	Input High voltage	1.6	–	–	V	V_{DD} = 2.7 to 2.90 V and 3.10 V to 3.6 V
V_H	Input hysteresis voltage	–	60	–	mV	–
I_{IL}	Input leakage	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent. Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent. Temp = 25 °C

Note
27. The maximum sink current is 20 mA for 20140 and 20142 devices and for all other devices the maximum sink current is 30 mA.

DC POR Specifications

Table 6. DC POR Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PPOR0} V_{PPOR1}	V_{DD} Value for PPOR Trip V_{DD} = 2.7 V V_{DD} = 3.3 V, 5 V	 – –	 2.36 2.60	 2.40 2.65	 V V	V_{DD} must be greater than or equal to 2.5 V during startup or internal reset.
VLVD0 VLVD2 VLVD6	V_{DD} Value for LVD Trip V_{DD} = 2.7 V V_{DD} = 3.3 V V_{DD} = 5 V	 2.39 2.75 3.98	 2.45 2.92 4.05	 2.51 2.99 4.12	 V V V	–

DC Flash Write Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C < T_A < 85 °C, 3.10 V to 3.6 V and –40 °C < T_A < 85 °C or 2.4 V to 2.90 V and –40 °C < T_A < 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash Endurance and Retention specifications are valid only within the range: 25 °C ± 20 °C during the flash write operation. It is at the user's own risk to operate out of this temperature range. If flash writing is done out of this temperature range, the endurance and data retention reduces.

Table 7. DC Flash Write Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{DDIWRITE}$	Supply voltage for flash write operations	2.7	–	–	V	–
I_{DDP}	Supply current for flash write operations	–	5	25	mA	–
$Flash_{ENPB}$	Flash endurance	50,000 [28]	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash data retention	10	–	–	Years	–

DC I^2C Specifications

This table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C < T_A < 85 °C, 3.10 V to 3.6 V and –40 °C < T_A < 85 °C or 2.4 V to 2.90 V and –40 °C < T_A < 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 8. DC I^2C Specifications

Symbol[29]	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 2.9 V 3.1 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V
V_{OLP}	Low output voltage	–	–	0.4	V	I_{OL} = 5 mA/pin
C_{I2C}	Capacitive load on I^2C pins	0.5	1.7	5	pF	Package and pin dependent.
Temp = 25 °C		–	–	–	–	–
R_{PU}	Pull-up resistor	4	5.6	8	kO	–

Notes

28. Commands involving flash writes (0x01, 0x02, 0x03) and flash read (0x04) must be executed only within the same VCC voltage range detected at POR (power on, or command 0x06) and above 2.7 V
29. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

CapSense Electrical Characteristics

Max (V)	Typ (V)	Min (V)	Conditions for Supply Voltage	Result
3.6	3.3	3.1	< 2.9	The device automatically reconfigures itself to work in 2.7 V mode of operation.
			> 2.9 or < 3.10	This range is not recommended for CapSense usage.
2.90	2.7	2.45	< 2.45 V	The scanning for CapSense parameters shuts down until the voltage returns to over 2.45 V.
			> 3.10	The device automatically reconfigures itself to work in 3.3 V mode of operation.
			< 2.4 V	The device goes into reset.
5.25	5.0	4.75	< 4.73 V	The scanning for CapSense parameters shuts down until the voltage returns to over 4.73 V.

AC Electrical Specifications

AC Chip-Level Specifications

Table 9. 5-V and 3.3-V AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
F_{32K1}	Internal low-speed oscillator (ILO) frequency	15	32	64	kHz	Calculations during sleep operations are done based on ILO frequency.
t_{XRST}	External reset pulse width	10	–	–	µs	–
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	150	–	ms	–
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	–

Table 10. 2.7-V AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
F_{32K1}	ILO frequency	8	32	96	kHz	Calculations during sleep operations are done based on ILO frequency.
t_{XRST}	External reset pulse width	10	–	–	µs	–
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	600	–	ms	–
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	–

AC GPIO Specifications

Table 11. 5-V and 3.3-V AC GPIO Specifications

Parameter	Description	Min	Max	Unit	Notes
t_{Rise0}	Rise time, strong mode, Cload = 50 pF, Port 0	15	80	ns	V_{DD} = 3.10 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%
t_{Rise1}	Rise time, strong mode, Cload = 50 pF, Port 1	10	50	ns	V_{DD} = 3.10 V to 3.6 V, 10% – 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF, all ports	10	50	ns	V_{DD} = 3.10 V to 3.6 V and 4.75 V to 5.25 V, 10% to 90%

Table 12. 2.7-V AC GPIO Specifications

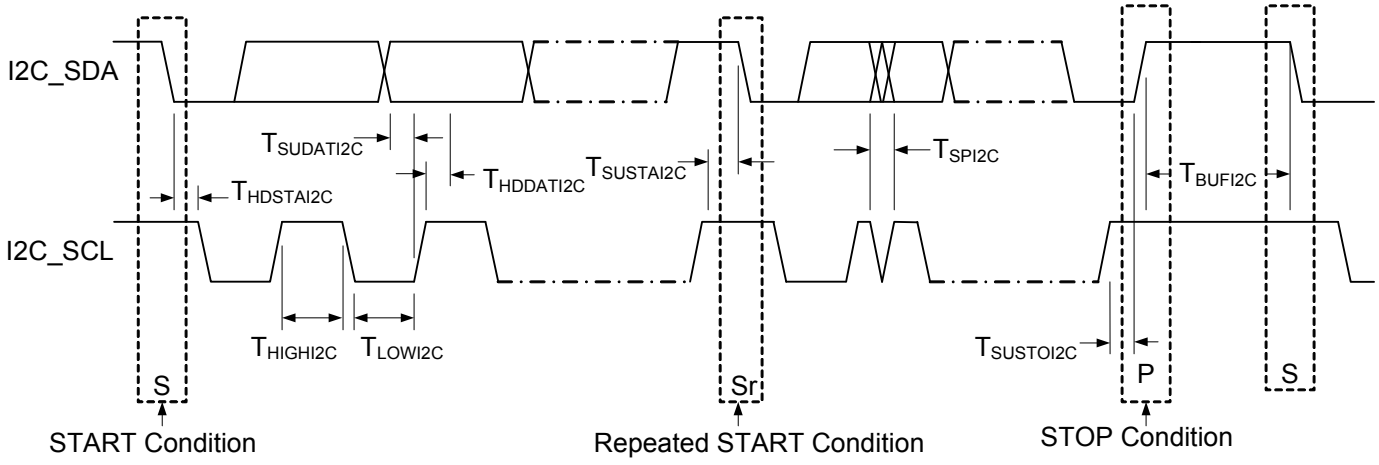
Parameter	Description	Min	Max	Unit	Notes
t_{Rise0}	Rise time, strong mode, Cload = 50 pF, Port 0	15	100	ns	V_{DD} = 2.4 V to 2.90 V, 10% – 90%
t_{Rise1}	Rise time, strong mode, Cload = 50 pF, Port 1	10	70	ns	V_{DD} = 2.4 V to 2.90 V, 10% – 90%
t_{Fall}	Fall time, strong mode, Cload = 50 pF	10	70	ns	V_{DD} = 2.4 V to 2.90 V, 10% – 90%

AC I²C Specifications

Table 13. AC I²C Specifications

Parameter	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kbps	Fast mode not supported for V_{DD} < 3.0 V
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs	–
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	–
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	–
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	–
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	–
$t_{SUDATI2C}$	Data setup time	250	–	100	–	ns	–
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	–
t_{BUFI2C}	BUS free time between a STOP and START condition	4.7	–	1.3	–	µs	–
t_{SPI2C}	Pulse width of spikes suppressed by the input filter	–	–	0	50	ns	–

Figure 10. Definition of Timing for Fast/Standard Mode on the I²C Bus



Appendix

Examples of Frequently Used I²C Commands

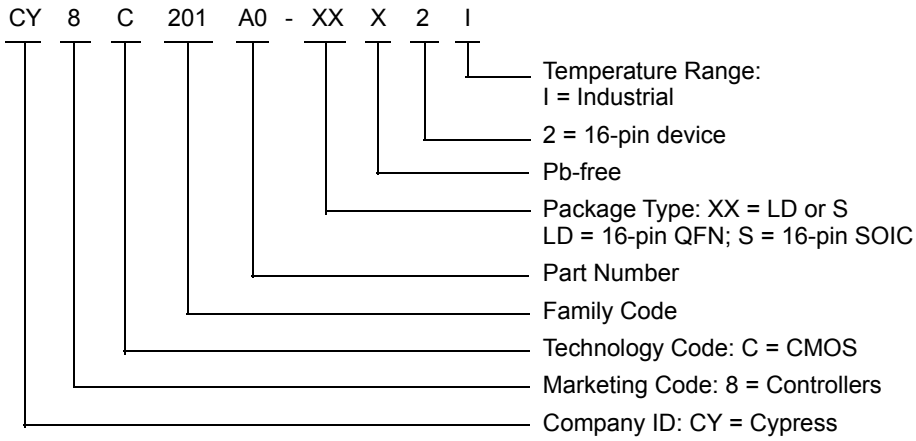
S. No.	Requirement	I²C commands[30]	Comment
1	Enter into setup mode	W 00 A0 08	–
2	Enter into normal mode	W 00 A0 07	–
3	Load factory defaults to RAM registers	W 00 A0 02	–
4	Do a software reset	W 00 A0 08 W 00 A0 06	Enter into setup mode Do software reset
5	Save current configuration to flash[31]	W 00 A0 01	–
6	Load factory defaults to RAM registers and save as user configuration	W 00 A0 08 W 00 A0 02 W 00 A0 01 W 00 A0 06	Enter into setup mode Load factory defaults to SRAM Save the configuration to flash. Wait for time specified in CapSense Express Commands on page 14. Do software reset
7	Enable GP00/01/02/03/04/05 and GP10 as CapSense button	W 00 A0 08 W 00 06 1F 01 W 00 A0 01 W 00 A0 06	Enter into setup mode Configuring CapSense buttons Save the configuration to flash. Wait for time specified in CapSense Express Commands on page 14. Do software reset
8	Enable 5 segment slider	W 00 75 01	Enable 5 segment slider
8	Read CapSense button (GP10) scan results	W 00 81 81 W 00 82 R 00 RD RD RD RD RD RD	Select CapSense button for reading scan result Set the read point to 82h Consecutive 6 reads get baseline, difference count and raw count (all two byte each)
9	Read CapSense button status register	W 00 89 R 00 RD	Set the read pointer to 89 Reading a byte gets status CapSense inputs
10	Read Slider Centroid position	W 00 8A R 00 RD RD	Set the read pointer to 8A Reading a byte gets slider Centroid position

Notes
30. The 'W' indicates the write transfer and the next byte of data represents the 7-bit I2C address. The I2C address is assumed to be '0' in the above examples. Similarly 'R' indicates the read transfer followed by 7-bit address and data byte read operations.
31. Errata: Save to flash command fails when the sleep interval is set to 512 or 64 Hz. For more information, see "Errata" on page 35.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Temperature	CapSense Block	GPIOs	XRES Pin
CY8C201A0-LDX2I	001-09116	16-pin QFN[32]	Industrial	Yes	10	Yes
CY8C201A0-SX2I	51-85068	16-pin SOIC	Industrial	Yes	10	Yes

Ordering Code Definitions



Thermal Impedances

Table 14. Thermal Impedances by Package

Package	Typical θ_{JA}[33]
16-pin QFN[1]	46 °C/W
16-pin SOIC	79.96 °C/W

Solder Reflow Specifications

Table 15. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
16-pin QFN[1]	260 °C	30 seconds
16-pin SOIC	260 °C	30 seconds

Notes
32. Earlier termed as QFN package.
33. $T_J = T_A$ + Power x θ_{JA}.

Package Diagrams

Figure 11. 16-pin Chip On Lead (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116

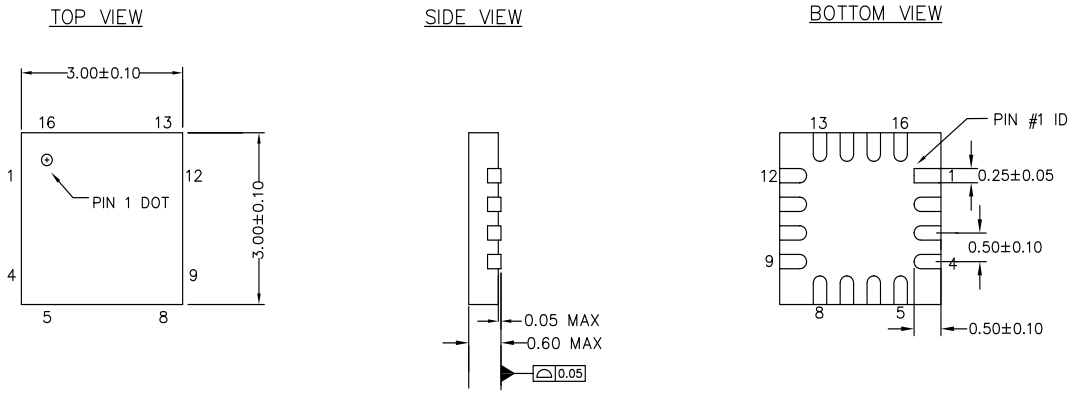
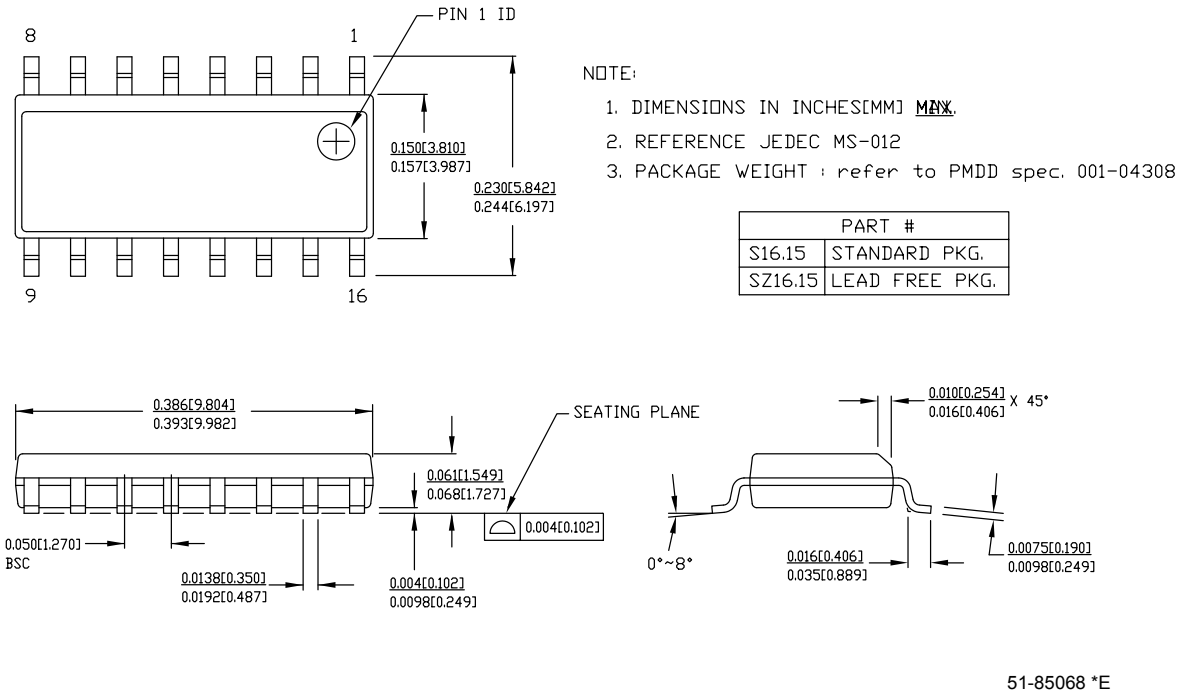


Figure 12. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068



Acronyms

Table 16 lists the acronyms that are used in this document.

Table 16. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	LSB	least-significant bit
CMOS	complementary metal oxide semiconductor	LVD	low voltage detect
DC	direct current	PCB	printed circuit board
EEPROM	electrically erasable programmable read-only memory	POR	power on reset
EMC	electromagnetic compatibility	PPOR	precision power on reset
GPIO	general-purpose I/O	PSoC®	Programmable System-on-Chip
I/O	input/output	QFN	quad flat no leads
IDAC	current DAC	RF	radio frequency
ILO	internal low speed oscillator	SOIC	small-outline integrated circuit
LCD	liquid crystal display	SRAM	static random access memory
LDO	low dropout regulator	XRES	external reset
LED	light-emitting diode		

Reference Documents

Capsense® Express™ Power And Sleep Considerations - AN44209 (001-44209)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Document Conventions

Units of Measure

Table 17 lists the unit sof measures.

Table 17. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	mm	millimeter
Hz	hertz	ms	millisecond
kbps	kilo bits per second	mV	millivolt
kHz	kilohertz	nA	nanoampere
kΩ	kilohm	ns	nanosecond
LSB	least significant bit	%	percent
µA	microampere	pF	picofarad
µF	microfarad	V	volts
µs	microsecond	W	watt
mA	milliampere		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.

Glossary (continued)

configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.

Glossary (continued)

interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device***.
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.

Glossary (continued)

PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.

Glossary (continued)

V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Errata

This section describes the changes between the firmware revisions ×15 and ×1B in CapSense Express devices (CY8C201A0). All shipments of samples and production parts with firmware version ×1B will encounter the following changes from the previous (×15) version of the firmware. Cypress inventory has been rotated to the ×1B firmware by WW35, and all distributor inventory will be rotated by WW42 of 2008.

Contact your local Cypress Sales Representative if you have questions.

CapSense Express Part Numbers Affected

Part Number	Package Type	Operating Range
CY8C201A0	All Packages	Commercial/Industrial

Product Status

The CY8C201A0 CapSense Express devices have been qualified and are available in production quantities. From now on, customers are requested to use the production release of CapSense Express device with x1B firmware version.

CapSense Express CY8C201A0 Errata Summary

The following table defines the errata applicable to Cypress CapSense Express devices.

Table 18. CapSense Express CY8C201A0 Errata Summary

Item	Issues	Description	Fix Status
1	I2C ACK	Reduction of I2C ACK timing response by the CapSense Express slave. (Time in Normal Operating Mode)	Worst case Ack timing of 140 µs for all critical registers (Input, Output, CapSense Global Parameters, and CapSense Buttons and Slider Read-back Values). For more information on critical register I2C timings, refer to application note AN44208 “CapSense Express - I2C Communication Timing Analysis”.
2	I2C ACK	Reduction of I2C ACK timing response by the CapSense Express slave. (Time when executing commands to store configuration in Flash)	The CapSense Express device ACK to host within 100 µs but is not accessible for any other operation until the configuration is successfully stored into flash memory, and the CapSense Express device is ready to execute the next command. For more information on I2C timings to store configuration in Flash, refer to application note AN44208 “CapSense Express - I2C Communication Timing Analysis”.
3	Data Filtering	Addition of two on-chip filtering algorithms for improved CapSense performance and better noise immunity.	**Averaging Filter** This smoothens the raw count data, and results in better noise immunity and performance. The filter can average 2, 4, 8, or 16 samples. **Drop the Sample Filter** This discards any acquired CapSense sample if an I^2C communication occurs after the scan process has already started. For more information on filtering, refer to application note AN48430 “CapSense Express-Noise Filtering Methods”.
4	Save to Flash	Save to flash command fails when the sleep interval is set to 512 or 64 Hz.	No fix will be provided. When using save to flash follow these steps: 1. Write configuration data to registers with sleep interval set to 8 or 1 Hz 2. Save the settings to flash 3. Change the sleep interval settings per design
5	False Triggering During Power-Up	If a finger is on the sensor during power-up the sensor triggers and the baseline gets stuck. This only happens when the Averaging Filter is enabled.	No fix will be provided. Disable the Averaging Filter if your design requires a finger on the sensor during power-up.
6	Erroneous I2C START condition detection	During boot-up, CapSense Express device misinterprets an incoming byte as its own address, leading to confusion in the I2C state machine. It controls the SCL and SDA line in-between the I2C transfer, leading to bus communication failure.	No fix will be provided. Do not initiate I2C transactions on bus before the device boots up.

Document History Page

Document Title: CY8C201A0, CapSense® Express™ Slider Capacitive Controllers Document Number: 001-54607				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2741726	SLAN / FSU	07/21/2009	New data sheet.
*A	2821828	SSHH / FSU	12/4/2009	Added Contents. Updated Layout Guidelines and Best Practices (Updated Dimensions for Slider Design (Added Note 23 and referred in the parameter column)). Updated Absolute Maximum Ratings (Added F32k u, $t_{POWERUP}$ parameters and their details). Updated Electrical Specifications (Updated DC Electrical Specifications (Updated DC Flash Write Specifications (Updated Note 28))).
*B	2892629	NJF	03/15/2010	Updated Absolute Maximum Ratings (Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters and their details). Updated Pin Definitions (Added a Note “For information on the preferred dimensions for mounting QFN packages, see the "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at http://www.amkor.com.” below the column).
*C	3043236	ARVM	09/30/2010	Updated Pin Definitions (Added Note 2 and referred the same Note in all GP1[1] and GP1[2] pins). Updated Pin Definitions (Added Note 3 and referred the same Note in all GP1[1] and GP1[2] pins). Updated Typical Circuits (Updated Figure 3 (Replaced with updated one)). Updated Absolute Maximum Ratings (Removed F32ku, $t_{POWERUP}$ parameters and their details). Updated Electrical Specifications (Updated AC Electrical Specifications (Added AC Chip-Level Specifications section)).
*D	3085081	NJF	11/12/2010	Updated Electrical Specifications (Updated DC Electrical Specifications (Updated DC GPIO Specifications (Removed sub-section “2.7-V DC Spec for I2C Line with 1.8 V External Pull-up”), added DC I2C Specifications), updated AC Electrical Specifications (Updated AC I^2C Specifications (Updated Figure 10 (No specific changed were made to I^2C Timing Diagram. Updated for clearer understanding.)))). Updated Solder Reflow Specifications. Added Acronyms and Units of Measure. Added Reference Documents and Glossary. Updated in new template.
*E	3276234	ARVM	01/20/2011	Updated Layout Guidelines and Best Practices (Updated Table 2 (Removed “Overlay thickness-buttons” category), added the following statement after Table 2 – “The Recommended maximum overlay thickness is 5 mm (with external CS_{Int})/ 2 mm (without external CS_{Int}). For more details refer to the section “The Integrating Capacitor (Cint)” in AN53490”.). Updated CapSense Constraints (Removed the parameter “Overlay thickness”). Updated Solder Reflow Specifications (Updated Table 15).
*F	3390450	SLAN	09/30/2011	Updated Package Diagrams (spec 001-09116 (Changed revision from *E to *F), spec 51-85068 (Changed revision from *C to *D)). Post to external web.
*G	3631370	VAIR / SLAN	05/31/2012	Updated Pin Definitions (Updated description of XRES pin). Updated Pin Definitions (Updated description of XRES pin). Updated Typical Circuits (Updated Figure 4 (Added Note 5 and referred the same Note in Figure 4)). Updated in new template.

Document History Page (continued)

Document Title: CY8C201A0, CapSense® Express™ Slider Capacitive Controllers Document Number: 001-54607				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	3837914	SLAN	12/11/2012	Updated Device Operation Modes (Updated Periodic Sleep Mode (Updated description)). Updated Package Diagrams (spec 001-09116 (Changed revision from *F to *G), spec 51-85068 (Changed revision from *D to *E)).
*I	3992042	SLAN	05/06/2013	Updated Package Diagrams: spec 001-09116 – Changed revision from *G to *H. Added Errata.
*J	4067336	SLAN	07/18/2013	Added Errata footnotes (Note 9, 10, 15, 16, 21, 31). Updated Operating Modes of I2C Commands: Updated Normal Mode: Added Note 9 and referred the same note in acknowledgment time. Updated Setup Mode: Added Note 10 and referred the same note in acknowledgment time. Updated Registers: Updated Register Map: Added Notes 15, 16 and referred the same notes in “CS_FILTERING”. Updated CapSense Express Commands: Added Note 21 and referred the same note in “W 00 A0 01”. Updated Appendix: Updated Examples of Frequently Used I2C Commands: Added Note 31 and referred the same note in “Save current configuration to flash”. Updated Errata. Updated in new template.
*K	4489897	PRIA	09/01/2014	Updated the “duration the device is not accessible after ACK" timing for "Set Setup mode of operation" command. Added notes 13, 20, and 22
*L	4873309	PRIA	08/25/2015	Updated I2C Clock Stretching and Dimensions for Slider Design. Added reference to *Getting Started with CapSense Design Guide* in Layout Guidelines and Best Practices. Updated slider design guidelines in Table 2 as per the latest guidelines in AN64846. Updated hyperlinks. Updated Errata: Added Errata item 6 in Table 18.
*M	5277446	PRIA	05/19/2016	Added “Not recommended for new designs” watermark. Updated the template.
*N	5733914	AESATMP7	05/12/2017	Updated Cypress Logo and Copyright.

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