



**THE DATASHEET OF
SN74AS286NSRG4**



16-PORT LVDS REPEATER

FEATURES

- One Receiver and Sixteen Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
- Typical Data Signaling Rates to 400 Mbps or Clock Frequencies to 400 MHz
- Enabling Logic Allows Separate Control of Each Bank of Four Channels or 2-Bit Selection of Any One of the Four Banks
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100- Ω Load
- Electrically Compatible With LVDS, PECL, LVPECL, LVTTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Termination Networks
- Propagation Delay Times < 4.7 ns
- Output Skew Is < 300 ps and Part-to-Part Skew < 1.5 ns
- Total Power Dissipation Typically 470 mW With All Ports Enabled and at 200 MHz
- Driver Outputs or Receiver Input Is High Impedance When Disabled or With $V_{CC} < 1.5$ V
- Bus-Pin ESD Protection Exceeds 12 kV
- Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch

DESCRIPTION

The SN65LVDS116 is one differential line receiver connected to sixteen differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644, is a data signaling technique that offers the low-power, low-noise coupling, and fast switching speeds to transmit data at relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device and signaling technique is for point-to-point or multidrop baseband data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of the signals repeated from the input. This is particularly advantageous in system clock distribution.

The SN65LVDS116 is characterised for operation from -40°C to 85°C .

DGG PACKAGE
(TOP VIEW)

GND	1	64	A1Y
V_{CC}	2	63	A1Z
V_{CC}	3	62	A2Y
GND	4	61	A2Z
ENA	5	60	A3Y
ENA	6	59	A3Z
NC	7	58	A4Y
NC	8	57	A4Z
NC	9	56	B1Y
ENB	10	55	B1Z
ENB	11	54	B2Y
NC	12	53	B2Z
NC	13	52	B3Y
NC	14	51	B3Z
GND	15	50	B4Y
V_{CC}	16	49	B4Z
V_{CC}	17	48	C1Y
GND	18	47	C1Z
A	19	46	C2Y
B	20	45	C2Z
NC	21	44	C3Y
ENC	22	43	C3Z
ENC	23	42	C4Y
S0	24	41	C4Z
S1	25	40	D1Y
SM	26	39	D1Z
END	27	38	D2Y
END	28	37	D2Z
GND	29	36	D3Y
V_{CC}	30	35	D3Z
V_{CC}	31	34	D4Y
GND	32	33	D4Z

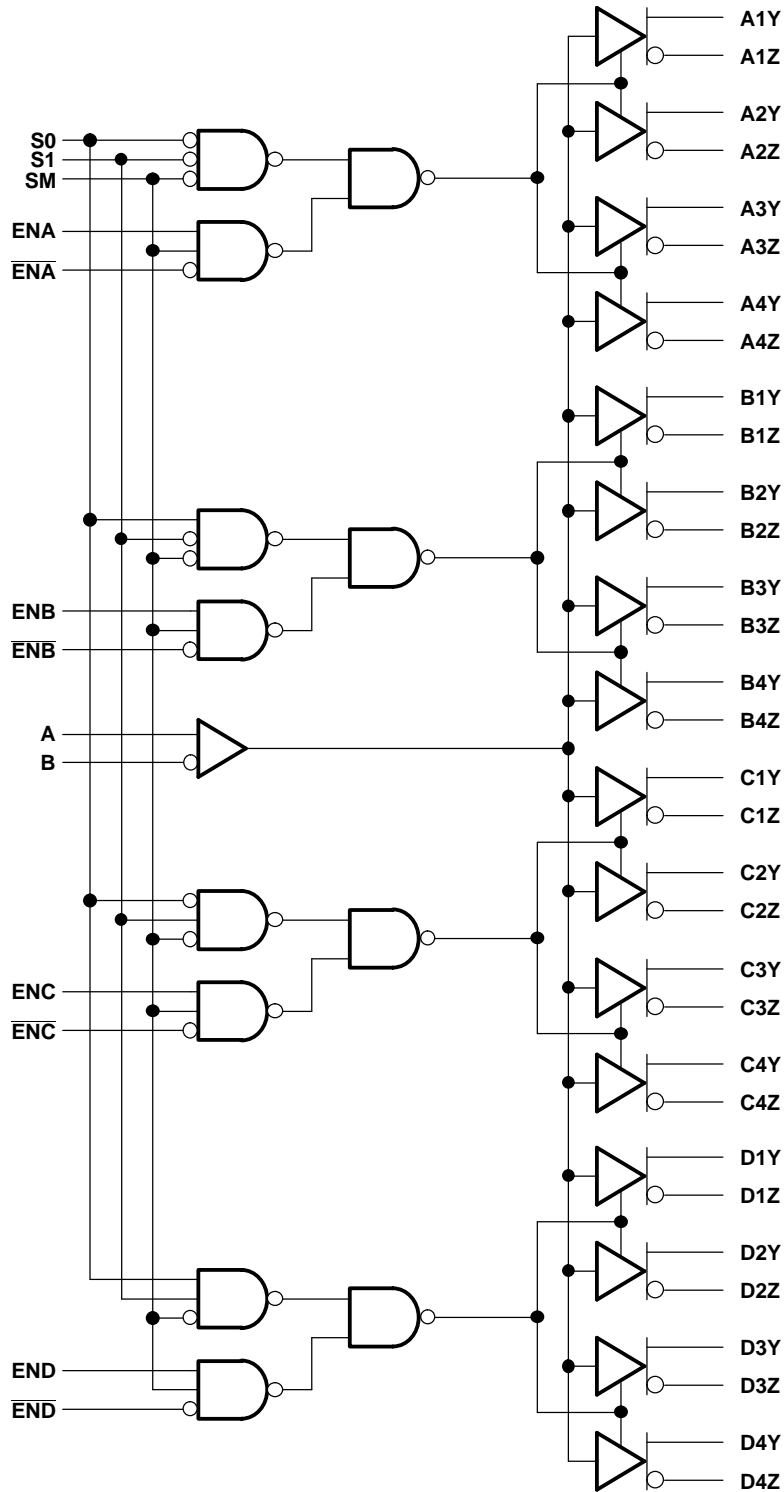


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LOGIC DIAGRAM (POSITIVE LOGIC)

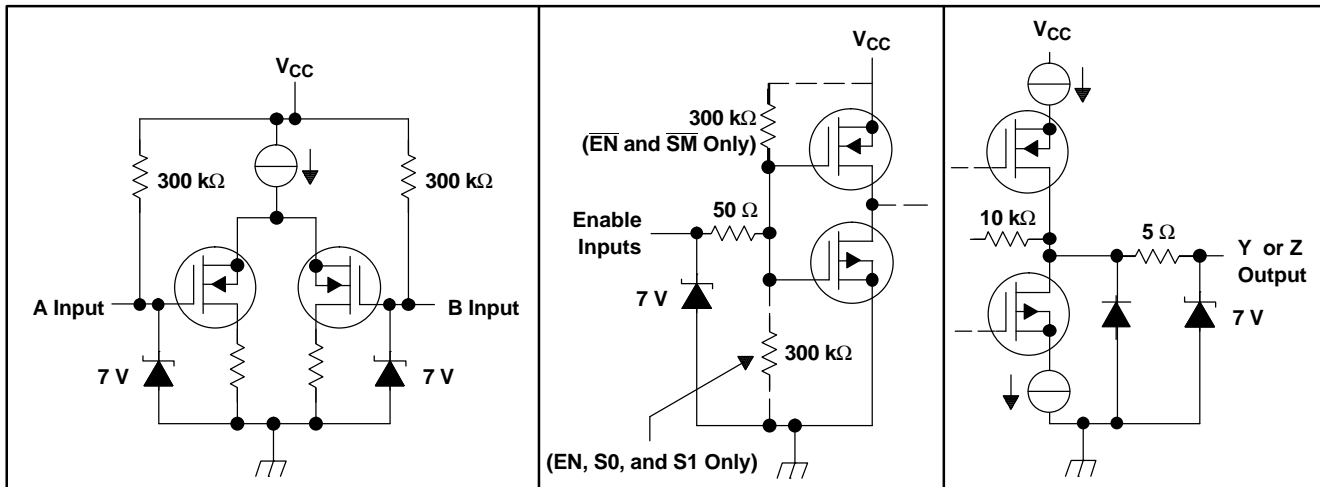


FUNCTION TABLE⁽¹⁾

INPUT						OUTPUT							
$V_{ID} = V_A - V_B$	SM	EN	\overline{EN}	S1	S0	AY	AZ	BY	BZ	CY	CZ	DY	DZ
X	H	L	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
$V_{ID} \geq 100 \text{ mV}$	H	H	L	X	X	H	L	H	L	H	L	H	L
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	H	H	L	X	X	?	?	?	?	?	?	?	?
$V_{ID} \leq -100 \text{ mV}$	H	H	L	X	X	L	H	L	H	L	H	L	H
X	H	X	H	X	X	Z	Z	Z	Z	Z	Z	Z	Z
$V_{ID} \geq 100 \text{ mV}$	L	X	X	L	L	H	L	Z	Z	Z	Z	Z	Z
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	L	X	X	L	L	?	?	Z	Z	Z	Z	Z	Z
$V_{ID} \leq -100 \text{ mV}$	L	X	X	L	L	L	H	Z	Z	Z	Z	Z	Z
$V_{ID} \geq 100 \text{ mV}$	L	X	X	L	H	Z	Z	H	L	Z	Z	Z	Z
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	L	X	X	L	H	Z	Z	?	?	Z	Z	Z	Z
$V_{ID} \leq -100 \text{ mV}$	L	X	X	L	H	Z	Z	L	H	Z	Z	Z	Z
$V_{ID} \geq 100 \text{ mV}$	L	X	X	H	L	Z	Z	Z	Z	H	L	Z	Z
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	L	X	X	H	L	Z	Z	Z	Z	?	?	Z	Z
$V_{ID} \leq -100 \text{ mV}$	L	X	X	H	L	Z	Z	Z	Z	L	H	Z	Z
$V_{ID} \geq 100 \text{ mV}$	L	X	X	H	H	Z	Z	Z	Z	Z	Z	H	L
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	L	X	X	H	H	Z	Z	Z	Z	Z	Z	?	?
$V_{ID} \leq -100 \text{ mV}$	L	X	X	H	H	Z	Z	Z	Z	Z	Z	L	H

(1) H = high level, L = low level, Z = high impedance, ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGSover operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
V_{CC}	Supply voltage range ⁽²⁾	-0.5 V to 4 V
Input voltage range	Enable inputs	-0.5 V to 6 V
	A, B, Y, or Z	-0.5 V to 4 V
Electrostatic discharge	A, B, Y, Z, and GND ⁽³⁾	Class 3, A:12 kV, B: 500 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DGG	2094 mW	16.7 mW/°C	1089 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)	0		$V_{CC}-0.8$	V
T_A	Operating free-air temperature	40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{ITH+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V _{ITH-}	Negative-going differential input voltage threshold		-100			
V _{OD}	Differential output voltage magnitude	R _L = 100 Ω, V _{ID} = ±100 mV, See Figure 1 and Figure 2	247	340	454	mV
Δ V _{OD}	Change in differential output voltage magnitude between logic states		-50		50	
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states		50		50	
V _{OC(PP)}	Peak-to-peak common-mode output voltage			50	150	
I _{CC}	Supply current	Enabled, R _L = 100 Ω		84	115	mA
		Disabled, $\overline{\text{EN}}_x = V_{CC}$ or EN _x = 0 V		3.2	6	
I _I	Input current (A or B inputs) ⁽²⁾	V _I = 0 V		-2	-20	μA
		V _I = 2.4 V		-1.2		
I _{I(OFF)}	Power-off input current (A or B inputs)	V _{CC} = 1.5 V, V _I = 2.4 V			20	μA
I _{IH}	High-level input current	EN _x , S0, S1 $\overline{\text{EN}}_x$, SM V _{IH} = 2 V			20	μA
					-20	
I _{IL}	Low-level input current	EN _x , S0, S1 $\overline{\text{EN}}_x$, SM V _{IL} = 0.8 V			10	μA
					-10	
I _{OS}	Short-circuit output current	V _{OY} or V _{OZ} = 0 V			±24	mA
		V _{OD} = 0 V			±12	
I _{OZ}	High-impedance output current	V _O = 0 V or V _{CC}			±1	μA
I _{O(OFF)}	Power-off output current	V _{CC} = 1.5 V, V _O = 3.6 V			±1	μA
C _{IN}	Input capacitance (A or B inputs)	V _I = 0.4 sin(4E6πt) + 0.5 V		5		pF
C _O	Output capacitance (Y or Z outputs)	V _I = 0.4 sin(4E6πt) + 0.5 V		9.4		

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) The non-algebraic convention, where the more positive (least negative) limit is designated minimum, is used in this data sheet for the input current (I_I) only.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	R _L = 100 Ω, C _L = 10 pF, See Figure 4	2.2	3.1	4.7	ns
t _{PHL}	Propagation delay time, high-to-low-level output		2.2	3.1	4.7	ns
t _r	Differential output signal rise time		0.3	0.8	1.2	ns
t _f	Differential output signal fall time		0.3	0.8	1.2	ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH}) ⁽²⁾			140	500	ps
t _{sk(o)}	Output skew, channel-to-channel ⁽³⁾			100	300	ps
t _{sk(pp)}	Part-to-part skew ⁽⁴⁾				1.5	ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		5.7	15	ns
t _{PZL}	Propagation delay time, high-impedance-to-low-level output			7.7	15	ns
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.2	15	ns
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			3.2	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) t_{sk(p)} is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.

(3) t_{sk(o)} is the magnitude of the time difference between the t_{PLH} or t_{PHL} measured at any two outputs.

(4) t_{sk(pp)} is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

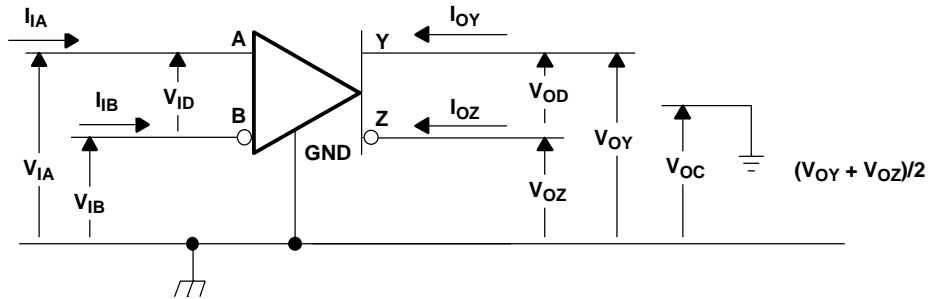


Figure 1. Voltage and Current Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V

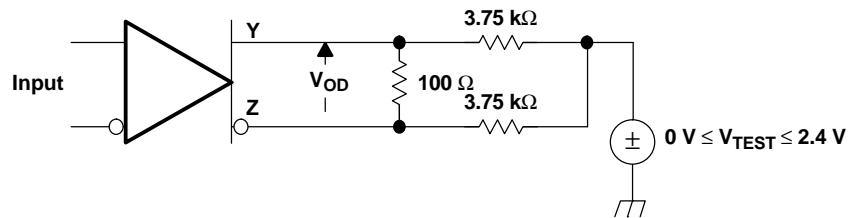
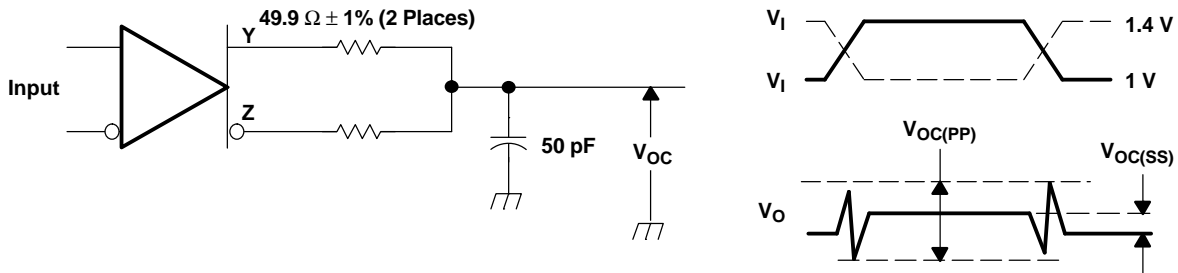
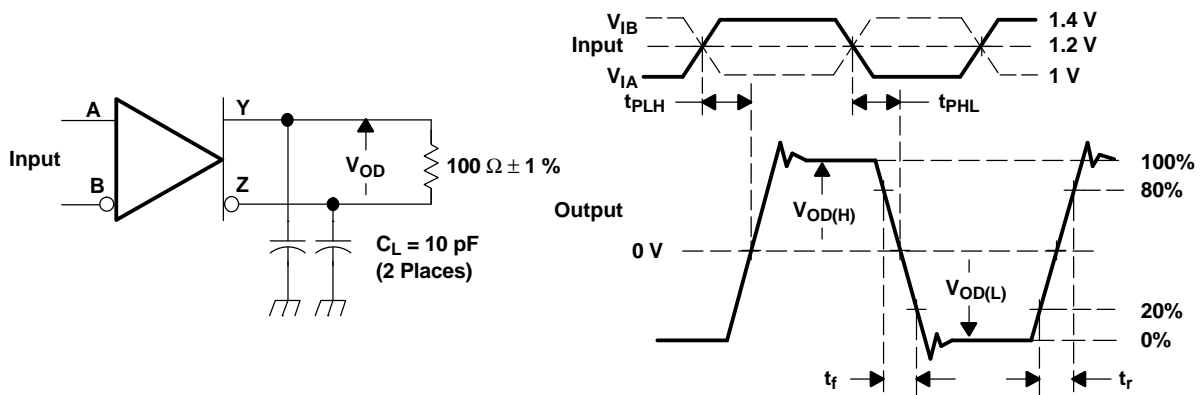


Figure 2. V_{OD} Test Circuit



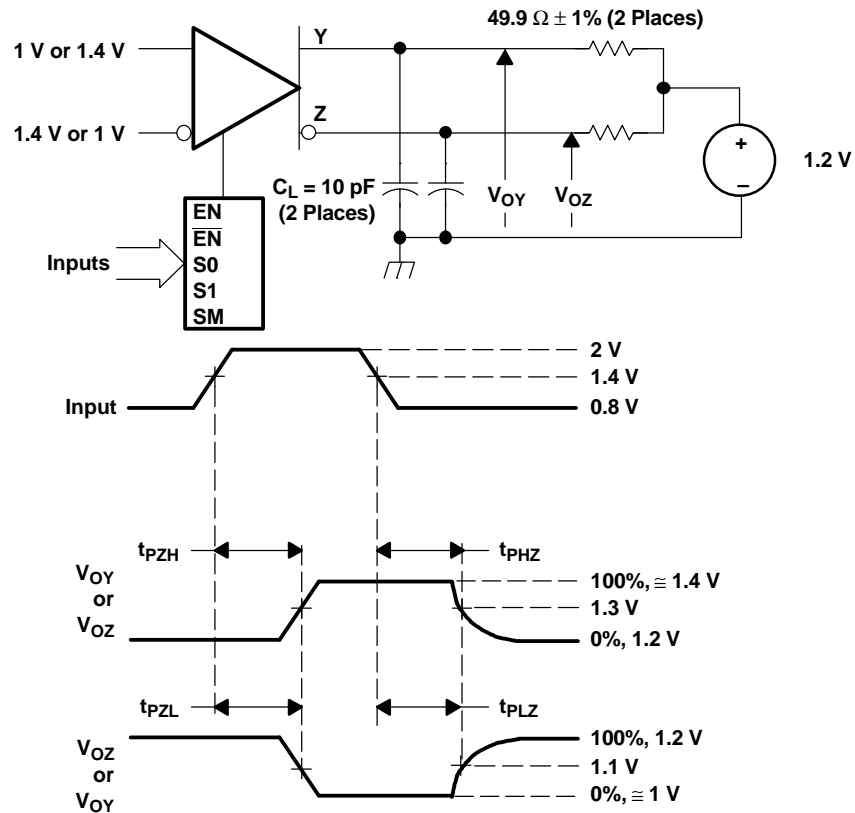
- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

TYPICAL CHARACTERISTICS

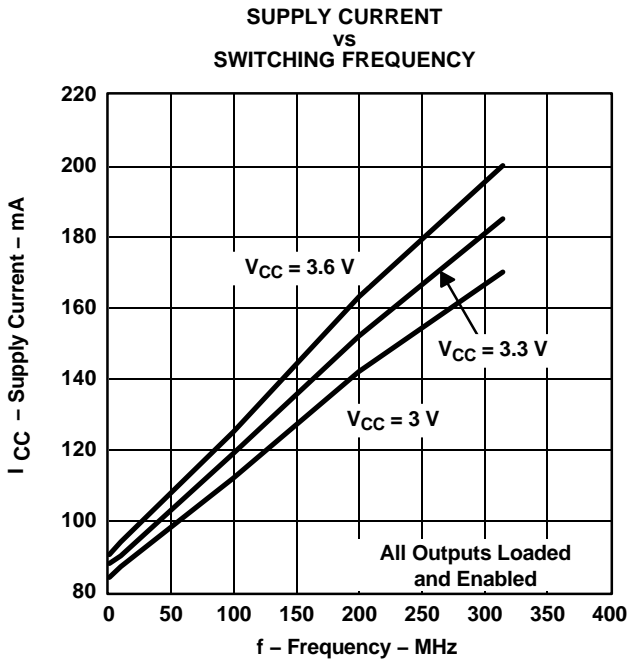


Figure 6.

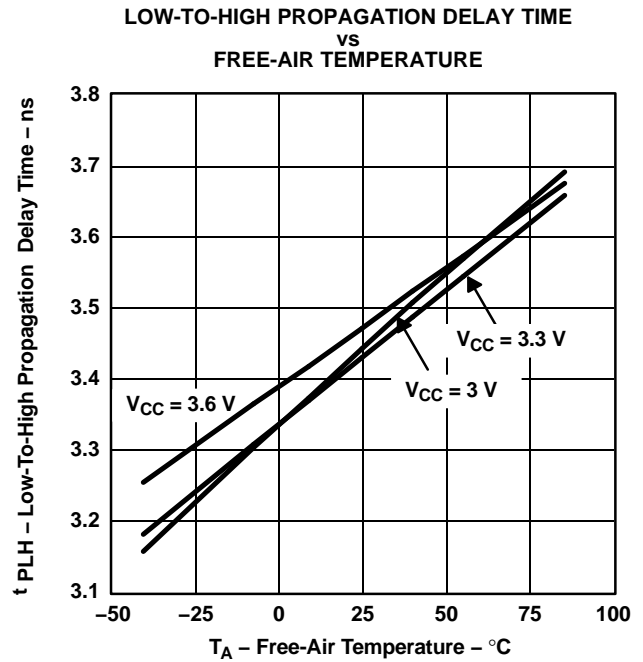


Figure 7.

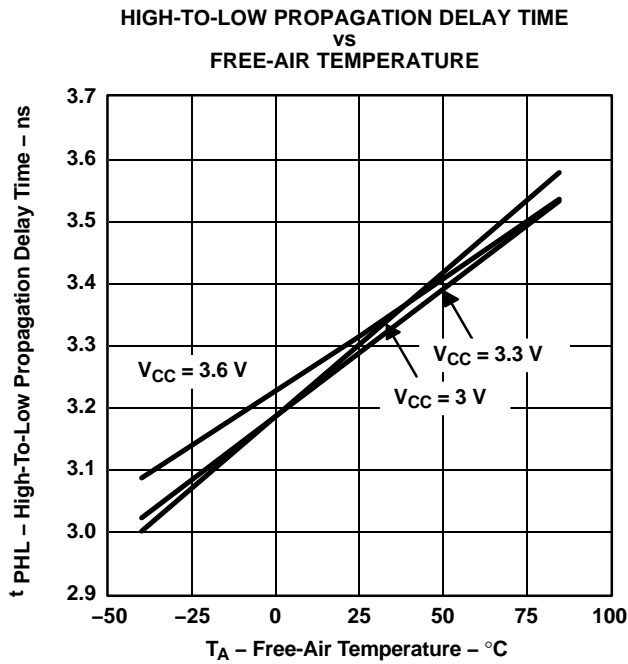


Figure 8.

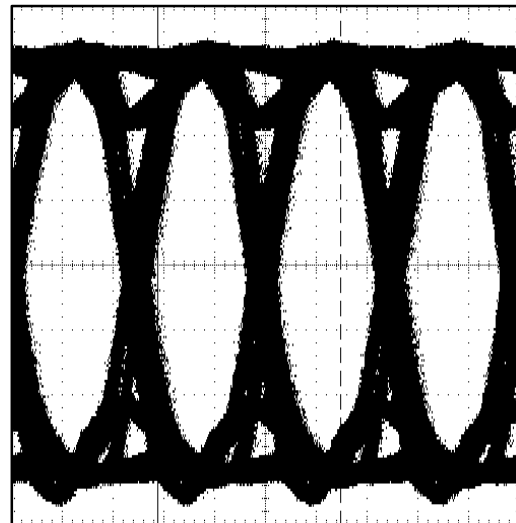
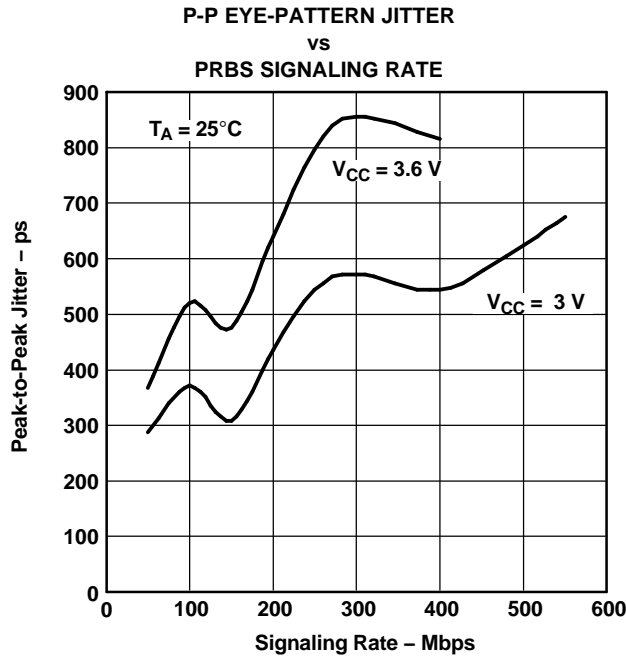


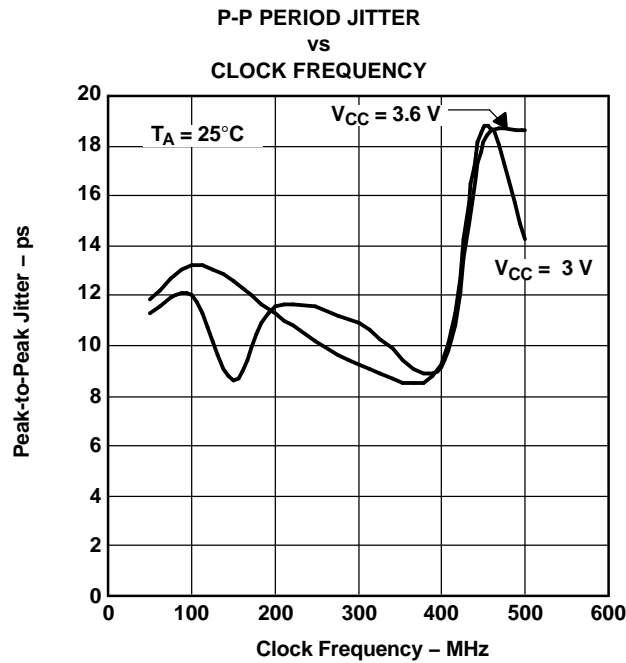
Figure 9. Typical Differential Eye Pattern at 400 Mbps

TYPICAL CHARACTERISTICS (continued)



NOTES: Input: 2¹⁵ PRBS with peak-to-peak jitter < 115 ps at 100 Mbps, all outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-μF and 0.001-μF ceramic 0805-style capacitors 1 cm from the device.

Figure 10.



NOTES: Input: 50% duty cycle square wave with period jitter < 10 ps at 100 MHz, all outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-μF and 0.001-μF ceramic 0805-style capacitors 1 cm from the device.

Figure 11.

APPLICATION INFORMATION

FAIL SAFE

A common problem with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The SN65LVDS116 receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and 100 mV and within its recommended input common-mode voltage range. However, TI LVDS receivers handle the open-input circuit situation differently.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through $300\text{-k}\Omega$ resistors as shown in Figure 12. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

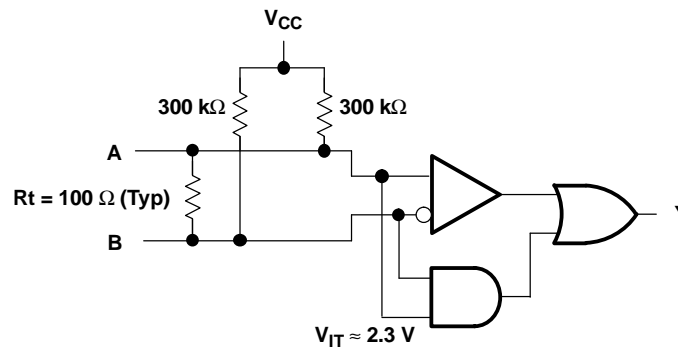


Figure 12. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, R_t , does not affect the fail-safe function as long as it is connected as shown in Figure 12. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

INPUT LEVEL TRANSLATION

An LVDS receiver can be used to receive various other types of logic signals. Figure 13 through Figure 21 show the termination circuits for SSTL, HSTL, GTL, BTL, LVPECL, PECL, CMOS, and TTL.

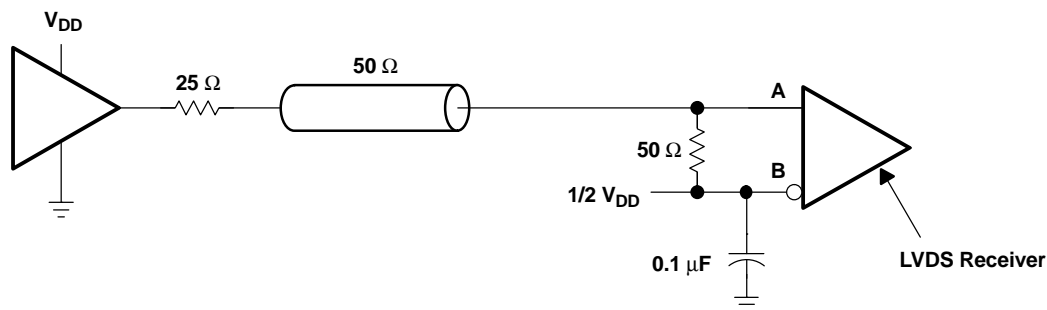


Figure 13. Stub-Series Terminated (SSTL) or High-Speed Transceiver Logic (HSTL)

APPLICATION INFORMATION (continued)

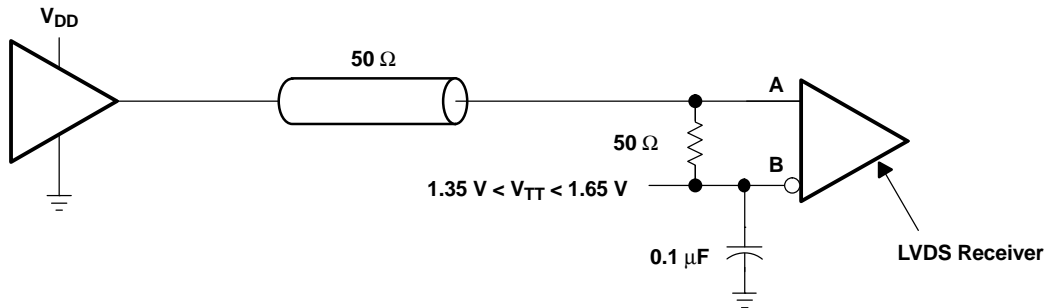


Figure 14. Center-Tap Termination (CTT)

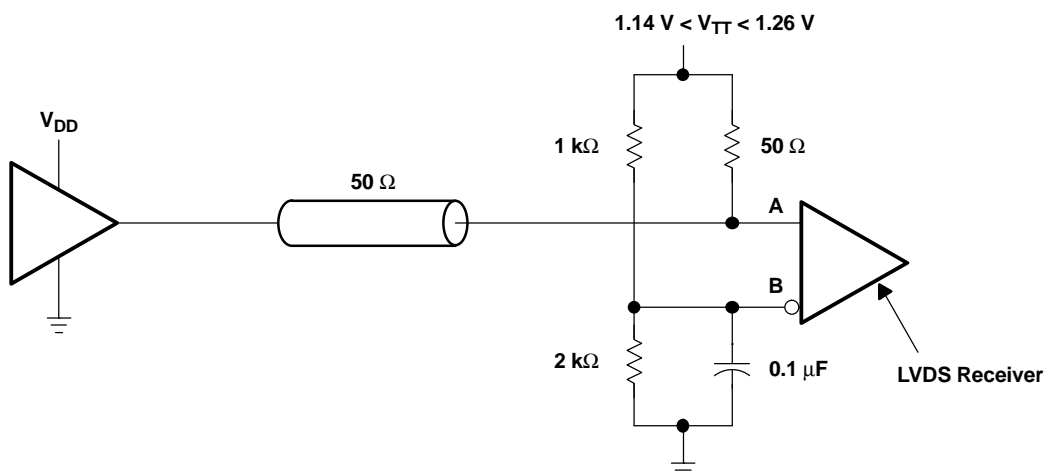


Figure 15. Gunning Transceiver Logic (GTL)

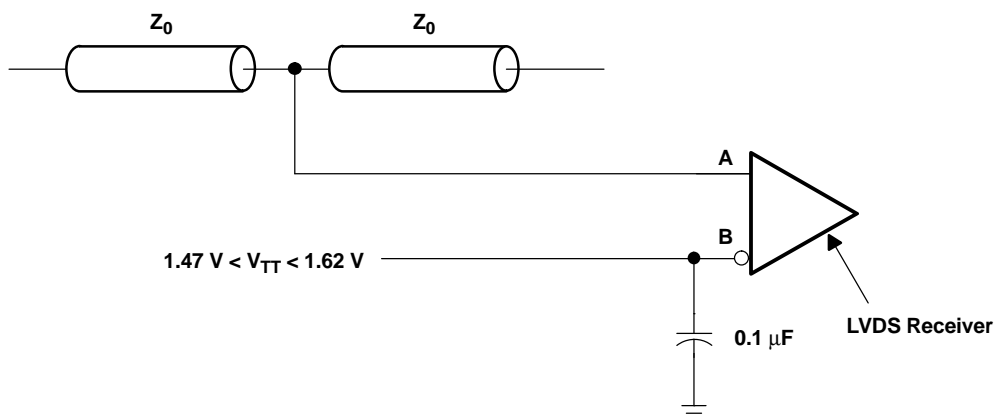


Figure 16. Backplane Transceiver Logic (BTL)

APPLICATION INFORMATION (continued)

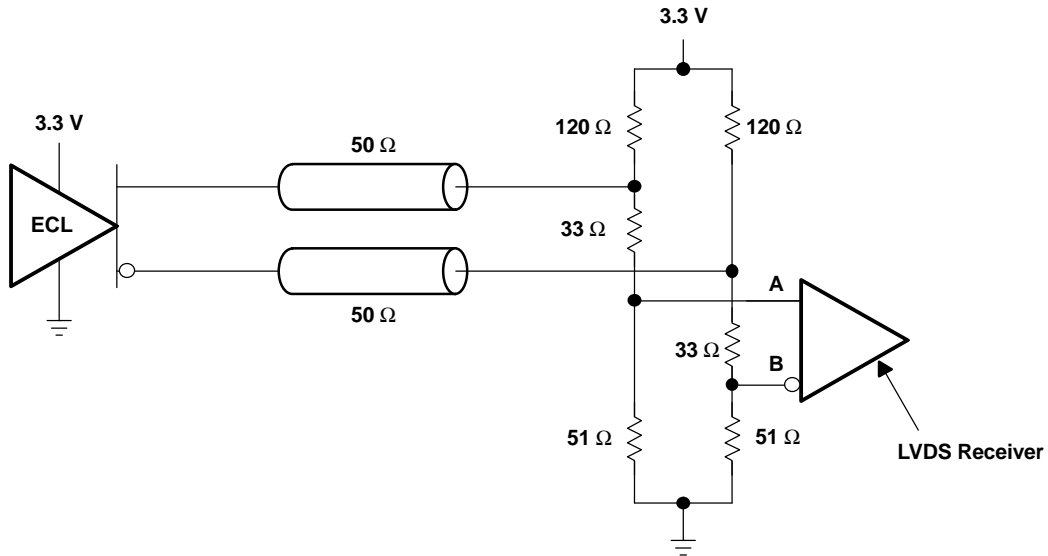


Figure 17. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

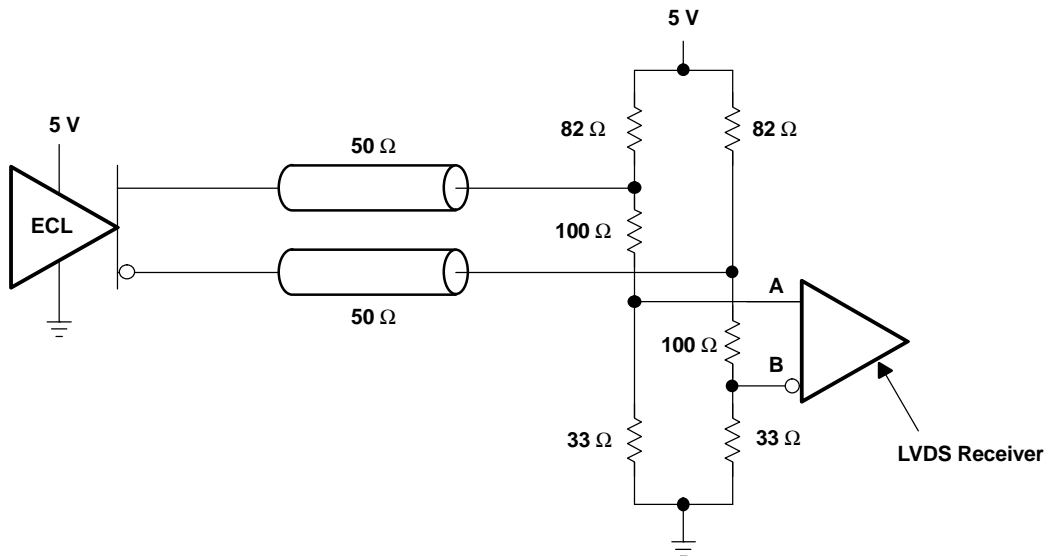


Figure 18. Positive Emitter-Coupled Logic (PECL)

APPLICATION INFORMATION (continued)

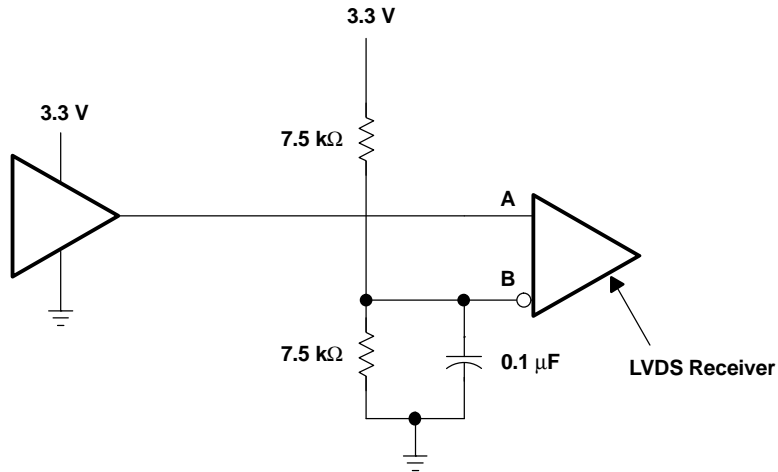


Figure 19. 3.3-V CMOS

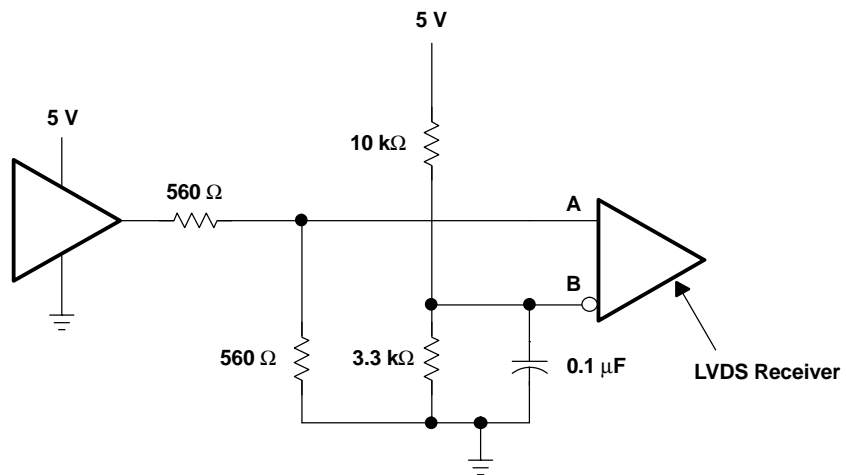


Figure 20. 5-V CMOS

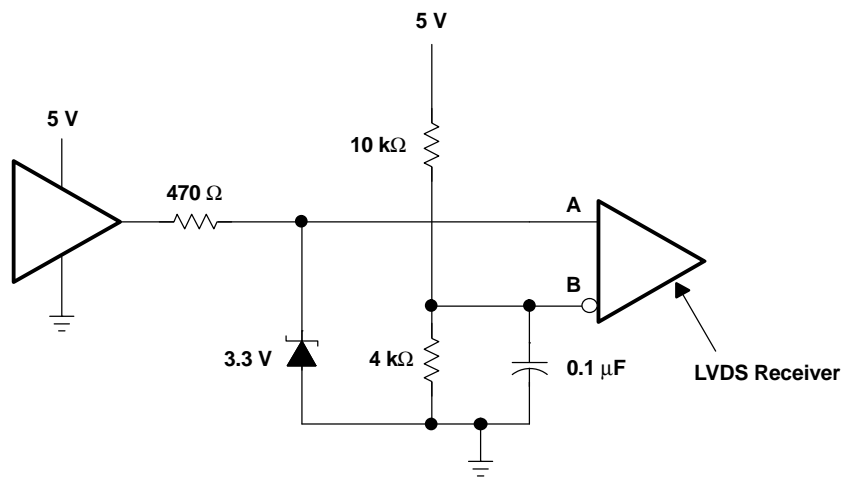


Figure 21. TTL

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS116DGG	ACTIVE	TSSOP	DGG	64	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS116	Samples
SN65LVDS116DGGR	ACTIVE	TSSOP	DGG	64	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS116	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS116DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS116DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0

TUBE

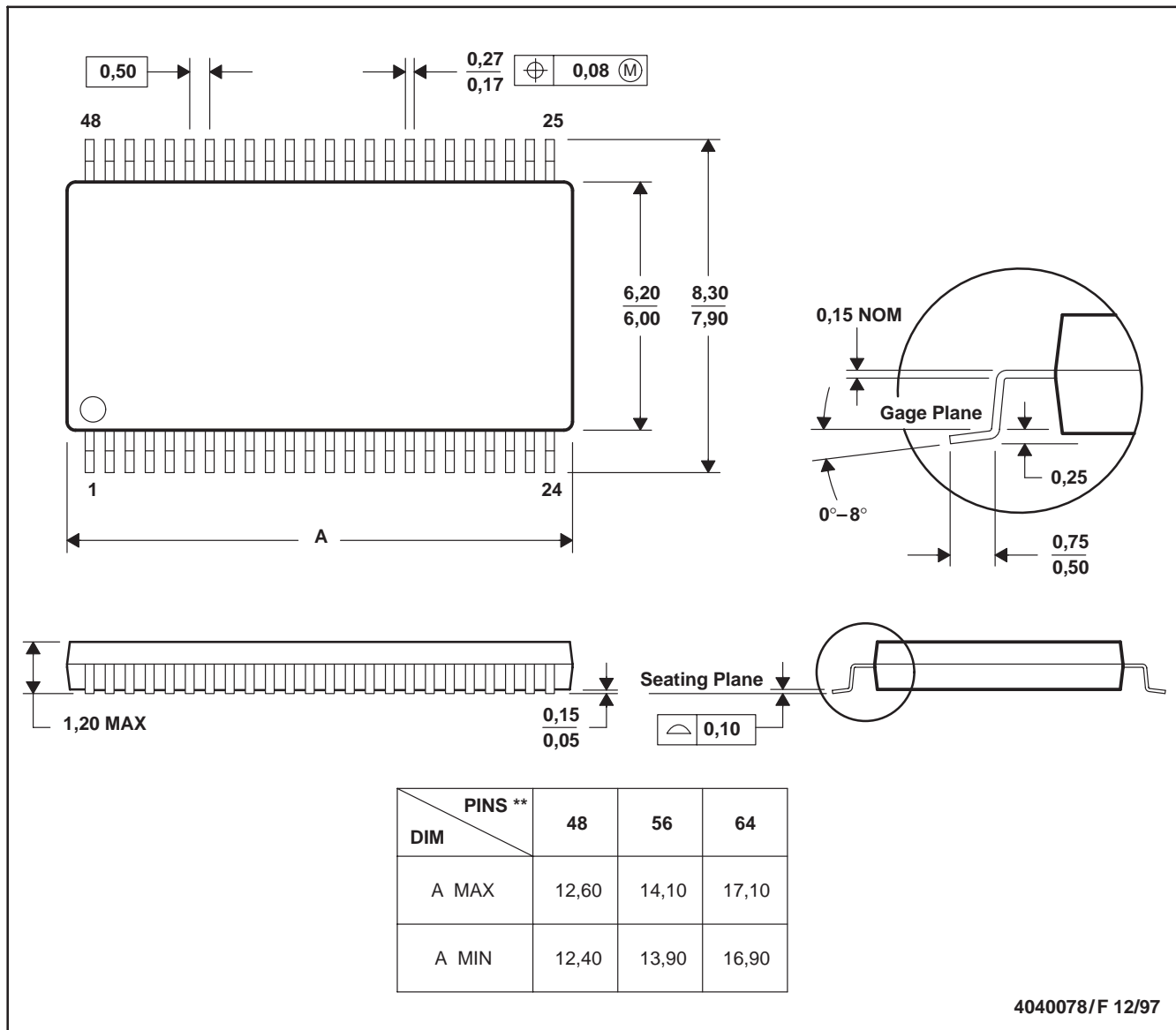

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LVDS116DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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