



**THE DATASHEET OF
SY100S341JC-TR**



**8-BIT SHIFT REGISTER****SY100S341****FEATURES**

- Max. shift frequency of 600MHz
- Max. Clock to Q delay of 1200ps
- IEE min. of -150mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 70% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

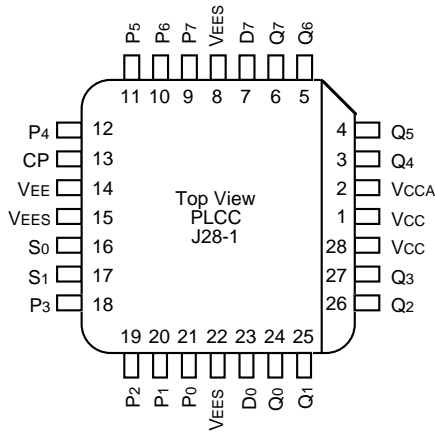
The SY100S341 offer eight D-type, edge-triggered flip-flops with both individual inputs for parallel operation as well as serial inputs for bidirectional shifting, and are designed for use in high-performance ECL systems. Data is clocked into the flip-flops on the rising edge of the clock.

The mode of operation is selected by two Select inputs (S₀, S₁) which determine if the device performs a shift, hold or parallel entry function, as described in the Truth Table. The inputs on these devices have 75kΩ pull-down resistors.

PIN NAMES

Label	Function
CP	Clock Pulse Input
S ₀ — S ₁	Select Inputs
D ₀ — D ₇	Serial Inputs
P ₀ — P ₇	Parallel Inputs
Q ₀ — Q ₇	Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

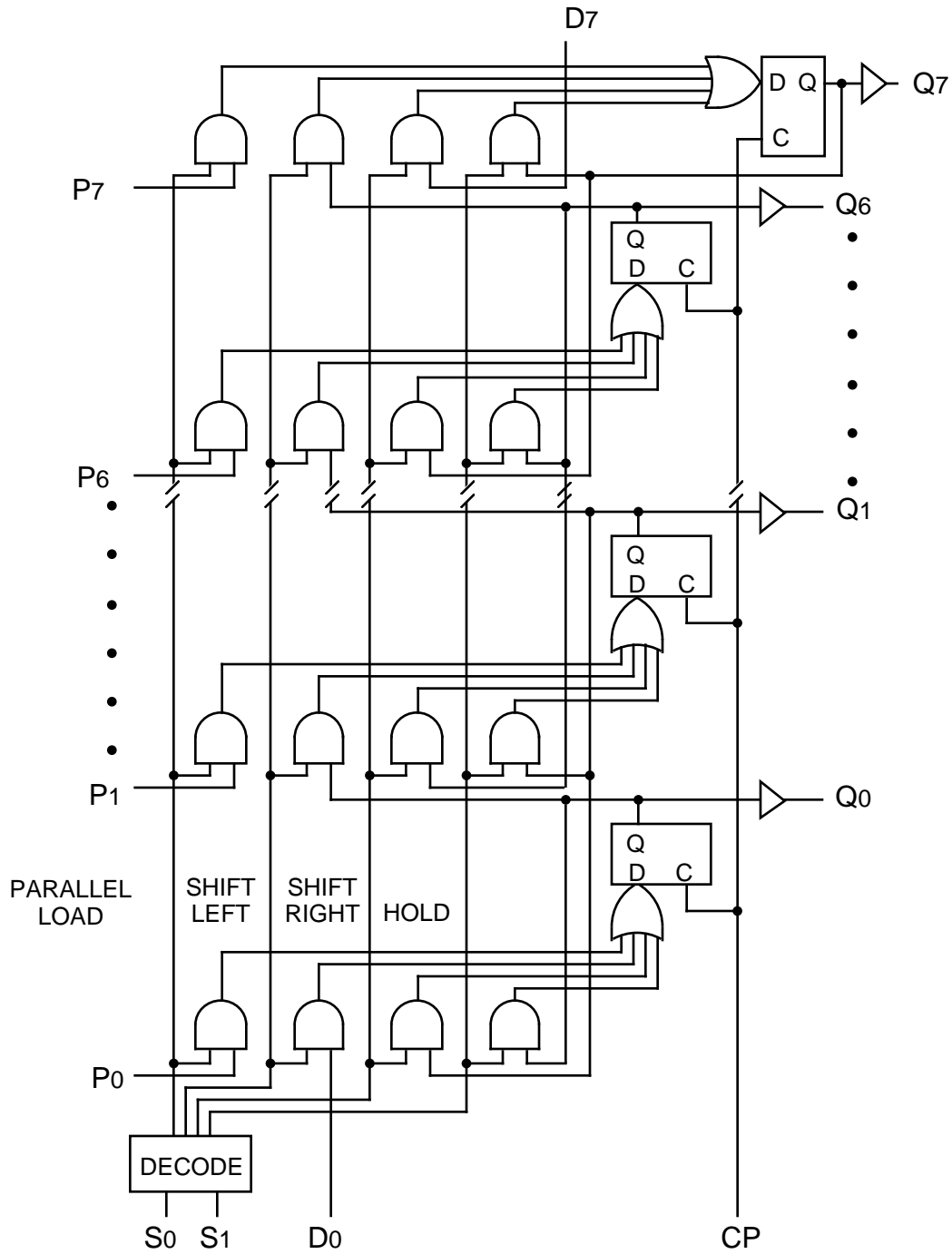
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S341JC	J28-1	Commercial	SY100S341JC	Sn-Pb
SY100S341JCTR ⁽¹⁾	J28-1	Commercial	SY100S341JC	Sn-Pb
SY100S341JZ ⁽²⁾	J28-1	Commercial	SY100S341JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S341JZTR ^(1, 2)	J28-1	Commercial	SY100S341JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM



TRUTH TABLE

Function	Inputs					Outputs							
	D7	D0	S1	S0	CP	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Load Register	X	X	L	L	u	P7	P6	P5	P4	P3	P2	P1	P0
Shift Left	X	L	L	H	u	Q6	Q5	Q4	Q3	Q2	Q1	Q0	L
Shift Left	X	H	L	H	u	Q6	Q5	Q4	Q3	Q2	Q1	Q0	H
Shift Right	L	X	H	L	u	L	Q7	Q6	Q5	Q4	Q3	Q2	Q1
Shift Right	H	X	H	L	u	H	Q7	Q6	Q5	Q4	Q3	Q2	Q1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H	No Change							
Hold	X	X	X	X	L	No Change							

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
u = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

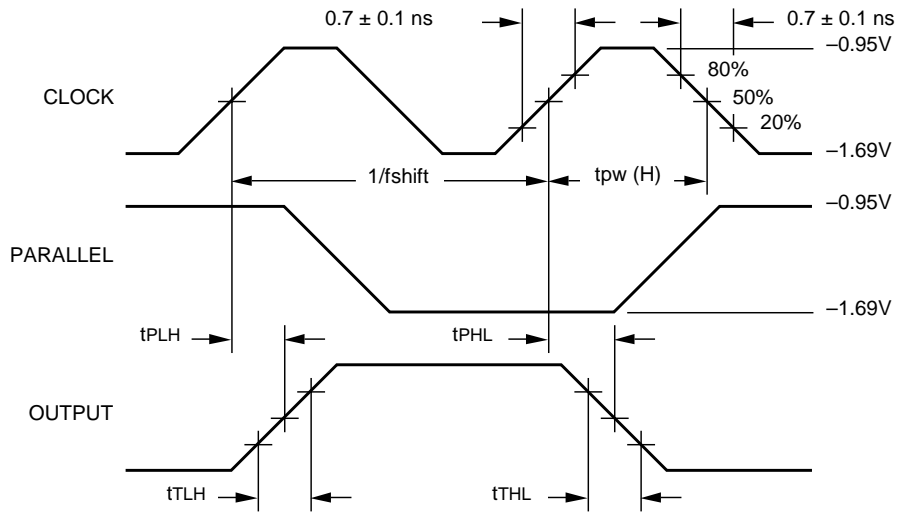
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-150	-102	-71	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

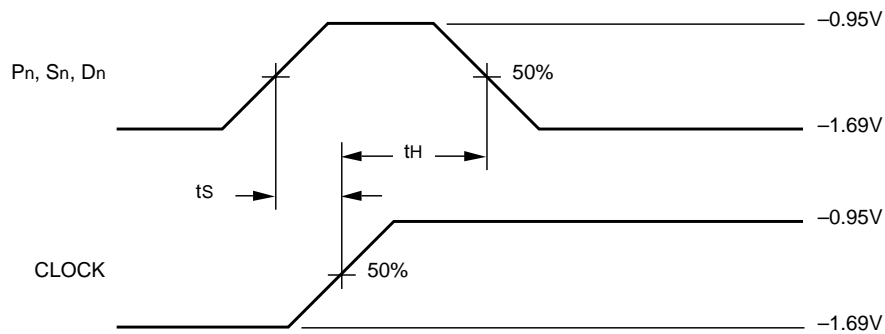
$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f _{shift}	Shift Frequency	600	—	600	—	600	—	MHz	
t _{PLH} t _{PHL}	Propagation Delay CP to Output	450	1200	450	1200	450	1200	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time D _n , P _n S _n	300 600	—	300 600	—	300 600	—	ps	
t _h	Hold Time D _n , P _n S _n	300 0	—	300 0	—	300 0	—	ps	
t _{pw} (H)	Pulse Width HIGH, CP	—	600	—	600	—	600	ps	

TIMING DIAGRAMS



Propagation Delay and Transition Times

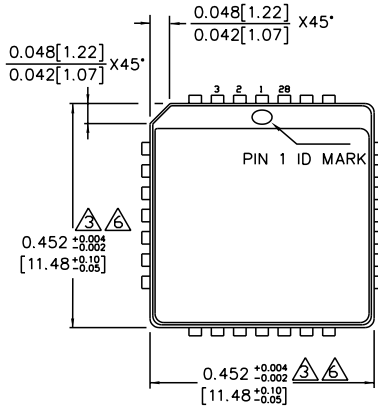


Set-up and Hold Times

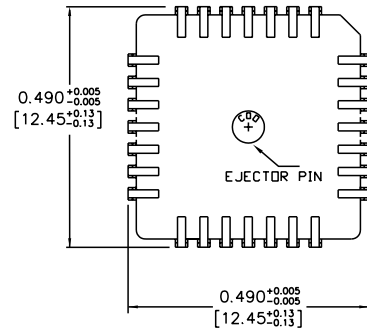
Notes:

1. $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$.
2. t_s is the minimum time before the transition of the clock that information must be present at the data input.
3. t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

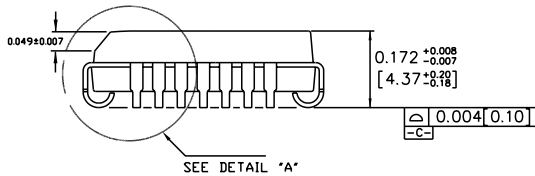
28-PIN PLCC (J28-1)



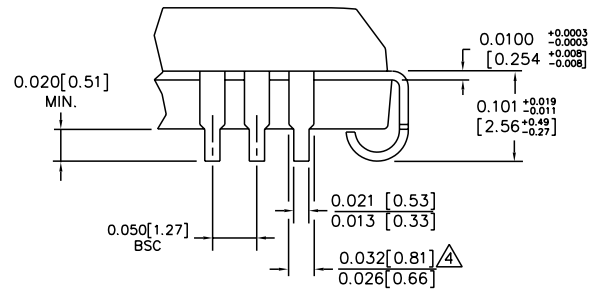
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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