



THE DATASHEET OF SN74GTLP817DGVR

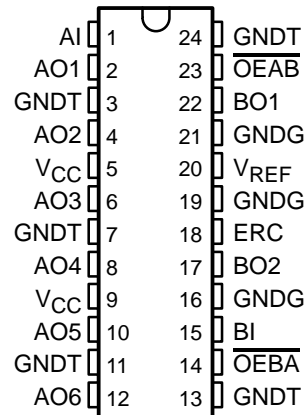


SN74GTLP817 GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285E – OCTOBER 1999 – REVISED AUGUST 2001

- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP-to-LVTTL 1-to-6 Fanout Driver**
- **LVTTL-to-GTLP 1-to-2 Fanout Driver**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **Reduced-Drive LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DG, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLP817 is a medium-drive fanout driver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, and OEC™ circuitry. The improved GTLP OEC circuitry minimizes bus settling time and has been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω. BO1 and BO2 can be tied together to drive an equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP817 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

GNDT is the TTL output ground, while GNDG is the GTLP output ground, and both may be separated from each other for a quieter device.



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 **TEXAS
INSTRUMENTS**

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SN74GTLP817

GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

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description (continued)

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

This device features adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load. ERC automatically is selected to the same speed as alternate source 1-to-6 fanout drivers that use pin 18 for 3.3-V or 5-V V_{CC} .

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SOIC – DW | Tube | SN74GTLP817DW | GTLP817 |
| | | Tape and reel | SN74GTLP817DWR | |
| | TSSOP – PW | Tape and reel | SN74GTLP817PWR | GT817 |
| | TVSOP – DGV | Tape and reel | SN74GTLP817DGVR | GT817 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLP817 is a fanout driver providing LVTTL-to-GTLP translation and GTLP-to-LVTTL translation in the same package.

The LVTTL-to-GTLP direction is a 1-to-2 fanout driver with a single output enable (\overline{OEAB}).

The GTLP-to-LVTTL direction is a 1-to-6 fanout driver with a single output enable (\overline{OEBA}).

Data polarity is inverting for both directions.



Function Tables

OUTPUT CONTROL
 (A to B)

| INPUTS | | OUTPUT | MODE |
|--------|-------------------|-----------------|----------------------|
| AI | \overline{OEAB} | BO _n | |
| X | H | Z | Isolation |
| H | L | L | Inverted transparent |
| L | L | H | |

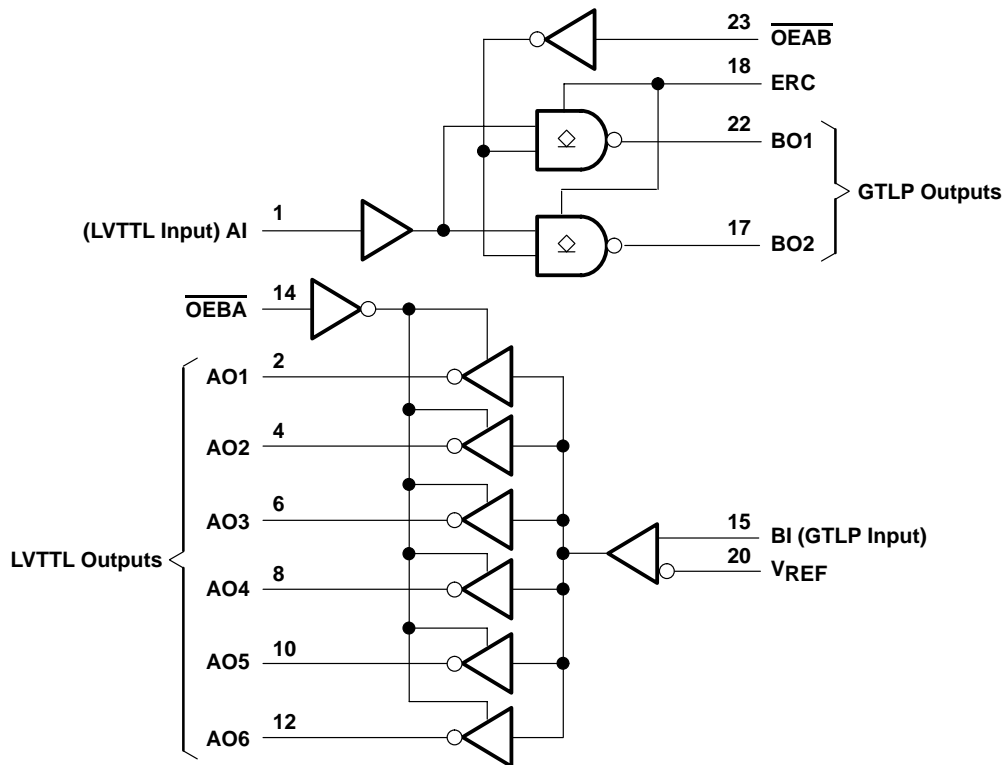
OUTPUT CONTROL
 (B to A)

| INPUTS | | OUTPUT | MODE |
|--------|-------------------|-----------------|----------------------|
| BI | \overline{OEBA} | AO _n | |
| X | H | Z | Isolation |
| H | L | L | Inverted transparent |
| L | L | H | |

B-PORT EDGE-RATE CONTROL (ERC)

| INPUT ERC | | OUTPUT B-PORT EDGE RATE |
|----------------|--------------------|-------------------------------|
| LOGIC LEVEL | NOMINAL VOLTAGE | |
| H | V _{CC} | Slow |
| L | GND | Fast |

logic diagram (positive logic)



SN74GTLP817 GTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

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recommended operating conditions (see Notes 4 through 7)

| | | MIN | NOM | MAX | UNIT | |
|--------------------------|------------------------------------|---------------------|------------------------|-----------------|-----------|-----|
| V _{CC} | Supply voltage | 3.15 | 3.3 | 3.45 | V | |
| V _{TT} | Termination voltage | GTL | 1.14 | 1.2 | 1.26 | V |
| | | GTLP | 1.35 | 1.5 | 1.65 | |
| V _{REF} | Reference voltage | GTL | 0.74 | 0.8 | 0.87 | V |
| | | GTLP | 0.87 | 1 | 1.1 | |
| V _I | Input voltage | BI | V _{TT} | | V | |
| | | AI, \overline{OE} | V _{CC} | 5.5 | | |
| V _{IH} | High-level input voltage | BI | V _{REF} +0.05 | | V | |
| | | ERC | V _{CC} -0.6 | V _{CC} | | 5.5 |
| | | AI, \overline{OE} | 2 | | | |
| V _{IL} | Low-level input voltage | BI | V _{REF} -0.05 | | V | |
| | | ERC | GND | 0.6 | | |
| | | AI, \overline{OE} | 0.8 | | | |
| I _{IK} | Input clamp current | | | -18 | mA | |
| I _{OH} | High-level output current | AO port | | | -12 | mA |
| I _{OL} | Low-level output current | AO port | | | 12 | mA |
| | | BO port | | | 50 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | ns/V | |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 20 | | | μ s/V | |
| T _A | Operating free-air temperature | -40 | | 85 | °C | |

- NOTES:
- All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
 - Normal connection sequence is GND first and V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, V_{REF} (any order) last.
 - V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
 - V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.



SN74GTLP817

GTLTLP-TO-LVTTL 1-TO-6 FANOUT DRIVER

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electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--------------------|-------------------------------|---|--|----------------------|------|---------|------|
| V _{IK} | | V _{CC} = 3.15 V, I _I = -18 mA | | | | -1.2 | V |
| V _{OH} | AO port | V _{CC} = 3.15 V to 3.45 V, I _{OH} = -100 μA | | V _{CC} -0.2 | | | V |
| | | V _{CC} = 3.15 V, I _{OH} = -100 μA | | V _{CC} -0.2 | | | |
| | | V _{CC} = 3.15 V, I _{OH} = -6 mA | | 2.4 | | | |
| | | V _{CC} = 3.15 V, I _{OH} = -12 mA | | 2.2 | | | |
| V _{OL} | AO port | V _{CC} = 3.15 V to 3.45 V, I _{OL} = 100 μA | | | | 0.2 | V |
| | | V _{CC} = 3.15 V, I _{OL} = 100 μA | | | | 0.2 | |
| | | V _{CC} = 3.15 V, I _{OL} = 6 mA | | | | 0.4 | |
| | | V _{CC} = 3.15 V, I _{OL} = 12 mA | | | | 0.5 | |
| | BO port | V _{CC} = 3.15 V, I _{OL} = 100 μA | | | | 0.2 | |
| | | V _{CC} = 3.15 V, I _{OL} = 40 mA | | | | 0.5 | |
| | | V _{CC} = 3.15 V, I _{OL} = 50 mA | | | | 0.55 | |
| I _I | BI, AI, \overline{OE} , ERC | V _{CC} = 3.45 V, V _I = 0 or 5.5 V | | | | ±5 | μA |
| I _{OZH} | AO port | V _{CC} = 3.45 V, V _O = V _{CC} | | | | 10 | μA |
| | BO port | V _{CC} = 3.45 V, V _O = 1.5 V | | | | 5 | |
| I _{OZL} | AO port | V _{CC} = 3.45 V, V _O = GND | | | | -10 | μA |
| | BO port | V _{CC} = 3.45 V, V _O = 5.5 V | | | | -5 | |
| I _{CC} | AO or BO port | V _{CC} = 3.45 V, I _O = 0, V _I (AI or control input) = V _{CC} or GND, V _I (BI input) = V _{TT} or GND | | Outputs high | | 10 | mA |
| | | | | Outputs low | | 10 | |
| | | | | Outputs disabled | | 10 | |
| ΔI _{CC} ‡ | AI, \overline{OE} | V _{CC} = 3.45 V, One A-port or control input at V _{CC} - 0.6 V, Other A-port or control inputs at V _{CC} or GND | | | | 1 | mA |
| C _i | AI, \overline{OE} , ERC | V _I = V _{CC} or 0 | | | | 4 4.4 | pF |
| | BI | V _I = V _{TT} or 0 | | | | 3.5 3.9 | |
| C _o | AO port | V _O = V _{CC} or 0 | | | | 4 4.5 | pF |
| | BO port | V _O = V _{TT} or 0 | | | | 5 5.4 | |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified LVTTTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS | | | MIN | MAX | UNIT |
|-------------------|-------------------------------|---|---------------------|-----|-----|--------|
| I _{off} | V _{CC} = 0, | V _I or V _O = 0 to 5.5 V | | | | 10 μA |
| I _{OZPU} | V _{CC} = 0 to 1.5 V, | V _O = 0.5 V to 3 V, | \overline{OE} = 0 | | | ±30 μA |
| I _{OZPD} | V _{CC} = 1.5 V to 0, | V _O = 0.5 V to 3 V, | \overline{OE} = 0 | | | ±30 μA |

hot-insertion specifications for B port over recommended operating free-air temperature range

| PARAMETER | TEST CONDITIONS | | | MIN | MAX | UNIT |
|-------------------|-------------------------------|---|---------------------|-----|-----|--------|
| I _{off} | V _{CC} = 0, | V _I or V _O = 0 to 1.5 V | | | | 10 μA |
| I _{OZPU} | V _{CC} = 0 to 1.5 V, | V _O = 0.5 V to 1.5 V, | \overline{OE} = 0 | | | ±30 μA |
| I _{OZPD} | V _{CC} = 1.5 V to 0, | V _O = 0.5 V to 1.5 V, | \overline{OE} = 0 | | | ±30 μA |



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTLP (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | EDGE RATE† | MIN | TYP‡ | MAX | UNIT |
|-----------|-----------------------------------|-------------|------------|-----|------|-----|------|
| t_{PLH} | AI | BO | Slow | 3 | | 6 | ns |
| t_{PHL} | | | | 1.8 | | 4.7 | |
| t_{PLH} | AI | BO | Fast | 2 | | 5 | ns |
| t_{PHL} | | | | 1.5 | | 4.2 | |
| t_{en} | \overline{OEAB} | BO | Slow | 3 | | 6.1 | ns |
| t_{dis} | | | | 2 | | 4.7 | |
| t_{en} | \overline{OEAB} | BO | Fast | 2.1 | | 6 | ns |
| t_{dis} | | | | 1.5 | | 4.7 | |
| t_r | Rise time, B outputs (20% to 80%) | | Slow | 2.5 | | ns | |
| | | | Fast | 1.4 | | | |
| t_f | Fall time, B outputs (80% to 20%) | | Slow | 1.7 | | ns | |
| | | | Fast | 1 | | | |
| t_{PLH} | BI | AO | – | 2.3 | | 6 | ns |
| t_{PHL} | | | | 1.9 | | 4.7 | |
| t_{en} | \overline{OEBA} | AO | – | 1.1 | | 6.3 | ns |
| t_{dis} | | | | 1.2 | | 5 | |

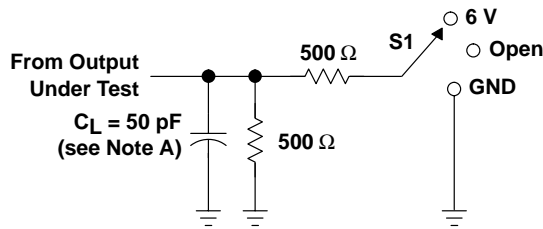
† Slow (ERC = V_{CC}) and Fast (ERC = GND)

‡ All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN74GTLP817 GTLT-TO-LVTTL 1-TO-6 FANOUT DRIVER

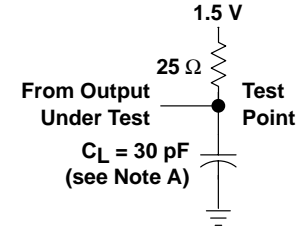
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PARAMETER MEASUREMENT INFORMATION

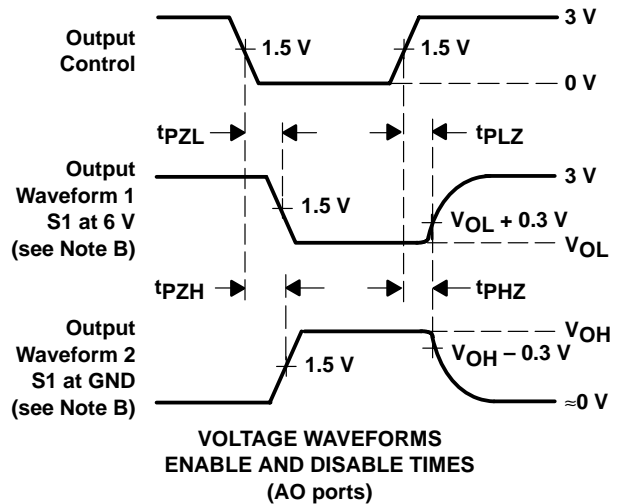
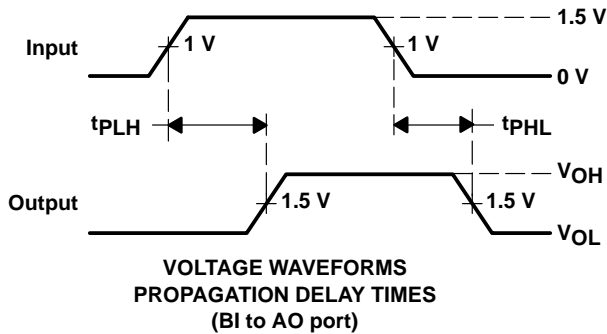
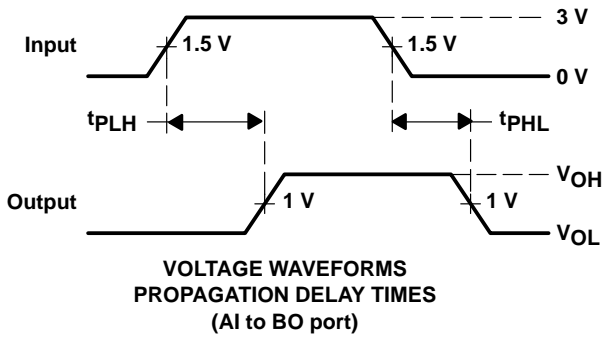


LOAD CIRCUIT FOR AO PORTS

| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PHZ} | GND |



LOAD CIRCUIT FOR BO PORTS



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50 \Omega$, $t_r \approx 2$ ns, $t_f \approx 2$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

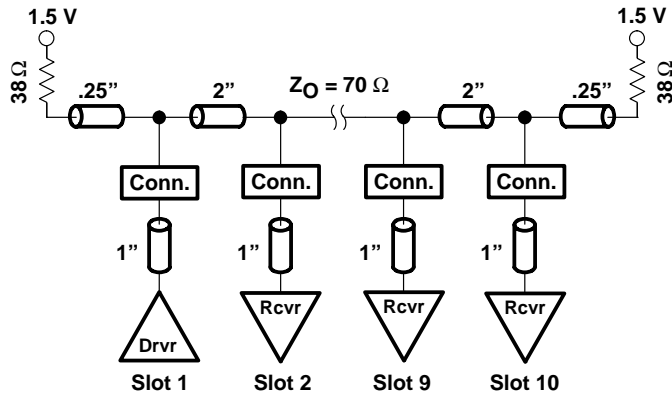


Figure 2. Medium-Drive Test Backplane

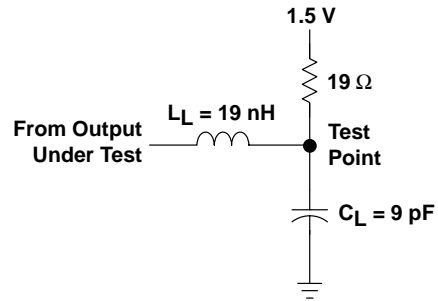


Figure 3. Medium-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTLP (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | EDGE RATE† | TYP‡ | UNIT |
|-----------|-----------------------------------|-------------|------------|------|------|
| t_{PLH} | AI | BO | Slow | 4.4 | ns |
| t_{PHL} | | | | 4.4 | |
| t_{PLH} | AI | BO | Fast | 3.2 | ns |
| t_{PHL} | | | | 3.2 | |
| t_{en} | \overline{OEAB} | BO | Slow | 4 | ns |
| t_{dis} | | | | 4.4 | |
| t_{en} | \overline{OEAB} | BO | Fast | 2.9 | ns |
| t_{dis} | | | | 3.1 | |
| t_r | Rise time, B outputs (20% to 80%) | | Slow | 1.8 | ns |
| | | | Fast | 1 | |
| t_f | Fall time, B outputs (80% to 20%) | | Slow | 2 | ns |
| | | | Fast | 1.6 | |

† Slow (ERC = V_{CC}) and Fast (ERC = GND)

‡ All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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