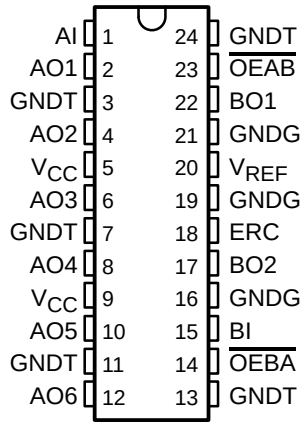
THE DATASHEET OF

SN74GTLP817DW

- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP-to-LVTTL 1-to-6 Fanout Driver**
- **LVTTL-to-GTLP 1-to-2 Fanout Driver**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **Reduced-Drive LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLP817 is a medium-drive fanout driver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, and OEC™ circuitry. The improved GTLP OEC circuitry minimizes bus settling time and has been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω. BO1 and BO2 can be tied together to drive an equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP817 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

GNDT is the TTL output ground, while GNDG is the GTLP output ground, and both may be separated from each other for a quieter device.

description (continued)

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

This device features adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load. ERC automatically is selected to the same speed as alternate source 1-to-6 fanout drivers that use pin 18 for 3.3-V or 5-V V_{CC}.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLP817DW	GTLP817
		Tape and reel	SN74GTLP817DWR	
	TSSOP – PW	Tape and reel	SN74GTLP817PWR	GT817
	TVSOP – DGV	Tape and reel	SN74GTLP817DGVR	GT817

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLP817 is a fanout driver providing LVTTL-to-GTLP translation and GTLP-to-LVTTL translation in the same package.

The LVTTL-to-GTLP direction is a 1-to-2 fanout driver with a single output enable ($\overline{OEAB}$).

The GTLP-to-LVTTL direction is a 1-to-6 fanout driver with a single output enable ($\overline{OEBA}$).

Data polarity is inverting for both directions.

Function Tables

OUTPUT CONTROL (A to B)

INPUTS		OUTPUT BOn	MODE
AI	$\overline{OEAB}$		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

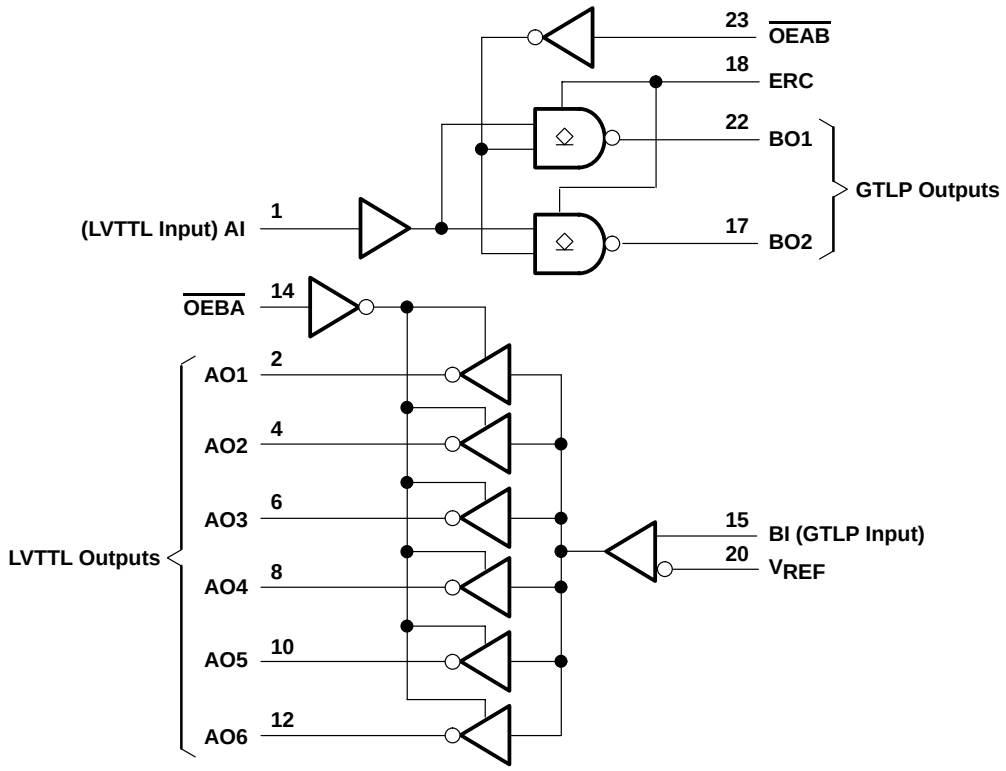
OUTPUT CONTROL (B to A)

INPUTS		OUTPUT AOn	MODE
BI	$\overline{OEBA}$		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V_{CC}	Slow
L	GND	Fast

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Ground dc voltage difference, ($|V_{GNDG} – V_{GNDT}|$) . . . . . 0.3 V
Input voltage range, V_I (see Note 1): AI port and control inputs . . . . . –0.5 V to 7 V
BI port and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1): AO port . . . . . –0.5 V to 7 V
BO port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: AO port . . . . . 24 mA
BO port . . . . . 100 mA
Current into any A output in the high state, I_O (see Note 2) . . . . . 24 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGV package . . . . . 86°C/W
DW package . . . . . 46°C/W
PW package . . . . . 88°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	BI			V_{TT}	V
		AI, $\overline{OE}$		V_{CC}	5.5	
V_{IH}	High-level input voltage	BI	V_{REF}+0.05			V
		ERC	V_{CC}–0.6	V_{CC}	5.5	
		AI, $\overline{OE}$	2			
V_{IL}	Low-level input voltage	BI			V_{REF}–0.05	V
		ERC		GND	0.6	
		AI, $\overline{OE}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–12	mA
I_{OL}	Low-level output current	AO port			12	mA
		BO port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			μs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Normal connection sequence is GND first and V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –100 µA	V_{CC}–0.2			
			I_{OH} = –6 mA	2.4			
			I_{OH} = –12 mA	2.2			
V_{OL}	AO port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	
			I_{OL} = 6 mA			0.4	
			I_{OL} = 12 mA			0.5	
	BO port	V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	
			I_{OL} = 40 mA			0.5	
			I_{OL} = 50 mA			0.55	
I_I	BI, AI, $\overline{OE}$, ERC	V_{CC} = 3.45 V	V_I = 0 or 5.5 V			±5	µA
I_{OZH}	AO port	V_{CC} = 3.45 V	V_O = V_{CC}			10	µA
	BO port		V_O = 1.5 V			5	
I_{OZL}	AO port	V_{CC} = 3.45 V	V_O = GND			–10	µA
	BO port		V_O = 5.5 V			–5	
I_{CC}	AO or BO port	V_{CC} = 3.45 V, I_O = 0, V_I (AI or control input) = V_{CC} or GND, V_I (BI input) = V_{TT} or GND	Outputs high			10	mA
			Outputs low			10	
			Outputs disabled			10	
ΔI_{CC}‡	AI, $\overline{OE}$	V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1	mA
C_i	AI, $\overline{OE}$, ERC	V_I = V_{CC} or 0			4	4.4	pF
	BI	V_I = V_{TT} or 0			3.5	3.9	
C_o	AO port	V_O = V_{CC} or 0			4	4.5	pF
	BO port	V_O = V_{TT} or 0			5	5.4	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified LVTTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

hot-insertion specifications for B port over recommended operating free-air temperature range

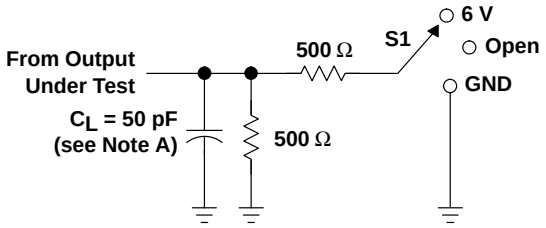
PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 1.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±30	µA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

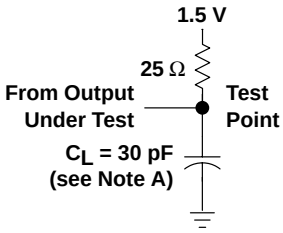
PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	AI	BO	Slow	3		6	ns
t_{PHL}				1.8		4.7	
t_{PLH}	AI	BO	Fast	2		5	ns
t_{PHL}				1.5		4.2	
t_{en}	$\overline{OEAB}$	BO	Slow	3		6.1	ns
t_{dis}				2		4.7	
t_{en}	$\overline{OEAB}$	BO	Fast	2.1		6	ns
t_{dis}				1.5		4.7	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.5		ns
			Fast		1.4		
t_f	Fall time, B outputs (80% to 20%)		Slow		1.7		ns
			Fast		1		
t_{PLH}	BI	AO	–	2.3		6	ns
t_{PHL}				1.9		4.7	
t_{en}	$\overline{OEBA}$	AO	–	1.1		6.3	ns
t_{dis}				1.2		5	

† Slow (ERC = V_{CC}) and Fast (ERC = GND)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

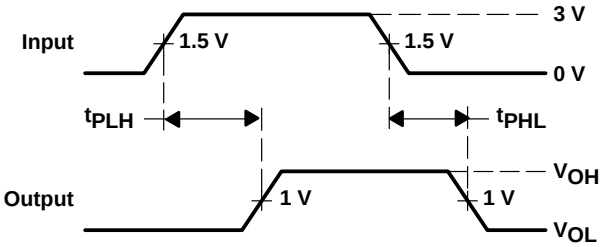


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

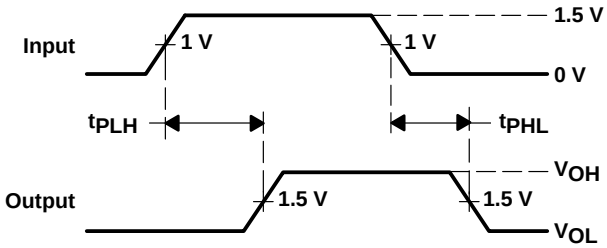


LOAD CIRCUIT FOR AO PORTS

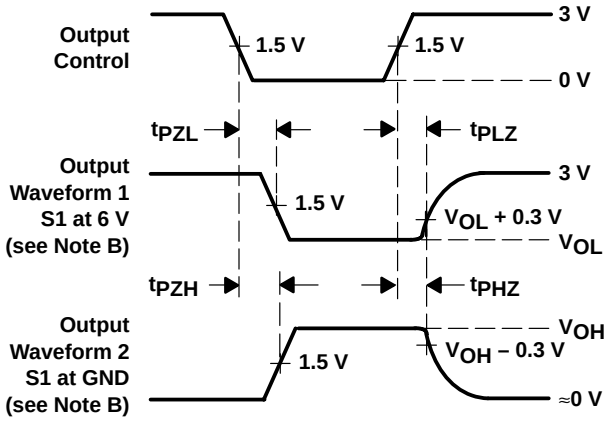
LOAD CIRCUIT FOR BO PORTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(AI to BO port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(BI to AO port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(AO ports)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

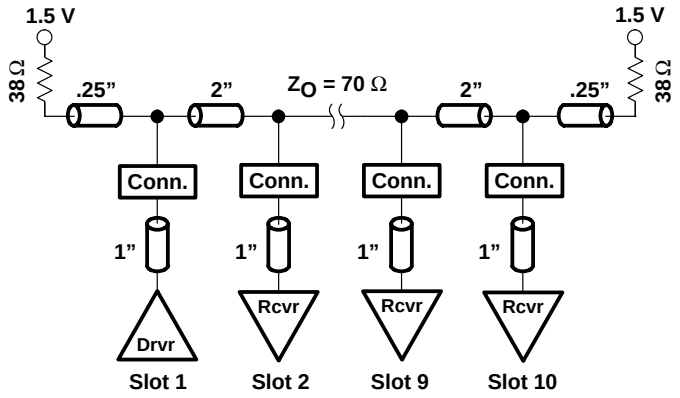


Figure 2. Medium-Drive Test Backplane

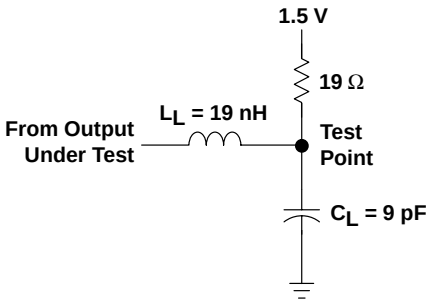


Figure 3. Medium-Drive RLC Network

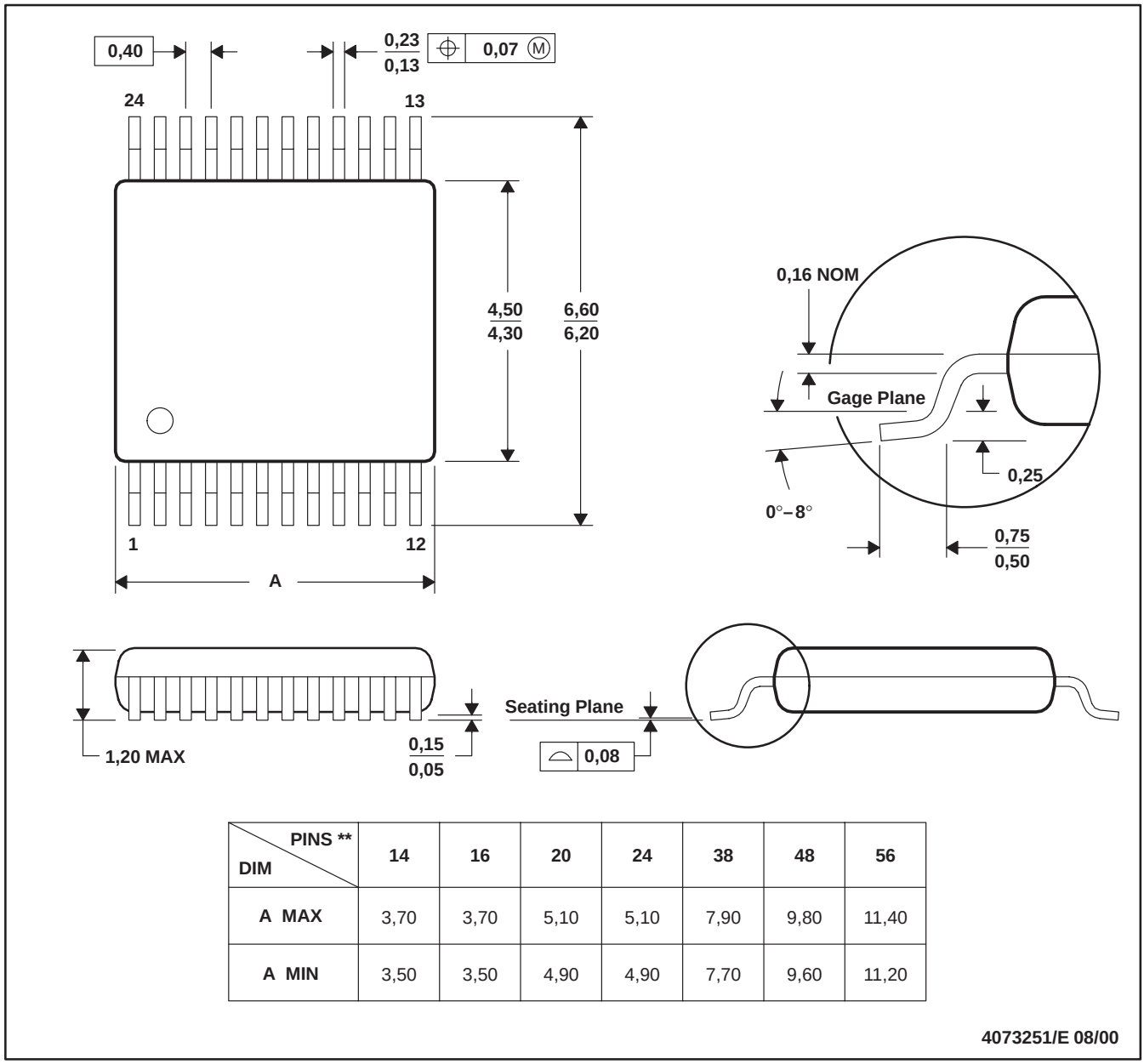
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	AI	BO	Slow	4.4	ns
t_{PHL}				4.4	
t_{PLH}	AI	BO	Fast	3.2	ns
t_{PHL}				3.2	
t_{en}	$\overline{OEAB}$	BO	Slow	4	ns
t_{dis}				4.4	
t_{en}	$\overline{OEAB}$	BO	Fast	2.9	ns
t_{dis}				3.1	
t_r	Rise time, B outputs (20% to 80%)		Slow	1.8	ns
			Fast	1	
t_f	Fall time, B outputs (80% to 20%)		Slow	2	ns
			Fast	1.6	

† Slow (ERC = V_{CC}) and Fast (ERC = GND)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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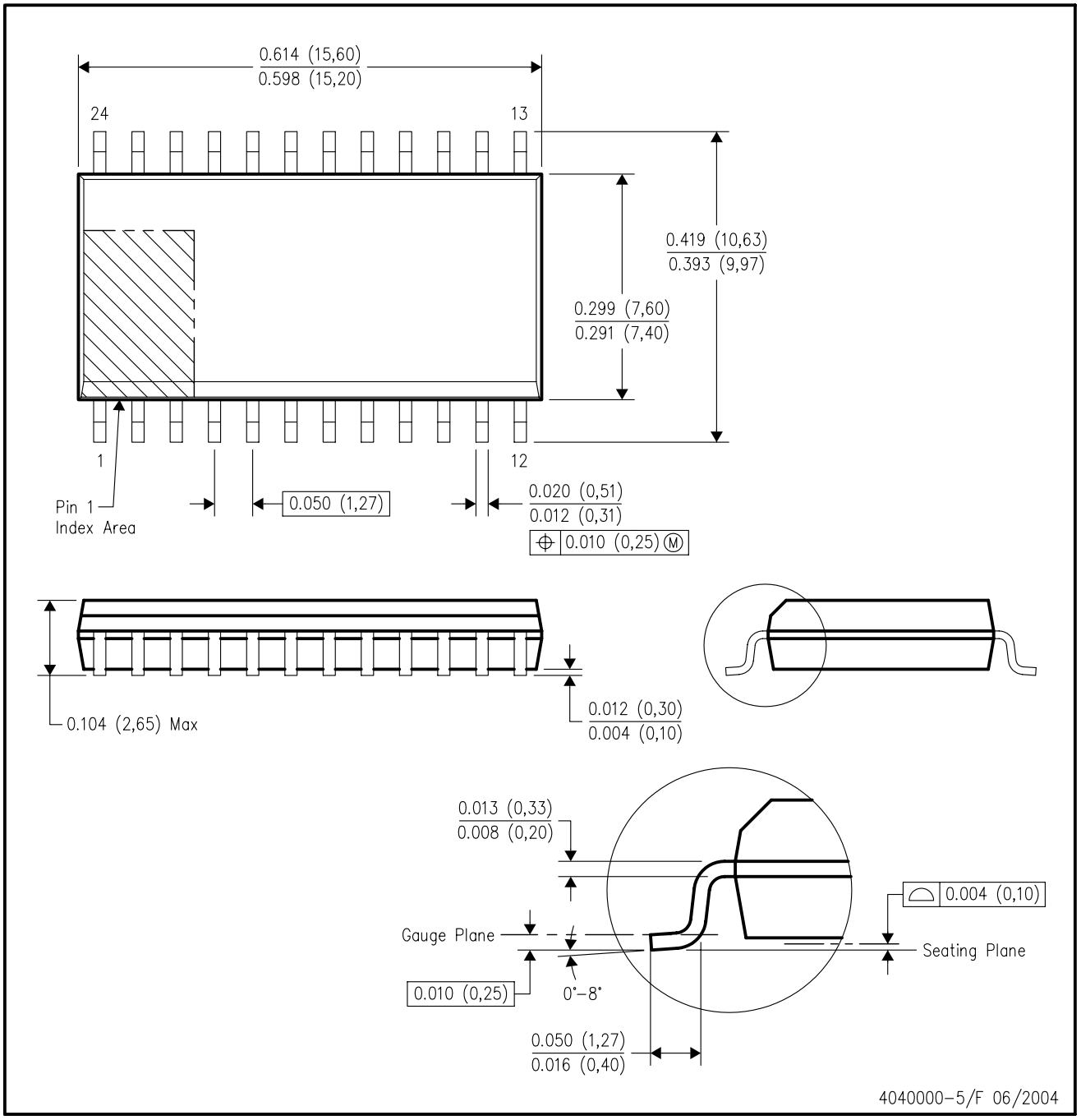
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

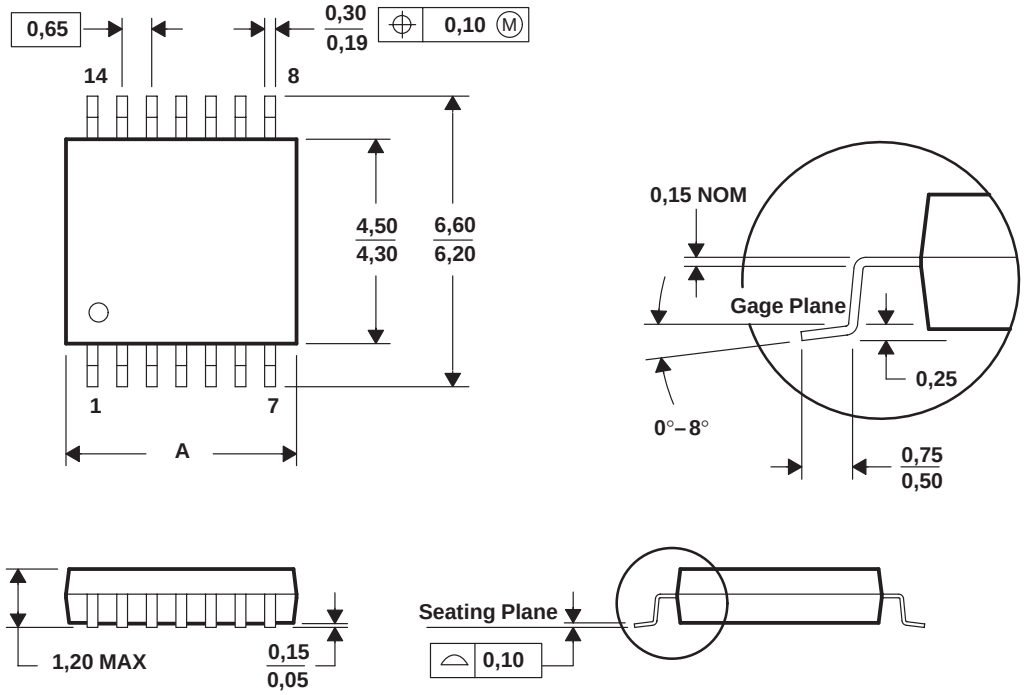
DW (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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