THE DATASHEET OF

SN74LVCC4245ADBRE4

SN74LVCC4245A Octal Dual-Supply Bus Transceiver With Configurable Output Voltage and 3-State Outputs

1 Features

- Bidirectional voltage translator
- 4.5 V to 5.5 V on A port and 2.7 V to 5.5 V on B port
- Control inputs V_{IH} and V_{IL} levels are referenced to V_{CCA} voltage
- Latch-up performance exceeds 250 mA per JESD 17
- ESD protection exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Level translation
- Personal electronics
- Industrial
- Enterprise
- Telecom

3 Description

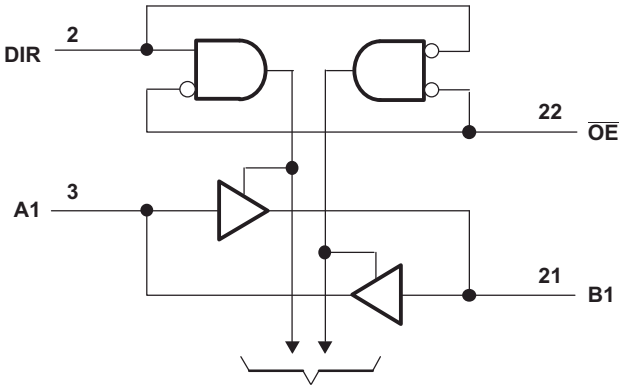
This 8-bit (octal) noninverting bus transceiver uses two separate power-supply rails. The A port, V_{CCA}, is dedicated to accepting a 5-V supply level, and the configurable B port, which is designed to track V_{CCB}, accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

The SN74LVCC4245A device is designed for asynchronous communication between data buses. The SN74LVCC4245A device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses effectively are isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA}.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCC4245A	DB (SSOP, 24)	8.20 mm × 5.30 mm
	DW (SOIC, 24)	15.40 mm × 7.50 mm
	NS (SOP, 24)	15.00 mm × 5.30 mm
	PW (TSSOP, 24)	7.80 mm × 4.40 mm

(1) For available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (March 2005) to Revision N (December 2022)	Page
• Removed ordering information	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Pin Configuration and Functions*, *Detailed Description*, *Application and Implementation*, *Layout* sections	1
• Added thermal values for PW package	5

5 Pin Configuration and Functions

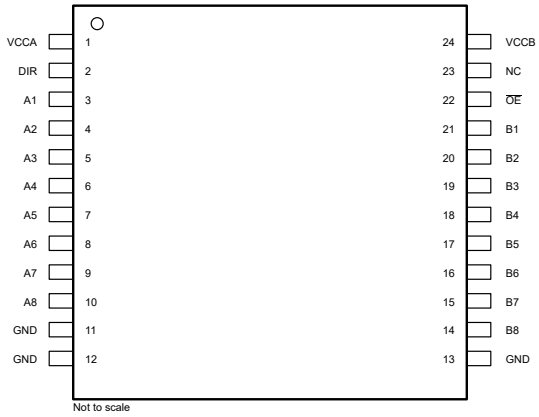


Figure 5-1. DB, DW, NS, or PW Package, SSOP, SOIC, SOP, or TSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
V_{CCA}	1	—	A port power
DIR	2	I	Dir input
A1	3	I/O	A1 port
A2	4	I/O	A2 port
A3	5	I/O	A3 port
A4	6	I/O	A4 port
A5	7	I/O	A5 port
A6	8	I/O	A6 port
A7	9	I/O	A7 port
A8	10	I/O	A8 port
GND	11	—	Ground
GND	12	—	
GND	13	—	
B8	14	I/O	B8 port
B7	15	I/O	B7 port
B6	16	I/O	B6 port
B5	17	I/O	B5 port
B4	18	I/O	B4 port
B3	19	I/O	B3 port
B2	20	I/O	B2 port
B1	21	I/O	B1 port
$\overline{OE}$	22	I	Output Enable active low
NC	23	—	Unconnected
V_{CCB}	24	—	B port power

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	6	V
V_I	Input voltage range(2)	I/O ports (A port)	–0.5	V_{CCA} + 0.5	V
		I/O ports (B port)	–0.5	V_{CCB} + 0.5	
		Except I/O ports	–0.5	V_{CCA} + 0.5	
V_O	Output voltage range(2)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance(3)	DW package		46	°C/W
		NS package		65	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 6 V maximum.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

PARAMETER		DEFINITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(1)

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage			4.5	5	5.5	V
V_{CCB}	Supply voltage			2.7	3.3	5.5	V
V_{IHA}	High-level input voltage	4.5 V	2.7 V	2			V
			3.6 V	2			
		5.5 V	5.5 V	2			
V_{IHB}	High-level input voltage	4.5 V	2.7 V	2			V
			3.6 V	2			
		5.5 V	5.5 V	3.85			
V_{ILA}	Low-level input voltage	4.5 V	2.7 V			0.8	V
			3.6 V			0.8	
		5.5 V	5.5 V			0.8	
V_{ILB}	Low-level input voltage	4.5 V	2.7 V			0.8	V
			3.6 V			0.8	
		5.5 V	5.5 V			1.65	
V_{IH}	High-level input voltage (control pins) (referenced to V_{CCA})	4.5 V	2.7 V	2			V
			3.6 V	2			
		5.5 V	5.5 V	2			
V_{IL}	Low-level input voltage (control pins) (referenced to V_{CCA})	4.5 V	2.7 V			0.8	V
			3.6 V			0.8	
		5.5 V	5.5 V			0.8	
V_{IA}	Input voltage			0		V_{CCA}	V
V_{IB}	Input voltage			0		V_{CCB}	V
V_{OA}	Output voltage			0		V_{CCA}	V
V_{OB}	Output voltage			0		V_{CCB}	V
I_{OHA}	High-level output current	4.5 V	3 V			–24	mA
I_{OHB}	High-level output current	4.5 V	2.7 V to 4.5 V			–24	mA
I_{OLA}	Low-level output current	4.5 V	3 V			24	mA
I_{OLB}	Low-level output current	4.5 V	2.7 V to 4.5 V			24	mA
T_A	Operating free-air temperature			–40		85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVCC4245A		UNIT
		PW (TSSOP)	DB (SSOP)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.6	90.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.7	51.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.8	49.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	18.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.4	49.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –100 µA		4.5 V	3 V	4.4	4.49		V
		I_{OH} = –24 mA		4.5 V	3 V	3.76	4.25		
V_{OHB}		I_{OH} = –100 µA		4.5 V	3 V	2.9	2.99		V
		I_{OH} = –12 mA		4.5 V	2.7 V	2.2	2.5		
					3 V	2.46	2.85		
		I_{OH} = –24 mA		4.5 V	2.7 V	2.1	2.3		
					3 V	2.25	2.65		
					4.5 V	3.76	4.25		
V_{OLA}		I_{OL} = 100 µA		4.5 V	3 V			0.1	V
		I_{OL} = 24 mA		4.5 V	3 V		0.21	0.44	
V_{OLB}		I_{OL} = 100 µA		4.5 V	3 V			0.1	V
		I_{OL} = 12 mA		4.5 V	2.7 V		0.11	0.44	
		I_{OL} = 24 mA		4.5 V	2.7 V		0.22	0.5	
					3 V		0.21	0.44	
					4.5 V		0.18	0.44	
I_I	Control inputs	V_I = V_{CCA} or GND		5.5 V	3.6 V		±0.1	±1	µA
					5.5 V		±0.1	±1	
I_{OZ} (1)	A or B ports	V_O = $V_{CCA/B}$ or GND,	V_I = V_{IL} or V_{IH}	5.5 V	3.6 V		±0.5	±5	µA
I_{CCA}	B to A	A_n = V_{CC} or GND		5.5 V	Open		8	80	µA
		I_O (A port) = 0,	B_n = V_{CCB} or GND	5.5 V	3.6 V		8	80	
					5.5 V		8	80	
I_{CCB}	A to B	A_n = V_{CCA} or GND,	I_O (B port) = 0	5.5 V	3.6 V		5	50	µA
					5.5 V		8	80	
ΔI_{CCA} (2)	A port	V_I = V_{CCA} – 2.1 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND and DIR at V_{CCA}		5.5 V	5.5 V		1.35	1.5	mA
	$\overline{OE}$	V_I = V_{CCA} – 2.1 V, Other inputs at V_{CCA} or GND, DIR at V_{CCA} or GND		5.5 V	5.5 V		1	1.5	
	DIR	V_I = V_{CCA} – 2.1 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at V_{CCA} or GND		5.5 V	3.6 V		1	1.5	
ΔI_{CCB} (2)	B port	V_I = V_{CCB} – 0.6 V, Other inputs at V_{CCB} or GND, $\overline{OE}$ at GND and DIR at GND		5.5 V	3.6 V		0.35	0.5	mA
C_i	Control inputs	V_I = V_{CCA} or GND		Open	Open		5		pF
C_{io}	A or B ports	V_O = $V_{CCA/B}$ or GND		5 V	3.3 V		11		pF

(1) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 8-1 through Figure 11-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 5 V ± 0.5 V		V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 2.7 V to 3.6 V		UNIT
			MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	7.1	1	7	ns
t_{PLH}			1	6	1	7	
t_{PHL}	B	A	1	6.8	1	6.2	ns
t_{PLH}			1	6.1	1	5.3	
t_{PZL}	$\overline{OE}$	A	1	9	1	9	ns
t_{PZH}			1	8.3	1	8	
t_{PZL}	$\overline{OE}$	B	1	8.2	1	10	ns
t_{PZH}			1	8.1	1	10.2	
t_{PLZ}	$\overline{OE}$	A	1	4.7	1	5.2	ns
t_{PHZ}			1	4.9	1	5.2	
t_{PLZ}	$\overline{OE}$	B	1	5.4	1	5.9	ns
t_{PHZ}			1	6.3	1	7.4	

6.7 Operating Characteristics

V_{CCA} = 5 V, V_{CCB} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 0, f = 10 MHz	20	pF
		Outputs disabled		6.5	

6.8 Typical Characteristics

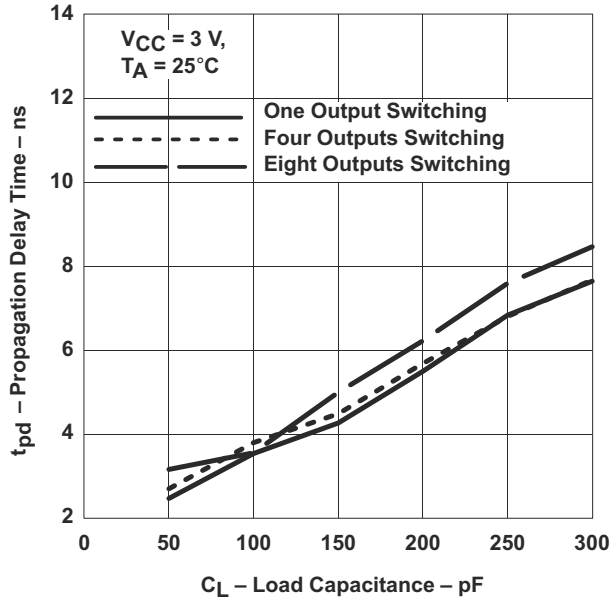


Figure 6-1. Propagation Delay (Low to High Transition) vs Load Capacitance

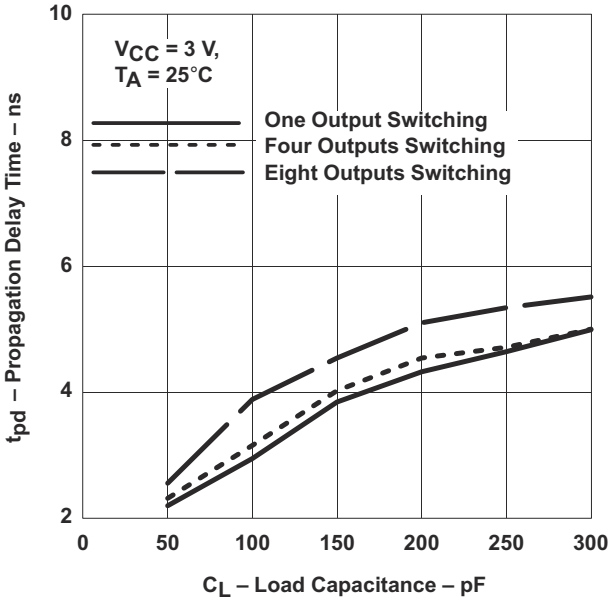


Figure 6-2. Propagation Delay (High to Low Transition) vs Load Capacitance

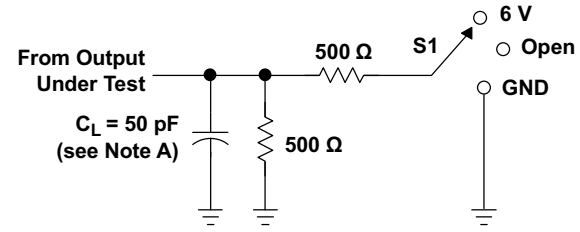
7 Power-Up Consideration

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pull up resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), then ramp it with V_{CCA}. Otherwise, keep DIR low.

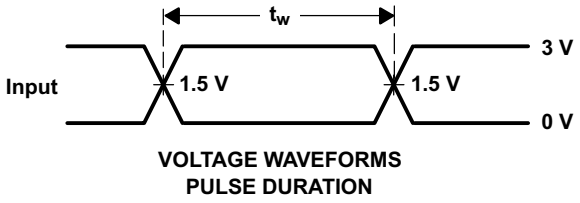
For more information, refer to the *Voltage-Level-Translation Devices* application note.

8 Parameter Measurement Information For A to B V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 2.7 V to 3.6 V

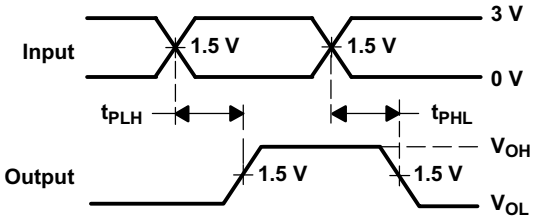


LOAD CIRCUIT

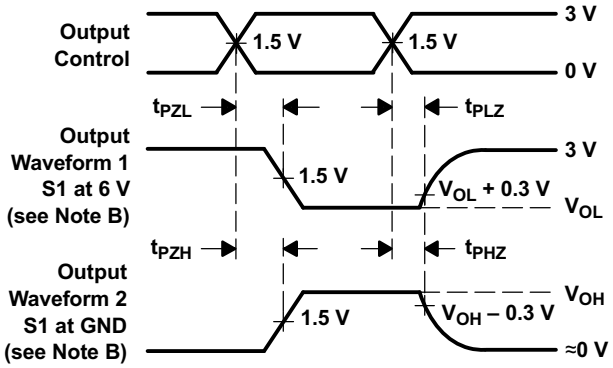
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

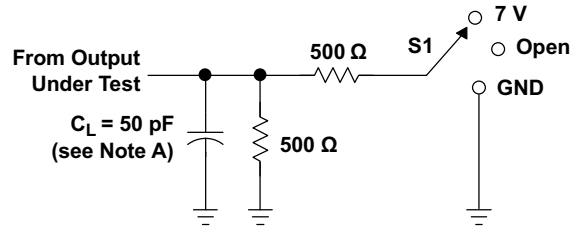


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

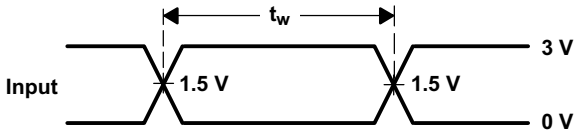
Figure 8-1. Load Circuit and Voltage Waveforms

9 Parameter Measurement Information For A to B
V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 3.6 V to 5.5 V

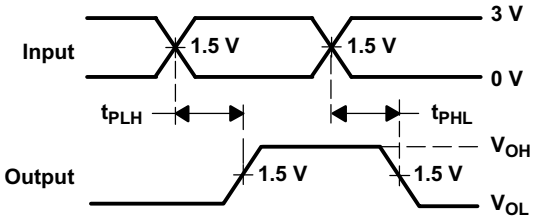


LOAD CIRCUIT

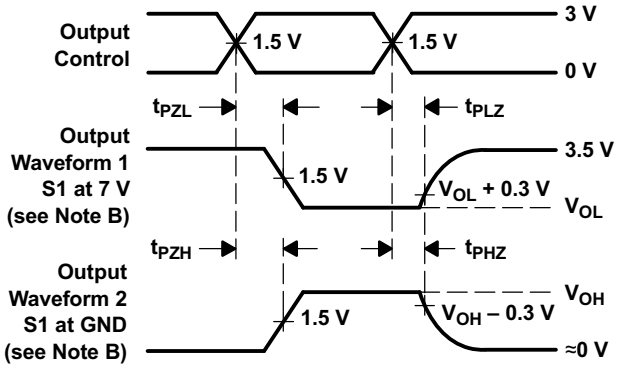
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

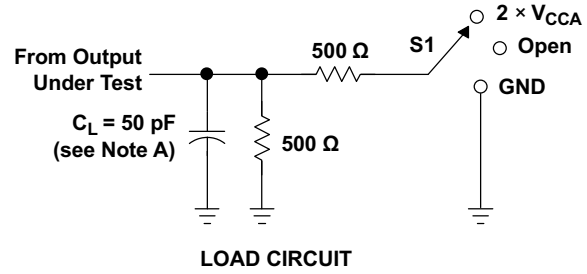


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

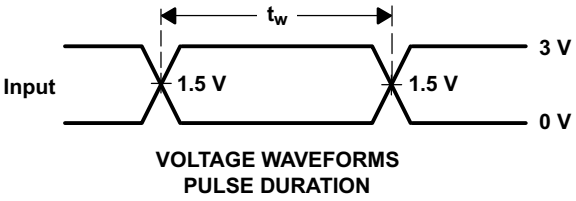
Figure 9-1. Load Circuit and Voltage Waveforms

10 Parameter Measurement Information For B to A V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 2.7 V to 3.6 V

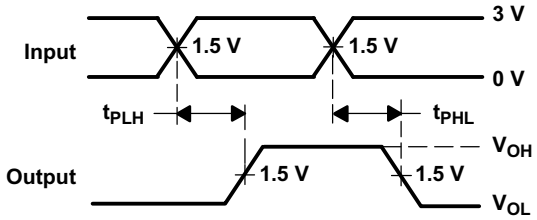


LOAD CIRCUIT

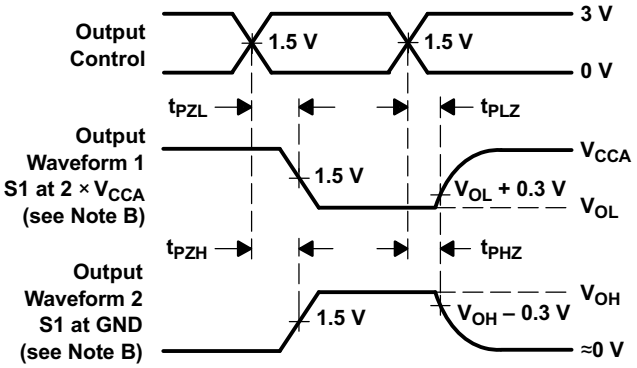
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CCA} GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

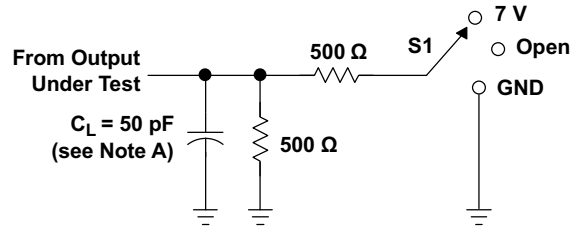


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

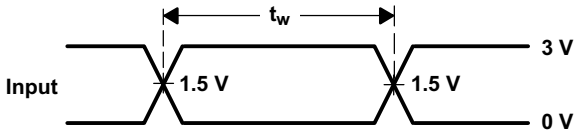
Figure 10-1. Load Circuit and Voltage Waveforms

11 Parameter Measurement Information For B to A V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 3.6 V to 5.5 V

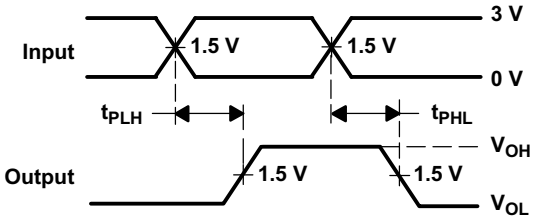


LOAD CIRCUIT

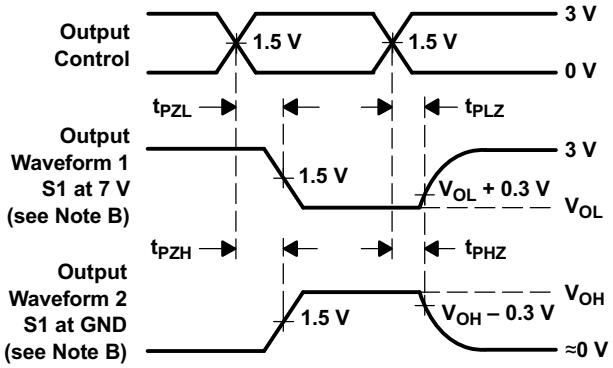
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

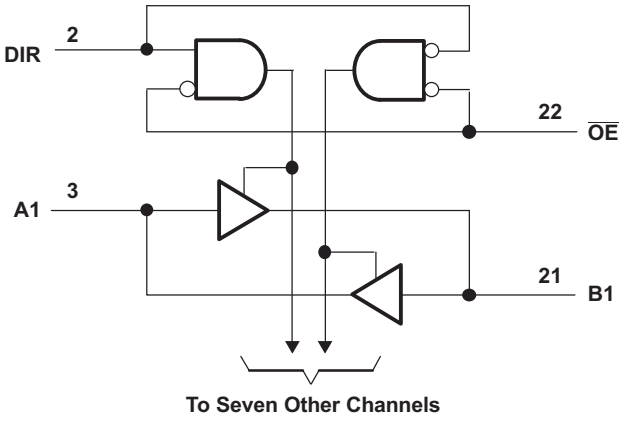
Figure 11-1. Load Circuit and Voltage Waveforms

12 Detailed Description

12.1 Overview

SN74LVCC4245A is an 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 3.3 V, and A port has V_{CCA}, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa, designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA}.

12.2 Functional Block Diagram



12.3 Feature Description

- 24 mA drive at 3-V supply
  - Good for heavier loads and longer traces
- Low V_{IH}
  - Allows 3.3-V to 5-V translation

12.4 Device Functional Modes

Table 12-1. Function Table (Each Transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

13 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

13.1 Application Information

The SN74LVCC4245A device pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional SN74LVC4245A device's pinout. SN74LVCC4245A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

13.2 Typical Application

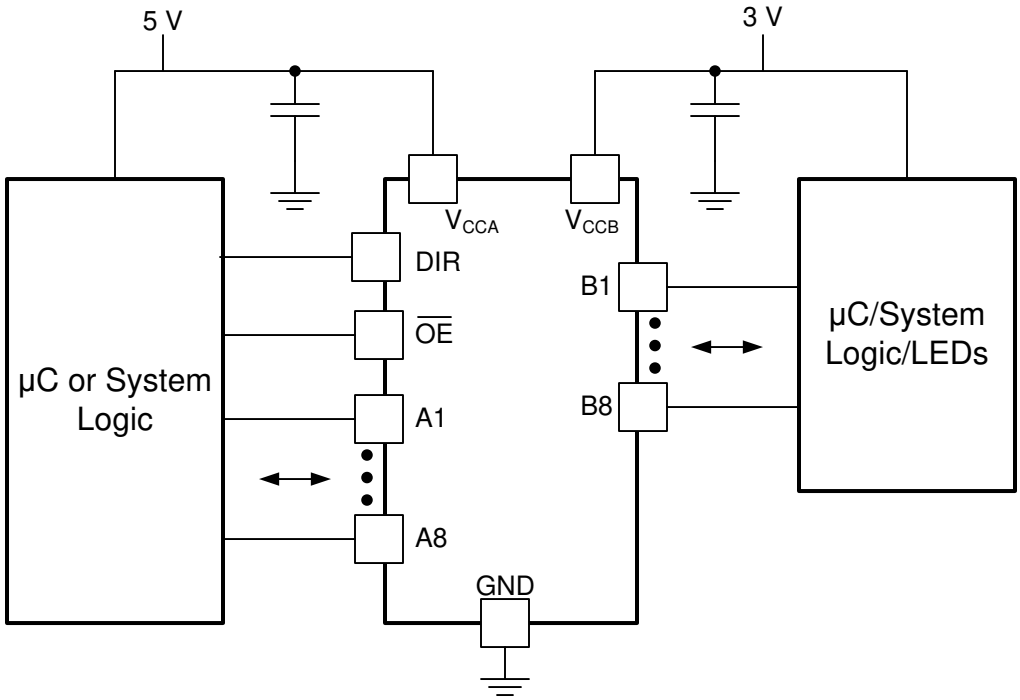


Figure 13-1. Typical Application Schematic

13.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

13.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifcations, see (Δt/ΔV) in the *Section 6.3* table.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in the *Section 6.3* table.
2. Recommend Output Conditions:
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Section 6.1* table.
   - Outputs should not be pulled above V_{CC}.
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

13.2.3 Application Curves

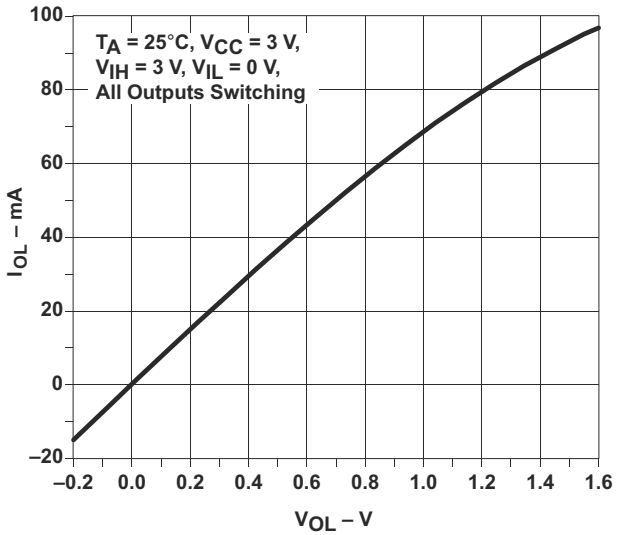


Figure 13-2. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

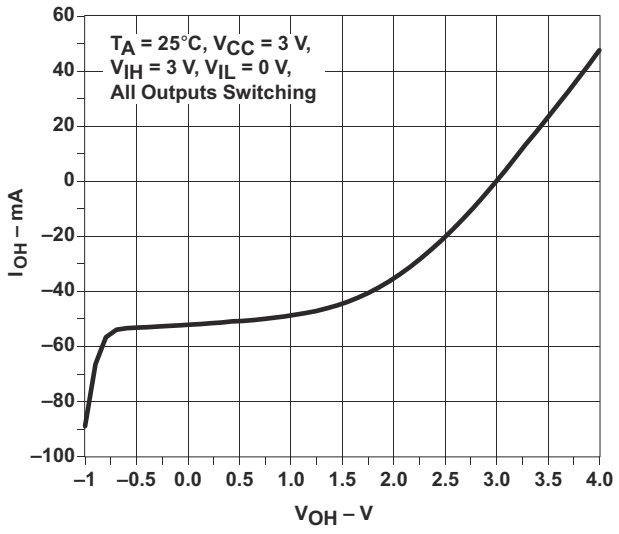


Figure 13-3. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

14 Power Supply Recommendations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), then ramp it with V_{CCA}. Otherwise, keep DIR low.

15 Layout

15.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 15-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

15.2 Layout Example

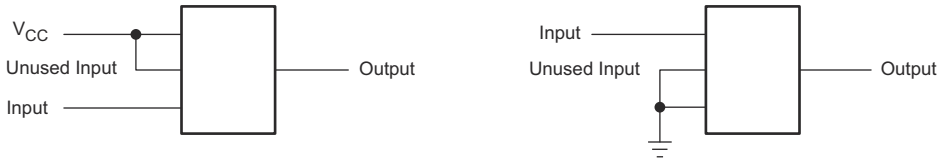


Figure 15-1. Layout Diagram

16 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

16.1 Documentation Support

16.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Voltage-Level-Translation Devices* application note

16.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

16.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

16.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

16.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

16.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

17 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCC4245ADBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LG245A	Samples
SN74LVCC4245ADW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC4245A	Samples
SN74LVCC4245ADWE4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC4245A	Samples
SN74LVCC4245ADWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LVCC4245A	Samples
SN74LVCC4245ADWRG4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC4245A	Samples
SN74LVCC4245ANSR	ACTIVE	SO	NS	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC4245A	Samples
SN74LVCC4245APW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LG245A	Samples
SN74LVCC4245APWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LG245A	Samples
SN74LVCC4245APWRE4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LG245A	Samples
SN74LVCC4245APWRG4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LG245A	Samples
SN74LVCC4245APWT	ACTIVE	TSSOP	PW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LG245A	Samples
SN74LVCC4245APWTE4	ACTIVE	TSSOP	PW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LG245A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVCC4245A :

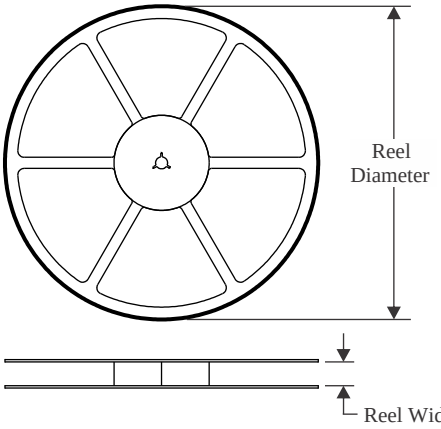
- Enhanced Product : SN74LVCC4245A-EP

NOTE: Qualified Version Definitions:

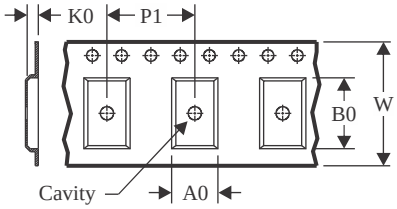
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

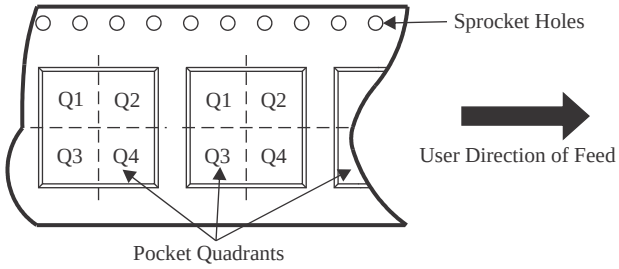


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

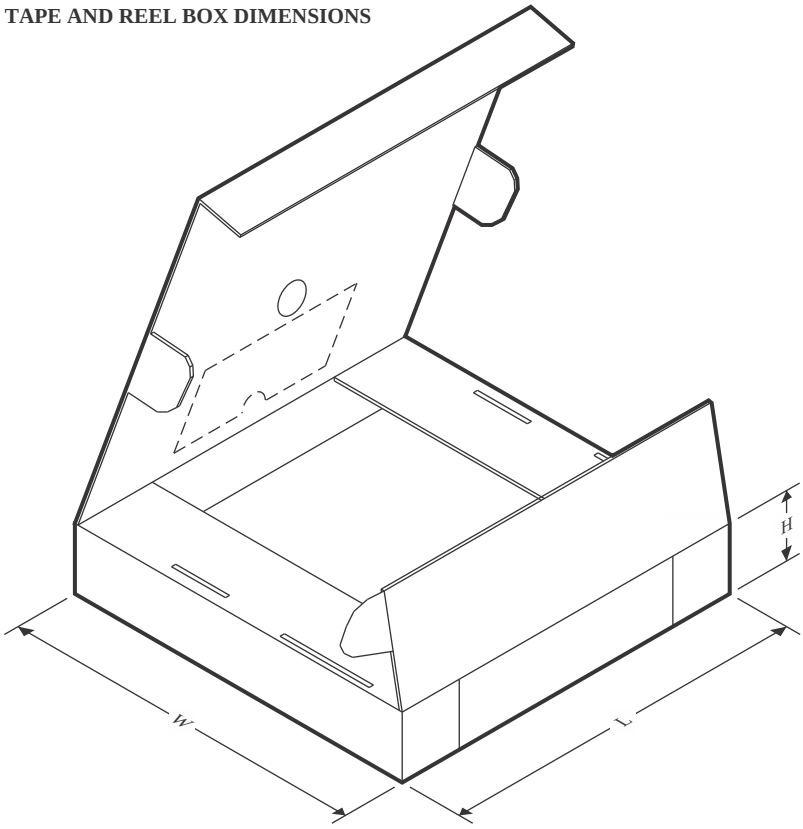
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCC4245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCC4245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC4245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC4245ANSR	SO	NS	24	2000	330.0	24.4	8.3	15.4	2.6	12.0	24.0	Q1
SN74LVCC4245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCC4245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCC4245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

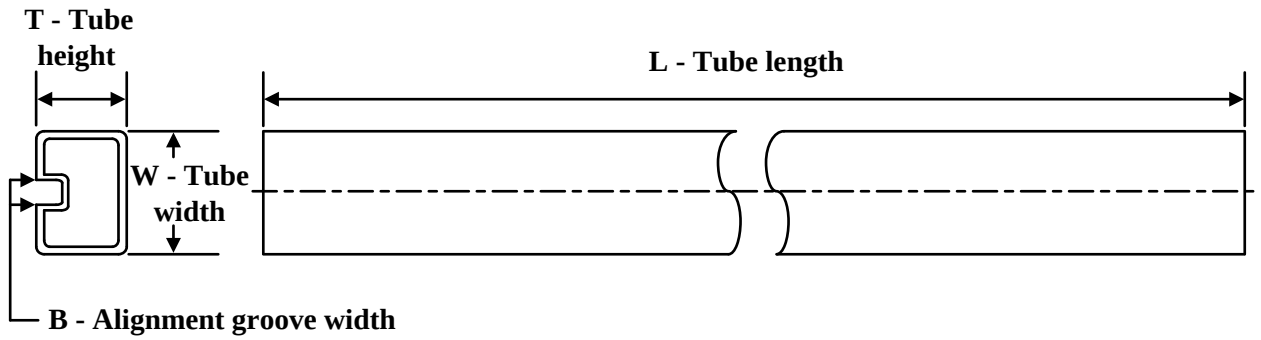
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCC4245ADBR	SSOP	DB	24	2000	356.0	356.0	35.0
SN74LVCC4245ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC4245ADWRG4	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC4245ANSR	SO	NS	24	2000	367.0	367.0	45.0
SN74LVCC4245APWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVCC4245APWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVCC4245APWT	TSSOP	PW	24	250	356.0	356.0	35.0

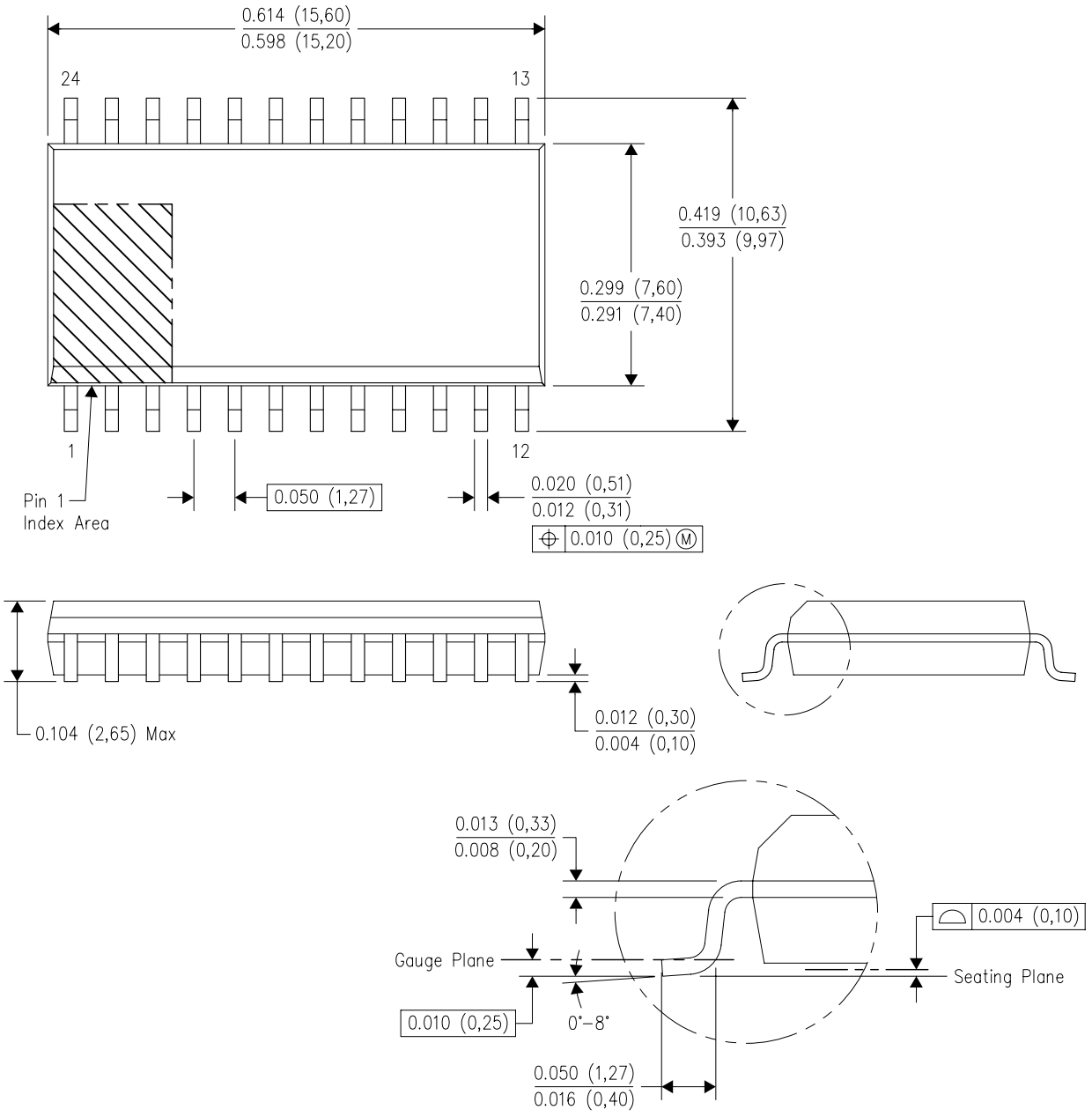
TUBE



*All dimensions are nominal

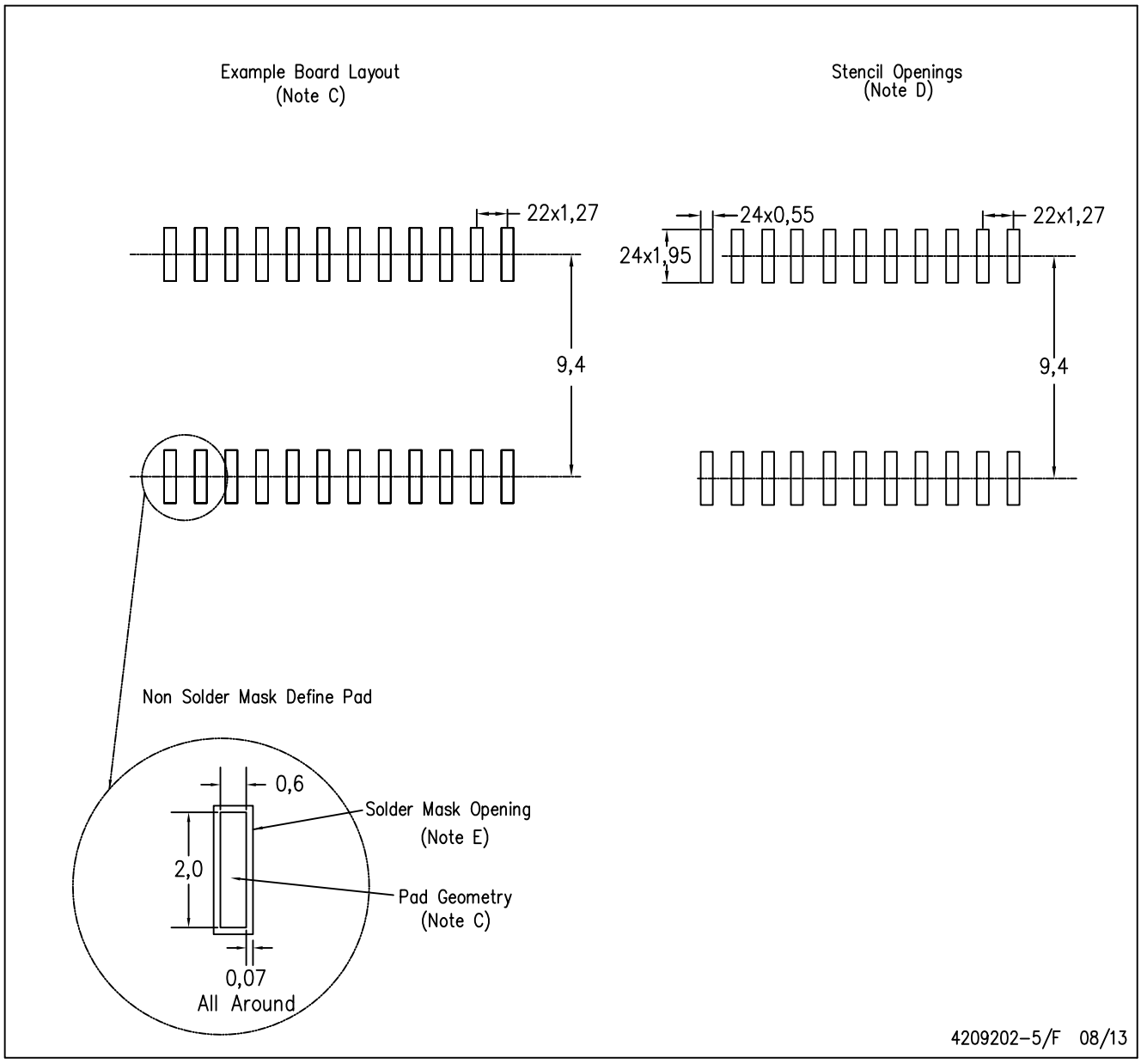
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVCC4245ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVCC4245ADWE4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVCC4245APW	PW	TSSOP	24	60	530	10.2	3600	3.5

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

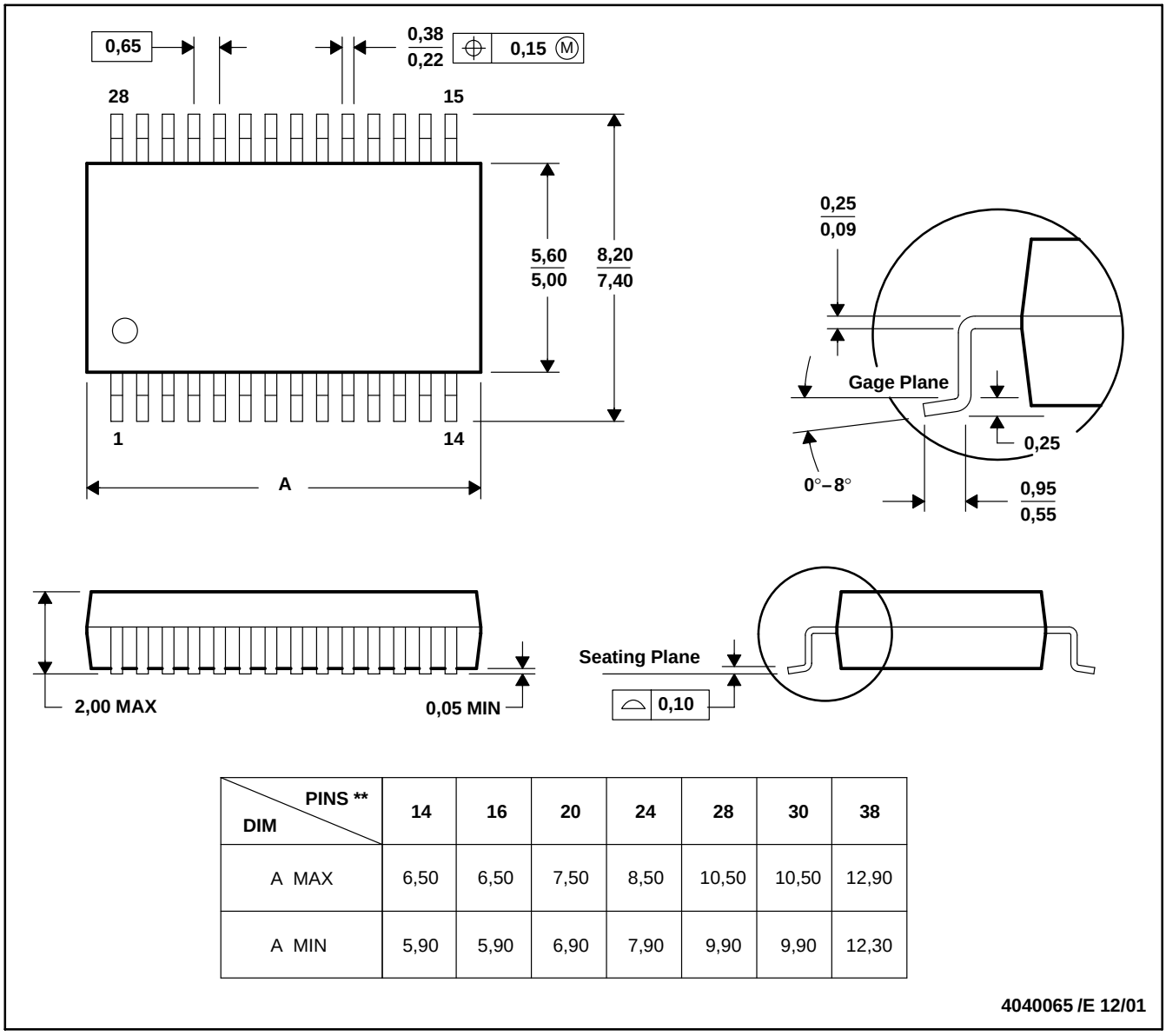


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

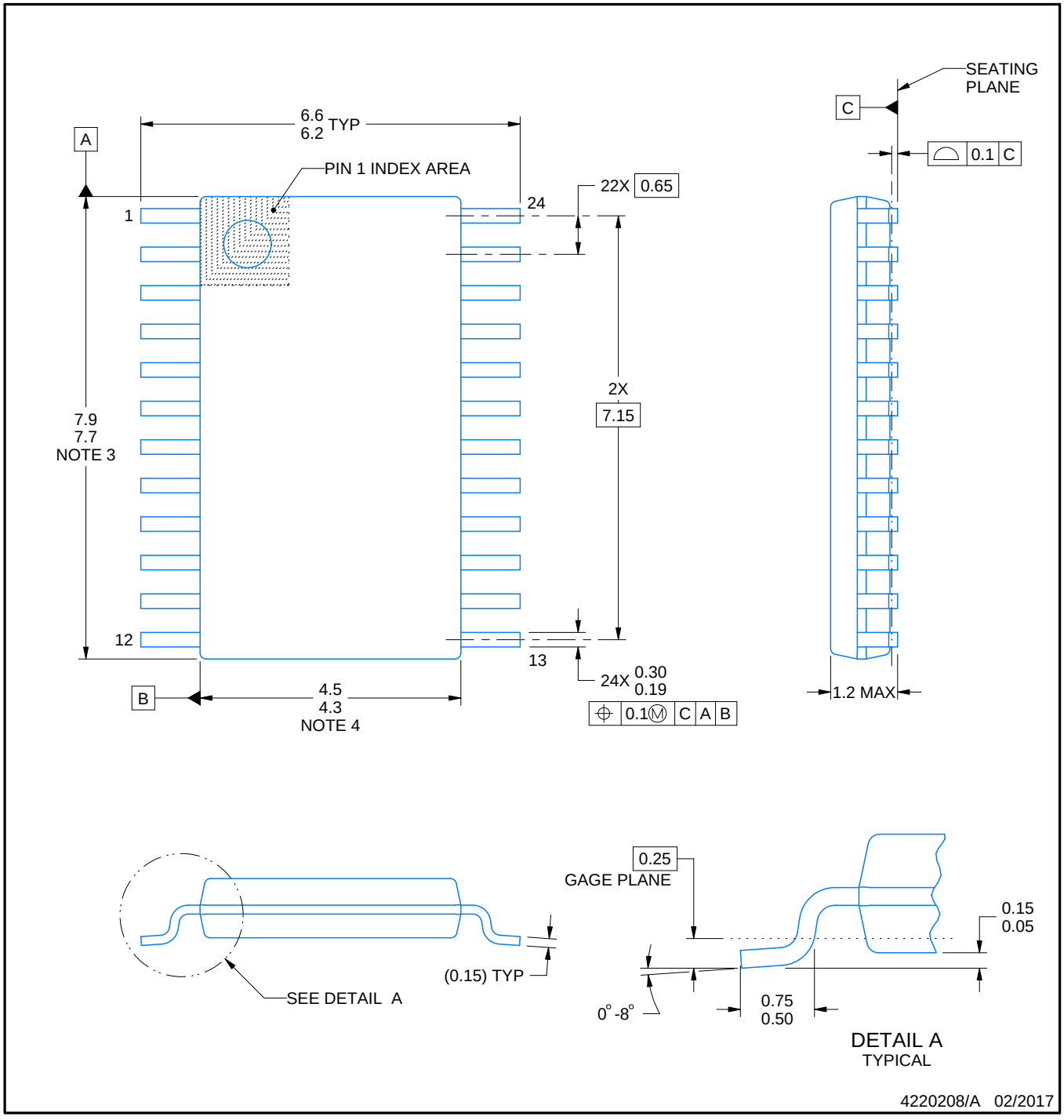
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PACKAGE OUTLINE

PW0024A

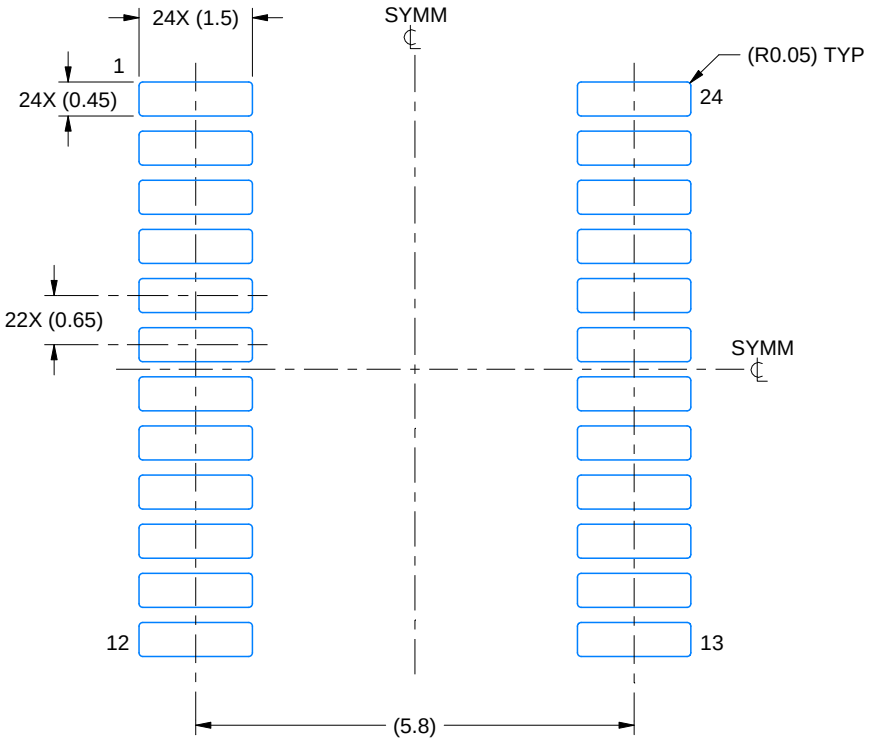
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

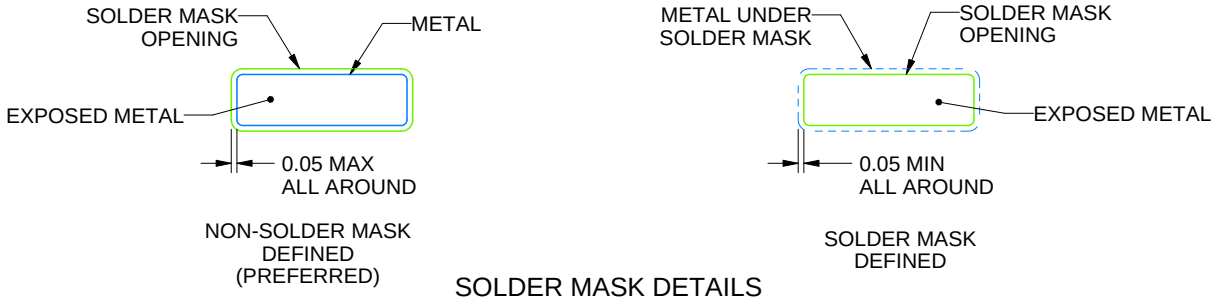


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

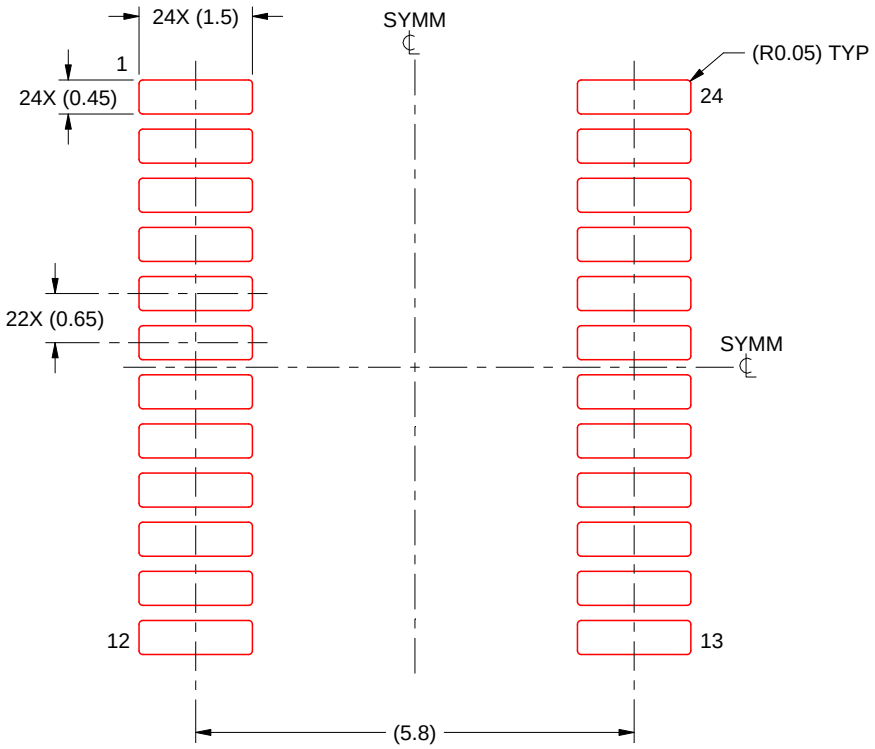


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

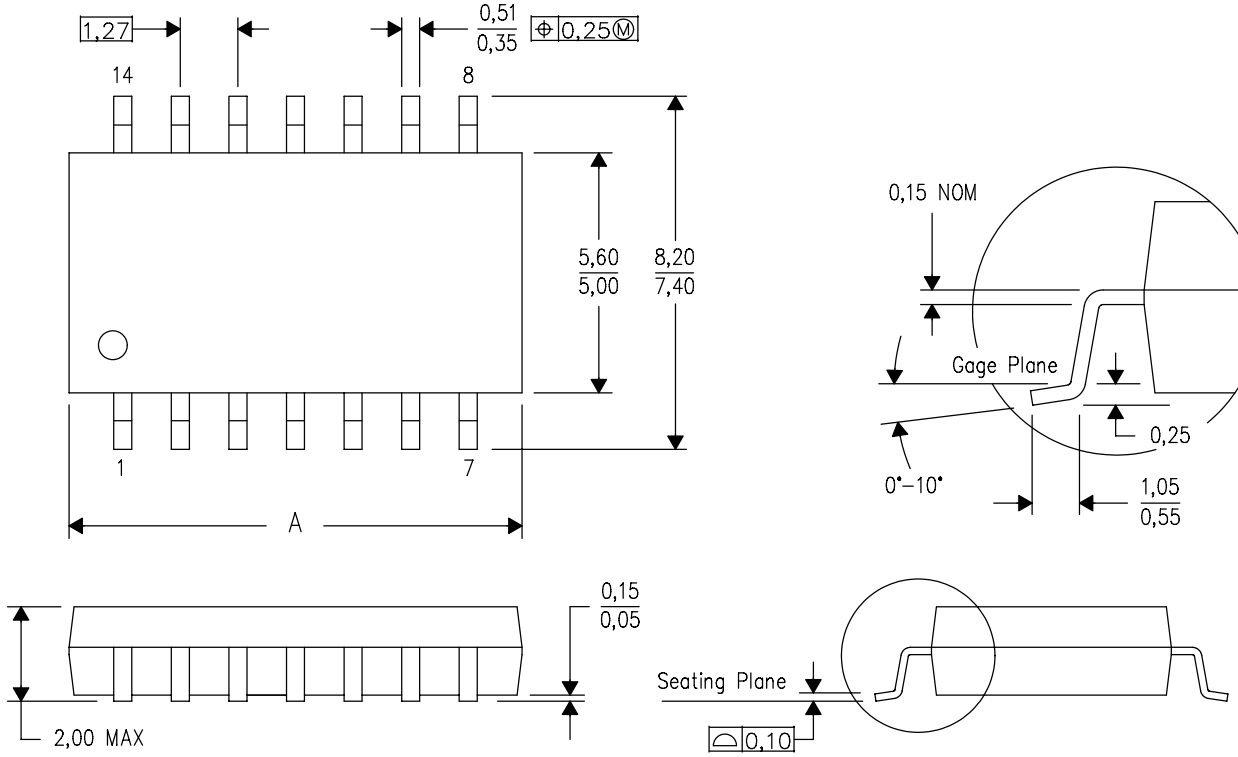
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View SN74LVCC4245ADBRE4 on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management