



**THE DATASHEET OF
SN74ALVCH16600DLR**



FEATURES

- Member of the Texas Instruments Widebus™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enable Mode
- Operates From 1.65-V to 3.6-V V_{CC}
- Max t_{pd} of 4 ns at 3.3-V V_{CC}
- ± 24 -mA Output Drive at 3.3-V V_{CC}
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DESCRIPTION/ORDERING INFORMATION

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

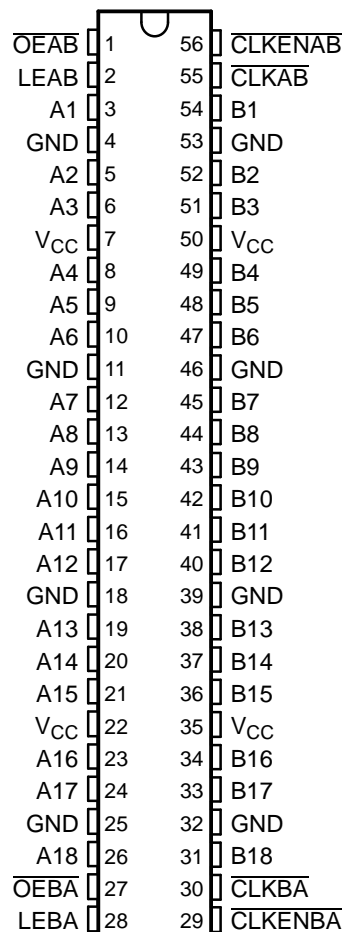
The SN74ALVCH16600 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , LEBA, \overline{CLKBA} , and $\overline{CLKENBA}$.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

DGG OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40 to 85°C	SSOP - DL	Tube	SN74ALVCH16600DL	ALVCH16600
		Tape and reel	SN74ALVCH16600DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH16600DGGR	ALVCH16600

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN74ALVCH16600
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

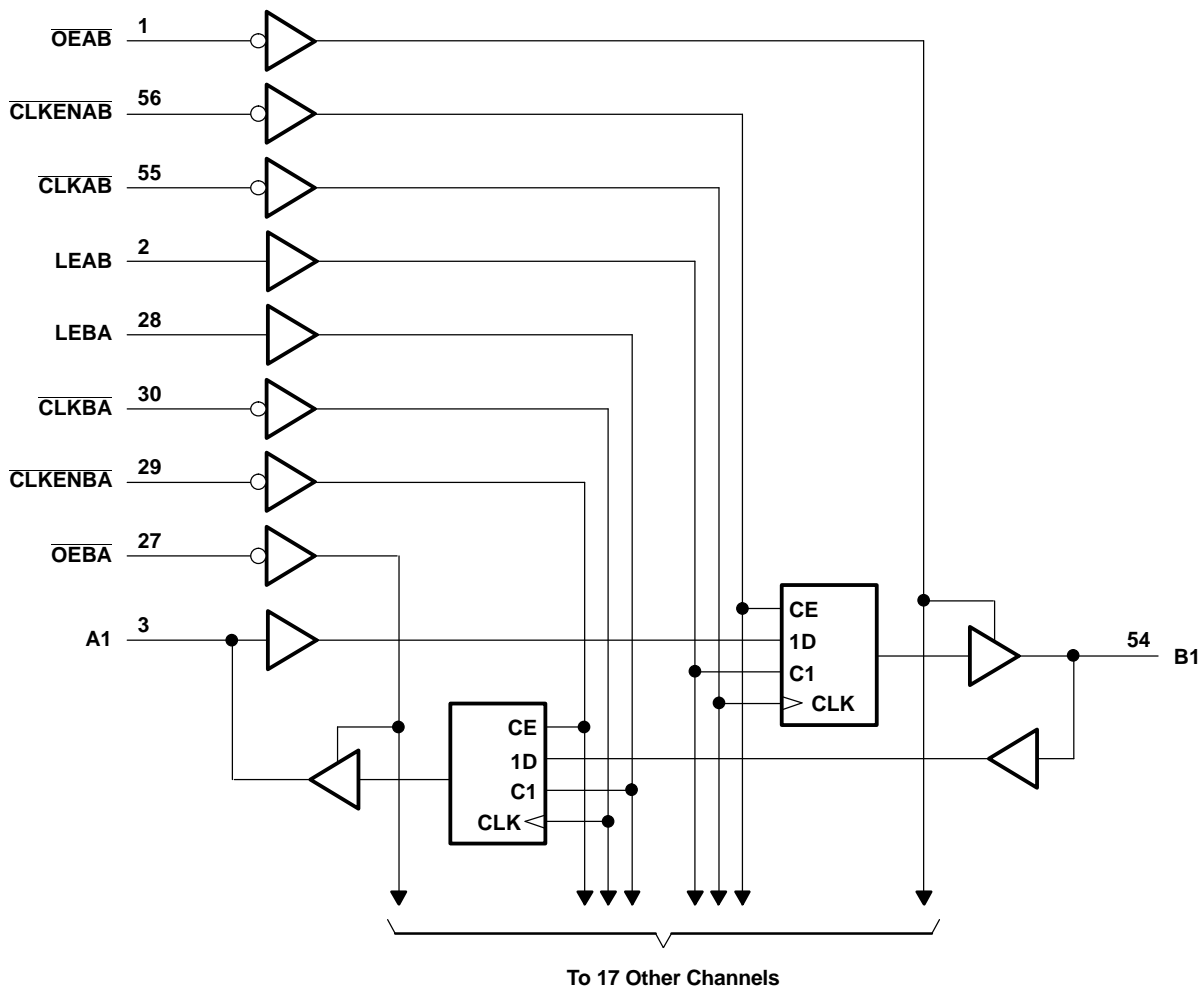
SCES030G—JULY 1995—REVISED JULY 2004

FUNCTION TABLE⁽¹⁾

INPUTS					A	OUTPUT B
CLKENAB	OEAB	LEAB	CLKAB			
X	H	X	X	X	Z	
X	L	H	X	L	L	
X	L	H	X	H	H	
H	L	L	X	X	B ₀ ⁽²⁾	
H	L	L	X	X	B ₀ ⁽²⁾	
L	L	L	↓	L	L	
L	L	L	↓	H	H	
L	L	L	H	X	B ₀ ⁽²⁾	
L	L	L	L	X	B ₀ ⁽³⁾	

- (1) A-to-B data flow is shown; B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.
- (2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
- (3) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range	Except I/O ports ⁽²⁾		V
		-0.5	$V_{CC} + 0.5$	
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50
				mA
I_{OK}	Output clamp current	$V_O < 0$		-50
				mA
I_O	Continuous output current		± 50	mA
	Continuous current through each V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package		64
		DL package		56
				°C/W
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V, maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65\text{ V}$		mA
		$V_{CC} = 2.3\text{ V}$		
		$V_{CC} = 2.7\text{ V}$		
		$V_{CC} = 3\text{ V}$		
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$		mA
		$V_{CC} = 2.3\text{ V}$		
		$V_{CC} = 2.7\text{ V}$		
		$V_{CC} = 3\text{ V}$		
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH16600

18-BIT UNIVERSAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES030G–JULY 1995–REVISED JULY 2004

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V	
	I _{OH} = -4 mA	1.65 V	1.2				
	I _{OH} = -6 mA	2.3 V	2				
	I _{OH} = -12 mA	2.3 V	1.7				
		2.7 V	2.2				
		3 V	2.4				
I _{OH} = -24 mA	3 V	2					
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.2			V	
	I _{OL} = 4 mA	1.65 V	0.45				
	I _{OL} = 6 mA	2.3 V	0.4				
	I _{OL} = 12 mA	2.3 V	0.7				
		2.7 V	0.4				
	I _{OL} = 24 mA	3 V	0.55				
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA	
I _{I(hold)}	V _I = 0.58 V	1.65 V	25			μA	
	V _I = 1.07 V	1.65 V	-25				
	V _I = 0.7 V	2.3 V	45				
	V _I = 1.7 V	2.3 V	-45				
	V _I = 0.8 V	3 V	75				
	V _I = 2 V	3 V	-75				
	V _I = 0 to 3.6 V ⁽²⁾	3.6 V	±500				
I _{OZ} ⁽³⁾	V _O = V _{CC} or GND	3.6 V	±10			μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	40			μA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			μA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			4	pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V			8	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency	(1)		150		150		150		MHz	
t_w	Pulse duration	LE high		(1)		3.3		3.3		ns	
		$\overline{\text{CLK}}$ high or low		(1)		3.3		3.3			
t_{su}	Setup time	Data before $\overline{\text{CLK}}\uparrow$		(1)		1.3		1.3		ns	
		Data before LE \downarrow	$\overline{\text{CLK}}$ high		(1)		1.2		1.1		
			$\overline{\text{CLK}}$ low		(1)		1.8		1.5		
		$\overline{\text{CLKEN}}$ before $\overline{\text{CLK}}\uparrow$		(1)		0.7		0.7			0.8
t_h	Hold time	Data after $\overline{\text{CLK}}\uparrow$		(1)		1.5		1.8		ns	
		Data after LE \downarrow	$\overline{\text{CLK}}$ high		(1)		1.6		1.9		
			$\overline{\text{CLK}}$ low		(1)		1.2		1.6		
		$\overline{\text{CLKEN}}$ after $\overline{\text{CLK}}\uparrow$		(1)		1.4		1.7			1.4

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		150		150		150		MHz
t_{pd}	A or B	B or A	(1)		1	5.1	4.7		1	4	ns
	LEAB or LEBA	A or B	(1)		1	5.9	5.5		1	4.8	
	$\overline{\text{CLKAB}}$ or $\overline{\text{CLKBA}}$		(1)		1	7.3	6.8		1.3	5.7	
t_{en}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	A or B	(1)		1	6.5	6.3		1.1	5.2	ns
t_{dis}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	A or B	(1)		1	5.1	4.7		1.2	4.4	ns

(1) This information was not available at the time of publication.

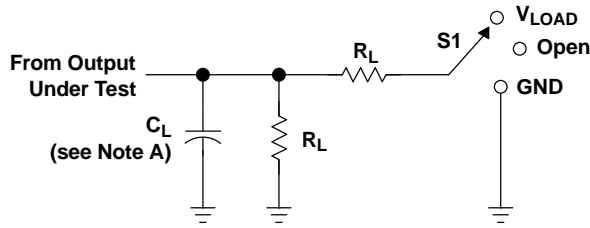
OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	(1)	43	56	pF
		Outputs disabled	(1)	6	6	

(1) This information was not available at the time of publication.

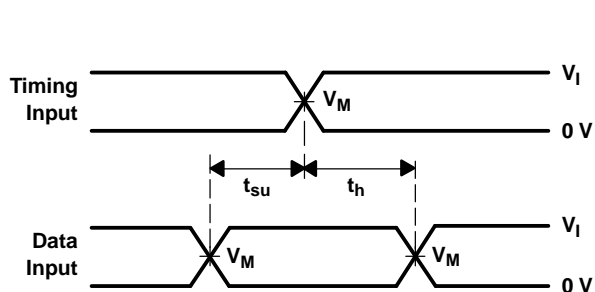
PARAMETER MEASUREMENT INFORMATION



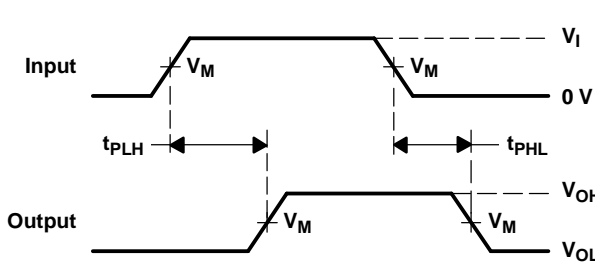
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

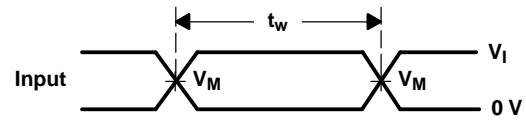
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



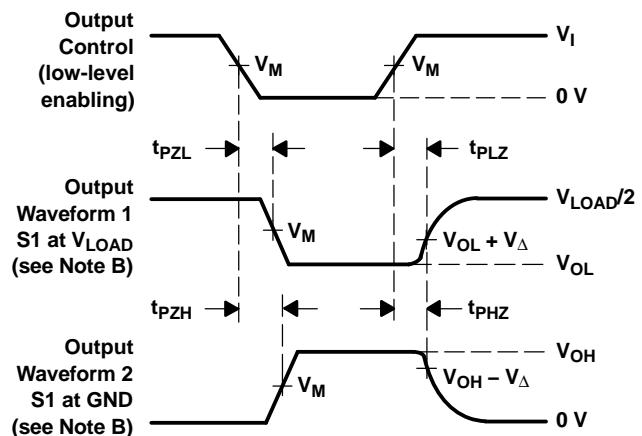
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

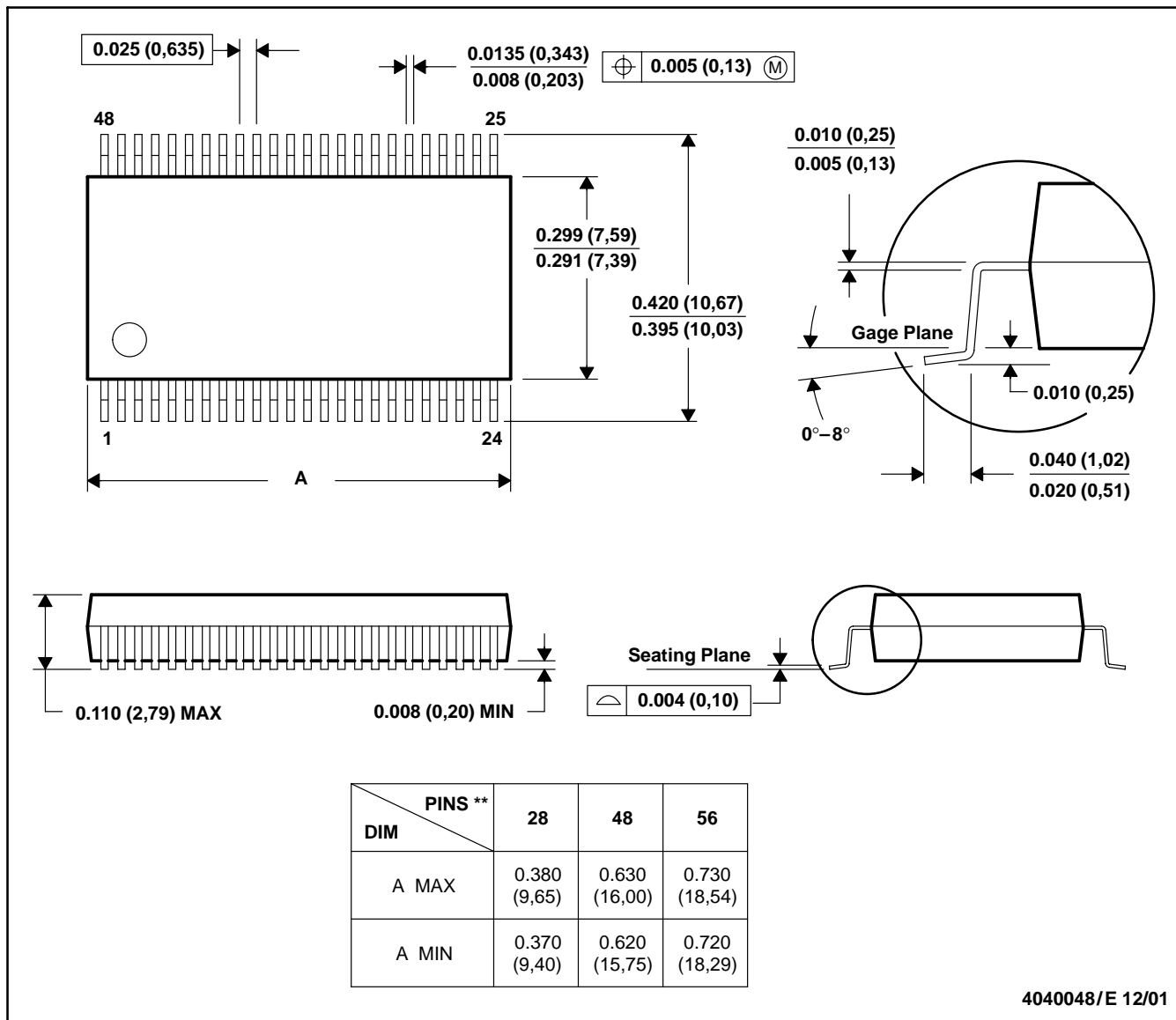
- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

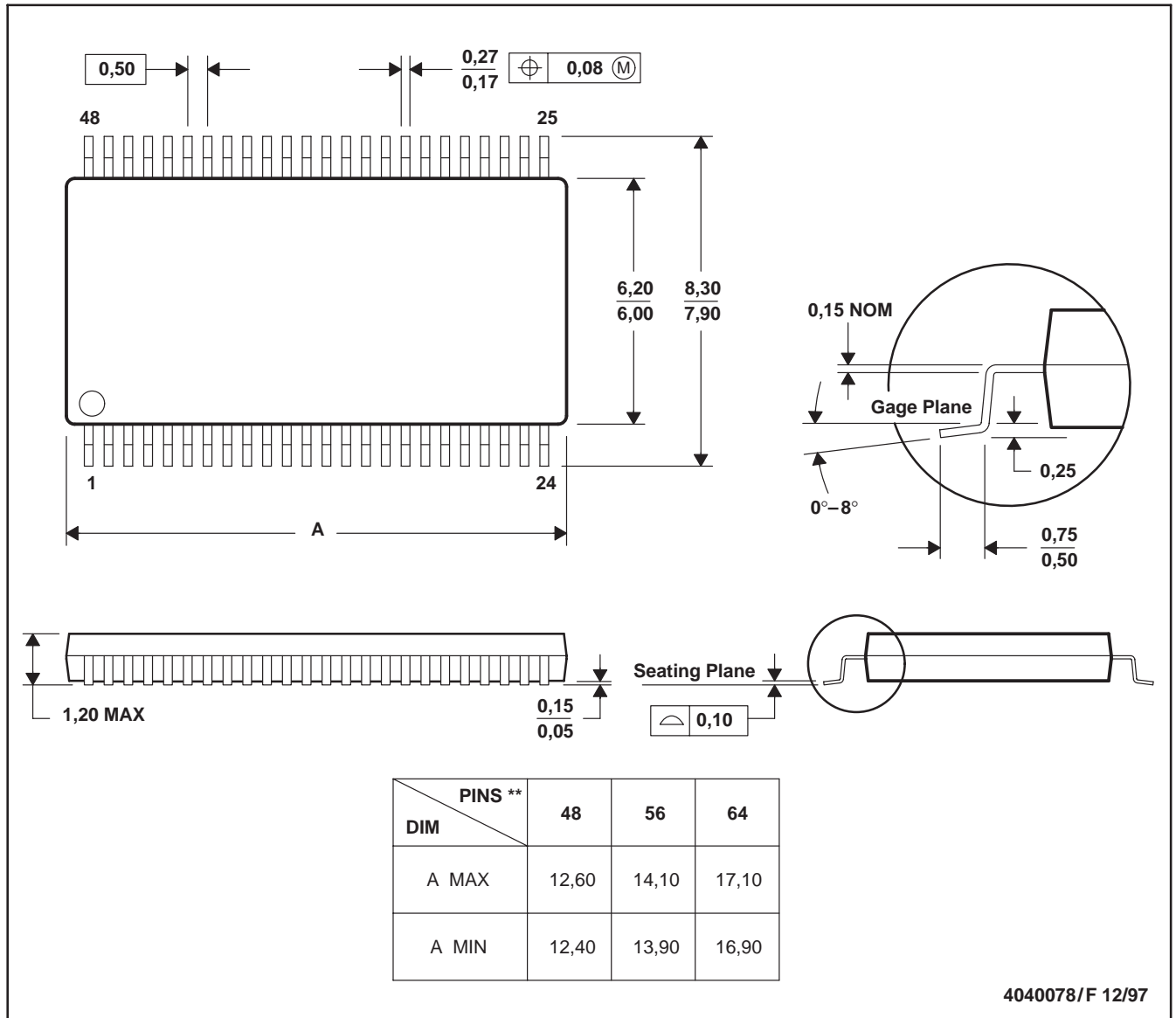


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
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 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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