



**THE DATASHEET OF  
SN74ALVCH16500DL**



## FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-UP Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

## DESCRIPTION

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock ( $\overline{CLKAB}$  and  $\overline{CLKBA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if  $\overline{CLKAB}$  is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of  $\overline{CLKAB}$ . Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses  $\overline{OEBA}$ , LEBA, and  $\overline{CLKBA}$ . The output enables are complementary (OEAB is active high, and  $\overline{OEBA}$  is active low).

To ensure the high-impedance state during power up or power down,  $\overline{OEBA}$  should be tied to  $V_{CC}$  through a pullup resistor, and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16500 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE  
(TOP VIEW)

|                   |    |    |                    |
|-------------------|----|----|--------------------|
| OEAB              | 1  | 56 | GND                |
| LEAB              | 2  | 55 | $\overline{CLKAB}$ |
| A1                | 3  | 54 | B1                 |
| GND               | 4  | 53 | GND                |
| A2                | 5  | 52 | B2                 |
| A3                | 6  | 51 | B3                 |
| $V_{CC}$          | 7  | 50 | $V_{CC}$           |
| A4                | 8  | 49 | B4                 |
| A5                | 9  | 48 | B5                 |
| A6                | 10 | 47 | B6                 |
| GND               | 11 | 46 | GND                |
| A7                | 12 | 45 | B7                 |
| A8                | 13 | 44 | B8                 |
| A9                | 14 | 43 | B9                 |
| A10               | 15 | 42 | B10                |
| A11               | 16 | 41 | B11                |
| A12               | 17 | 40 | B12                |
| GND               | 18 | 39 | GND                |
| A13               | 19 | 38 | B13                |
| A14               | 20 | 37 | B14                |
| A15               | 21 | 36 | B15                |
| $V_{CC}$          | 22 | 35 | $V_{CC}$           |
| A16               | 23 | 34 | B16                |
| A17               | 24 | 33 | B17                |
| GND               | 25 | 32 | GND                |
| A18               | 26 | 31 | B18                |
| $\overline{OEBA}$ | 27 | 30 | $\overline{CLKBA}$ |
| LEBA              | 28 | 29 | GND                |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**SN74ALVCH16500**  
**18-BIT UNIVERSAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

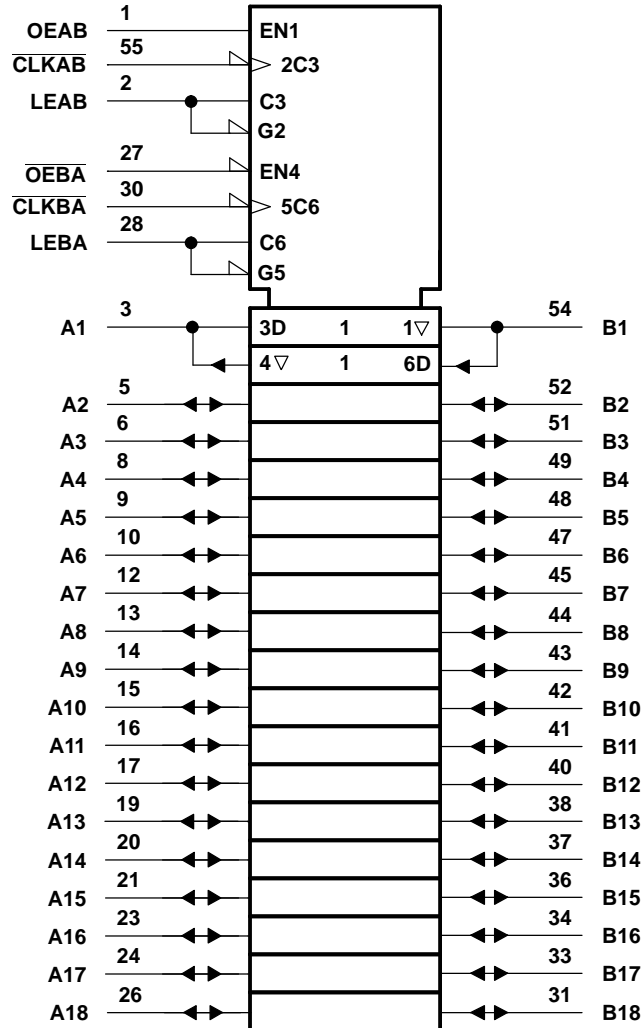
SCES023I—JULY 1995—REVISED OCTOBER 2004

**FUNCTION TABLE<sup>(1)</sup>**

| INPUTS |      |       |   | OUTPUT<br>B                   |
|--------|------|-------|---|-------------------------------|
| OEAB   | LEAB | CLKAB | A |                               |
| L      | X    | X     | X | Z                             |
| H      | H    | X     | L | L                             |
| H      | H    | X     | H | H                             |
| H      | L    | ↓     | L | L                             |
| H      | L    | ↓     | H | H                             |
| H      | L    | H     | X | B <sub>0</sub> <sup>(2)</sup> |
| H      | L    | L     | X | B <sub>0</sub> <sup>(3)</sup> |

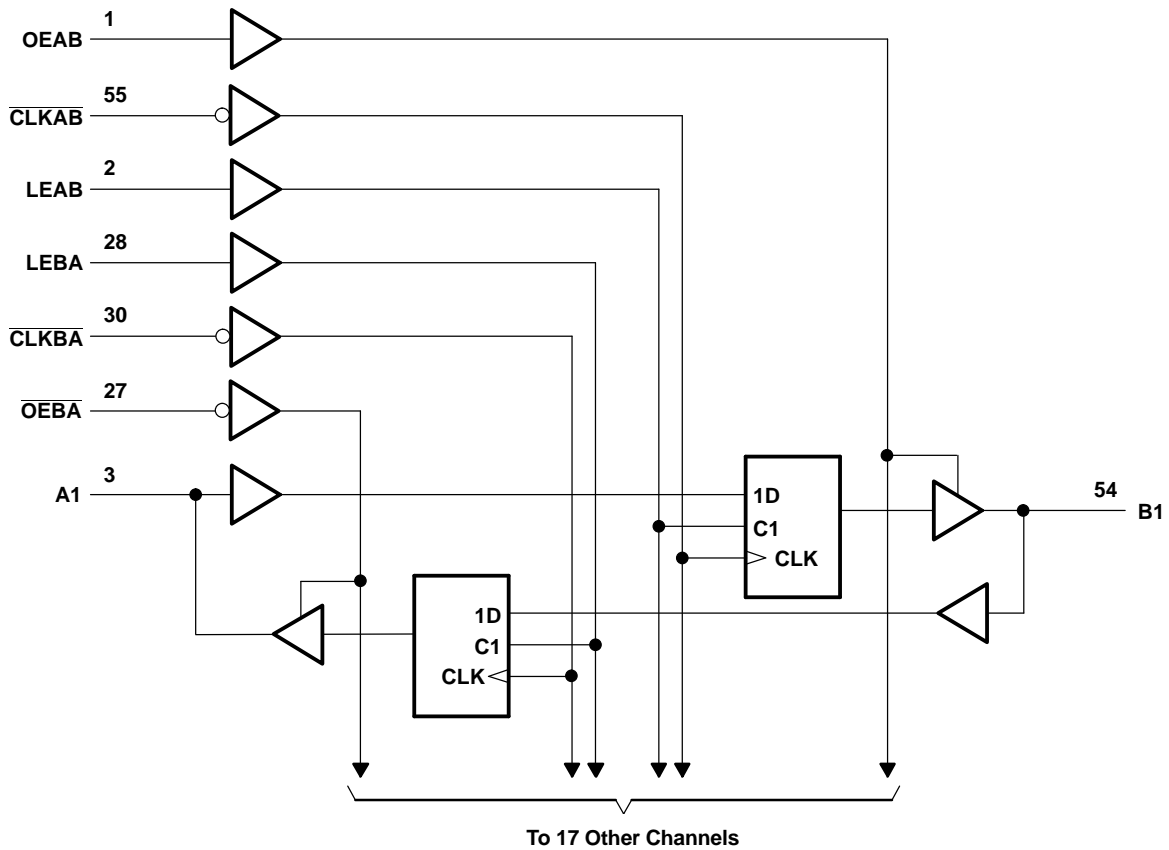
- (1) A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{OEBA}$ , LEBA, and CLKBA.
- (2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
- (3) Output level before the indicated steady-state input conditions were established

**LOGIC SYMBOL<sup>(1)</sup>**



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



# SN74ALVCH16500

## 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES023I–JULY 1995–REVISED OCTOBER 2004

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |  | MIN  | MAX                   | UNIT |
|------------------|--|--|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage range                     | -0.5   | 4.6                   | V    |
| V <sub>I</sub>   | Input voltage range                      | Except I/O ports <sup>(2)</sup>                        |                       | V    |
|                  |  | -0.5   | 4.6                   |      |
| V <sub>O</sub>   | Output voltage range <sup>(2)(3)</sup>   | I/O ports <sup>(2)(3)</sup>                            |                       | V    |
|                  |  | -0.5   | V <sub>CC</sub> + 0.5 |      |
| I <sub>IK</sub>  | Input clamp current                      | V <sub>I</sub> < 0                                     |                       | mA   |
| I <sub>OK</sub>  | Output clamp current                     | V <sub>O</sub> < 0                                     |                       | mA   |
| I <sub>O</sub>   | Continuous output current                |  |                       | mA   |
|                  |  | Continuous current through each V <sub>CC</sub> or GND |                       | ±100 |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(4)</sup> | DGG package  |                       | °C/W |
|                  |  | DL package   |                       | 56   |
| T <sub>stg</sub> | Storage temperature range                | -65  | 150                   | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

|                 |                                    | MIN                                | MAX                    | UNIT |
|-----------------|------------------------------------|------------------------------------|------------------------|------|
| V <sub>CC</sub> | Supply voltage                     | 1.65                               | 3.6                    | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2                      |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.35 × V <sub>CC</sub> | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 0.7                    |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 0.8                    |      |
| V <sub>I</sub>  | Input voltage                      | 0                                  | V <sub>CC</sub>        | V    |
| V <sub>O</sub>  | Output voltage                     | 0                                  | V <sub>CC</sub>        | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V           | -4                     | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | -12                    |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | -12                    |      |
|                 |                                    | V <sub>CC</sub> = 3 V              | -24                    |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V           | 4                      | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | 12                     |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | 12                     |      |
|                 |                                    | V <sub>CC</sub> = 3 V              | 24                     |      |
| Δt/Δv           | Input transition rise or fall rate |                                    | 10                     | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     | -40                                | 85                     | °C   |

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                      |                | TEST CONDITIONS  | V <sub>CC</sub>                            | MIN                   | TYP <sup>(1)</sup> | MAX  | UNIT |
|--------------------------------|----------------|--|--|-----------------------|--------------------|------|------|
| V <sub>OH</sub>                |                | I <sub>OH</sub> = -100 μA  | 1.65 V to 3.6 V                            | V <sub>CC</sub> - 0.2 |                    |      | V    |
|                                |                | I <sub>OH</sub> = -4 mA  | 1.65 V                                     | 1.2                   |                    |      |      |
|                                |                | I <sub>OH</sub> = -6 mA  | 2.3 V                                      | 2                     |                    |      |      |
|                                |                | I <sub>OH</sub> = -12 mA   | 2.3 V                                      | 1.7                   |                    |      |      |
|                                |                |  | 2.7 V                                      | 2.2                   |                    |      |      |
|                                |                |  | 3 V  | 2.4                   |                    |      |      |
| V <sub>OL</sub>                |                | I <sub>OL</sub> = 100 μA   | 1.65 V to 3.6 V                            |                       |                    | 0.2  | V    |
|                                |                | I <sub>OL</sub> = 4 mA   | 1.65 V                                     |                       |                    | 0.45 |      |
|                                |                | I <sub>OL</sub> = 6 mA   | 2.3 V                                      |                       |                    | 0.4  |      |
|                                |                | I <sub>OL</sub> = 12 mA  | 2.3 V                                      |                       |                    | 0.7  |      |
|                                |                |  | 2.7 V                                      |                       |                    | 0.4  |      |
|                                |                |  | I <sub>OL</sub> = 24 mA                    | 3 V                   |                    |      |      |
| I <sub>I</sub>                 |                | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V                                      |                       |                    | ±5   | μA   |
| I <sub>I(hold)</sub>           |                | V <sub>I</sub> = 0.58 V  | 1.65 V                                     | 25                    |                    |      | μA   |
|                                |                | V <sub>I</sub> = 1.07 V  | 1.65 V                                     | -25                   |                    |      |      |
|                                |                | V <sub>I</sub> = 0.7 V   | 2.3 V                                      | 45                    |                    |      |      |
|                                |                | V <sub>I</sub> = 1.7 V   | 2.3 V                                      | -45                   |                    |      |      |
|                                |                | V <sub>I</sub> = 0.8 V   | 3 V  | 75                    |                    |      |      |
|                                |                | V <sub>I</sub> = 2 V   | 3 V  | -75                   |                    |      |      |
|                                |                |  | V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup> | 3.6 V                 |                    |      |      |
| I <sub>OZ</sub> <sup>(3)</sup> |                | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.6 V                                      |                       |                    | ±10  | μA   |
| I <sub>CC</sub>                |                | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V                                      |                       |                    | 40   | μA   |
| ΔI <sub>CC</sub>               |                | One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 3.6 V                               |                       |                    | 750  | μA   |
| C <sub>i</sub>                 | Control inputs | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V                                      |                       | 4                  |      | pF   |
| C <sub>io</sub>                | A or B ports   | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.3 V                                      |                       | 8                  |      | pF   |

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

 (3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

# SN74ALVCH16500

## 18-BIT UNIVERSAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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### TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

|                    |                 | $V_{CC} = 1.8\text{ V}$                       |                              | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | UNIT |  |
|--------------------|-----------------|---|------------------------------|--|-----|-------------------------|-----|--|-----|------|--|
|                    |                 | MIN   | MAX                          | MIN                                      | MAX | MIN                     | MAX | MIN                                      | MAX |      |  |
| $f_{\text{clock}}$ | Clock frequency | (1)   |                              | 150                                      |     | 150                     |     | 150                                      |     | MHz  |  |
| $t_w$              | Pulse duration  | LE high                                       |                              | (1)                                      | 3.3 | 3.3                     | 3.3 |  |     | ns   |  |
|                    |                 | $\overline{\text{CLK}}$ high or low           |                              | (1)                                      | 3.3 | 3.3                     | 3.3 |  |     |      |  |
| $t_{\text{su}}$    | Setup time      | Data before $\overline{\text{CLK}}\downarrow$ |                              | (1)                                      | 1.7 | 1.4                     | 1.3 |  |     | ns   |  |
|                    |                 | Data before LE $\downarrow$                   | $\overline{\text{CLK}}$ high |  | (1) | 1.1                     | 1   | 1  |     |      |  |
|                    |                 |   | $\overline{\text{CLK}}$ low  |  | (1) | 1.9                     | 1.6 | 1.4                                      |     |      |  |
| $t_h$              | Hold time       | Data after $\overline{\text{CLK}}\downarrow$  |                              | (1)                                      | 1.7 | 1.6                     | 1.3 |  |     | ns   |  |
|                    |                 | Data after LE $\downarrow$                    | $\overline{\text{CLK}}$ high |  | (1) | 2                       | 1.8 | 1.5                                      |     |      |  |
|                    |                 |   | $\overline{\text{CLK}}$ low  |  | (1) | 1.6                     | 1.5 | 1.2                                      |     |      |  |

(1) This information was not available at the time of publication.

### SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| PARAMETER        | FROM (INPUT)   | TO (OUTPUT) | $V_{CC} = 1.8\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | UNIT |
|------------------|--|-------------|-------------------------|-----|--|-----|-------------------------|-----|--|-----|------|
|                  |  |             | MIN                     | TYP | MIN                                      | MAX | MIN                     | MAX | MIN                                      | MAX |      |
| $f_{\text{max}}$ |  |             | (1)                     |     | 150                                      |     | 150                     |     | 150                                      |     | MHz  |
| $t_{\text{pd}}$  | A or B   | B or A      | (1)                     |     | 1  | 5.1 | 4.7                     |     | 1  | 3.9 | ns   |
|                  | LEAB or LEBA   | A or B      | (1)                     |     | 1  | 5.9 | 5.5                     |     | 1  | 4.7 |      |
|                  | $\overline{\text{CLK}}\text{AB}$ or $\overline{\text{CLK}}\text{BA}$ |             | (1)                     |     | 1  | 6.6 | 6.6                     |     | 1.1                                      | 5.5 |      |
| $t_{\text{en}}$  | OEAB   | B           | (1)                     |     | 1  | 5.7 | 5.4                     |     | 1  | 4.6 | ns   |
| $t_{\text{dis}}$ | OEAB   | B           | (1)                     |     | 1  | 6.1 | 5.7                     |     | 1.5                                      | 5   | ns   |
| $t_{\text{en}}$  | $\overline{\text{OE}}\text{BA}$                                      | A           | (1)                     |     | 1  | 6.2 | 6.2                     |     | 1  | 5.2 | ns   |
| $t_{\text{dis}}$ | $\overline{\text{OE}}\text{BA}$                                      | A           | (1)                     |     | 1  | 5.4 | 4.6                     |     | 1  | 4.3 | ns   |

(1) This information was not available at the time of publication.

### OPERATING CHARACTERISTICS

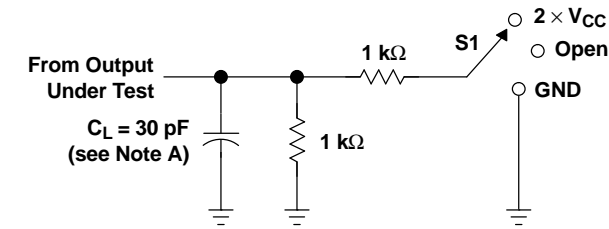
$T_A = 25^\circ\text{C}$

| PARAMETER       |                               | TEST CONDITIONS  | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|-----------------|-------------------------------|------------------|-------------------------|-------------------------|-------------------------|------|
|                 |                               |                  | TYP                     | TYP                     | TYP                     |      |
| $C_{\text{pd}}$ | Power dissipation capacitance | Outputs enabled  | (1)                     | 40                      | 51                      | pF   |
|                 |                               | Outputs disabled | (1)                     | 6                       | 6                       |      |

(1) This information was not available at the time of publication.

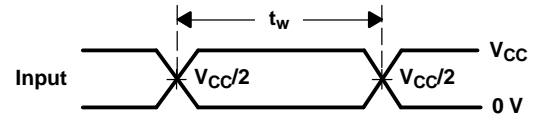
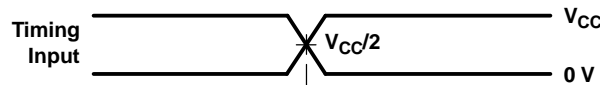
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V}$

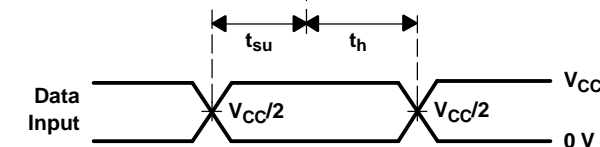


LOAD CIRCUIT

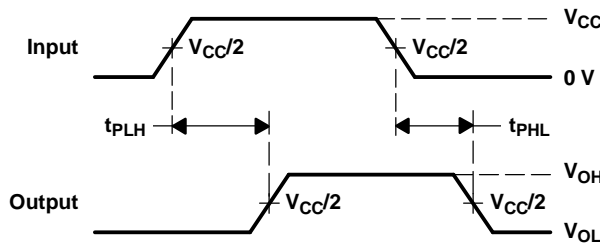
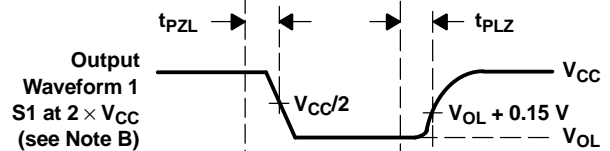
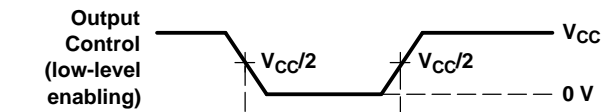
| TEST              | S1                |
|-------------------|-------------------|
| $t_{pd}$          | Open              |
| $t_{PLZ}/t_{PZL}$ | 2 $\times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |



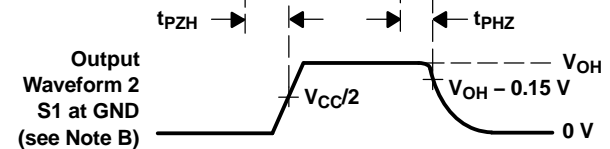
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



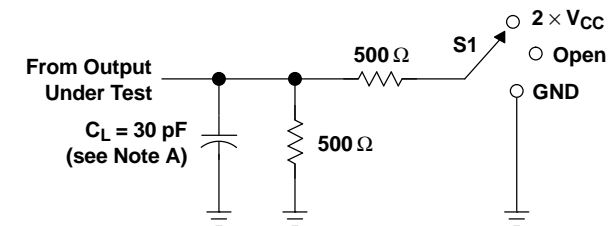
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

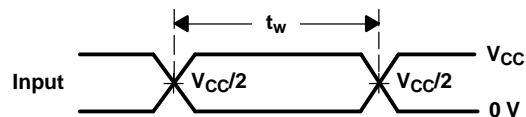
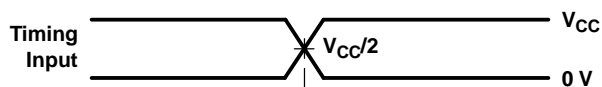
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

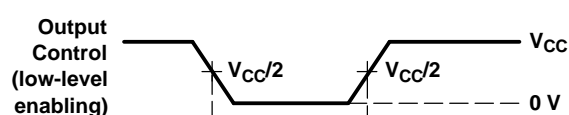
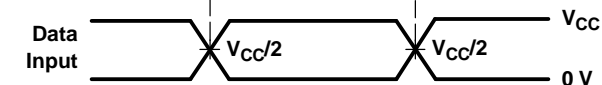


**LOAD CIRCUIT**

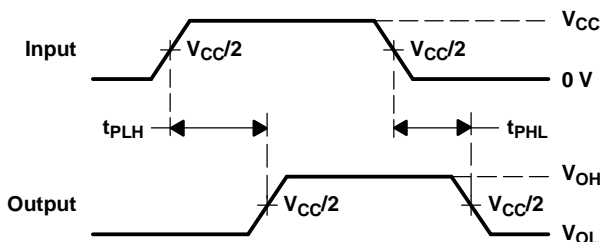
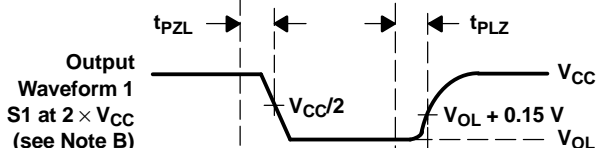
| TEST              | S1                |
|-------------------|-------------------|
| $t_{pd}$          | Open              |
| $t_{PLZ}/t_{PZL}$ | 2 $\times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |



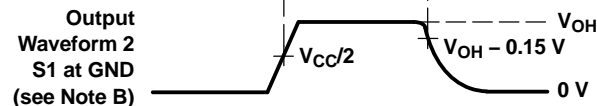
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**

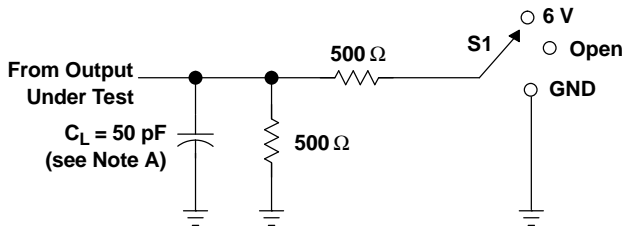


**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

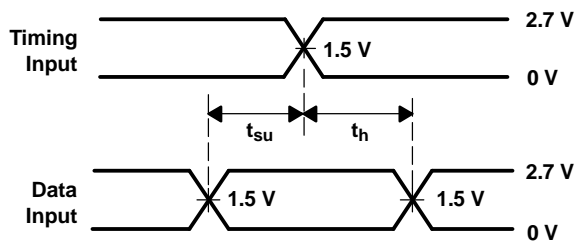
**Figure 2. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

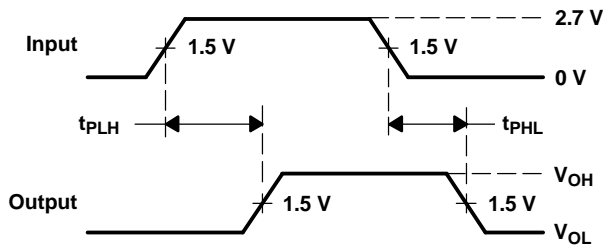


LOAD CIRCUIT

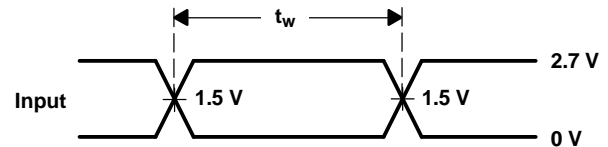
| TEST              | S1   |
|-------------------|------|
| $t_{pd}$          | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |



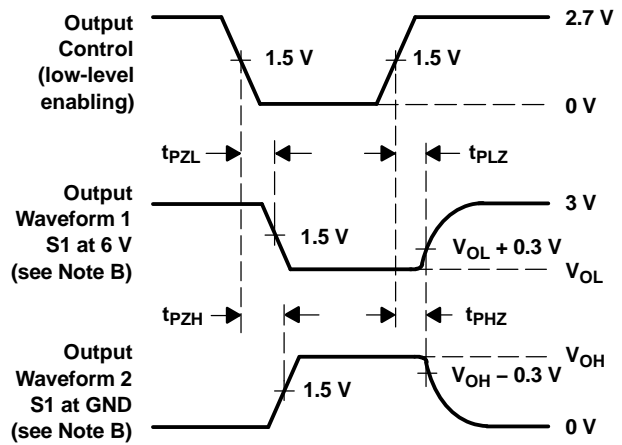
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN74ALVCH16500DLR | ACTIVE        | SSOP         | DL              | 56   | 1000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ALVCH16500              | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVCH16500DLR | SSOP         | DL              | 56   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVCH16500DLR | SSOP         | DL              | 56   | 1000 | 367.0       | 367.0      | 55.0        |

# MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed  $0.006$  (0,15).
  - Falls within JEDEC MO-118

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