



**THE DATASHEET OF  
SN74LVT16500DL**



# SN54LVT16500, SN74LVT16500

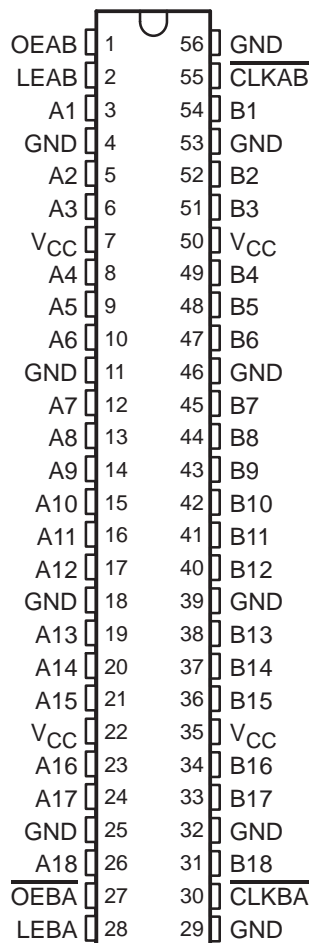
## 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS146D – MAY 1992 – REVISED NOVEMBER 1996

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Live Insertion
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16500 . . . WD PACKAGE  
SN74LVT16500 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'LVT16500 are 18-bit universal bus transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock ( $\overline{CLKAB}$  and  $\overline{CLKBA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if  $\overline{CLKAB}$  is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of  $\overline{CLKAB}$ . Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.



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**TEXAS  
INSTRUMENTS**

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#### description (continued)

Data flow for B to A is similar to that of A to B but uses  $\overline{OEBA}$ , LEBA, and  $\overline{CLKBA}$ . The output enables are complementary (OEAB is active high and  $\overline{OEBA}$  is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN54LVT16500 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVT16500 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	$B_0^{\ddagger}$
H	L	L	X	$B_0^{\S}$

† A-to-B data flow is shown: B-to-A flow is similar but uses  $\overline{OEBA}$ , LEBA, and  $\overline{CLKBA}$ .

‡ Output level before the indicated steady-state input conditions were established

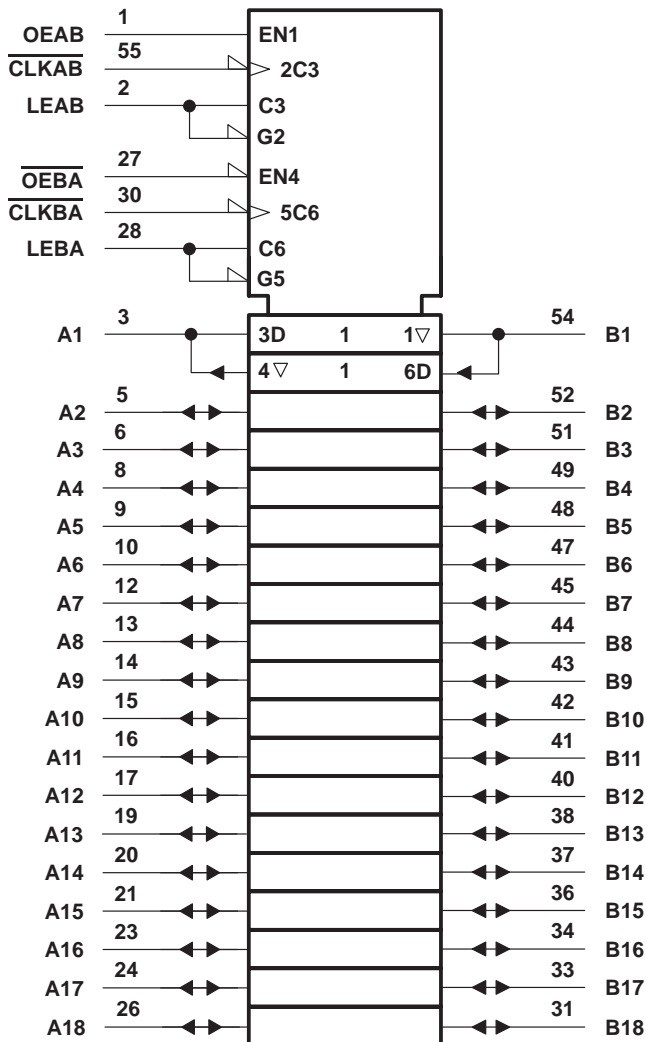
§ Output level before the indicated steady-state input conditions were established, provided that  $\overline{CLKAB}$  was low before LEAB went low



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logic symbol†

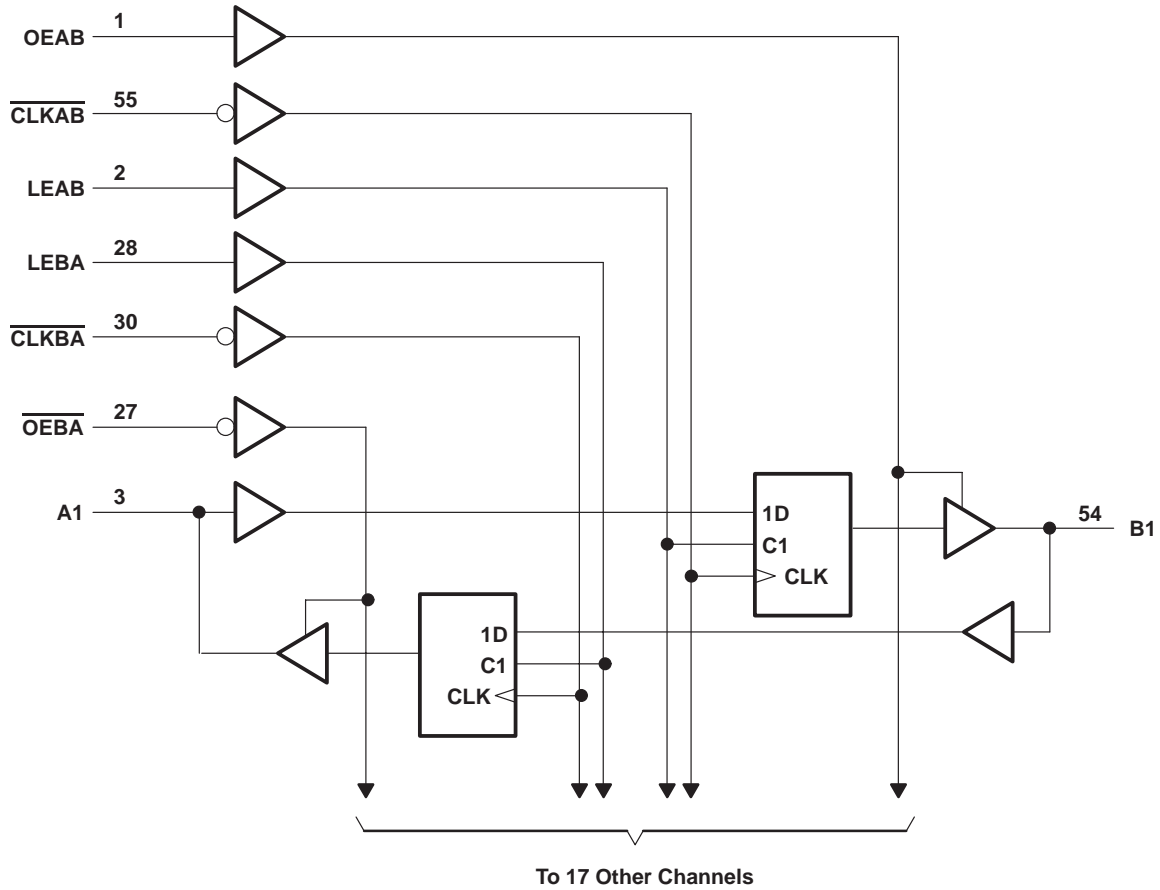


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Current into any output in the low state, $I_{OL}$ : SN54LVT16500 .....	96 mA
SN74LVT16500 .....	128 mA
Current into any output in the high state, $I_{OH}$ (see Note 2): SN54LVT16500 .....	48 mA
SN74LVT16500 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package .....	1 W
DL package .....	1.4 W
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.



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**recommended operating conditions (see Note 4)**

		SN54LVT16500		SN74LVT16500		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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## 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16500			SN74LVT16500			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2			-1.2			V	
$V_{OH}$	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V	
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4			2.4				
	$V_{CC} = 3\text{ V}$		2			2				
$V_{OL}$	$V_{CC} = 2.7\text{ V}$		$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2		
			$I_{OL} = 24\text{ mA}$		0.5			0.5		
	$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$		0.4			0.4		
			$I_{OL} = 32\text{ mA}$		0.5			0.5		
			$I_{OL} = 48\text{ mA}$		0.55			0.55		
			$I_{OL} = 64\text{ mA}$					0.55		
$I_I$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$		Control inputs		$\pm 1$			$\pm 1$		
	$V_{CC} = 0\text{ or }3.6\text{ V}$ , $V_I = 5.5\text{ V}$				10			10		
	$V_{CC} = 3.6\text{ V}$		$V_I = 5.5\text{ V}$		20			20		
			$V_I = V_{CC}$		5			5		
			$V_I = 0$		-10			-10		
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$		$\pm 100$			$\pm 100$			$\mu\text{A}$	
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$		75			75		
			$V_I = 2\text{ V}$		-75			-75		
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$		1			1			$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$		-1			-1			$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$ , $I_O = 0$		Outputs high		0.12			0.12		
			Outputs low		5			5		
			Outputs disabled		0.12			0.12		
$\Delta I_{CC}\S$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$		0.2			0.2			mA	
$C_i$	$V_I = 3\text{ V or }0$		3.5			3.5			pF	
$C_{io}$	$V_O = 3\text{ V or }0$		12			12			pF	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Unused pins at  $V_{CC}$  or GND

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		SN54LVT16500				SN74LVT16500				UNIT
		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	150	0	125	0	150	0	125	MHz
t <sub>w</sub>	Pulse duration	LE high		3.3		3.3		3.3		ns
		CLK high or low		3.3		3.3		3.3		
t <sub>su</sub>	Setup time	A before CLKAB↓		1.8		1.1		1.8		ns
		B before CLKBA↓		1.9		1.2		1.9		
		A or B before LE↓, CLK high		2.2		1.3		2.2		
		A or B before LE↓, CLK low		2.7		1.9		2.7		
t <sub>h</sub>	Hold time	A or B after CLK↓		1.2		1.2		1.2		ns
		A or B after LE↓		0.9		1.1		0.9		

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16500				SN74LVT16500				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f <sub>max</sub>			150		125			150		125	MHz	
t <sub>PLH</sub>	B or A	A or B	1.7	5.8		7	1.7	3	5.4		6.8	ns
t <sub>PHL</sub>			1.6	6		7.8	1.6	3.2	5.9		7.7	
t <sub>PLH</sub>	LEBA or LEAB	A or B	2.3	7.3		8.9	2.3	4	7		8.5	ns
t <sub>PHL</sub>			2.7	8.2		9.8	2.7	4.3	7.9		9.7	
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	2	7.4		8.8	2	4.1	7		8.3	ns
t <sub>PHL</sub>			2.4	8.1		10	2.4	4.4	7.9		9.9	
t <sub>PZH</sub>	OEBA or OEAB	A or B	1.2	5.2		6.1	1.2	3	5		5.9	ns
t <sub>PZL</sub>			1.5	5.9		7	1.5	3	5.8		6.9	
t <sub>PHZ</sub>	OEBA or OEAB	A or B	2.7	7.7		8.6	2.7	4.6	7.4		8.3	ns
t <sub>PLZ</sub>			2.8	7.3		7.7	2.8	4.7	6.7		7.2	

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

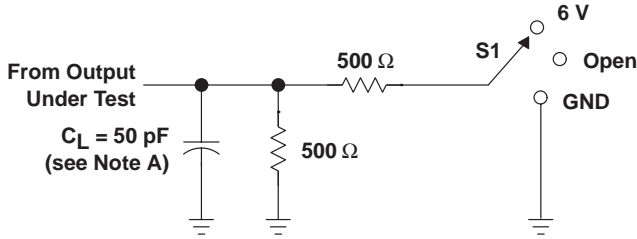
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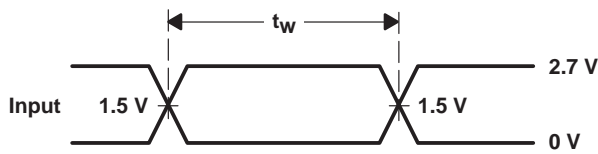
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**PARAMETER MEASUREMENT INFORMATION**

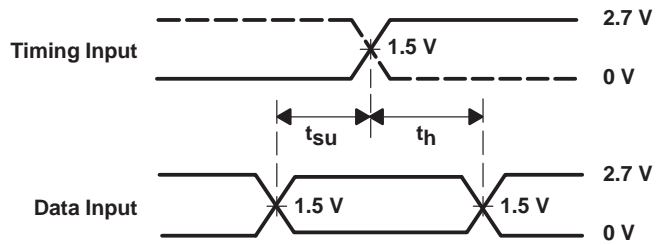


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

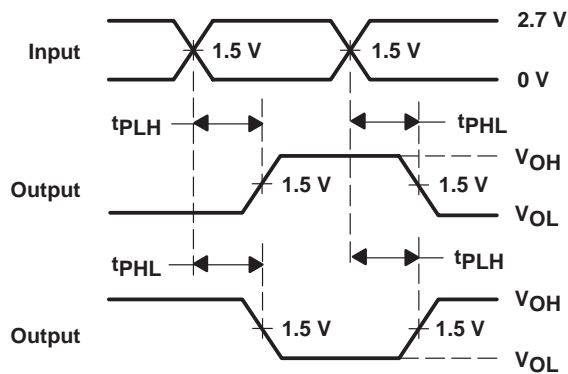
**LOAD CIRCUIT**



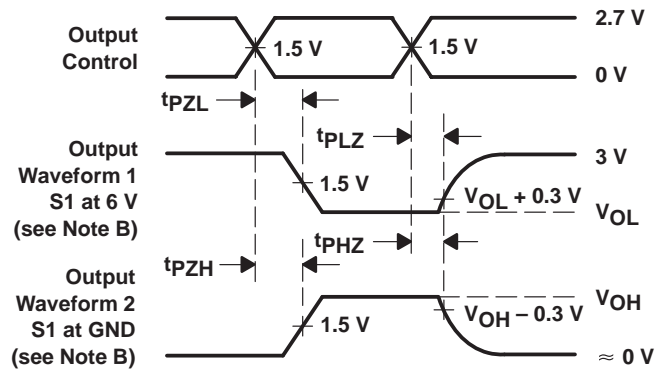
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74LVT16500DGGRE4	NRND	TSSOP	DGG	56		TBD	Call TI	Call TI	
74LVT16500DGGRG4	NRND	TSSOP	DGG	56		TBD	Call TI	Call TI	
SN74LVT16500DGGR	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	
SN74LVT16500DL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	
SN74LVT16500DLR	NRND	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVT16500DLRG4	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

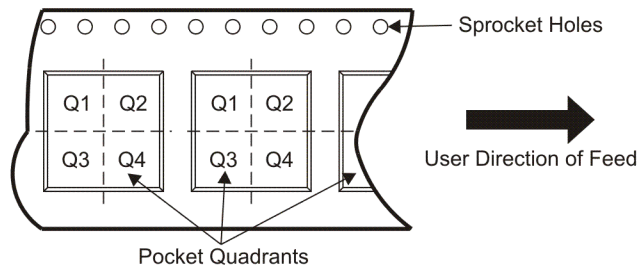
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT16500DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT16500DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

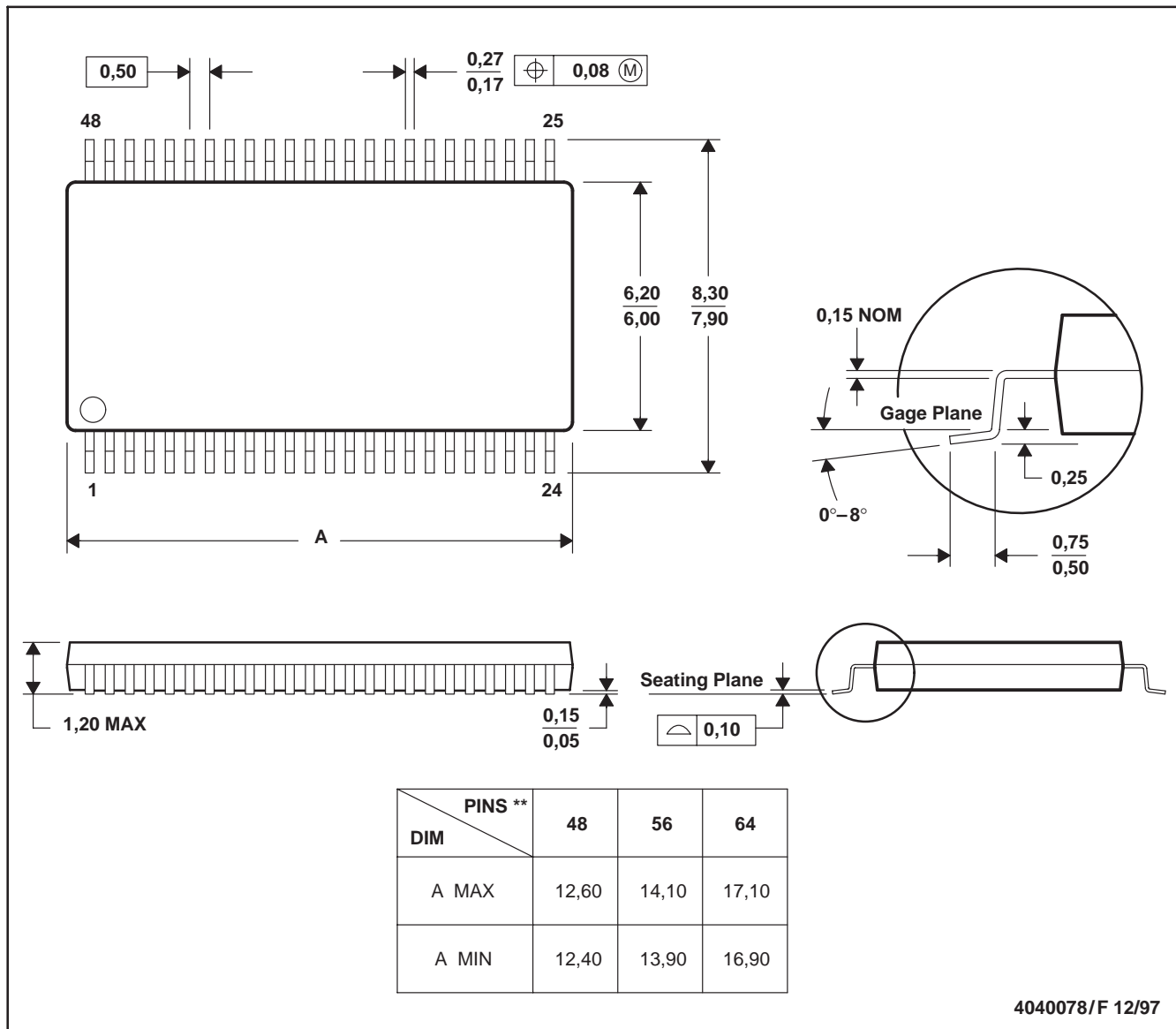


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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