THE DATASHEET OF

S29CD016J0MDGH017

S29CD016J Known Good Die

16 Megabit (512k x 32-Bit) CMOS 2.5 Volt-only Burst Mode, Dual Boot, Simultaneous Read/Write Flash Memory

Data Sheet Supplement

ADVANCE INFORMATION

General Description

The Spansion S29CD016J and S29CL016J devices are Floating Gate products fabricated in 110 nm process technology. These burst mode Flash devices are capable of performing simultaneous read and write operations with zero latency on two separate banks. These products can operate up to 56 MHz and use a single V_{CC} of 2.5 V to 2.75 V (S29CD-J) or 3.0 V to 3.6 V (S29CL-J) that make them ideal for today's demanding automotive applications.

Distinctive Characteristics

- **Single 2.6 V (S29CD-J) or 3.3 V (S29CL-J) for read / program / erase**
- **110 nm Floating Gate Technology**
- **Simultaneous Read / Write operation with zero latency**
- **X32 Data Bus**
- **Dual Boot Sector Configuration (top and bottom)**
- **Flexible Sector Architecture**
  - — CD016J & CL016J: Eight 2K Double word, Thirty-two 16K Double word, and Eight 2K Double Word sectors
- **VersatileI / O™ control (1.65 V to V_{CC})**
- **Programmable Burst Interface**
  - — Linear for 2, 4, and 8 double word burst with or without wrap around
- **Secured Silicon Sector that can be either factory or customer locked**
- **20 year data retention (typical)**
- **Cycling Endurance: 100,000 write cycles per sector (typical)**
- **Command set compatible with JECEC (42.4) standard**
- **Supports Common Flash Interface (CFI)**
- **Persistent and Password methods of Advanced Sector Protection**
- **Unlock Bypass program command to reduce programming time**
- **Write operation status bits indicate program and erase operation completion**
- **Hardware (WP#) protection of two outermost sectors in the large bank**
- **Ready / Busy (RY / BY#) output indicates data available to system**
- **Suspend and Resume commands for Program and Erase Operation**

Performance Characteristics

Read Access Times		
Speed Option (MHz)	**56**	**40**
Max Asynch. Access Time, ns (t_{ACC})	64	67
Max Synch. Latency, ns (t_{IACC})	64	67
Max Synch. Burst Access, ns (t_{BACC})	10	17
Max CE# Access Time, ns (t_{CE})	69	71
Max OE# Access time, ns (t_{OE})	22	22

Current Consumption (Max values)	
Continuous Burst Read @ 56 MHz	90 mA
Program	50 mA
Erase	50 mA
Standby Mode	150 µA

Typical Program and Erase Times	
Double Word Programming	18 µs
Sector Erase	1.0 s

Publication Number S29CD016J_KGD **Revision** A **Amendment** 1 **Issue Date** August 16, 2006

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S29CD/CL016J Features

The S29CD016J & S29CL016J Flash devices are burst mode, Dual Boot, Simultaneous Read/Write Flash Memory with VersatileI/O™ manufactured on 110 nm Process Technology.

The S29CD016J is a 16 Megabit, 2.6 Volt-only single power supply burst mode flash memory device that can be configured for 524,288 double words. The S29CL016J is the 3.3 Volt-only version of that device. Both devices can be programmed in standard EPROM programmers.

To eliminate bus contention, each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls. Additional control inputs are required for synchronous burst operations: Load Burst Address Valid (ADV#), and Clock (CLK).

Each device requires only a single 2.6 Volt-only (2.50 V – 2.75 V) or 3.3 Volt-only (3.00 V – 3.60 V) for both read and write functions. A 12.0-volt VPP is not required for program or erase operations, although an acceleration pin is available if faster programming performance is required.

The device is entirely command set compatible with the JEDEC single-power-supply Flash standard. The software command set is compatible with the command sets of the 5 V Am29F and 3 V Am29LV Flash families. Commands are written to the command register using standard micro-processor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

The **Simultaneous Read / Write architecture** provides simultaneous operation by dividing the memory space into two banks. The device can begin programming or erasing in one bank, and then simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device provides a 256-byte **Secured Silicon Sector** with an one-time-programmable (OTP) mechanism.

In addition, the device features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups: **Persistent Sector Protection** is a command sector protection method that replaces the old 12 V controlled protection method; **Password Sector Protection** is a highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted; **WP# Hardware Protection** prevents program or erase in the two outermost 8 Kbytes sectors of the larger bank.

The device defaults to the Persistent Sector Protection mode. The customer must then choose if the Standard or Password Protection method is most desirable. The WP# Hardware Protection feature is always available, independent of the other protection method chosen.

The **VersatileI/O™ (V_{CCQ})** feature allows the output voltage generated on the device to be determined based on the VIO level. This feature allows this device

to operate in the 1.8 V I/O environment, driving and receiving signals to and from other 1.8 V devices on the same bus.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, by reading the DQ7 (Data# Polling), or DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **password and software sector protection** feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system at V_{CC} level.

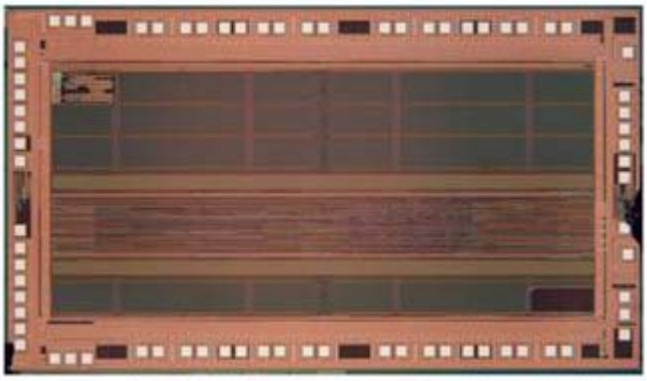
The **Program / Erase Suspend / Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data.

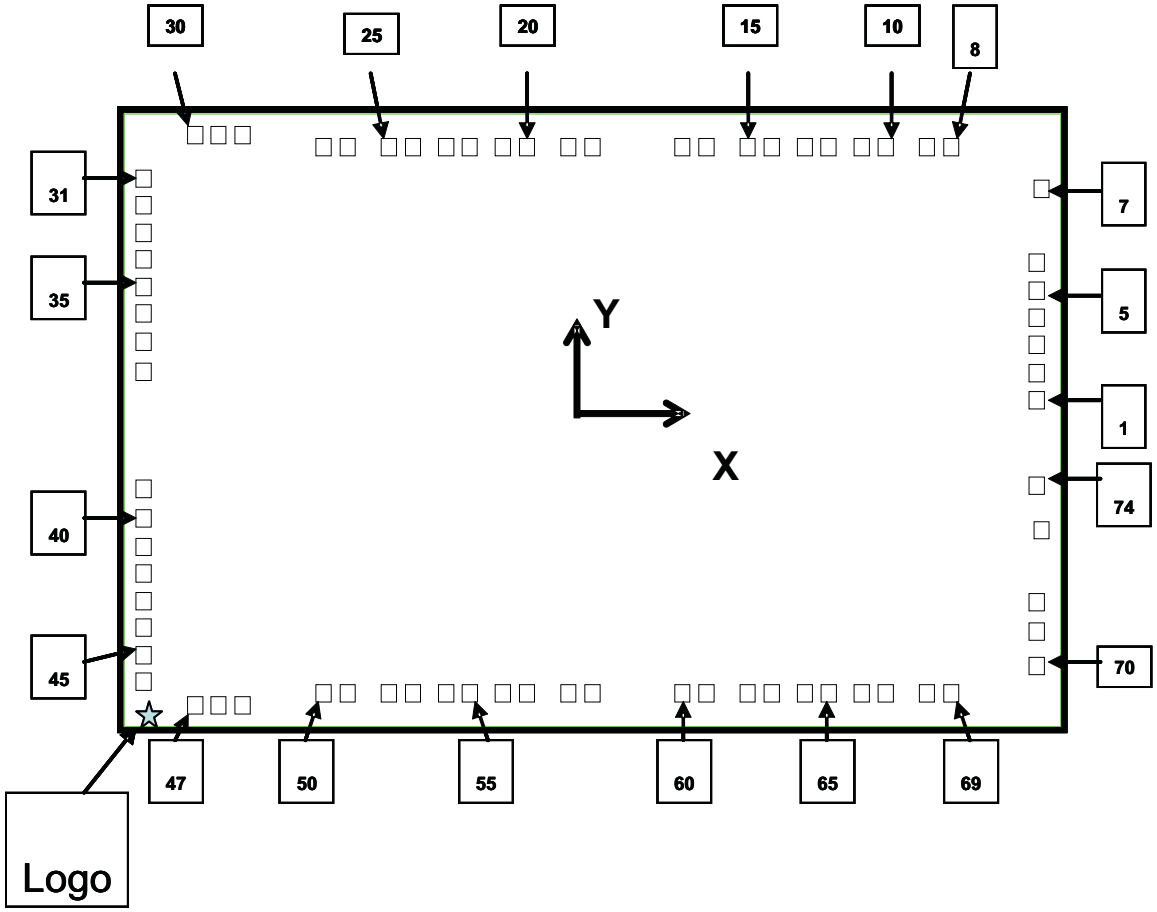
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

Die Photograph



Die Pad Locations



Pad Description

Table I. Pads Relative To Die Center (Sheet I of 3)

Pad Description – Coordinates are Relative to Die Center					
Pad	Signal	Mils		um	
		X	Y	X	Y
1	VSS	87.381	3.347	2219.485	85.016
2	VCC	87.381	8.031	2219.485	203.994
3	CE#	87.381	12.892	2219.485	327.456
4	OE#	87.381	17.556	2219.485	445.921
5	WE#	87.381	22.22	2219.485	564.386
6	WP#	87.381	27.039	2219.485	686.793
7	IND/WAIT#	88.346	39.741	2243.986	1009.432
8	DQ(16)	70.562	46.96	1792.27	1192.773
9	DQ(17)	65.797	46.96	1671.24	1192.773
10	DQ(18)	57.691	46.96	1465.356	1192.773
11	DQ(19)	52.926	46.96	1344.326	1192.773

Table I. Pads Relative To Die Center (Sheet 2 of 3)

Pad Description – Coordinates are Relative to Die Center					
Pad	Signal	Mils		um	
		X	Y	X	Y
12	VCCQ	46.4	46.96	1178.57	1192.773
13	V_{SS}	41.738	46.96	1060.153	1192.773
14	DQ(20)	35.235	46.96	894.957	1192.773
15	DQ(21)	30.47	46.96	773.927	1192.773
16	DQ(22)	22.364	46.96	568.043	1192.773
17	DQ(23)	17.599	46.96	447.013	1192.773
18	DQ(24)	-0.093	46.96	-2.356	1192.773
19	DQ(25)	-4.858	46.96	-123.386	1192.773
20	DQ(26)	-12.963	46.96	-329.27	1192.773
21	DQ(27)	-17.728	46.96	-450.3	1192.773
22	V_{CCQ}	-24.254	46.96	-616.056	1192.773
23	V_{SS}	-28.916	46.96	-734.474	1192.773
24	DQ(28)	-35.42	46.96	-899.669	1192.773
25	DQ(29)	-40.185	46.96	-1020.699	1192.773
26	DQ(30)	-48.291	46.96	-1226.583	1192.773
27	DQ(31)	-53.056	46.96	-1347.613	1192.773
28	A0	-69.006	49.02	-1752.741	1245.108
29	A1	-73.77	49.02	-1873.771	1245.108
30	A2	-78.333	49.02	-1989.671	1245.108
31	A3	-88.473	41.504	-2247.216	1054.196
32	A4	-88.473	36.941	-2247.216	938.296
33	A5	-88.473	32.176	-2247.216	817.266
34	A6	-88.473	27.613	-2247.216	701.366
35	A7	-88.473	22.848	-2247.216	580.336
36	A8	-88.473	18.285	-2247.216	464.436
37	V_{SS}	-88.473	13.402	-2247.216	340.414
38	ACC	-88.473	8.245	-2247.216	209.418
39	V_{CC}	-88.473	-11.899	-2247.216	-302.224
40	A9	-88.473	-17	-2247.216	-431.794
41	A10	-88.473	-21.905	-2247.216	-556.387
42	A11	-88.473	-26.468	-2247.216	-672.287
43	A12	-88.473	-31.233	-2247.216	-793.317
44	A13	-88.473	-35.796	-2247.216	-909.217
45	A14	-88.473	-40.561	-2247.216	-1030.247
46	A15	-88.473	-45.124	-2247.216	-1146.147
47	A16	-78.333	-49.192	-1989.671	-1249.469
48	A17	-73.77	-49.192	-1873.771	-1249.469

Table I. Pads Relative To Die Center (Sheet 3 of 3)

Pad Description – Coordinates are Relative to Die Center					
Pad	Signal	Mils		um	
		X	Y	X	Y
49	A18	-69.006	-49.192	-1752.741	-1249.469
50	DQ(0)	-53.056	-47.131	-1347.613	-1197.133
51	DQ(1)	-48.291	-47.131	-1226.583	-1197.133
52	DQ(2)	-40.185	-47.131	-1020.699	-1197.133
53	DQ(3)	-35.42	-47.131	-899.669	-1197.133
54	V_{CCQ}	-28.894	-47.131	-733.913	-1197.133
55	V_{SS}	-24.232	-47.131	-615.496	-1197.133
56	DQ(4)	-17.728	-47.131	-450.3	-1197.133
57	DQ(5)	-12.963	-47.131	-329.27	-1197.133
58	DQ(6)	-4.858	-47.131	-123.386	-1197.133
59	DQ(7)	-0.093	-47.131	-2.356	-1197.133
60	DQ(8)	17.599	-47.131	447.013	-1197.133
61	DQ(9)	22.364	-47.131	568.043	-1197.133
62	DQ(10)	30.47	-47.131	773.927	-1197.133
63	DQ(11)	35.235	-47.131	894.957	-1197.133
64	V_{CCQ}	41.76	-47.131	1060.713	-1197.133
65	V_{SS}	46.422	-47.131	1179.131	-1197.133
66	DQ(12)	52.926	-47.131	1344.326	-1197.133
67	DQ(13)	57.691	-47.131	1465.356	-1197.133
68	DQ(14)	65.797	-47.131	1671.24	-1197.133
69	DQ(15)	70.562	-47.131	1792.27	-1197.133
70	V_{CCQ}	87.381	-42.383	2219.485	-1076.54
71	RESET#	87.381	-36.499	2219.485	-927.067
72	CLK	87.381	-31.394	2219.485	-797.402
73	RY/BY#	88.346	-19.018	2243.986	-483.066
74	ADV#	87.381	-11.386	2219.485	-289.199

Ordering Information

The order number (Valid Combination) is formed by the following:

S29CD0I6J 0J D E I 00 4

PACKING TYPE
4 = Surf Tape
5 = Emboss Tape
7 = Waffe Pack

ADDITIONAL ORDERING OPTIONS
15th Character - Autoselect ID:
0 = 7E, 08, 01/00 Autoselect ID
1 = 7E, 36, 01/00 Autoselect ID

16th Character - Top or Bottom Boot:
0 = Top Boot with Simultaneous Operation
1 = Bottom Boot with Simultaneous Operation
2 = Top Boot with No Simultaneous Operation
3 = Bottom Boot with No Simultaneous Operation

TEMPERATURE RANGE
I = Industrial –40°C to +85°C)
E = Extended (–40°C to +125°C)
H = Hot (–40°C to +145°C)

DIE THICKNESS
G = 500 µm

PACKAGE TYPE
D = Die

CLOCK FREQUENCY
10th Character - Initial Burst Access Delay
0 = 5-1-1-1, 6-1-1-1, and above
1 = 4-1-1-1

11h Character - Frequency
J = 40 Mhz
M = 56 Mhz

DEVICE NUMBER / DESCRIPTION
S29CD016J
16 Megabit (512K x 32-Bit) CMOS 2.5 Volt-only Burst Mode,
Dual Boot, Simultaneous Read/Write Flash Memory
Manufactured on 110 nm floating gate technology

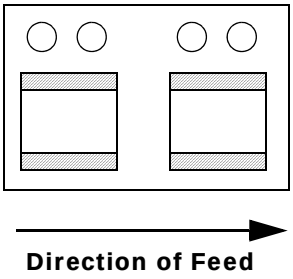
OPN Valid Combinations					
S29CD016J	OJ, 1J, OM	D	G	I, E, H	00, 01, 02, 03, 10, 11, 12, 13
	1M				02, 03, 12, 13

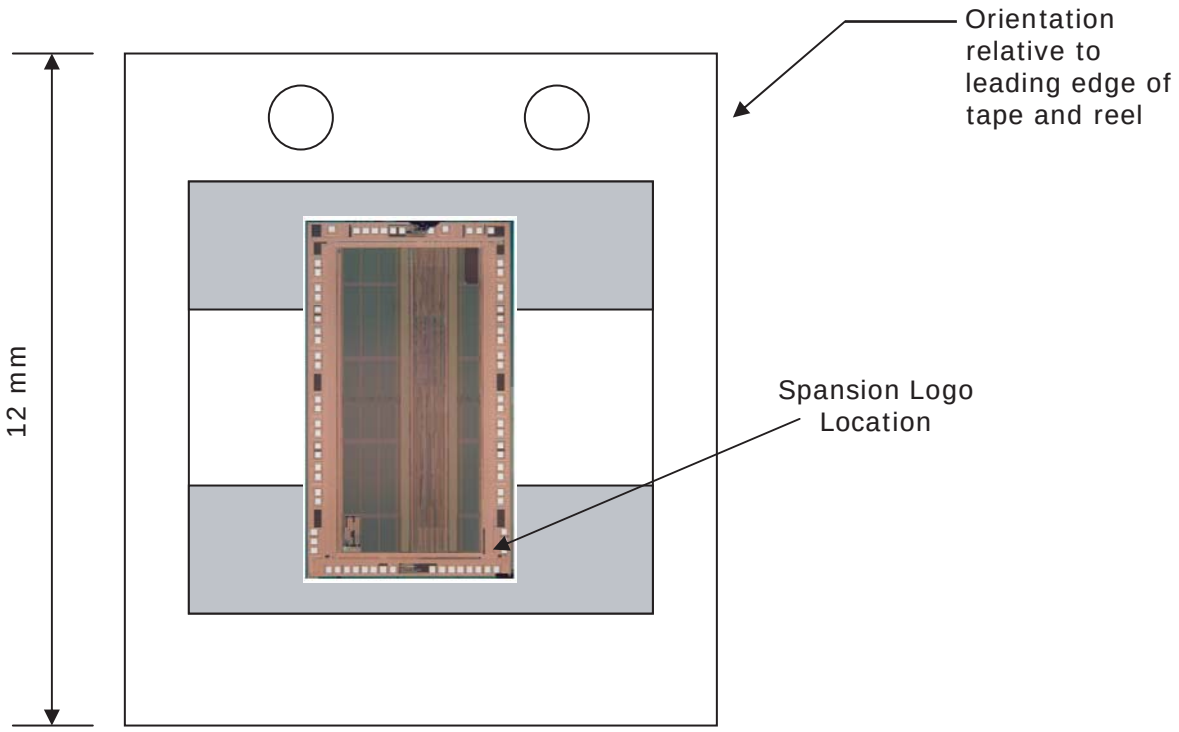
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

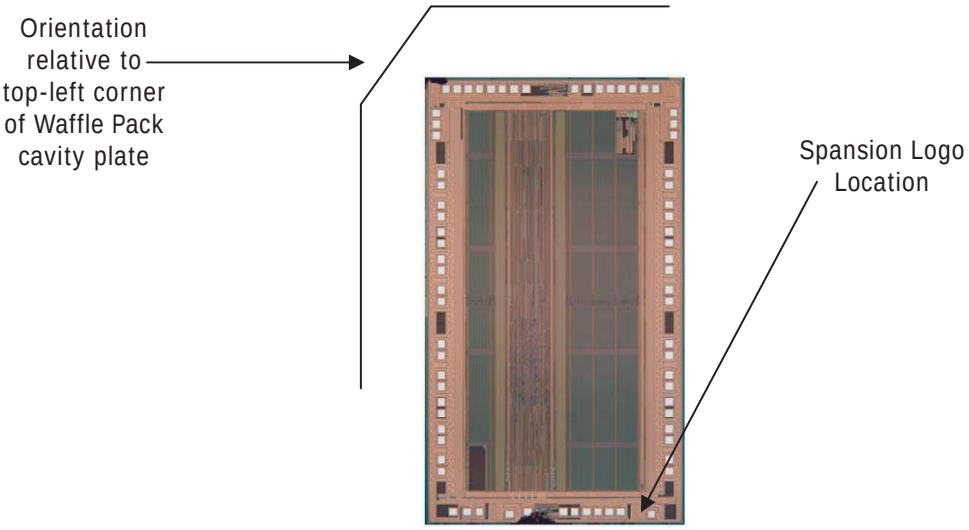
Packaging Information

Surftape Packaging

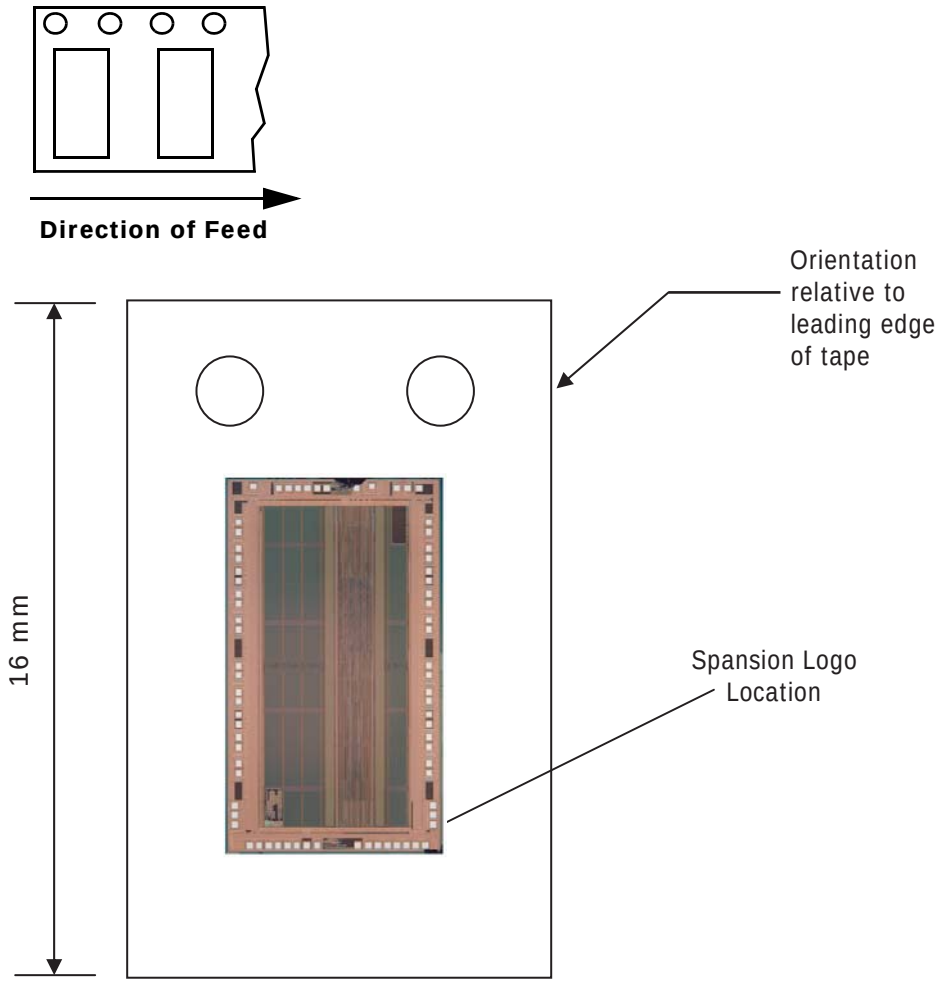




Waffle Pack Packaging



Embossed Tape Packaging



Product Test Flow

Figure 1 provides an overview of Spansion's Known Good Die test flow. For more detailed information, refer to the S29CD016J product qualification database. Spansion implements quality assurance procedures throughout the product test flow. These QA procedures also allow Spansion to produce KGD products without requiring or implementing burn-in. In addition, an off-line quality monitoring program (QMP) further guarantees Spansion quality standards are met on Known Good Die products.

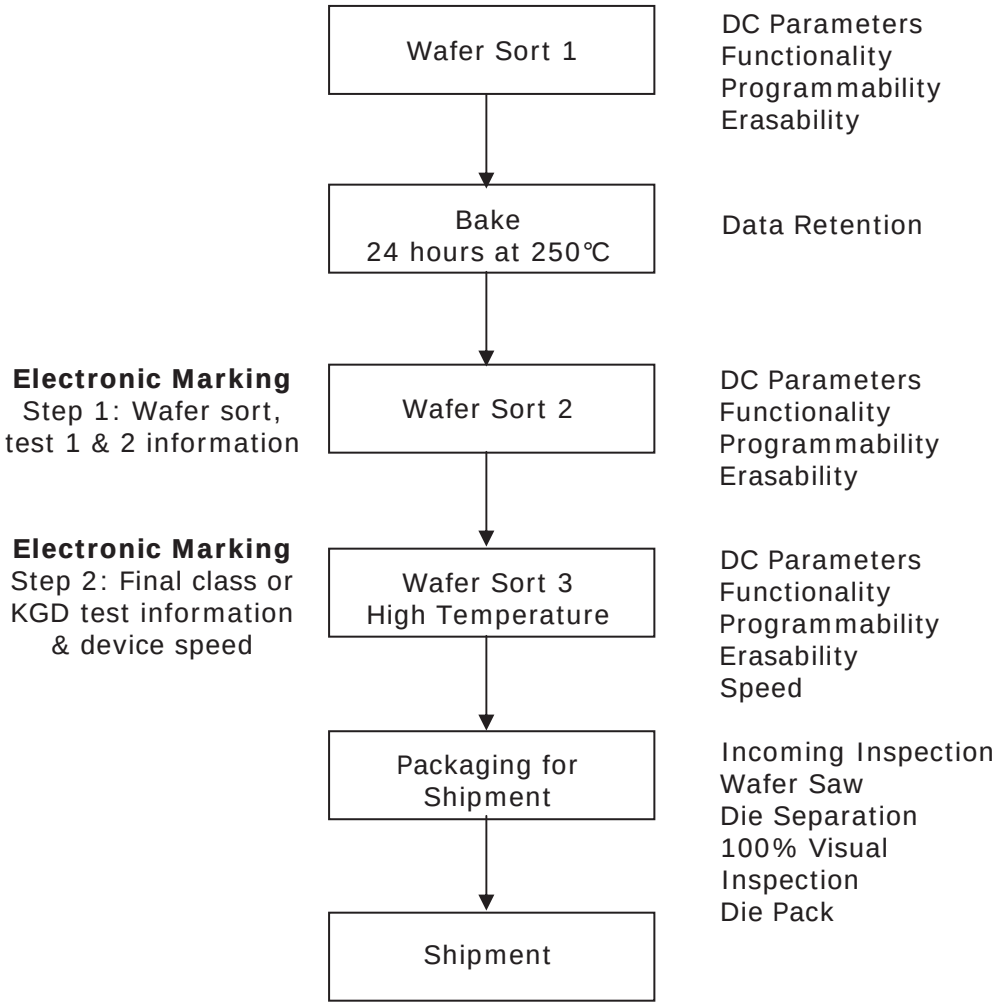


Figure I. Spansion KGD Product Test Flow

Electronic marking is programmed into every KGD for the purpose of traceability. The electronic marking contains wafer lot number, wafer number of origin, die location on the wafer, mask revision, test program revision, test dates, and speed grade. Figure 1 illustrates the steps where specific electronic marking information is programmed. For more information regarding electronic marking, reference the S29CD016J Electronic Marking Datasheet Supplement.

Absolute Maximum Ratings

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –65°C to +145°C

V_{CC}, V_{IO} (Note 1)

CD016J . . . . . –0.5 V to + 3.0 V

CL016J . . . . . –0.5 V to + 3.6 V

ACC, A9, OE#, and RESET# (Note 2)–0.5 V to +13.0 V

Address, Data, Control Signals

(with the exception of CLK) (Note 1) . . . . . –0.5 V to +3.6 V

All other pins (Note 1) . . . . . –0.5 V to +3.6 V

Output Short Circuit Current (Note 3). . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input at I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 2. Maximum DC voltage on output and I/O pins is 3.0 V. During voltage transitions output pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 9.*
2. *Minimum DC input voltage on pins ACC, A9, OE#, and RESET# is –0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 3. Maximum DC input voltage on pin A9 and OE# is +13.0 V which may overshoot to 13.7 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

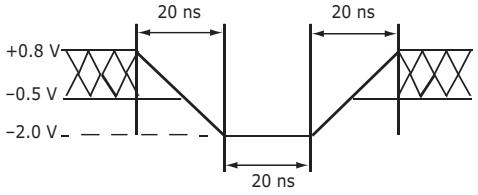


Figure 2. Maximum Negative Overshoot Waveform

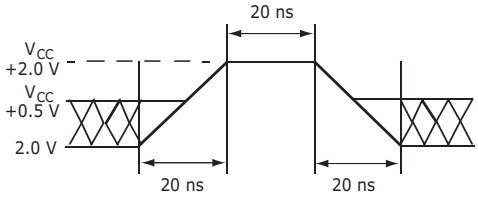


Figure 3. Maximum Positive Overshoot Waveform

Operating Ranges

Ambient Temperature (T_A), Extended Range . . . . . –40°C to +125°C
Ambient Temperature (T_A), Hot Range . . . . . –40°C to +145°C
V_{CC} Supply Voltage for regulated voltage range
CD016J . . . . . 2.5 V to 2.75 V
CL016J . . . . . 3.0 V to 3.6 V
V_{IO} Supply Voltage . . . . . 1.65 V to V_{CC}

Note: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

Physical Specifications

Die Dimensions . . . . . 4.77 x 2.83 mm
Die Thickness . . . . . 500 µm
Bond Pad Size . . . . . 86 x 86 µm
Pad Area Free of Passivation 5,776 µm2
Pads Per Die 74
Bond Pad Metalization . . . . . Al/Cu
Passivation . . . . . $Si0_2$/SiN

Manufacturing Information

Manufacturing . . . . . Fab 25, TX
Test . . . . . PNG
Manufacturing ID (Bottom Boot) 98P05AB
Preparation for Shipment . . . . . Penang, Malaysia
Fabrication Process CS69S
Die Revision 1

Special Handling Instructions

Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, Spansion recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

DC characteristics for KGD Devices at I45°C

CMOS Compatible

Parameter	Description	Test Condition		Min	Typ	Max	Unit
I_{CC1}	V_{CC} Active Asynchronous Read Current	CE# = V_{IL}, OE# = V_{IL}	1 MHz			10	mA
I_{CC3}	V_{CC} Active Program Current	CE# = V_{IL}, OE# = V_{IL}, ACC = V_{IH}			40	50	mA
I_{CC5} (Note 1)	V_{CC} Standby Current (CMOS)	V_{CC} = V_{CCMAX}, CE# = V_{CC} ± 0.3 V				250	µA
I_{CC7} (Note 1)	V_{CC} Reset Current	Reset = V_{IL}				250	µA
I_{CC8} (Note 1)	Automatic Sleep Mode Current	V_{IH} = V_{CC} ± 0.3 V, V_{IL} = VSS ± 0.3 V				250	µA

Terms and Conditions of Sale for Spansion Non-Volatile Memory Die

All transactions relating to unpackaged die under this agreement shall be subject to Spansion's standard terms and conditions of sale, or any revisions thereof, which revisions Spansion reserves the right to make at any time and from time to time. In the event of conflict between the provisions of Spansion's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

Spansion warrants its manufactured unpackaged die whether shipped to customer in individual dice or wafer form ("Known Good Die," "KGD", "Die," "Known Good Wafer", "KGW", or Wafer(s)) will meet Spansion's published specifications and against defective materials or workmanship for a period of one (1) year from date of shipment.

This limited warranty does not extend beyond the first purchaser of said Die or Wafer(s).

Buyer assumes full responsibility to ensure compliance with the appropriate handling, assembly and processing of KGD or KGW (including but not limited to proper Die preparation, Die attach, backgrinding, singulation, wire bonding and related assembly and test activities), and compliance with all guidelines set forth in Spansion's specifications for KGD or KGW, and Spansion assumes no responsibility for environmental effects on KGD or KGW or for any activity of Buyer or a third party that damages the Die or Wafer(s) due to improper use, abuse, negligence, improper installation, improper backgrinding, improper singulation, accident, loss, damage in transit, or unauthorized repair or alteration by a person or entity other than Spansion ("Limited Warranty Exclusions")

The liability of Spansion under this limited warranty is limited, at Spansion's option, solely to repair the Die or Wafer(s), to send replacement Die or Wafer(s), or to make an appropriate credit adjustment or refund in an amount not to exceed the original purchase price actually paid for the Die or Wafer(s) returned to Spansion, provided that: (a) Spansion is promptly notified by Buyer in writing during the applicable warranty period of any defect or nonconformity in the Die or Wafer(s); (b) Buyer obtains authorization from Spansion to return the defective Die or Wafer(s); (c) the defective Die or Wafer(s) is returned to Spansion by Buyer in accordance with Spansion's shipping instructions set forth below; and (d) Buyer shows to Spansion's satisfaction that such alleged defect or nonconformity actually exists and was not caused by any of the above-referenced Warranty Exclusions. Buyer shall ship such defective Die or Wafer(s) to Spansion via Spansion's carrier, collect. Risk of loss will transfer to Spansion when the defective Die or Wafer(s) is provided to Spansion's carrier. If Buyer fails to adhere to these warranty returns guidelines, Buyer shall assume all risk of loss and shall pay for all freight to Spansion's specified location. The aforementioned provisions do not extend the original limited warranty period of any Die or Wafer(s) that has either been replaced by Spansion.

THIS LIMITED WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THE IMPLIED WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THE IMPLIED WARRANTY OF MERCHANTABILITY OR NONINFRINGEMENT AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON Spansion's PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR Spansion ANY OTHER LIABILITIES. THE FOREGOING CONSTITUTES THE BUYER'S SOLE AND EXCLUSIVE REMEDY FOR THE FURNISHING OF DEFECTIVE OR NON CONFORMING KNOWN GOOD DIE OR KNOWN GOOD

WAFER(S) AND Spansion SHALL NOT IN ANY EVENT BE LIABLE FOR INCREASED MANUFACTURING COSTS, DOWNTIME COSTS, DAMAGES RELATING TO BUYER'S PROCUREMENT OF SUBSTITUTE DIE OR WAFER(S) (i.e., “COST OF COVER”), LOSS OF PROFITS, REVENUES OR GOODWILL, LOSS OF USE OF ORDAMAGE TO ANY ASSOCIATED EQUIPMENT, OR ANY OTHER INDIRECT, INCIDENTAL, SPECIAL OR CONSEQUENTIAL DAMAGES BY REASON OF THE FACT THAT SUCH KNOWN GOOD DIE OR KNOWN GOOD WAFER(S) SHALL HAVE BEEN DETERMINED TO BE DEFECTIVE OR NON CONFORMING.

Buyer agrees that it will make no warranty representations to its customers which exceed those given by Spansion to Buyer unless and until Buyer shall agree to indemnify Spansion in writing for any claims which exceed Spansion's limited warranty. Known Good Die or Known Good Wafer(s) are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of the Die or Wafer(s) can reasonably be expected to result in a personal injury. Buyer's use of Known Good Die or Known Good Wafer(s) for use in life support applications is at Buyer's own risk and Buyer agrees to fully indemnify Spansion for any damages resulting in such use or sale.

Known Good Die or Known Good Wafer are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of the die or wafer can reasonably be expected to result in a personal injury. Buyer's use of Known Good Die or Known Good Wafer for use in life support applications is at Buyer's own risk and Buyer agrees to fully indemnify Spansion for any damages resulting in such use or sale.

Revision Summary

Revision A0 (December 23, 2005)

Initial release.

Revision AI (August 16, 2006)

Corrected die pad locations figure.

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