THE DATASHEET OF

IS31FL3218-GRLS2

IS31FL3218

18 CHANNELS LED DRIVER

October 2020

GENERAL DESCRIPTION

IS31FL3218 is comprised of 18 constant current channels each with independent PWM control, designed for driving LEDs. The output current of each channel can be set at up to 38mA (Max.) by an external resistor. The average LED current of each channel can be changed in 256 steps by changing the PWM duty cycle through an I2C interface.

The chip can be turned off by pulling the SDB pin low or by using the software shutdown feature to reduce power consumption. The slave address is fixed “1010 1000”.

IS31FL3218 is available in QFN-24 (4mm × 4mm) and SOP-24 packages. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- 2.7V to 5.5V supply
- I2C interface, automatic address increment function
- Internal reset register
- Modulate LED brightness with 256 steps PWM
- Each channel can be controlled independently
- -40°C to +85°C temperature range
- QFN-24 (4mm×4mm), SOP-24 packages

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

TYPICAL APPLICATION CIRCUIT

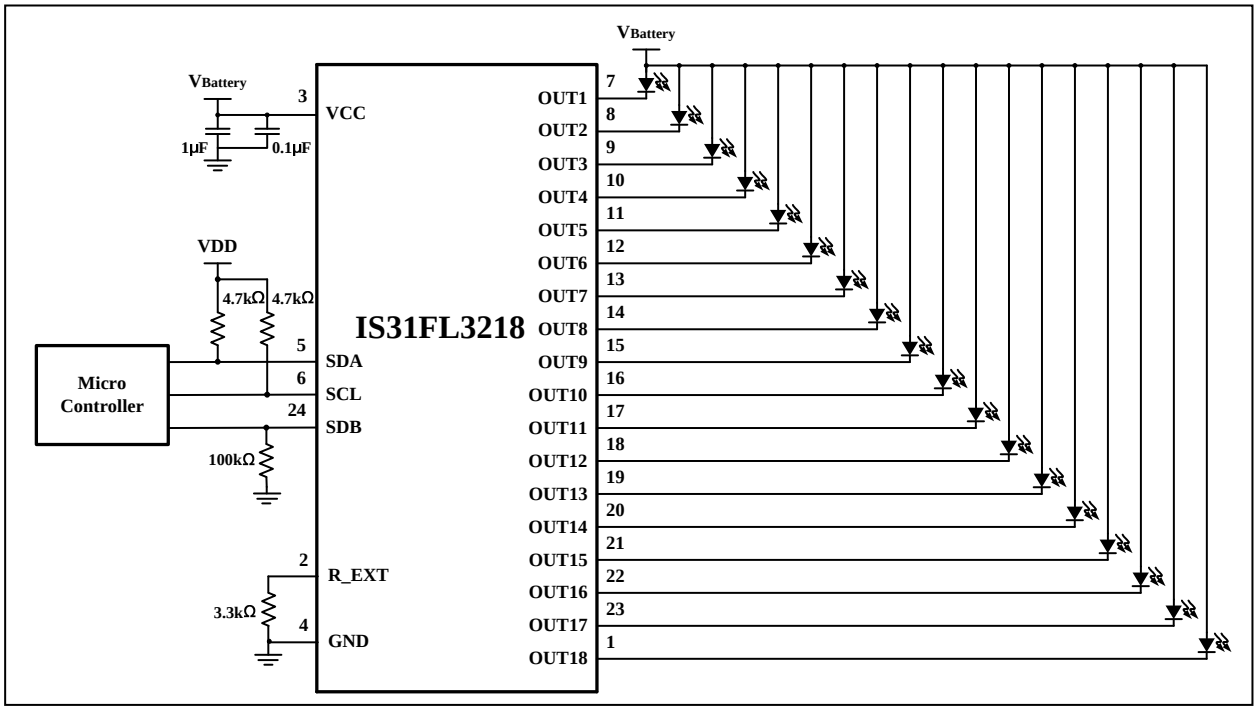
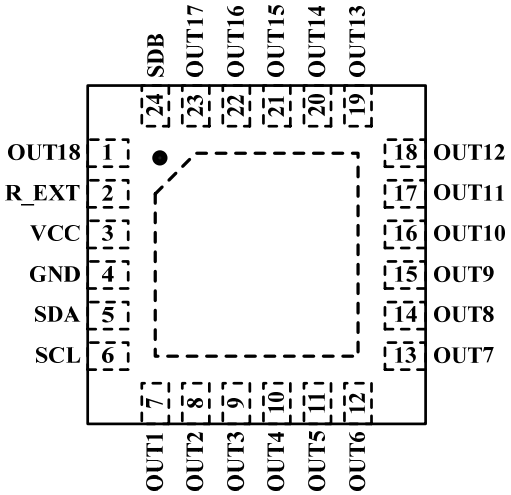
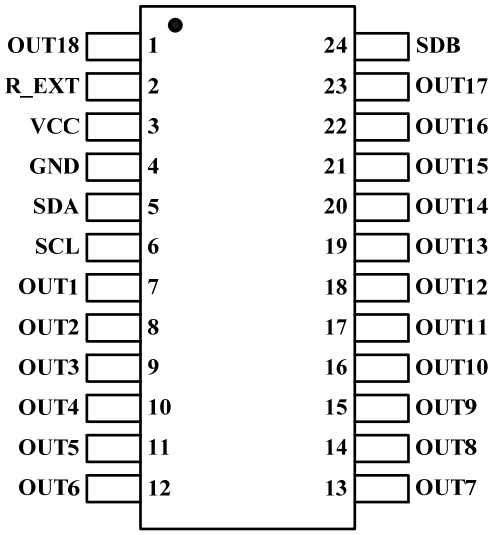


Figure 1 Typical Application Circuit

Note 1: The maximum output current is set up to 23mA when R_{EXT}= 3.3kΩ. The maximum output current can be set by external resistor, R_{EXT}. Please refer to the detail information in Page 9.

Note 2: The IC should be placed far away from the mobile antenna in order to prevent the EMI.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-24	
SOP-24	

PIN DESCRIPTION

No.	Pin	Description
1	OUT18	Output channel for LEDs.
2	R_EXT	Input terminal used to connect an external resistor. This regulates the output current.
3	VCC	Power supply.
4	GND	Ground.
5	SDA	I2C serial data.
6	SCL	I2C serial clock.
7~23	OUT1 ~ OUT17	Output channel for LEDs.
24	SDB	Shutdown the chip when pulled low.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY
IS31FL3218-QFLS2-TR	QFN-24, Lead-free	2500/Reel
IS31FL3218-GRLS2-TR	SOP-24, Lead-free	1000/Reel
IS31FL3218-GRLS2	SOP-24, Lead-free	30/Tube

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at SCL, SDA, SDB, OUT1 ~ OUT18	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	-40°C ~ +85°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	29°C /W (QFN) 40.8°C /W (SOP)
ESD (HBM) ESD (CDM)	±4kV ±1kV

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A= -40°C ~ +85°C, V_{CC}= 2.7V ~ 5.5V, unless otherwise noted. Typical values are T_A= 25°C, V_{CC}= 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{MAX}	Maximum output current of each channel	V_{CC}= 4.2V, V_{OUT}= 0.8V R_{EXT}= 2kΩ (Note 1)		38		mA
I_{CC}	Quiescent power supply current	R_{EXT}= 3.3kΩ		5.25		mA
I_{SD}	Shutdown current	V_{SDB}= 0V or software shutdown		3.1		μA
I_{OZ}	Output leakage current	V_{SDB}= 0V or software shutdown, V_{OUT}= 5V			1	μA
V_{EXT}	Output voltage of R-EXT pin			1.3		V
Logic Electrical Characteristics (SDA, SCL, SDB)						
V_{IL}	Logic "0" input voltage	V_{CC}= 2.7V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC}= 5.5V	1.4			V
I_{IL}	Logic "0" input current	(Note 2)		5		nA
I_{IH}	Logic "1" input current	(Note 2)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 2)

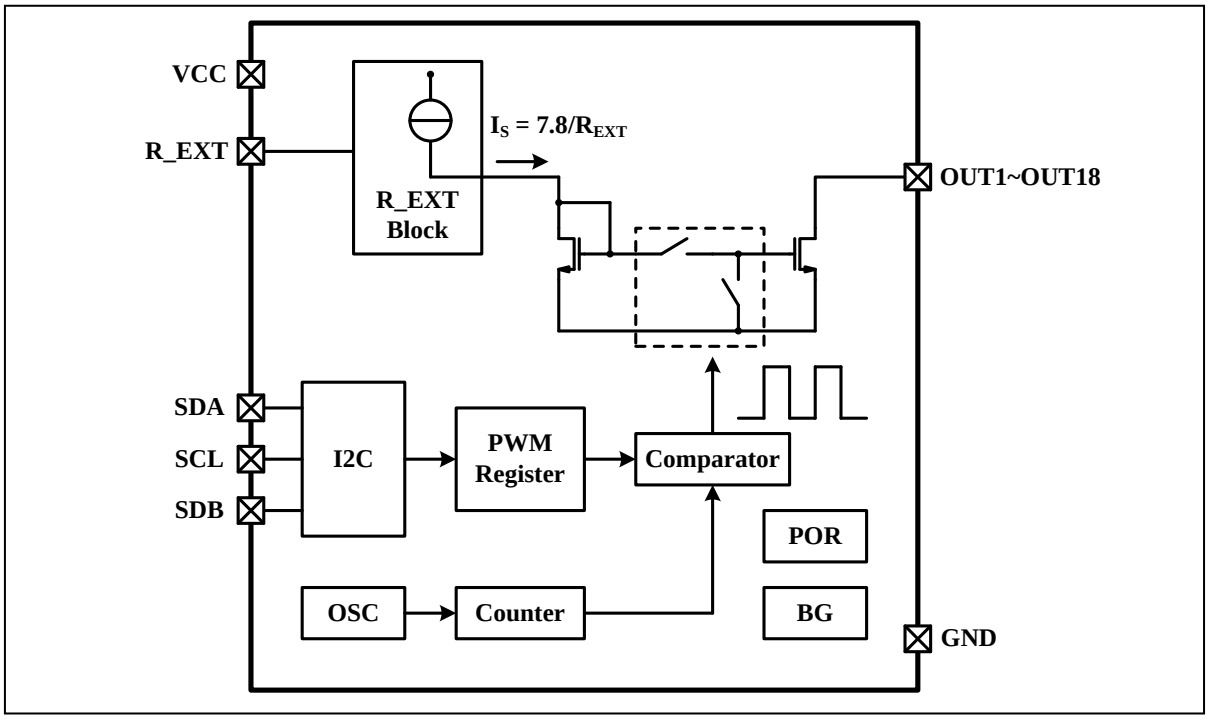
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 3)		$20+0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 3)		$20+0.1C_b$	300	ns

Note 1: The recommended minimum value of R_{EXT} is 2kΩ, or it may cause a large current.

Note 2: Guaranteed by design.

Note 3: C_b= total capacitance of one bus line in pF. $I_{SINK} \leq 6mA$. t_R and t_F measured between $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3218 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3218's slave address is "1010 1000". It only supports write operations.

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3218.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3218's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3218 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3218, the register address byte is sent, most significant bit first. IS31FL3218 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3218 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3218, load the address of the data register that the first data byte is intended for. During the IS31FL3218 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3218 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3218 (Figure 5).

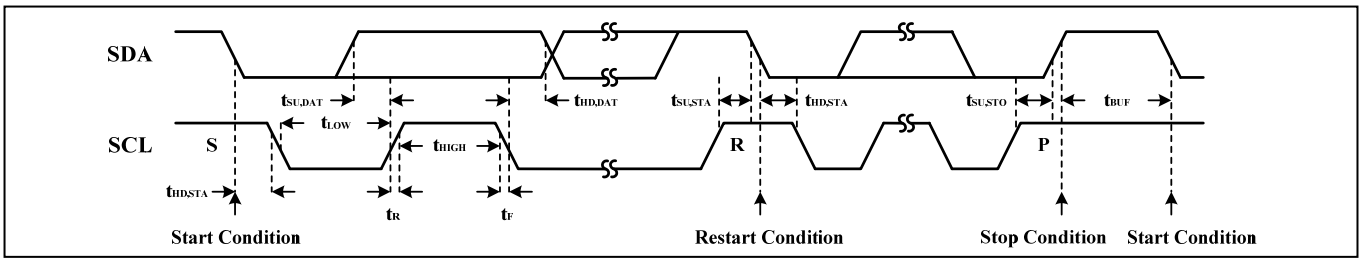


Figure 2 Interface timing

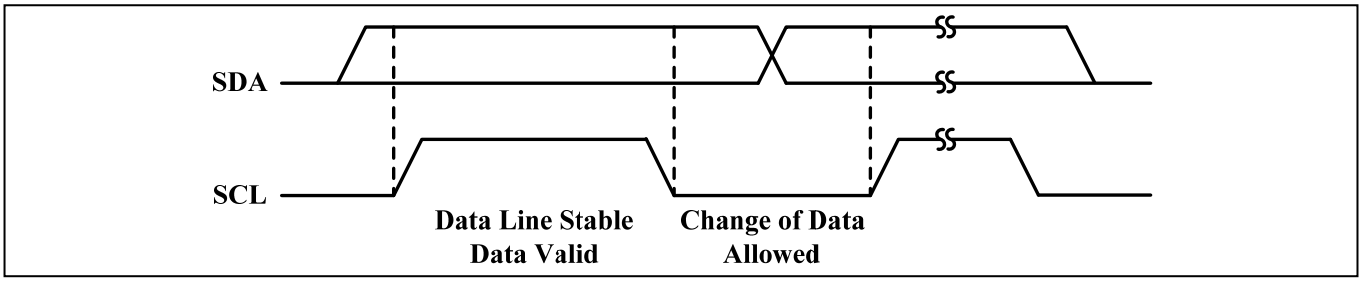


Figure 3 Bit transfer

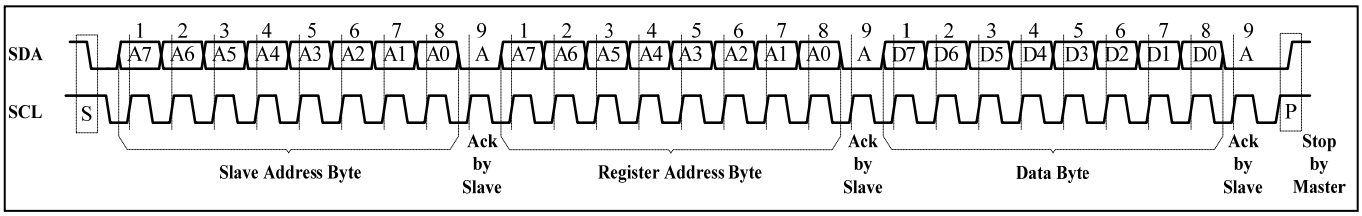


Figure 4 Writing to IS31FL3218 (Typical)

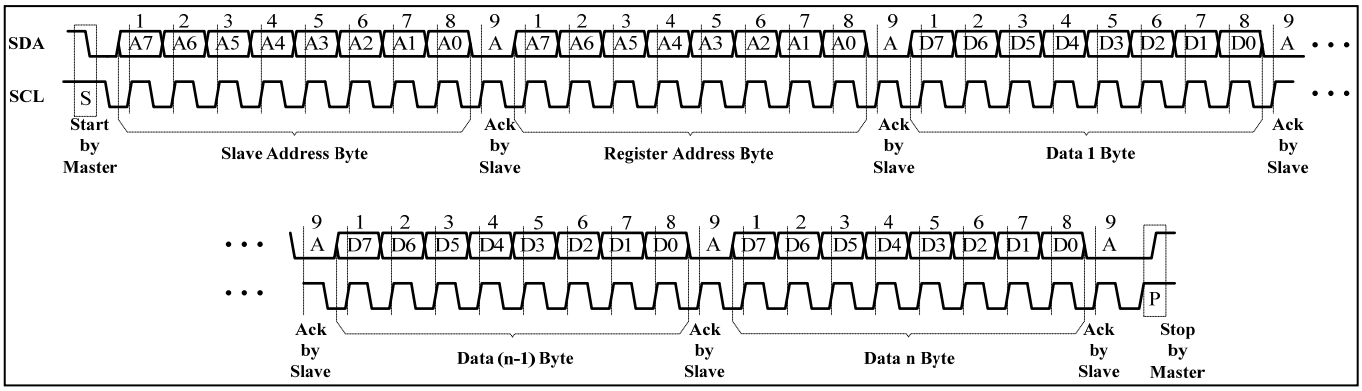


Figure 5 Writing to IS31FL3218 (Automatic Address Increment)

REGISTERS DEFINITIONS

Table 1 Register Function

Address	Name	Function	R/W	Table	Default
00h	Shutdown Register	Set software shutdown mode	W	2	0000 0000
01h~12h	PWM Register	18 channels PWM duty cycle data register		3	
13h	LED Control Register 1	Channel 1 to 6 enable bit		4	
14h	LED Control Register 2	Channel 7 to 12 enable bit		5	
15h	LED Control Register 3	Channel 13 to 18 enable bit		6	
16h	Update Register	Load PWM Register and LED Control Register's data		-	xxxx xxxx
17h	Reset Register	Reset all registers into default		-	

Table 2 00h Shutdown Register

Bit	D7:D1	D0
Name	Reserved	SSD
Default	000000	0

The Shutdown Register sets software shutdown mode of IS31FL3218.

SSD Software Shutdown Enable

0 Software shutdown mode

1 Normal operation

Table 3 01h~12h PWM Register (OUT1~OUT18)

Bit	D7:D0
Name	PWM
Default	0000 0000

The PWM Registers adjusts LED luminous intensity in 256 steps.

The value of a channel's PWM Register decides the average output current for each output, OUT1~OUT18. The average output current may be computed using the Formula (1):

$$I_{OUT} = \frac{I_{MAX}}{256} \cdot \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (1)$$

Where "n" indicates the bit location in the respective PWM register.

For example: D7:D0 = 10110101,

$$I_{OUT} = I_{MAX} (2^0+2^2+2^4+2^5+2^7)/256$$

See Formula (2) in Page 10 to calculate the I_{MAX}.

Table 4 13h LED Control Register 1 (OUT1~OUT6)

Bit	D7:D6	D5:D0
Name	Reserved	OUT6:OUT1
Default	00	000000

Table 5 14h LED Control Register 2 (OUT7~OUT12)

Bit	D7:D6	D5:D0
Name	Reserved	OUT12:OUT7
Default	00	000000

Table 6 15h LED Control Register 3 (OUT13~OUT18)

Bit	D7:D6	D5:D0
Name	Reserved	OUT18:OUT13
Default	00	000000

The LED Control Registers store the on or off state of each column LED.

OUTx	LED State
0	LED off
1	LED on

16h PWM Update Register

The data sent to the PWM Registers and the LED Control Registers will be stored in temporary registers. A write operation of “0000 0000” value to the Update Register is required to update the registers (01h~15h).

17h Reset Register

Once user writes “0000 0000” data to the Reset Register, IS31FL3218 will reset all registers to default value. On initial power-up, the IS31FL3218 registers are reset to their default values for a blank display.

APPLICATION INFORMATION

PWM CONTROL

The PWM Registers (01h~12h) can modulate LED brightness of 18 channels with 256 steps. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

R_{EXT}

The maximum output current of OUT1~OUT18 can be adjusted by the external resistor, R_{EXT}, as described in Formula (2).

$$I_{MAX} = x \cdot \frac{V_{EXT}}{R_{EXT}} \qquad (2)$$

x = 58.5, V_{OUT} = 0.8V, V_{EXT} = 1.3V.

The recommended minimum value of R_{EXT} is 2kΩ.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3218 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 7 32 Gamma Steps With 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

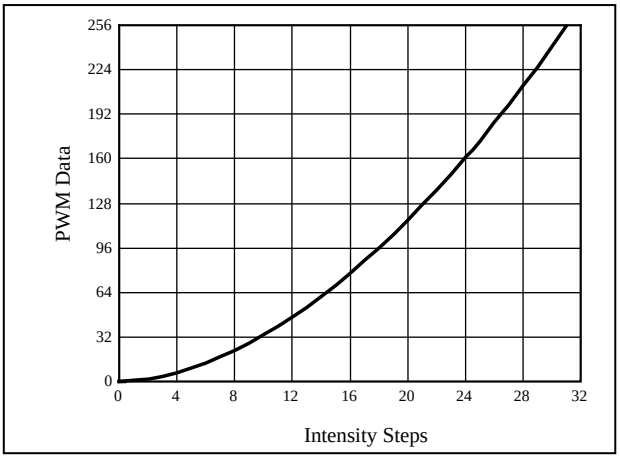


Figure 6 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 8 64 Gamma Steps With 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

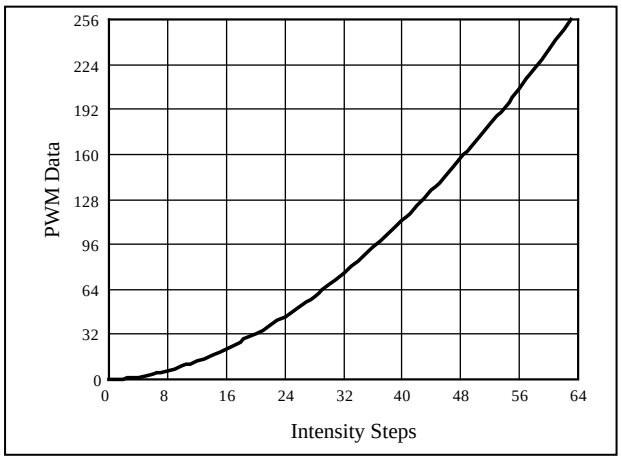


Figure 7 Gamma Correction (64 Steps)

Note, the data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (00h) to “0”, the IS31FL3218 will operate in software shutdown mode, wherein they consume only 3.1μA (Typ.) current. When the IS31FL3218 is in software shutdown mode, all current sources are switched off.

Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

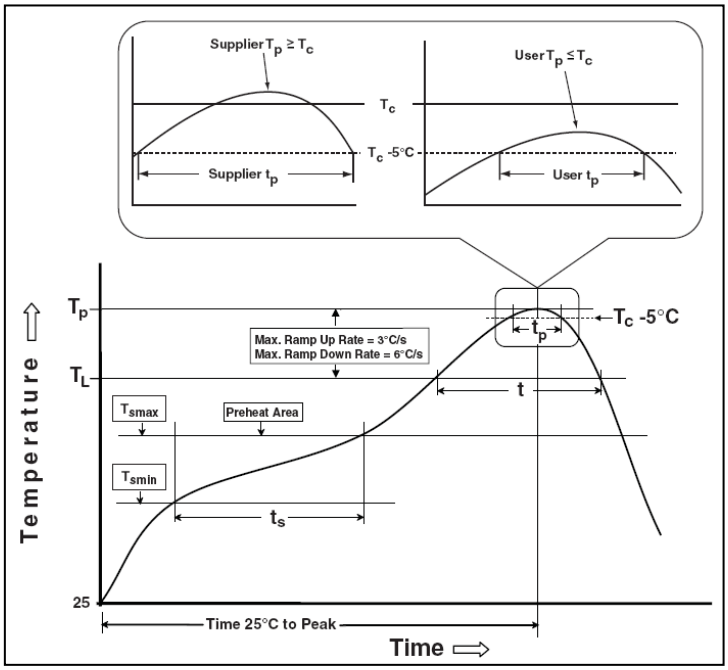
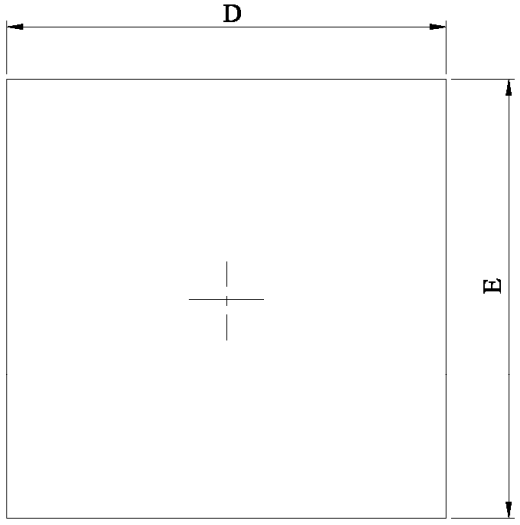


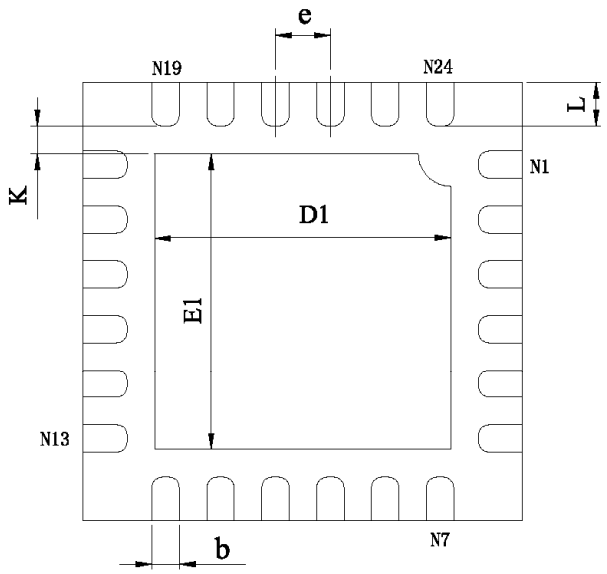
Figure 8 Classification profile

PACKAGE INFORMATION

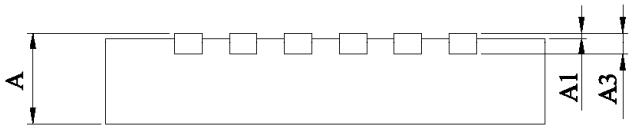
QFN-24



TOP VIEW



BOTTOM VIEW

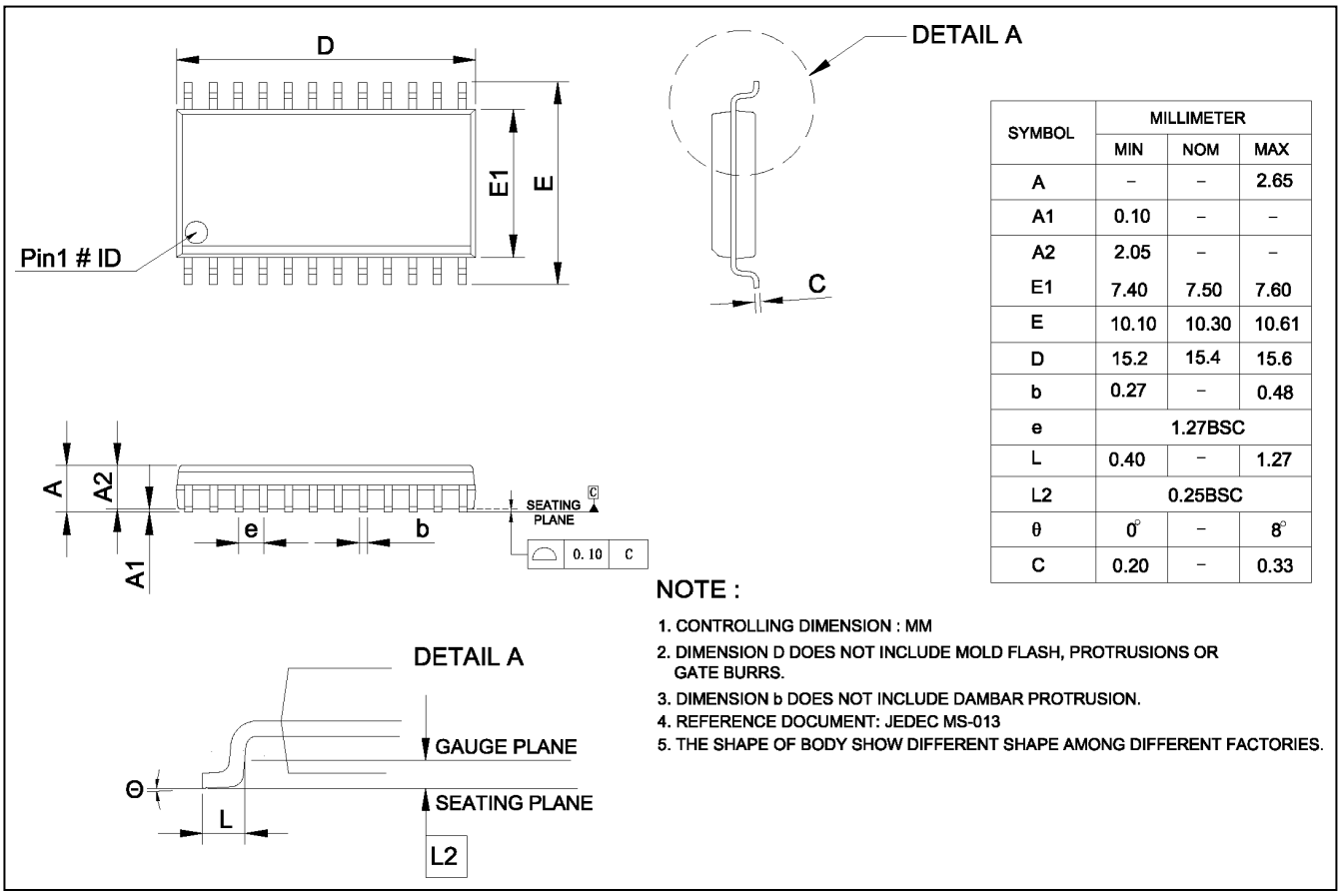


SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.30	—	2.80
e	0.50BSC		
E1	2.30	—	2.80
L	0.30	0.40	0.50
b	0.18	0.25	0.30
K	0.20MIN		

NOTES:
The thermal pad shows different shape among different factories.

SOP-24



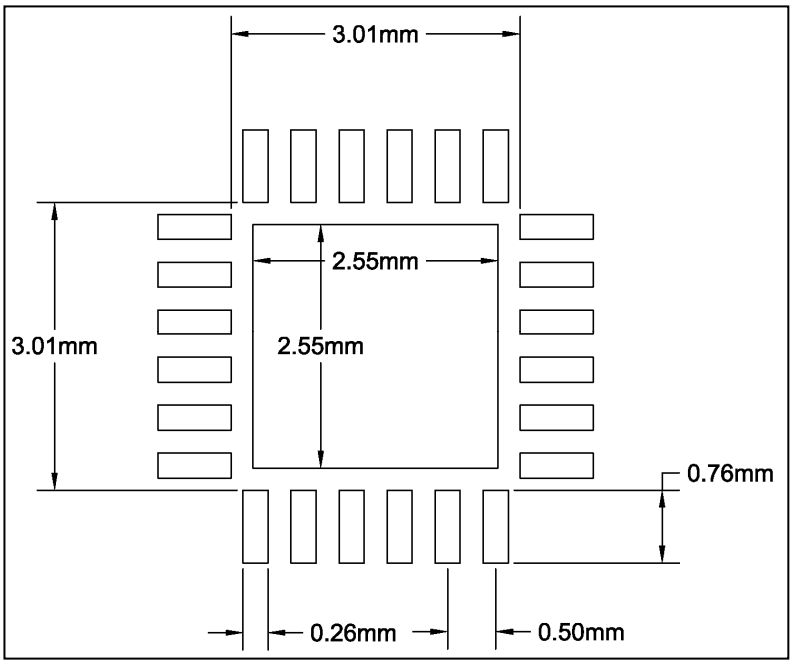
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	2.65
A1	0.10	–	–
A2	2.05	–	–
E1	7.40	7.50	7.60
E	10.10	10.30	10.61
D	15.2	15.4	15.6
b	0.27	–	0.48
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.20	–	0.33

NOTE :

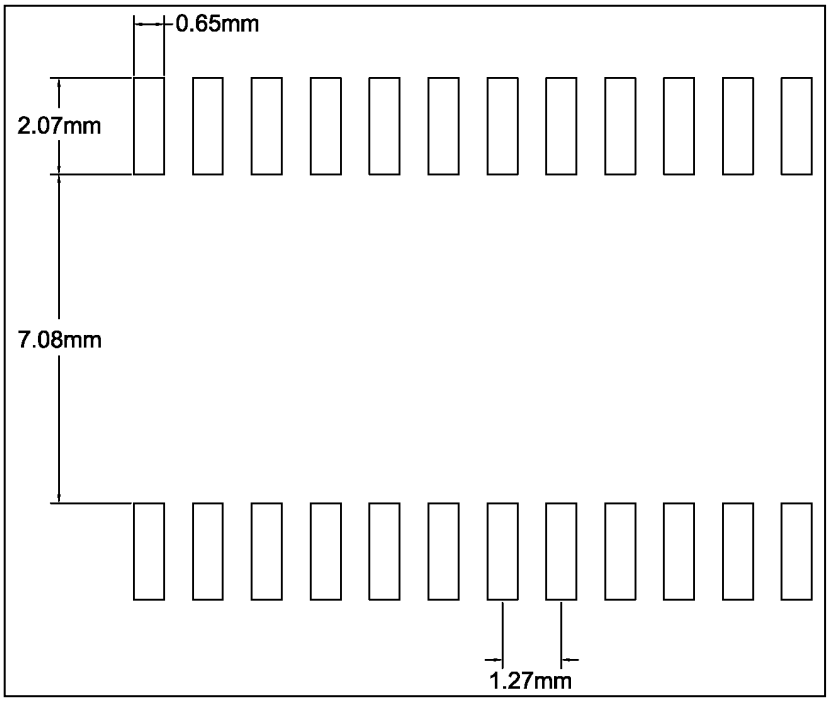
1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-013
5. THE SHAPE OF BODY SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-24



SOP-24



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Data
A	Initial release	2012.01.09
B	1. Page 3 ORDERING INFORMATION, SOP-24 QTY changes to 30/Tube 2. Remove TAPE AND REEL INFORMATION	2012.04.08
C	Absolute Maximum Ratings: voltage at OUTX change from 5V to -0.3V~VCC+0.3V	2014.09.04
D	1. Update POD 2. Update ESD (HBM) 3. Add land pattern 4. Add θ_{JA} 5. Add ESD(CDM)	2016.09.02
E	Update θ_{JA} for QFN package	2017.06.06
F	1. Add 1000/Reel packing for SOP-24 2. Update RJA and land pattern	2020.10.10

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- Shortage Management
- Alternative Solution
- Excess Inventory Management