



**THE DATASHEET OF  
ASL4500SHNY**



# ASL4500SHN

## Four-phase boost converter

Rev. 6 — 26 October 2017

Product data sheet

## 1. Introduction

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The ASL4500SHN is a highly integrated and flexible four-phase DC-to-DC boost converter IC. It has an SPI interface allowing control & diagnostic communication with an external microcontroller.

It is designed primarily for use in automotive LED lighting applications and provides an optimized supply voltage for ASLx41xSHN Multi-channel LED Buck Driver.

## 2. General description

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The ASL4500SHN has a fixed frequency peak current mode control with parabolic/non-linear slope compensation. It can operate with input voltages from 5.5 V to 40 V. It can be configured via SPI for output voltages of up to 80 V, to power the LED buck driver IC.

The ASL4500SHN is a four-phase converter which can have two independent outputs. The driver has the flexibility to be configured, via the SPI interface, as a single output converter, or with multiple combinations of number of outputs & phases.

The ASL4500SHN boost converter can drive up to four external low-side N channel MOSFETs from an internally regulated adjustable supply. It can be used to drive either logic or standard level MOSFETs.

The integrated SPI interface also allows for programming the supply under/over voltage range, output voltage range and DC-to-DC switching frequency. It enables the optimization of external components and flexibility for EMC design. This interface can also be used to provide diagnostic information such as the driver temperature.

Additional features include protection against load dump transient voltages of up to 60 V and thermal shutdown when the junction temperature of the ASL4500SHN exceeds +175 °C.

The device is housed in a very small HVQFN32 pin package and is designed to meet the stringent requirements of automotive applications. It is fully AEC Q100 grade 1 qualified. It operates over the -40 °C to +125 °C ambient automotive temperature range.



### 3. Features and benefits

- The ASL4500SHN is an automotive grade product that is AEC-Q100 grade 1 qualified
- Operating ambient temperature range of -40 °C to +125 °C
- Wide operating input voltage range from +5.5 V to +40 V
- Output voltage programmable via SPI interface
- Multi-Phase Operation for higher power
- Up to four phases per output
- Up to two flexible output voltages with 3 % accuracy programmable via SPI
- Both output voltages can be controlled independently
- Fixed Frequency Operation via built-in oscillator
- Slope Compensation tracks the frequency and output voltage
- Programmable control loop compensation
- Fast high efficiency FET switching
- Programmable Internal Gate Driver Voltage Regulator
- Gate switching is halted when overvoltage on output is detected
- Supports both Logic Level and Standard Level FETs
- Low Electro Magnetic Emission (EME) and high Electro Magnetic Immunity (EMI)
- Output Voltage Monitoring
- Supply voltage measurement
- Control Signal to Enable the Device
- Read Back programmed voltage and frequency range via SPI
- Junction Temperature monitoring via SPI
- Small Package outline HVQFN32
- Low Quiescent current <5  $\mu$ A at 25 °C when EN = 0

### 4. Applications

- Automotive LED lighting
  - ◆ Low Beam
  - ◆ High beam
  - ◆ Daytime running lights
  - ◆ Turn indicator
  - ◆ Position or Park light
  - ◆ Front fog light
  - ◆ Cornering light

### 5. Ordering information

Table 1. Ordering information

| Type number | Package |  | Version   |
|-------------|---------|--|-----------|
|             | Name    | Description  |           |
| ASL4500SHN  | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm | SOT617-12 |

## 6. Block diagram

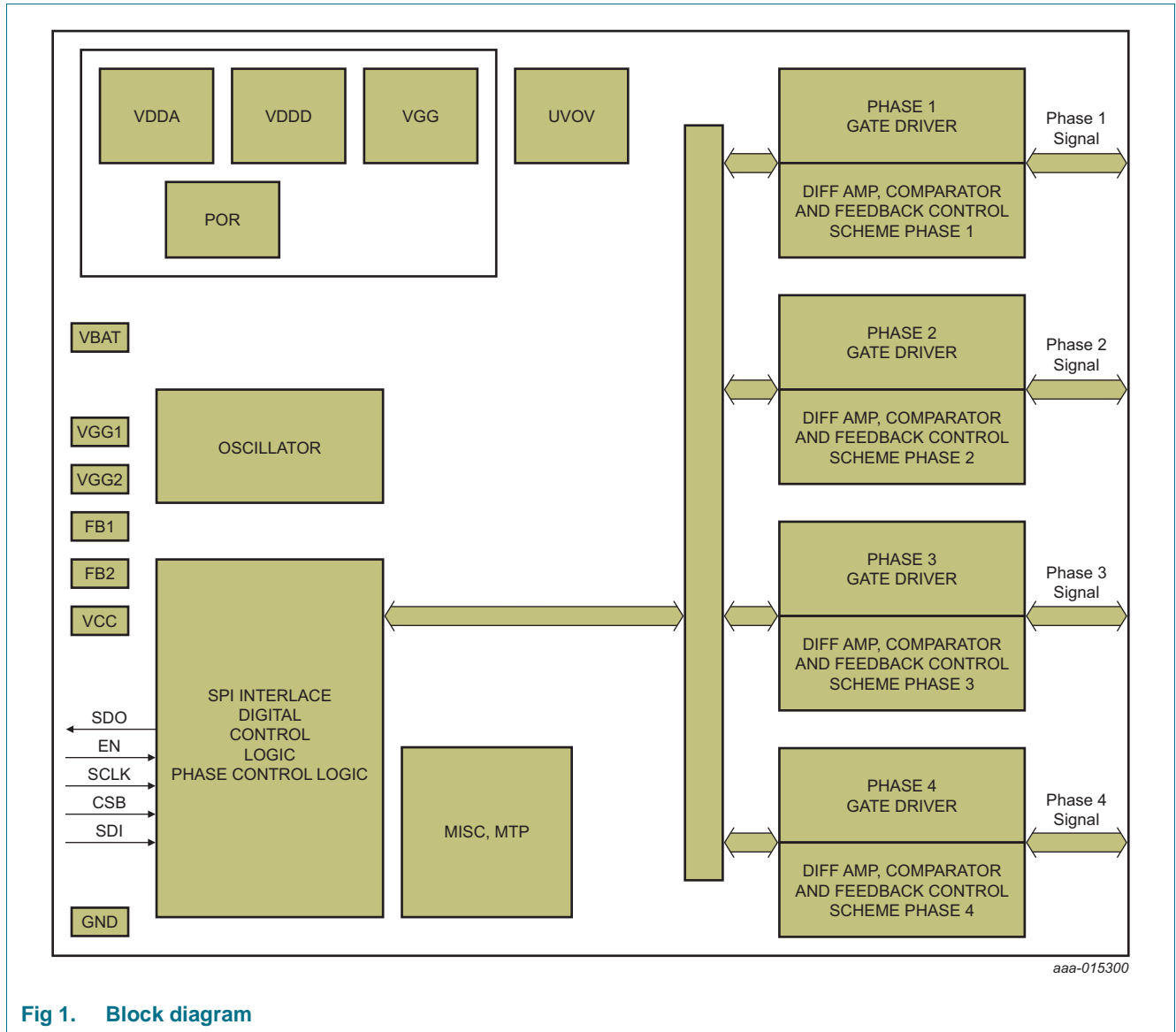
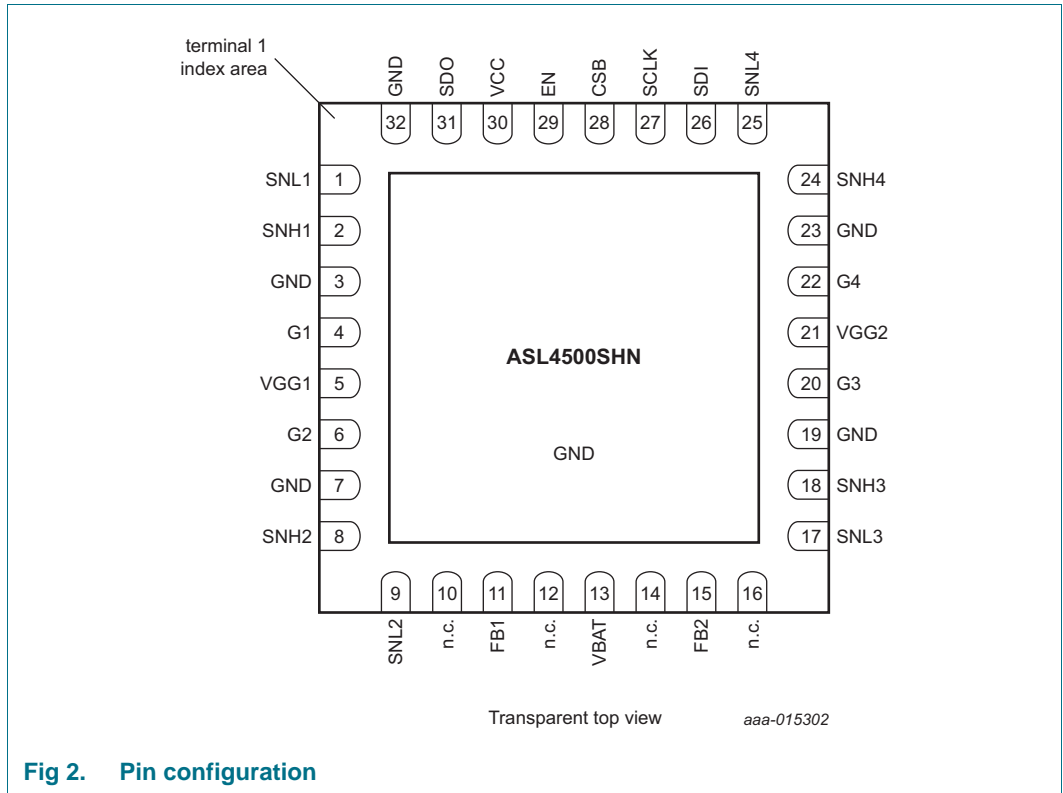


Fig 1. Block diagram

## 7. Pinning information

### 7.1 Pinning



### 7.2 Pin description

Table 2. Pin description [\[1\]](#)

| Symbol | Pin | Description  |
|--------|-----|--|
| SNL1   | 1   | phase 1 sense low                                      |
| SNH1   | 2   | phase 1 sense high                                     |
| GND    | 3   | ground   |
| G1     | 4   | phase 1 gate driver                                    |
| VGG1   | 5   | gate driver supply <a href="#">1[2]</a>                |
| G2     | 6   | phase 2 gate driver                                    |
| GND    | 7   | ground   |
| SNH2   | 8   | phase 2 sense high                                     |
| SNL2   | 9   | phase 2 sense low                                      |
| n.c.   | 10  | not connected  |
| FB1    | 11  | feedback; to be connected to Vout1 <a href="#">[3]</a> |
| n.c.   | 12  | not connected  |
| VBAT   | 13  | battery supply   |
| n.c.   | 14  | not connected  |

Table 2. Pin description ...continued<sup>[1]</sup>

| Symbol | Pin | Description                                       |
|--------|-----|---|
| FB2    | 15  | feedback; to be connected to Vout2 <sup>[3]</sup> |
| n.c.   | 16  | not connected                                     |
| SNL3   | 17  | phase 3 sense low                                 |
| SNH3   | 18  | phase 3 sense high                                |
| GND    | 19  | ground  |
| G3     | 20  | phase 3 gate driver                               |
| VGG2   | 21  | gate driver supply 2 <sup>[2]</sup>               |
| G4     | 22  | phase 4 gate driver                               |
| GND    | 23  | ground  |
| SNH4   | 24  | phase 4 sense high                                |
| SNL4   | 25  | phase 4 sense low                                 |
| SDI    | 26  | SPI data input                                    |
| SCLK   | 27  | SPI clock   |
| CSB    | 28  | SPI chip select                                   |
| EN     | 29  | enable signal                                     |
| VCC    | 30  | external 5 V supply                               |
| SDO    | 31  | SPI data out                                      |
| GND    | 32  | chip ground                                       |

[1] For enhanced thermal and electrical performance, the exposed center pad of the package should be soldered to board ground (and not to any other voltage level).

[2] VGG1 and VGG2 are connected internally.

[3] Refer to [Figure 4](#) and [Figure 14](#) for the recommended connections for pin FB1 and pin FB2.

## 8. Functional description

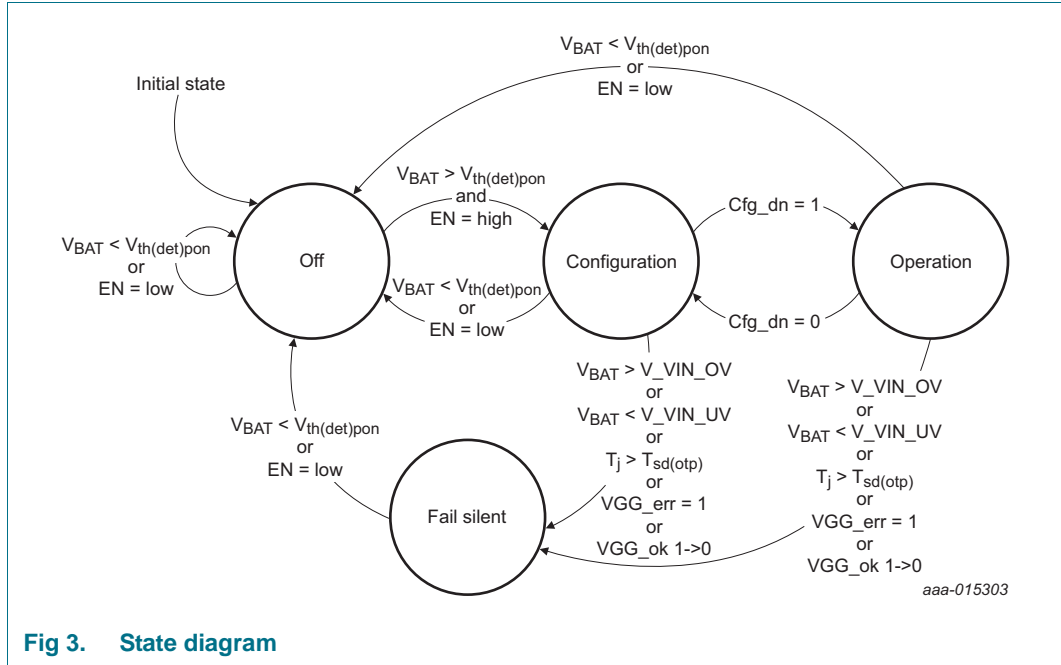


Fig 3. State diagram

### 8.1 Operating modes

Table 3. Operating modes

| Mode          | Control registers | Configuration registers | Diagnostic registers | VGG                   | Vout1<br>Vout2        | Remarks   |
|---------------|-------------------|-------------------------|----------------------|-----------------------|-----------------------|---|
| Off           | n.a.              | n.a.                    | n.a.                 | off                   | off                   | device is off, no communication possible.                             |
| Configuration | read/write        | read/write              | read                 | off                   | off                   | VGG is off if no outputs were previously enabled                      |
|               |                   |                         | read                 | according to register | off                   | VGG is on as soon as one of the outputs has been enabled              |
| Operation     | read/write        | read                    | read                 | locked                | according to register | configuration registers are locked                                    |
| Fail silent   | read/write        | read                    | read <sup>[1]</sup>  | off                   | off                   | communication possible, but all outputs off. Restart via EN possible. |

[1] Setting the bit `cfg_dn` to 0 also grants write access to the configuration registers.

#### 8.1.1 Off mode

The ASL4500SHN switches to off mode, if the input voltage drops below the power-on detection threshold ( $V_{th(det)pon}$ ) or the EN pin is low.

In Off mode, the SPI interface and all outputs are turned off.

#### 8.1.2 Configuration mode

The ASL4500SHN switches immediately from Off mode to Configuration mode, when the input voltage rises above the power-on detection threshold ( $V_{th(det)pon}$ ) and pin EN is high.

The configuration registers can be set when the ASL4500SHN is in the Configuration mode.

**8.1.3 Operation mode**

The ASL4500SHN switches from configuration mode to operation mode, as soon as the configuration done bit is set. Once the bit is set, the configuration registers are locked and cannot be changed.

In operation mode, the output is available as configured via the SPI interface. Setting bits Vout1en or Vout2en, initiates the gate driver. Once the gate driver is in regulation, signaled by bit VGG\_ok, the respective programmed target voltages are turned on. When the converters are on, the battery monitoring functionality is available.

**8.1.4 Fail silent mode**

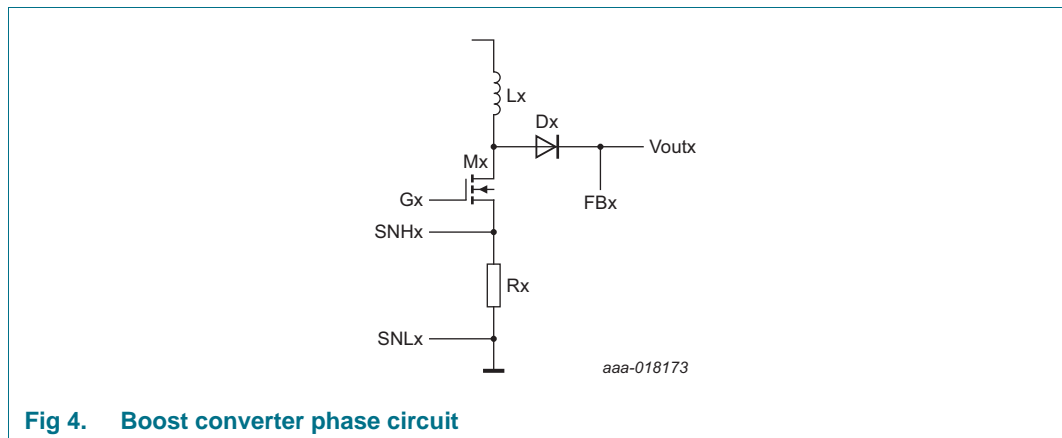
The ASL4500SHN switches from Operation mode to Fail silent mode, when the junction temperature exceeds the over temperature shutdown threshold or a gate driver error is detected. It will also switch modes when the input voltage is below the under voltage detection threshold or above the over voltage detection threshold.

In Fail silent mode, all outputs are turned off and only the SPI interface remains operational.

**8.2 Boost converter configuration**

The ASL4500SHN is an automatic boost converter IC delivering constant DC-to-DC voltage to a load. It has a fixed frequency current-mode control for an enhanced stable operation.

The ASL4500SHN offers four phases. Each phase consists of a coil, a resistor, a MOSFET and a diode as shown in [Figure 4](#).



**Fig 4. Boost converter phase circuit**

To allow flexible use of the ASL4500SHN, the configuration is based on virtual phases. They are then mapped to a real physical phase according to the physical connections and conditions of the circuitry around the ASL4500SHN as shown in [Figure 5](#).

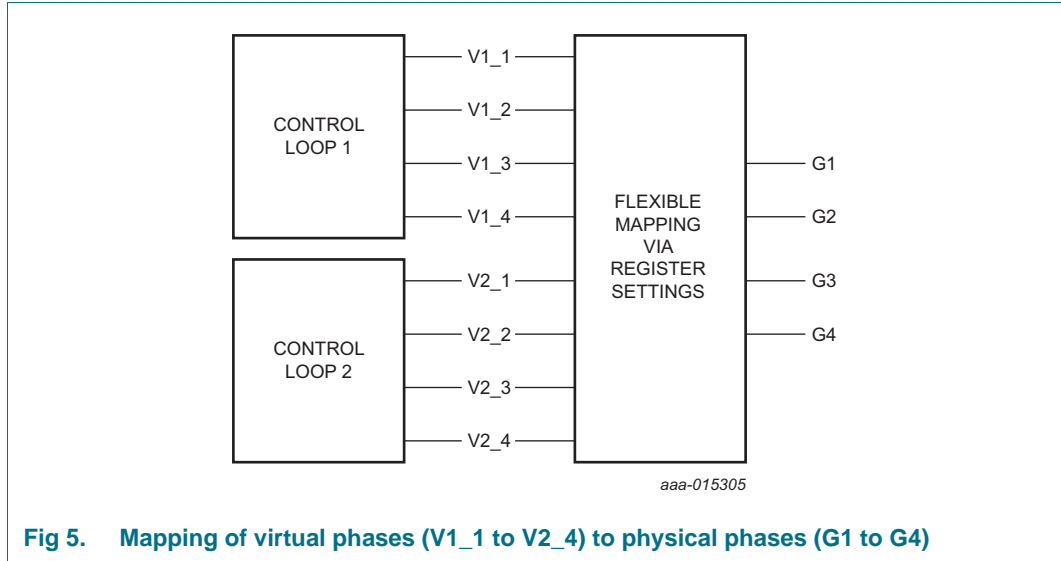


Fig 5. Mapping of virtual phases (V1\_1 to V2\_4) to physical phases (G1 to G4)

**8.2.1 Virtual phase configuration**

The ASL4500SHN can generate up to four internal phases at up to two virtual outputs. With the internal phase control enable registers, it can be selected, how many virtual phases are generated for the individual virtual outputs.

**Table 4. Internal phase control enable for output 1 (address 0x0Bh)**

| Bit | Symbol  | Description     | Value | Function                            |
|-----|---------|-----------------|-------|-------------------------------------|
| 7:4 | -       | reserved        | 0000  | reserved for future use: keep clear |
| 3   | EN_P4_1 | phase 4 enabled | 0     | phase 4 is off                      |
|     |         |                 | 1     | phase 4 is enabled                  |
| 2   | EN_P3_1 | phase 3 enabled | 0     | phase 3 is off                      |
|     |         |                 | 1     | phase 3 is enabled                  |
| 1   | EN_P2_1 | phase 2 enabled | 0     | phase 2 is off                      |
|     |         |                 | 1     | phase 2 is enabled                  |
| 0   | EN_P1_1 | phase 1 enabled | 0     | phase 1 is off                      |
|     |         |                 | 1     | phase 1 is enabled                  |

**Table 5. Internal phase control enable for output 2 (address 0x0Ch)**

| Bit | Symbol  | Description     | Value | Function                            |
|-----|---------|-----------------|-------|-------------------------------------|
| 7:4 | -       | reserved        | 0000  | reserved for future use: keep clear |
| 3   | EN_P4_2 | Phase 4 enabled | 0     | phase 4 is off                      |
|     |         |                 | 1     | phase 4 is enabled                  |
| 2   | EN_P3_2 | Phase 3 enabled | 0     | phase 3 is off                      |
|     |         |                 | 1     | phase 3 is enabled                  |
| 1   | EN_P2_2 | Phase 2 enabled | 0     | phase 2 is off                      |
|     |         |                 | 1     | phase 2 is enabled                  |
| 0   | EN_P1_2 | Phase 1 enabled | 0     | phase 1 is off                      |
|     |         |                 | 1     | phase 1 is enabled                  |

### 8.2.2 Association of physical phases to the output voltages

The phase that the ASL4500SHN offers, must be associated to the output.

**Table 6. Gate driver output (address 0x02h)**

| Bit | Symbol | Description         | Value | Function                            |
|-----|--------|---------------------|-------|-------------------------------------|
| 7:4 | -      | reserved            | 0000  | reserved for future use: keep clear |
| 3   | O_G4   | association phase 4 | 0     | phase 4 is connected to $V_{out 1}$ |
|     |        |                     | 1     | phase 4 is connected to $V_{out 2}$ |
| 2   | O_G3   | association phase 3 | 0     | phase 3 is connected to $V_{out 1}$ |
|     |        |                     | 1     | phase 3 is connected to $V_{out 2}$ |
| 1   | O_G2   | association phase 2 | 0     | phase 2 is connected to $V_{out 1}$ |
|     |        |                     | 1     | phase 2 is connected to $V_{out 2}$ |
| 0   | O_G1   | association phase 1 | 0     | phase 1 is connected to $V_{out 1}$ |
|     |        |                     | 1     | phase 1 is connected to $V_{out 2}$ |

### 8.2.3 Association of connected phases to the internal phase generation

Each physical phase that the ASL4500SHN offers, must be associated to one of the virtual phases of the output. It is established with the gate driver phase and phase select configuration registers.

**Table 7. Gate driver phase, address (address 0x0Fh)**

| Bit | Symbol | Description         | Value | Function                            |
|-----|--------|---------------------|-------|-------------------------------------|
| 7:4 | -      | reserved            | 0000  | reserved for future use: keep clear |
| 3   | O_GP4  | association phase 4 | 0     | phase 4 is connected to $V_{out 1}$ |
|     |        |                     | 1     | phase 4 is connected to $V_{out 2}$ |
| 2   | O_GP3  | association phase 3 | 0     | phase 3 is connected to $V_{out 1}$ |
|     |        |                     | 1     | phase 3 is connected to $V_{out 2}$ |
| 1   | O_GP2  | association phase 2 | 0     | phase 2 is connected to $V_{out 1}$ |
|     |        |                     | 1     | phase 2 is connected to $V_{out 2}$ |
| 0   | O_GP1  | association phase 1 | 0     | phase 1 is connected to $V_{out 1}$ |
|     |        |                     | 1     | phase 1 is connected to $V_{out 2}$ |

**Table 8. Gate driver phase, address (address 0x0Fh)**

| Bit | Symbol      | Description                | Value | Function             |
|-----|-------------|----------------------------|-------|----------------------|
| 7:6 | Phsel4[1:0] | phase select gate driver 4 | 0x0h  | routing from phase 1 |
|     |             |                            | 0x1h  | routing from phase 2 |
|     |             |                            | 0x2h  | routing from phase 3 |
|     |             |                            | 0x3h  | routing from phase 4 |
| 5:4 | Phsel3[1:0] | phase select gate driver 3 | 0x0h  | routing from phase 1 |
|     |             |                            | 0x1h  | routing from phase 2 |
|     |             |                            | 0x2h  | routing from phase 3 |
|     |             |                            | 0x3h  | routing from phase 4 |
| 3:2 | Phsel2[1:0] | phase select gate driver 2 | 0x0h  | routing from phase 1 |
|     |             |                            | 0x1h  | routing from phase 2 |
|     |             |                            | 0x2h  | routing from phase 3 |
|     |             |                            | 0x3h  | routing from phase 4 |
| 1:0 | Phsel1[1:0] | phase select gate driver 1 | 0x0h  | routing from phase 1 |
|     |             |                            | 0x1h  | routing from phase 2 |
|     |             |                            | 0x2h  | routing from phase 3 |
|     |             |                            | 0x3h  | routing from phase 4 |

### 8.2.4 Enabling of connected phases

The gate driver enable register is used to configure which of the phases is active.

**Table 9. Gate driver enable (address 0x01h)**

| Bit | Symbol | Description     | Value | Function                            |
|-----|--------|-----------------|-------|-------------------------------------|
| 7:4 | -      | reserved        | 0000  | reserved for future use: keep clear |
| 3   | EN_G4  | phase 4 enabled | 0     | phase 4 is off                      |
|     |        |                 | 1     | phase 4 is enabled                  |
| 2   | EN_G3  | phase 3 enabled | 0     | phase 3 is off                      |
|     |        |                 | 1     | phase 3 is enabled                  |
| 1   | EN_G2  | phase 2 enabled | 0     | phase 2 is off                      |
|     |        |                 | 1     | phase 2 is enabled                  |
| 0   | EN_G1  | phase 1 enabled | 0     | phase 1 is off                      |
|     |        |                 | 1     | phase 1 is enabled                  |

### 8.2.5 Boost converter frequencies configuration

The operation frequency of the boost converters can be set with via several SPI registers. To ensure a stable phase delay between the different phases, all timings are derived from the same oscillator. An integer number downscales the internal oscillator frequency for each regulation loop. This slower clock is then used to control the off time of a phase. It also controls the delay from one phase of the regulation loop to the next internal phase. The number of phases determinates finally when the phase is turned on again and defines so the operation frequency of the boost converter.

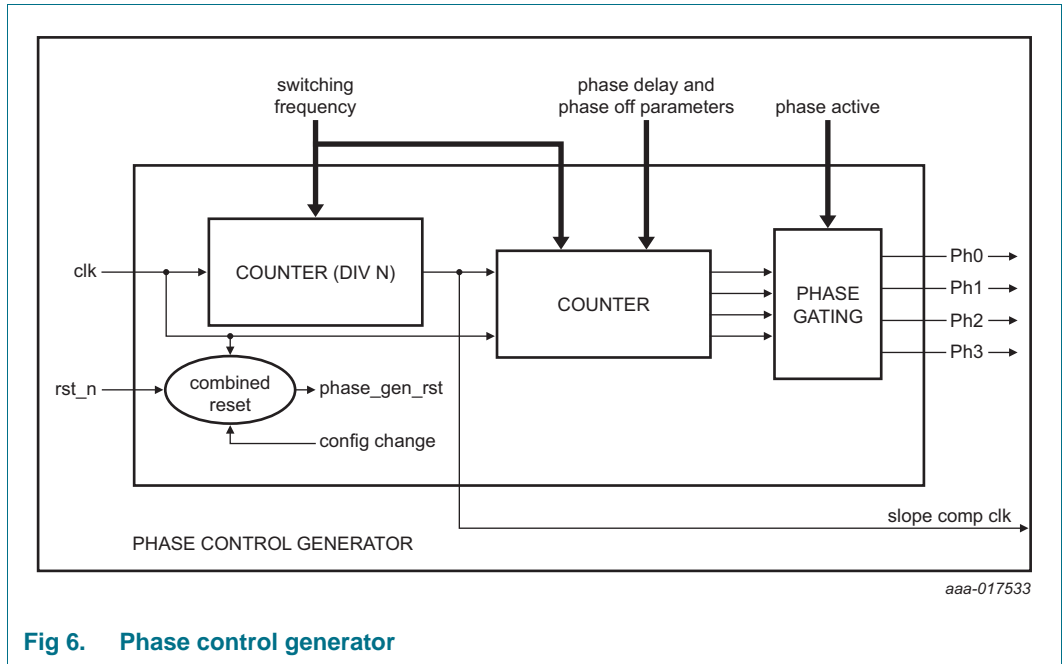


Fig 6. Phase control generator

Table 10. Clock divider for Vout1 (address 0x09h)

| Bit | Symbol       | Description                        | Value | Function                             |
|-----|--------------|------------------------------------|-------|--------------------------------------|
| 7:0 | Clkdiv1[7:0] | clock divider for output voltage 1 | 0x00h | clock is not divided                 |
|     |              |                                    | ...   | clock is divided by Clkdiv1[7:0] + 1 |
|     |              |                                    | 0xFFh | clock is divided by 256              |

Table 11. Clock divider for Vout2 (address 0x0Ah)

| Bit | Symbol       | Description                        | Value | Function                             |
|-----|--------------|------------------------------------|-------|--------------------------------------|
| 7:0 | Clkdiv2[7:0] | clock divider for output voltage 2 | 0x00h | clock is not divided                 |
|     |              |                                    | ...   | clock is divided by Clkdiv2[7:0] + 1 |
|     |              |                                    | 0xFFh | clock is divided by 256              |

Table 12. Phase-off time and phase delay of output 1 (address 0x0Dh)

| Bit | Symbol      | Description                     | Value | Function   |
|-----|-------------|---------------------------------|-------|--|
| 7:3 | Phdel1[4:0] | delay to next phase of output 1 | 0x0h  | phase delay is 1 clock period of the divided clock               |
|     |             |                                 | ...   | phase delay is Phdel1[4:0] + 1 clock period of the divided clock |
|     |             |                                 | 0x1Fh | phase delay is 32 clock periods of the divided clock             |
| 2:0 | Phoff1[2:0] | phase-off time of output 1      | 0x0h  | phase-off time is 1 clock period of the divided clock            |
|     |             |                                 | ...   | phase-off time is Phoff1[2:0] clock period of the divided clock  |
|     |             |                                 | 0x7h  | phase-off time is 7 clock periods of the divided clock           |

**Table 13. Phase-off time and phase delay of output 2 (address 0x0Eh)**

| Bit | Symbol      | Description                     | Value | Function   |
|-----|-------------|---------------------------------|-------|--|
| 7:3 | Phdel2[4:0] | delay to next phase of output 2 | 0x0h  | phase delay is 1 clock period of the divided clock               |
|     |             |                                 | ...   | phase delay is Phdel2[4:0] + 1 clock period of the divided clock |
|     |             |                                 | 0x1Fh | phase delay is 32 clock periods of the divided clock             |
| 2:0 | Phoff2[2:0] | phase-off time of output 2      | 0x0h  | phase-off time is 1 clock period of the divided clock            |
|     |             |                                 | ...   | phase-off time is Phoff2[2:0] clock period of the divided clock  |
|     |             |                                 | 0x7h  | phase-off time is 7 clock periods of the divided clock           |

**Note:** To obtain the best performance of the internal slope compensation, keep the settings of the delay between the phases as close to 32 as possible.

### 8.2.6 Control loop parameter settings

The ASL4500SHN is able to operate with a wide range of external components and offers a wide range of operating frequencies. To achieve maximum performance for each set of operation conditions, set the control loop parameters in accordance with the external components and operating frequency.

**Table 14. Loop filter proportional configuration (address 0x11h)**

| Bit | Symbol     | Description                  | Value | Function  |
|-----|------------|------------------------------|-------|---|
| 7:4 | Prop2[3:0] | proportional factor output 2 | 0x0h  | proportional factor output 2 is 0.05                                  |
|     |            |                              | ...   | proportional factor output 2 is $\text{Prop2}[3:0] \cdot 0.05 + 0.05$ |
|     |            |                              | 0xFh  | proportional factor output 2 is 0.8                                   |
| 3:0 | Prop1[3:0] | proportional factor output 1 | 0x0h  | proportional factor output 1 is 0.05                                  |
|     |            |                              | ...   | proportional factor output 1 is $\text{Prop1}[3:0] \cdot 0.05 + 0.05$ |
|     |            |                              | 0xFh  | proportional factor output 1 is 0.8                                   |

**Table 15. Loop filter integral configuration (address 0x12h)**

| Bit | Symbol      | Description              | Value | Function   |
|-----|-------------|--------------------------|-------|--|
| 7:4 | Integ2[3:0] | integral factor output 2 | 0x0h  | integral factor output 2 is 0.005                                    |
|     |             |                          | ...   | integral factor output 2 is $\text{Integ2}[3:0] \cdot 0.005 + 0.005$ |
|     |             |                          | 0xFh  | integral factor output 2 is 0.08                                     |
| 3:0 | Integ1[3:0] | integral factor output 1 | 0x0h  | integral factor output 1 is 0.005                                    |
|     |             |                          | ...   | integral factor output 1 is $\text{Integ1}[3:0] \cdot 0.005 + 0.005$ |
|     |             |                          | 0xFh  | integral factor output 1 is 0.08                                     |

Table 16. Slope compensation configuration (address 0x13h)

| Bit | Symbol       | Description                        | Value | Function  |
|-----|--------------|------------------------------------|-------|---|
| 7:4 | Slpcmp2[3:0] | slope compensation factor output 2 | 0x0h  | slope compensation factor output 2 = 112 k $\Omega$ |
|     |              |                                    | 0x1h  | slope compensation factor output 2 = 84 k $\Omega$  |
|     |              |                                    | 0x2h  | slope compensation factor output 2 = 70 k $\Omega$  |
|     |              |                                    | 0x4h  | slope compensation factor output 2 = 56 k $\Omega$  |
|     |              |                                    | 0x8h  | slope compensation factor output 2 = 28 k $\Omega$  |
| 3:0 | Slpcmp1[3:0] | slope compensation factor output 1 | 0x0h  | slope compensation factor output 1 = 112 k $\Omega$ |
|     |              |                                    | 0x1h  | slope compensation factor output 1 = 84 k $\Omega$  |
|     |              |                                    | 0x2h  | slope compensation factor output 1 = 70 k $\Omega$  |
|     |              |                                    | 0x4h  | slope compensation factor output 1 = 56 k $\Omega$  |
|     |              |                                    | 0x8h  | slope compensation factor output 1 = 28 k $\Omega$  |

Table 17. Current sense slope resistor configuration (address 0x14h)

| Bit | Symbol     | Description                                    | Value | Function              |
|-----|------------|--|-------|-----------------------|
| 7:6 | Slpr4[1:0] | slope resistor configuration for gate driver 4 | 0x0h  | 2'b00 - 250 $\Omega$  |
|     |            |  | 0x1h  | 2'b01 - 500 $\Omega$  |
|     |            |  | 0x2h  | 2'b10 - 1000 $\Omega$ |
|     |            |  | 0x3h  | 2'b11 - 1500 $\Omega$ |
| 5:4 | Slpr3[1:0] | slope resistor configuration for gate driver 3 | 0x0h  | 2'b00 - 250 $\Omega$  |
|     |            |  | 0x1h  | 2'b01 - 500 $\Omega$  |
|     |            |  | 0x2h  | 2'b10 - 1000 $\Omega$ |
|     |            |  | 0x3h  | 2'b11 - 1500 $\Omega$ |
| 3:2 | Slpr2[1:0] | slope resistor configuration for gate driver 2 | 0x0h  | 2'b00 - 250 $\Omega$  |
|     |            |  | 0x1h  | 2'b01 - 500 $\Omega$  |
|     |            |  | 0x2h  | 2'b10 - 1000 $\Omega$ |
|     |            |  | 0x3h  | 2'b11 - 1500 $\Omega$ |
| 1:0 | Slpr1[1:0] | slope resistor configuration for gate driver 1 | 0x0h  | 2'b00 - 250 $\Omega$  |
|     |            |  | 0x1h  | 2'b01 - 500 $\Omega$  |
|     |            |  | 0x2h  | 2'b10 - 1000 $\Omega$ |
|     |            |  | 0x3h  | 2'b11 - 1500 $\Omega$ |

### 8.3 Output voltage programmability

The ASL4500SHN provides the possibility to program the output voltage and output overvoltage protection of the output via the SPI interface.

#### 8.3.1 Output voltage target programmability

The target output voltage can be programmed via the Output voltage registers. As the ASL4500SHN is a boost converter, the output voltage cannot be lower than the supply voltage minus the drop of the converter diode (Dx in [Figure 4](#)).

Table 18. Output voltage 1 register (address 0x03h)

| Bit | Symbol        | Description             | Value | Function  |
|-----|---------------|-------------------------|-------|---|
| 7:0 | V_Vout_1[7:0] | target voltage output 1 | 0x00h | output 1 is turned off  |
|     |               |                         | ...   | target voltage output 1 =<br>$0.3555 * V\_Vout\_1 [7:0] * (1 + (333e-6) * (T\_junction[7:0] - 38))$ |
|     |               |                         | 0xFFh | maximum target output voltage = 90 V  |

Table 19. Output voltage 2 register (address 0x04h)

| Bit | Symbol        | Description             | Value | Function  |
|-----|---------------|-------------------------|-------|---|
| 7:0 | V_Vout_2[7:0] | target voltage output 2 | 0x00h | output 2 is turned off  |
|     |               |                         | ...   | target voltage output 2 =<br>$0.3555 * V\_Vout\_2 [7:0] * (1 + (333e-6) * (T\_junction[7:0] - 38))$ |
|     |               |                         | 0xFFh | maximum target output voltage = 90 V  |

### 8.3.2 Output overvoltage protection programming

Due to fast changes in the supply or the output, it is possible that the output voltage is disturbed. To avoid high voltages that may result into damage of attached components, the ASL4500SHN offers a programmable overvoltage protection threshold. Once the output voltage is above this threshold, the gate pin of the output stops toggling. It results in a halt of the energy delivery to the output.

Once the output voltage recovers and is below the threshold again, the gate pin starts toggling again. The regulation loop regulates the output back to the target value.

For stable operation of the device, the limit voltage output register should be programmed around 5 V higher than the output voltage registers.

Table 20. Limit voltage output 1 register (address 0x05h)

| Bit | Symbol           | Description    | Value | Function   |
|-----|------------------|----------------|-------|--|
| 7:0 | Vmax_Vout_1[7:0] | limit output 1 | 0x00h | output 1 is turned off   |
|     |                  |                | ...   | output overvoltage protection output 1 =<br>$0.3555 * V\_Vout\_1 [7:0] * (1 + (333e-6) * (T\_junction[7:0] - 38))$ |
|     |                  |                | 0xFFh | maximum output over voltage protection output 1 = 90 V   |

Table 21. Limit voltage output 2 register (address 0x06h)

| Bit | Symbol           | Description    | Value | Function   |
|-----|------------------|----------------|-------|--|
| 7:0 | Vmax_Vout_2[7:0] | limit output 2 | 0x00h | output 2 is turned off   |
|     |                  |                | ...   | output overvoltage protection output 2 =<br>$0.3555 * V\_Vout\_2 [7:0] * (1 + (333e-6) * (T\_junction[7:0] - 38))$ |
|     |                  |                | 0xFFh | maximum output over voltage protection output 2 = 90 V   |

## 8.4 Coil peak current limitation

The ASL4500SHN offers a function to limit peak current inside the coil and therefore to limit the input current for the system. Furthermore, this functionality can be used to avoid magnetic saturation of the coils and allow some soft start feature to be realized.

With the maximum phase current Voutx registers, the maximum peak current for the individual phases assigned to the output can be configured. Once the voltage drop between pins SNLx and SNHx reaches this level, the gate will be turned off until the next switching cycle. To avoid sub harmonic oscillations when the coil peak current limitation is becoming active, the slope compensation is still active. It reduces the coil peak current towards the end of the switching cycle to ensure stable operation of the system.

To avoid that this function interferes with the normal regulation, the limit should be placed well above the maximum expected currents.

**Table 22. Maximum phase current Vout1 register (address 0x07h)**

| Bit | Symbol                      | Description  | Value | Function  |
|-----|-----------------------------|--|-------|---|
| 7:0 | I_max_per_phase_Vout1 [7:0] | coil current limitation for phases assigned to Vout1 | 0x00h | no current allowed  |
|     |                             |  | ...   | maximum peak current = $(I\_max\_per\_phase\_Vout1 [7:0] * 1.8 V / 256 - 0.24 V) / R_{sense}$ |
|     |                             |  | 0x80h | maximum allowed setting = $(128 / 256 * 1.8 V - 0.24 V) / R_{sense}$                          |
|     |                             |  | ...   | not allowed   |
|     |                             |  | 0xFFh | not allowed   |

**Table 23. Maximum phase current Vout2 register (address 0x08h)**

| Bit | Symbol                      | Description  | Value | Function  |
|-----|-----------------------------|--|-------|---|
| 7:0 | I_max_per_phase_Vout2 [7:0] | coil current limitation for phases assigned to Vout2 | 0x00h | no current allowed  |
|     |                             |  | ...   | maximum peak current = $(I\_max\_per\_phase\_Vout2 [7:0] * 1.8 V / 256 - 0.24 V) / R_{sense}$ |
|     |                             |  | 0x80h | maximum allowed setting = $(128/256*1,8 V - 0.24 V) / R_{sense}$                              |
|     |                             |  | ...   | not allowed   |
|     |                             |  | 0xFFh | not allowed   |

## 8.5 Enabling output voltage

The ASL4500SHN provides two independent output voltages. In operation mode, the output voltages are turned on with the bits Vout1en and Vout2en.

As soon as one of the outputs is turned on, the gate driver voltage regulator is turned on. After the gate driver start-up time, the gate drivers start switching if the bit VGG\_ok is set.

**Table 24. Function control register (address 0x00h)**

| Bit | Symbol  | Description            | Value | Function   |
|-----|---------|------------------------|-------|--|
| 7:4 | -       | reserved               | 0000  | reserved: keep clear for future use                            |
| 3   | Cnt_CSB | count chip select time | 0     | chip select low count feature is disabled                      |
|     |         |                        | 1     | chip select low count feature is enabled                       |
| 2   | Vout2en | enable output 2        | 0     | output 2 is turned off   |
|     |         |                        | 1     | output 2 is turned on, when the device is in operation mode    |
| 1   | Vout1en | enable output 1        | 0     | output 1 is turned off   |
|     |         |                        | 1     | output 1 is turned on, when the device is in operation mode    |
| 0   | Cfg_dn  | configuration done     | 0     | device is in configuration mode - no configuration lock        |
|     |         |                        | 1     | device is in configuration mode - configuration lock is active |

## 8.6 Frequency trimming

It is mandatory to adjust the internal oscillator frequency of the device to ensure the ASL4500SHN is operating within the specified oscillator frequency range.

To measure the actual internal frequency, the device measures the time that the CSB pin is low during an SPI transfer. This time information is used to adjust the oscillator frequency of the device. The recommended procedure for the time adjustment is shown in [Figure 7](#).

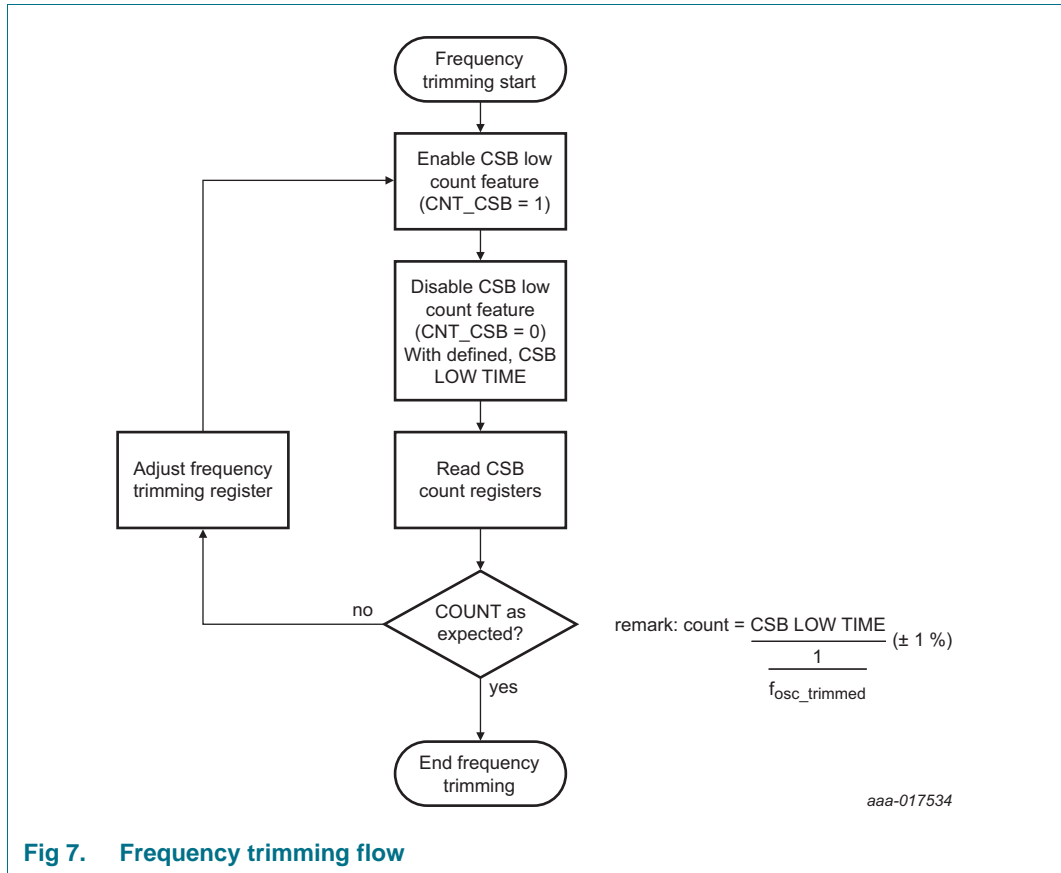


Fig 7. Frequency trimming flow

At the start of the sequence, the CSB low count feature is activated. It is done by setting the Cnt\_CSB bit high in the frequency trimming control register (bit 3; register 0x00h). The device now measures the time with its internal time domain each time the CSB pin is low. It makes this information available in the CSB count registers. To allow an exact stable reading, set the Cnt\_CSB bit low again with an accurately known CSB low time. Setting the bit low freezes the count registers. These registers store the last value, which in this case is the command that sets the Cnt\_CSB bit low.

The CSB count registers contain the count of the CSB low time of the last SPI command the CSB low count feature was enabled. CSB count register 1 contains the bits 7 to 0 of the counter, while the CSB count register 2 contains the bits 15:8.

Table 25. CSB count register 1 (address 0x041h)

| Bit | Symbol       | Description   | Value | Function               |
|-----|--------------|---------------|-------|------------------------|
| 7:0 | CSB_cnt[7:0] | CSB count low | ...   | count value (bits 7:0) |

Table 26. CSB count register 2 (address 0x042h)

| Bit  | Symbol        | Description    | Value | Function                |
|------|---------------|----------------|-------|-------------------------|
| 15:8 | CSB_cnt[15:8] | CSB count high | ...   | count value (bits 15:8) |

The count, the CSB count register returns, should correspond to the real time of the CSB low time. 1 count should correspond with  $1/f_{\text{osc\_trimmed}}$  (see Table 44).

When the CSB count register count, deviates from the applied CSB low time, adjust the device internal timing by modifying the frequency trimming register.

Table 27. Frequency trimming register (address 0x1Ch)

| Bit    | Symbol                      | Description        | Value  | Function                    |
|--------|-----------------------------|--------------------|--------|-----------------------------|
| 7:6    | -                           | reserved           | -      | n.a.                        |
| 5:0    | Freq_trim[5:0]              | frequene trim bits | 010001 | default frequency – 33.33 % |
|        |                             |                    | 010011 | default frequency – 30.56 % |
|        |                             |                    | 010101 | default frequency – 27.78 % |
|        |                             |                    | 010111 | default frequency – 25.00 % |
|        |                             |                    | 011001 | default frequency – 22.22 % |
|        |                             |                    | 011011 | default frequency – 19.44 % |
|        |                             |                    | 011101 | default frequency – 16.67 % |
|        |                             |                    | 011111 | default frequency – 13.89 % |
|        |                             |                    | 000001 | default frequency – 11.11 % |
|        |                             |                    | 000011 | default frequency – 8.33 %  |
|        |                             |                    | 000101 | default frequency – 5.56 %  |
|        |                             |                    | 000111 | default frequency – 2.78 %  |
|        |                             |                    | 001001 | default frequency           |
|        |                             |                    | 001011 | default frequency + 2.78 %  |
|        |                             |                    | 001101 | default frequency + 5.56 %  |
|        |                             |                    | 001111 | default frequency + 8.33 %  |
|        |                             |                    | 110001 | default frequency + 11.11 % |
|        |                             |                    | 110011 | default frequency + 13.89 % |
|        |                             |                    | 110101 | default frequency + 16.67 % |
|        |                             |                    | 110111 | default frequency + 19.44 % |
|        |                             |                    | 111001 | default frequency + 22.22 % |
| 111011 | default frequency + 25.00 % |                    |        |                             |
| 111101 | default frequency + 27.78 % |                    |        |                             |
| 111111 | default frequency + 30.56 % |                    |        |                             |
| 100001 | default frequency + 33.33 % |                    |        |                             |
| 100011 | default frequency + 36.11 % |                    |        |                             |
|        |                             | others             |        | not allowed                 |

To ensure that the adjustment had the desired effect, restart the procedure and check the count with the new settings in the frequency trimming register.

When the device internal time matches the applied CSB low time, no further adjustment is needed and the trimming procedure is finished.

## 8.7 Gate supply voltage

The ASL4500SHN has an integrated linear regulator to generate the supply voltage of the gate drivers. The integrated linear regulator is internally connected to the pins VGG1 and VGG2. The voltage generated by the linear regulator can be set via the VGG control register.

**Table 28. VGG control register (address 0x15h)**

| Bit | Symbol   | Description                     | Value | Function                                  |
|-----|----------|---------------------------------|-------|---|
| 7:0 | VGG[7:0] | supply voltage for gate drivers | 0x00h | not allowed                               |
|     |          |                                 | ...   | not allowed                               |
|     |          |                                 | 0x5Dh | maximum output voltage = 10.04 V          |
|     |          |                                 | ...   | $(255 - \text{VGG}[7:0]) * 62 \text{ mV}$ |
|     |          |                                 | 0xB7h | minimum output voltage = 4.46 V           |
|     |          |                                 | ...   | not allowed                               |
|     |          |                                 | 0xFFh | not allowed                               |

The actual value of VGG can deviate from the target setting due to the tolerances of the VGG regulation loop (see  $V_{o(\text{reg})\text{acc}}$  in [Table 43](#)).

When a setting between 0x00h and 0x5Dh is used, the resulting gate driver target voltage exceeds the limiting values of the IC. The limiting values of the VGG pin can also be violated with target settings of 0xA6h to 0x5Dh due to these tolerances. A violation of the limiting values with the actual VGG voltage must be avoided. To ensure that only allowed settings are used for the gate driver target voltage, an immediate read back of the programmed value is required after setting the registers.

If a setting between 0xFFh and 0xB7h is used, the device may not start up VGG. If the device operates, parameters of VGG are not guaranteed.

### 8.7.1 Gate voltage supply diagnostics

The diagnostic options for the gate voltage supply are:

- gate driver available. Details can be found in [Section 8.10](#)
- gate driver protection active. Details can be found in [Section 8.10](#)

## 8.8 Supply voltage monitoring

When at least one of the outputs is enabled and bit VGG\_ok is set, the ASL4500SHN continuously measures the voltage at pin VBAT. It allows the system to monitor the supply voltage without additional external components. It also offers the option to put an automatic undervoltage or overvoltage protection in place.

Note: The VIN\_UV and VIN\_OV bits in the status register use the battery voltage measurement. As a result, the VIN\_UV and VIN\_OV bits are only reliable when at least one output is enabled.

### 8.8.1 Battery voltage measurement

The ASL4500SHN continuously measures the voltage at pin VBAT. The measurement result is available in the battery voltage register when at least one output is enabled.

Table 29. Battery voltage register (address 0x045h)

| Bit | Symbol      | Description     | Value | Function   |
|-----|-------------|-----------------|-------|--|
| 7:0 | V_VBAT[7:0] | battery voltage | 0x00h | battery voltage = 0 V  |
|     |             |                 | ...   | battery voltage =<br>$0.3555 * V\_VBAT [7:0] * (1 + 333e-6 * (T\_junction[7:0] - 38))$ |
|     |             |                 | 0xFFh | maximum measurable battery voltage = 90 V  |

### 8.8.2 Undervoltage detection

The ASL4500SHN offers a variable undervoltage detection threshold. When the supply voltage drops below this threshold, the undervoltage detect bit is set, and Fail silent mode is entered. All gate pins stop toggling and power is no longer delivered to the output.

Table 30. Undervoltage threshold register (address 0x01Bh)

| Bit | Symbol        | Description                      | Value | Function  |
|-----|---------------|----------------------------------|-------|---|
| 7:0 | V_VIN_UV[7:0] | undervoltage detection threshold | 0x00h | undervoltage detection threshold = 0 V  |
|     |               |                                  | ...   | under voltage detection threshold =<br>$0.3555 * V\_VIN\_UV [7:0] * (1 + 333e-6 * (T\_junction[7:0] - 38))$ |
|     |               |                                  | 0xFFh | maximum under voltage detection threshold = 90 V  |

### 8.8.3 Overvoltage detection

The ASL4500SHN offers a variable overvoltage detection threshold. When the supply voltage rises above this threshold, the overvoltage detect bit is set, and Fail silent mode is entered. All gate pins stop toggling and power is no longer delivered to the output.

Table 31. Overvoltage threshold register (address 0x01Ah)

| Bit | Symbol        | Description                     | Value | Function  |
|-----|---------------|---------------------------------|-------|---|
| 7:0 | V_VIN_OV[7:0] | overvoltage detection threshold | 0x00h | overvoltage detection threshold = 0 V   |
|     |               |                                 | ...   | overvoltage detection threshold =<br>$0.3555 * V\_VIN\_OV [7:0] * (1 + 333e-6 * (T\_junction[7:0] - 38))$ |
|     |               |                                 | 0xFFh | maximum overvoltage detection threshold = 90 V  |

## 8.9 Junction temperature information

The ASL4500SHN provides a measurement of the IC junction temperature. The measurement information is available in the junction temperature register.

Table 32. Junction temperature register (address 0x046h)

| Bit | Symbol           | Description          | Value | Function  |
|-----|------------------|----------------------|-------|---|
| 7:0 | T_junction [7:0] | junction temperature | ...   | device junction temperature below $-40\text{ }^{\circ}\text{C}$   |
|     |                  |                      | 0x18h | device junction temperature = $-40\text{ }^{\circ}\text{C}$   |
|     |                  |                      | ...   | device junction temperature = $T\_junction[7:0] * (215/106)\text{ }^{\circ}\text{C} - 88\text{ }^{\circ}\text{C}$ |
|     |                  |                      | 0x82h | device junction temperature = $175\text{ }^{\circ}\text{C}$   |
|     |                  |                      | 0x82h | device junction temperature above $175\text{ }^{\circ}\text{C}$   |

## 8.10 Diagnostic information

The diagnostic register contains useful information for diagnostic purposes. Details for each bit can be found in the following subchapters.

**Table 33. Diagnostic register (address 0x05Fh)**

| Bit | Symbol   | Description                    | Value | Function   |
|-----|----------|--------------------------------|-------|--|
| 7   | Vout1_ok | Vout1 regulated                | 0     | Vout1 is deviating from the target value                     |
|     |          |                                | 1     | Vout1 is regulated to the target value                       |
| 6   | Vout2_ok | Vout2 regulated                | 0     | Vout2 is deviating from the target value                     |
|     |          |                                | 1     | Vout2 is regulated to the target value                       |
| 5   | VGG_ok   | gate driver regulation is ok   | 0     | gate driver is not available                                 |
|     |          |                                | 1     | gate driver is available                                     |
| 4   | Tj_err   | device temperature is too high | 0     | device temperature below $T_{sd(otp)}$                       |
|     |          |                                | 1     | device temperature above $T_{sd(otp)}$                       |
| 3   | VIN_UV   | VIN under voltage              | 0     | under voltage not detected at VIN                            |
|     |          |                                | 1     | under voltage detected at VIN                                |
| 2   | VIN_OV   | VIN over voltage               | 0     | over voltage not detected at VIN                             |
|     |          |                                | 1     | over voltage detected at VIN                                 |
| 1   | SPI_err  | SPI error                      | 0     | last SPI command was executed correctly                      |
|     |          |                                | 1     | last SPI command was erroneous and has been discarded        |
| 0   | VGG_err  | VGG error                      | 0     | VGG overload protection not active                           |
|     |          |                                | 1     | VGG overload protection has turned on and VGG is deactivated |

### 8.10.1 Bit VIN\_OV

The bit VIN\_OV depends on the battery monitoring functionality as described in [Section 8.8](#). It indicates that the device has detected an overvoltage condition and entered the Fail silent mode. A write access to the diagnostic register, or once the Off mode is entered, clears the bit. The device stays in Fail silent mode irrespective of the clearing of the bit.

### 8.10.2 Bit VIN\_UV

The bit VIN\_UV depends on the battery monitoring functionality as described in [Section 8.8](#). It indicates that the device has detected an undervoltage condition and entered the Fail silent mode. A write access to the diagnostic register, or once the Off mode is entered, clears the bit. The device stays in Fail silent mode irrespective of the clearing of the bit.

### 8.10.3 Bit SPI\_err

The device evaluates all SPI accesses to the device for the correctness of the commands. When the command is not allowed, the SPI\_err bit is set. A write access to the diagnostic register, or once Off mode has been entered, clears the bit.

#### 8.10.4 Bit Tj\_err

The bit Tj\_err indicates that the junction temperature has exceeded the maximum allowable temperature, and the device has entered Fail silent mode. A write access to the diagnostic register, or once Off mode has been entered, clears the bit. The device stays in Fail silent mode irrespective of the clearing of the bit. After leaving the OFF mode (at IC start-up), it is possible that bit Tj\_err is set. To avoid wrong diagnostics, clear the diagnostic register before it is evaluated.

#### 8.10.5 Bit VGG\_err

Bit VGG\_err is set when the gate driver does not reach the VGG\_ok\_window (when  $V_{VGG}$  is within range) within the regulator voltage start-up error time. Once bit VGG\_err is set, it indicates that an error on the gate driver has been detected and the device has entered Fail silent mode. A write access to the diagnostic register, or once Off mode has been entered, clears the bit. The device stays in Fail silent mode irrespective of the clearing of the bit.

#### 8.10.6 Bit VGG\_ok

The bit VGG\_ok indicates that the gate driver is regulated to the target voltage and allows the gate drivers to drive the gate driver pins. If the gate driver is outside the VGG\_ok window after  $t_{startup}$ , and  $V_{VGG}$  is within range, the device clears VGG\_ok bit and enters Fail silent mode.

#### 8.10.7 Bits Vout1\_ok and Vout2\_ok

The bits Vout1\_ok and Vout2\_ok indicate whether the output voltage is regulated to the target value or deviating from the target value. The bits are set as soon as the corresponding output is within the Vout\_ok window (when  $V_O$  is within the range) for more than  $t_{ftr(ov)}$ . The bits are cleared when the corresponding output is outside the Vout\_ok window for more than  $t_{ftr(ov)}$ .

### 8.11 Serial Peripheral Interface (SPI)

The ASL4500SHN uses an SPI interface to communicate with an external microcontroller. The SPI interface can be used for setting the LEDs current, reading and writing the control register.

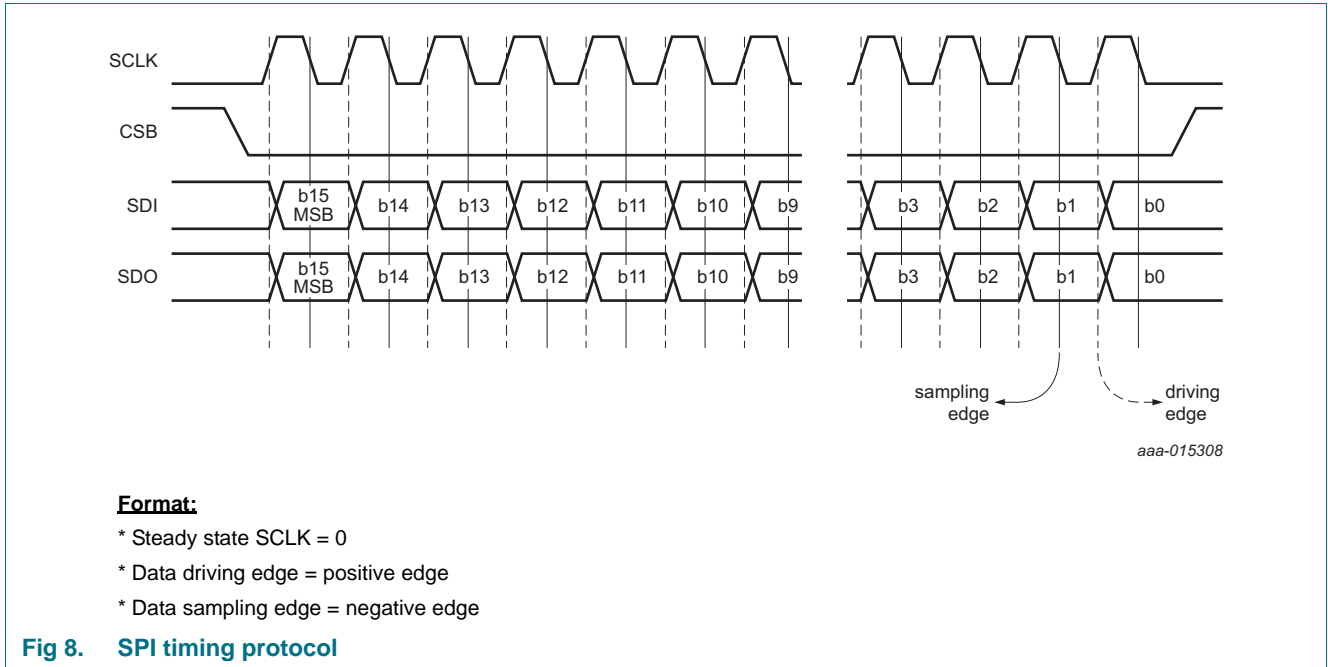
#### 8.11.1 SPI introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing the application to read back the registers without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

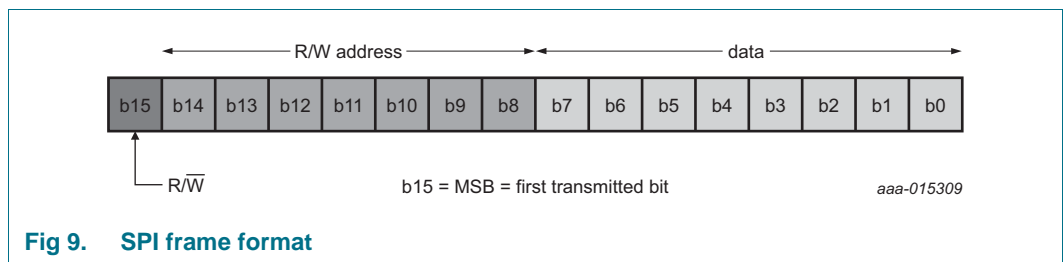
- CSB - SPI chip select; active LOW
- SCLK - SPI clock - default level is LOW due to low-power concept
- SDI - SPI data input
- SDO - SPI data output - floating when pin CSB is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge as illustrated in [Figure 8](#).



The data bits of the ASL4500SHN are arranged in registers of one-byte length. Each register is assigned to a 7-bit address. For writing into a register, 2 bytes must be sent to the LED driver. The first byte is an identifier byte that consists of the 7-bit address and one read-only bit. For writing, the read-only bit must be set to 0. The second byte is the data that is written into the register, so an SPI access consists of at least 16 bits.

The SPI frame format is shown in [Figure 9](#), [Table 34](#) and [Table 35](#).



**Table 34. SPI frame format for a transition to the device**

| Bit  | Symbol | Description  | Value | Function                 |
|------|--------|--------------|-------|--------------------------|
| 15   | b15    | R/W bit      | 0     | write access             |
|      |        |              | 1     | read access              |
| 14:8 | b14:8  | address bits | ...   | address that is selected |
| 7:0  | b7:0   | data bits    | ...   | data that is transmitted |

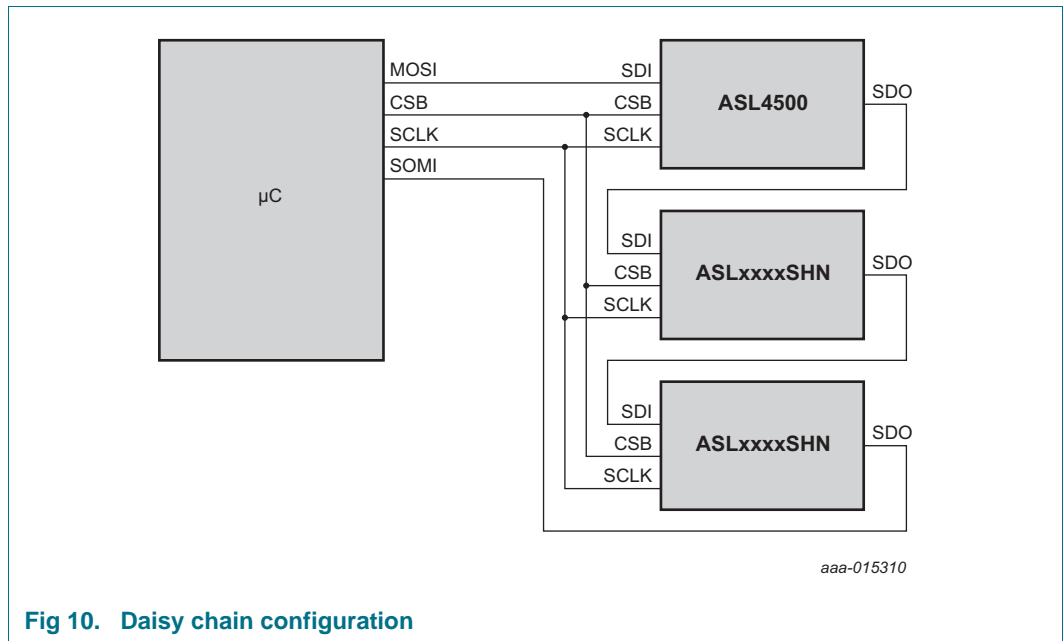
**Table 35. SPI frame format for a transition from the device**

| Bit  | Symbol | Description         | Value | Function <sup>[1]</sup>  |
|------|--------|---------------------|-------|--|
| 8:15 | b8:15  | diagnostic register | ...   | content of diagnostic register   |
| 7:0  | b7:0   | data bits           | ...   | when previous command was a valid read command, content of the register that is supposed to be read          |
|      |        |                     | ...   | when previous command was a valid write command, new content of the register that was supposed to be written |

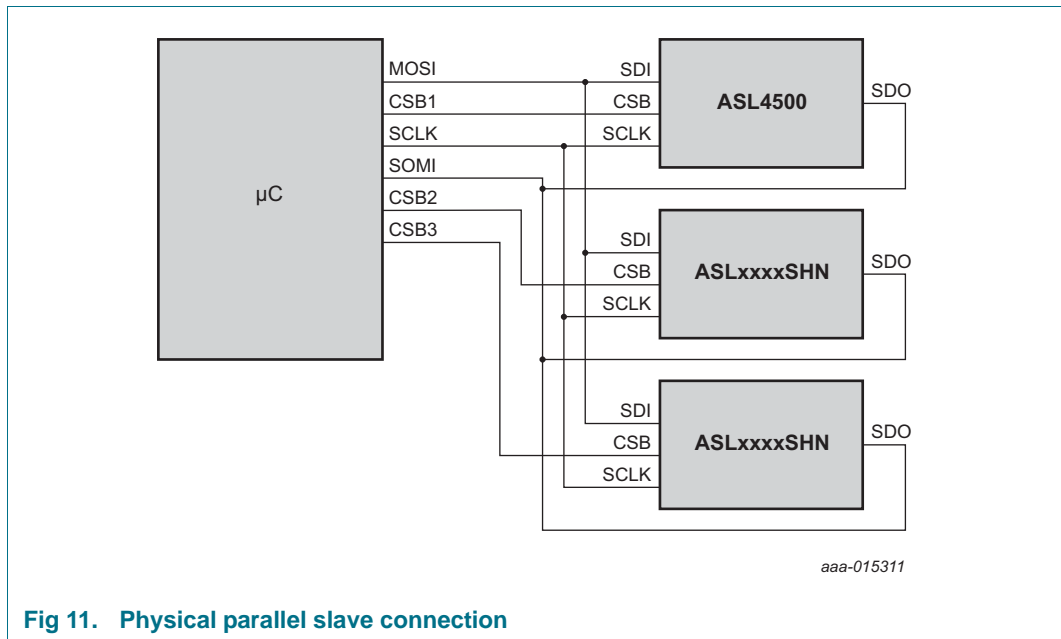
[1] The first SPI command after leaving the Off mode, will return 0x00h.

The Master initiates the command sequence. The sequence begins with CSB pin pulled low and lasts until it is asserted high.

The ASL4500SHN also tolerates SPI accesses with a multiple of 16 bits. It allows a daisy chain configuration of the SPI.



**Fig 10. Daisy chain configuration**



**Fig 11. Physical parallel slave connection**

During the SPI data transfer, the identifier byte and the actual content of the addressed registers is returned via the SDO pin. The same happens for pure read accesses. Here the read-only bit must be set on logic 1. The content of the data bytes that are transmitted to the ASL4500SHN is ignored.

The ASL4500SHN monitors the number of data bits that are transmitted. If the number is not 16, or a multiple of 16, then a write access is ignored and the SPI error indication bit is set.

**8.11.2 Typical use case illustration (Write/Read)**

Consider a daisy chain scheme with one master connected to 4 slaves in daisy chain fashion. The following commands are performed during one sequence (first sequence):

- Write data 0xFF to the register 0x1A Slave 1
- Read from register 0x02 of Slave 2
- Write data 0xAF to the register 0x2F of Slave 3
- Read from register 0x44 of Slave 4

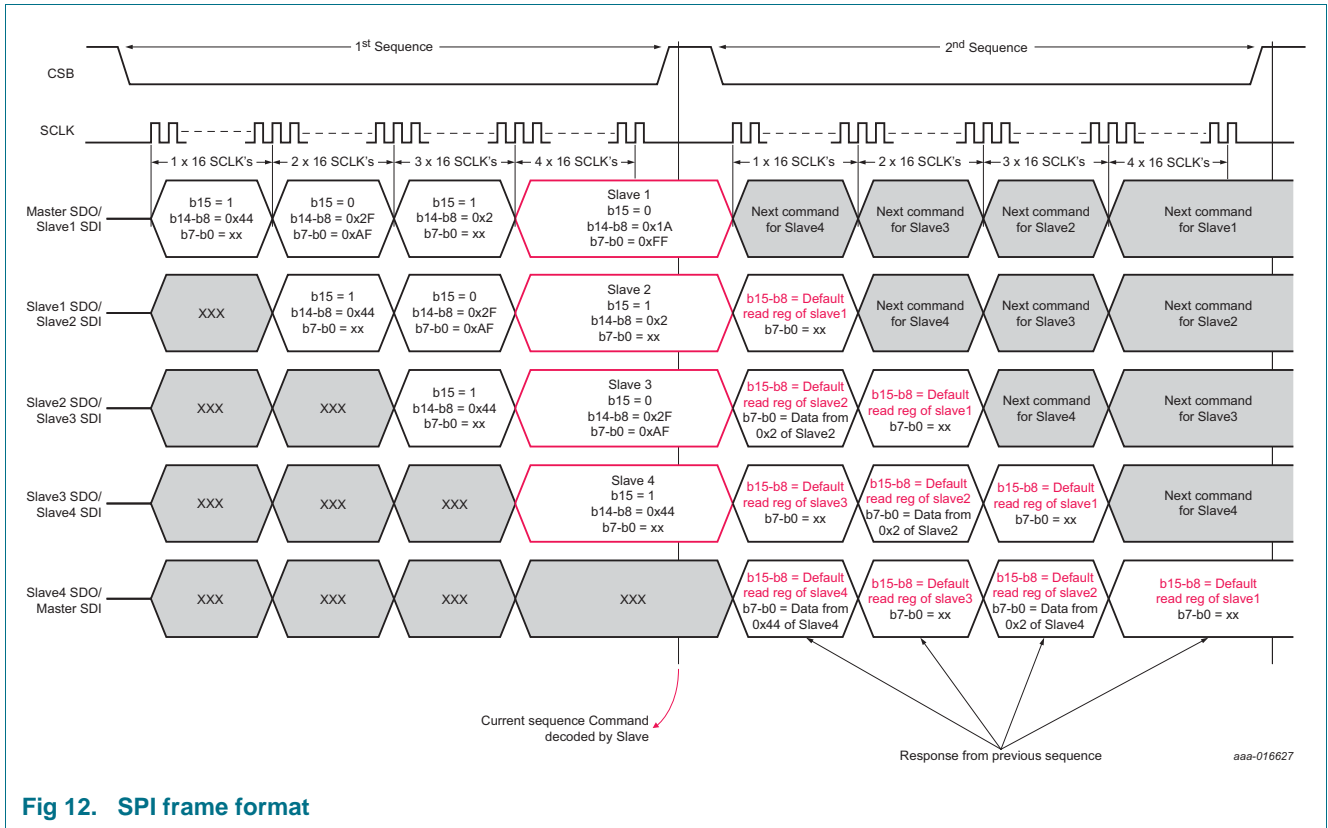


Fig 12. SPI frame format

### 8.11.3 Diagnostics for the SPI interface

The device is evaluating all SPI access to the device for the correctness of the commands. When the command is not allowed, the SPI\_err bit is set.

The conditions that are considered as erratic accesses are:

- SPI write is attempted to a read-only location or reserved location
- SPI write is attempted during operation to a configuration register
- SPI read is attempted from a reserved location
- SPI command does not consist of a multiple of 16 clock counts

If an SPI access is considered to be erratic, no modifications to a SPI register are made. The access after the erratic SPI command returns the diagnostic register and zero in the data field.

For details concerning the SPI\_err bit, see chapter [Section 8.10](#).

### 8.11.4 Register map

The addressable register space amounts to 128 registers from 0x00 to 0x7F. They are separated into 2 groups as shown in [Table 36](#). The register mapping is shown in [Table 37](#) and [Table 40](#). The functional description of each bit can be found in the dedicated chapter.

Table 36. Grouping of the register space

| Address range | Description          | Content                |
|---------------|----------------------|------------------------|
| 0x00...0x1F   | control registers    | control registers      |
| 0x20...0x7F   | diagnostic registers | diagnostic information |

8.11.4.1 Control registers

Table 37. Control register group overview

| Address | Name                        | Reset value | 7                           | 6 | 5              | 4 | 3                    | 2                      | 1                      | 0                    |
|---------|-----------------------------|-------------|-----------------------------|---|----------------|---|----------------------|------------------------|------------------------|----------------------|
| 0x00h   | function control            | 0x00h       | -                           | - | -              | - | Cnt_CSB              | Vout2en <sup>[1]</sup> | Vout1en <sup>[1]</sup> | Cfg_dn               |
| 0x01h   | gate driver enable          | 0x00h       | -                           | - | -              | - | EN_G4 <sup>[2]</sup> | EN_G3 <sup>[2]</sup>   | EN_G2 <sup>[2]</sup>   | EN_G1 <sup>[2]</sup> |
| 0x03h   | target voltage output 1     | 0x00h       | V_Vout_1[7:0]               |   |                |   |                      |                        |                        |                      |
| 0x04h   | target voltage output 2     | 0x00h       | V_Vout_2[7:0]               |   |                |   |                      |                        |                        |                      |
| 0x05h   | limit voltage output 1      | 0x00h       | Vmax_Vout_1[7:0]            |   |                |   |                      |                        |                        |                      |
| 0x06h   | limit voltage output 2      | 0x00h       | Vmax_Vout_2[7:0]            |   |                |   |                      |                        |                        |                      |
| 0x07h   | maximum phase current Vout1 | 0x46h       | I_max_per_phase_Vout_1[7:0] |   |                |   |                      |                        |                        |                      |
| 0x08h   | maximum phase current Vout2 | 0x46h       | I_max_per_phase_Vout_2[7:0] |   |                |   |                      |                        |                        |                      |
| 0x1Ch   | frequency trimming register | 0x09h       | -                           | - | Freq_trim[5:0] |   |                      |                        |                        |                      |

- [1] Bits are locked with bit Cfg\_dn is high. When bit Cfg\_dn is low, bits can be changed. Read is always possible.
- [2] Individual gate drivers that are enabled when Cfg\_dn and VGG\_ok are set high, can be turned on and off during operation of the system. Gate drivers, disabled when bits Cfg\_dn and VGG\_ok are set high, remain off, even when the gate enable bits are set high later.

8.11.4.2 Configuration registers

The configuration registers inside the control block can only be written in configuration mode. In the other modes, this register can only be read.

Table 38. Configuration register group overview

| Address | Name                                       | Reset value | 7             | 6 | 5          | 4 | 3            | 2       | 1          | 0       |
|---------|--|-------------|---------------|---|------------|---|--------------|---------|------------|---------|
| 0x02h   | gate driver output                         | 0x00h       | -             | - | -          | - | O_G4         | O_G3    | O_G2       | O_G1    |
| 0x09h   | clock divider for output 1                 | 0x0Fh       | Clkdiv1[7:0]  |   |            |   |              |         |            |         |
| 0x0Ah   | clock divider for output 2                 | 0x0Fh       | Clkdiv2[7:0]  |   |            |   |              |         |            |         |
| 0x0Bh   | internal phases output 1                   | 0x0Fh       | -             | - | -          | - | EN_P4_1      | EN_P3_1 | EN_P2_1    | EN_P1_1 |
| 0x0Ch   | internal phases output 2                   | 0x0Fh       | -             | - | -          | - | EN_P4_2      | EN_P3_2 | EN_P2_2    | EN_P1_2 |
| 0x0Dh   | phase off and delay output 1               | 0x39h       | Phdel1        |   |            |   | Phoff1       |         |            |         |
| 0x0Eh   | phase off and delay output 2               | 0x39h       | Phdel2        |   |            |   | Phoff2       |         |            |         |
| 0x0Fh   | gate driver phase                          | 0x00h       | -             | - | -          | - | O_GP4        | O_GP3   | O_GP2      | O_GP1   |
| 0x10h   | phase selection configuration              | 0xE4h       | Phsel4        |   | Phsel3     |   | Phsel2       |         | Phsel1     |         |
| 0x11h   | loop filter proportional configuration     | 0x00h       | Prop2[3:0]    |   |            |   | Prop1[3:0]   |         |            |         |
| 0x12h   | loop filter integral configuration         | 0x00h       | Integ2[3:0]   |   |            |   | Integ1[3:0]  |         |            |         |
| 0x13h   | slope compensation configuration           | 0x88h       | Slpcmp2[3:0]  |   |            |   | Slpcmp1[3:0] |         |            |         |
| 0x14h   | current sense slope resistor configuration | 0x00h       | Slpr4[1:0]    |   | Slpr3[1:0] |   | Slpr2[1:0]   |         | Slpr1[1:0] |         |
| 0x15h   | gate driver control                        | 0xFFh       | VGG[7:0]      |   |            |   |              |         |            |         |
| 0x1Ah   | overvoltage detection threshold            | 0xFFh       | V_VIN_OV[7:0] |   |            |   |              |         |            |         |
| 0x1Bh   | undervoltage detection threshold           | 0x00h       | V_VIN_UV[7:0] |   |            |   |              |         |            |         |

### 8.11.4.3 Internal registers

The ASL4500SHN uses the SPI registers to control some internal functions. In order to avoid any unintended behavior of the device, do not modify these registers but leave them all at their default value.

**Table 39. Internal register group**

| Address | Name       | Reset value | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------------|-------------|---|---|---|---|---|---|---|---|
| 0x19h   | internal 1 | 0x82h       | - | - | - | - | - | - | - | - |
| 0x25h   | internal 2 | 0x27h       | - | - | - | - | - | - | - | - |
| 0x26h   | internal 3 | 0x3Bh       | - | - | - | - | - | - | - | - |
| 0x2Fh   | internal 4 | 0xE8h       | - | - | - | - | - | - | - | - |
| 0x30h   | internal 5 | 0x09h       | - | - | - | - | - | - | - | - |

### 8.11.4.4 Diagnostic registers

The ASL4500SHN provides diagnostic data via some SPI registers. These registers are read only, but error bits can be cleared via a write access to the register.

**Table 40. Diagnostic register group overview**

| Address | Name                 | 7               | 6        | 5      | 4      | 3      | 2      | 1       | 0       |  |
|---------|----------------------|-----------------|----------|--------|--------|--------|--------|---------|---------|--|
| 0x41h   | CSB count low        | CSB_cnt[7:0]    |          |        |        |        |        |         |         |  |
| 0x42h   | CSB count high       | CSB_cnt[15:8]   |          |        |        |        |        |         |         |  |
| 0x45h   | battery voltage      | V_VBAT[7:0]     |          |        |        |        |        |         |         |  |
| 0x46h   | junction temperature | T_junction[7:0] |          |        |        |        |        |         |         |  |
| 0x5Fh   | diagnostic register  | Vout1_ok        | Vout2_ok | VGG_ok | Tj_err | VIN_UV | VIN_OV | SPI_err | VGG_err |  |

## 9. Limiting values

**Table 41. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol              | Parameter                         | Conditions  | Min  | Max  | Unit |
|---------------------|-----------------------------------|---|------|------|------|
| V <sub>BAT</sub>    | battery supply voltage            | EN = low  | -0.3 | +60  | V    |
|                     |                                   | EN = high   | -0.3 | +40  | V    |
| V <sub>VCC</sub>    | voltage on pin VCC                |   | -0.3 | +5.5 | V    |
| V <sub>GND</sub>    | ground supply voltage             | voltage between ground pins   | -0.6 | +0.6 | V    |
| V <sub>FBx</sub>    | voltage on feedback pins          | FB1 and FB2   | -0.3 | +90  | V    |
| V <sub>O</sub>      | output voltage                    | programmed target voltage according to registers 0x03h and 0x04h        | 10   | 80   | V    |
| V <sub>I(dig)</sub> | digital input voltage             | voltage on digital pins SDO, SDI, CSB, SCLK and EN                      | -0.3 | +5.5 | V    |
| V <sub>VGG</sub>    | voltage on pin VGG <sup>[1]</sup> | VGG1 <sup>[2]</sup>   | -0.3 | +10  | V    |
|                     |                                   | VGG2 <sup>[2]</sup>   | -0.3 | +10  | V    |
| V <sub>sense</sub>  | sense voltage                     | voltage on sense pins SNH1, SNH2, SNH3, SNH4, SNL1, SNL2, SNL3 and SNL4 | -0.3 | +1.8 | V    |
| V <sub>Gx</sub>     | voltage on gate pins              | voltage on gate pins G1, G2, G3 and G4                                  | -0.3 | +10  | V    |
| T <sub>j</sub>      | junction temperature              |   | -40  | +175 | °C   |
| T <sub>stg</sub>    | storage temperature               |   | -55  | +175 | °C   |
| V <sub>ESD</sub>    | electrostatic discharge voltage   | HBM <sup>[3]</sup>  |      |      |      |
|                     |                                   | at any pin  | -2   | +2   | kV   |
|                     |                                   | at pin VBAT with 100 nF at pin  | -6   | +6   | kV   |
|                     |                                   | CDM <sup>[4]</sup>  |      |      |      |
|                     |                                   | at any pin  | -500 | +500 | V    |

[1] VGG refers to both VGG1 and VGG2.

[2] VGG1 and VGG2 are IC internally connected (shorted).

[3] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ)

[4] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF).

## 10. Thermal characteristics

**Table 42. Thermal characteristics**

| Symbol               | Parameter                | Conditions                           | Typ | Unit |
|----------------------|--------------------------|--------------------------------------|-----|------|
| R <sub>th(tot)</sub> | total thermal resistance | HVQFN32 package JEDEC <sup>[1]</sup> | 37  | K/W  |

[1] In accordance with JEDEC, JESD51-2, JESD51-5 and JESD51-7 with natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array, under the exposed pad connected to the first inner copper layer.

## 11. Static characteristics

**Table 43. Static characteristics**

Min and Max values are specified for the following conditions:  $V_{BAT} = 5.5\text{ V to }40\text{ V}$ ,  $V_{EN} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{VCC} = 4.5\text{ V to }5.5\text{ V}$  and  $T_j = -40\text{ °C to }+175\text{ °C}$ [1]. All voltages are defined with respect to ground, positive currents flow into the IC. Typical values are given at  $V_{VIN} = 40\text{ V}$ ,  $V_{EN} = 5\text{ V}$ ,  $V_{VCC} = 5\text{ V}$  and  $T_j = 25\text{ °C}$  unless otherwise specified.

| Symbol  | Parameter                                 | Conditions  | Min                   | Typ | Max                   | Unit |
|---|---|---|-----------------------|-----|-----------------------|------|
| <b>Supply pin Vbat</b>  |   |   |                       |     |                       |      |
| I <sub>DD</sub>   | supply current                            | Operating; no load on VGG; Gate pins low; one phase; one output                                 | 5                     | 13  | -                     | mA   |
|   |   | Operating; no load on VGG; Gate pins low; four phases, two outputs                              | -                     | 20  | -                     | mA   |
| I <sub>off</sub>  | off-state current                         | EN = low  | -                     | -   | 5                     | μA   |
| V <sub>th(det)pon</sub>   | power-on detection threshold voltage      |   | -                     | -   | 4.5                   | V    |
| <b>Supply pin VCC</b>   |   |   |                       |     |                       |      |
| I <sub>VCC</sub>  | supply current on pin VCC                 | EN = high; CSB = low  | -                     | -   | 250                   | μA   |
| <b>Pin EN</b>   |   |   |                       |     |                       |      |
| I <sub>EN</sub>   | current on pin EN                         | EN = high   | -                     | -   | 2                     | mA   |
| <b>Output voltage</b>   |   |   |                       |     |                       |      |
| V <sub>O(acc)</sub>   | output voltage accuracy                   | Vout1: operating accuracy 1   | -0.03 × Vout1 - 0.711 | -   | +0.03 × Vout1 + 0.711 | V    |
|   |   | Vout2: operating accuracy 2   | -0.03 × Vout2 - 0.711 | -   | +0.03 × Vout2 + 0.711 | V    |
| V <sub>O</sub>  | output voltage                            | bit Vout1_ok/Vout2_ok is set when V <sub>O</sub> is within the range regarding the target value | -5.4                  | -   | +2.4                  | V    |
| <b>Regulated voltage output</b>                                   |   |   |                       |     |                       |      |
| V <sub>VGG</sub>  | voltage on pin VGG[2]                     | $V_{BAT} \geq V_{VGG} + V_{do(reg)VGG}$   | 4.46                  | -   | 10.04                 | V    |
|   |   | bit VGG_ok is set when V <sub>VGG</sub> is within the range regarding the target value          | -2.4                  | -   | +2.4                  | V    |
| V <sub>do(reg)VGG</sub>   | regulator dropout voltage on pin VGG      | I <sub>VGG</sub> ≤ 50 mA; regulator in saturation   | -                     | 0.5 | 1.0                   | V    |
|   |   | I <sub>VGG</sub> ≤ 160 mA; regulator in saturation  | -                     | 1.6 | 3.2                   | V    |
| V <sub>reg(acc)VGG</sub>  | regulator voltage accuracy on pin VGG     | 25 °C to T <sub>j(max)</sub>  | -5                    | -   | +5                    | %    |
|   |   | -40 °C to +25 °C  | -7                    | -   | +5                    | %    |
| <b>Serial peripheral interface inputs; pins SDI, SCLK and CSB</b> |   |   |                       |     |                       |      |
| V <sub>th(sw)</sub>   | switching threshold voltage               |   | 0.3V <sub>CC</sub>    | -   | 0.7V <sub>CC</sub>    | V    |
| R <sub>pd(int)SCLK</sub>  | internal pull-down resistance on pin SCLK |   | 40                    | -   | 80                    | kΩ   |
| R <sub>pd(int)CSB</sub>   | internal pull-down resistance on pin CSB  |   | 40                    | -   | 80                    | kΩ   |
| R <sub>pd(int)SDI</sub>   | internal pull-down resistance on pin SDI  |   | 40                    | -   | 80                    | kΩ   |

**Table 43. Static characteristics ...continued**

Min and Max values are specified for the following conditions:  $V_{BAT} = 5.5\text{ V to }40\text{ V}$ ,  $V_{EN} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{VCC} = 4.5\text{ V to }5.5\text{ V}$  and  $T_j = -40\text{ }^\circ\text{C to }+175\text{ }^\circ\text{C}$ [1]. All voltages are defined with respect to ground, positive currents flow into the IC. Typical values are given at  $V_{VIN} = 40\text{ V}$ ,  $V_{EN} = 5\text{ V}$ ,  $V_{VCC} = 5\text{ V}$  and  $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

| Symbol  | Parameter                                       | Conditions   | Min                                   | Typ | Max                                   | Unit             |
|---|---|--|---------------------------------------|-----|---------------------------------------|------------------|
| <b>Serial peripheral interface data output; pin SDO</b> |   |  |                                       |     |                                       |                  |
| $V_{OH}$  | HIGH-level output voltage                       | $I_{OH} = -4\text{ mA}$ ; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$                              | $V_{CC} - 0.4$                        | -   | -                                     | V                |
| $V_{OL}$  | LOW-level output voltage                        | $I_{OL} = -4\text{ mA}$ ; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$                              | -                                     | -   | 0.4                                   | V                |
| $I_{LOZ}$   | OFF-state output leakage current                | $V_{CSB} = V_{CC}$ ; $V_O = 0\text{ V to }V_{CC}$ ;<br>$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | -5                                    | -   | +5                                    | $\mu\text{A}$    |
| <b>Temperature protection</b>                           |   |  |                                       |     |                                       |                  |
| $\Delta T_j$  | junction temperature variation                  | measurement provided via register 0x46h; $T_j = 130\text{ }^\circ\text{C}$                     | -20                                   | -   | +20                                   | $^\circ\text{C}$ |
| $T_{sd(otp)}$   | overtemperature protection shutdown temperature |  | 150                                   | 175 | 200                                   | $^\circ\text{C}$ |
| <b><math>V_{BAT}</math> monitoring</b>                  |   |  |                                       |     |                                       |                  |
| $\Delta V_{BAT}$  | battery voltage accuracy                        | accuracy of $V_{BAT}$ measurement  | $-0.035 \times V_{BAT}$<br>$- 0.3555$ | -   | $+0.035 \times V_{BAT}$<br>$+ 0.3555$ | %                |

- [1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.
- [2] VGG refers to both VGG1 and VGG2.

## 12. Dynamic characteristics

**Table 44. Dynamic characteristics**

Min and Max values are specified for the following conditions:  $V_{BAT} = 5.5\text{ V to }40\text{ V}$ ,  $V_{EN} = 4.5\text{ V to }5.5\text{ V}$ ,  $f_{osc} = 130\text{ MHz to }200\text{ MHz}$ ,  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , and  $T_j = -40\text{ }^\circ\text{C to }+175\text{ }^\circ\text{C}$ [1]. All voltages are defined with respect to ground. Positive currents flow into the IC. Typical values are given at  $V_{BAT} = 12\text{ V}$ ,  $V_{EN} = 5\text{ V}$ ,  $V_{CC} = 5\text{ V}$  and  $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

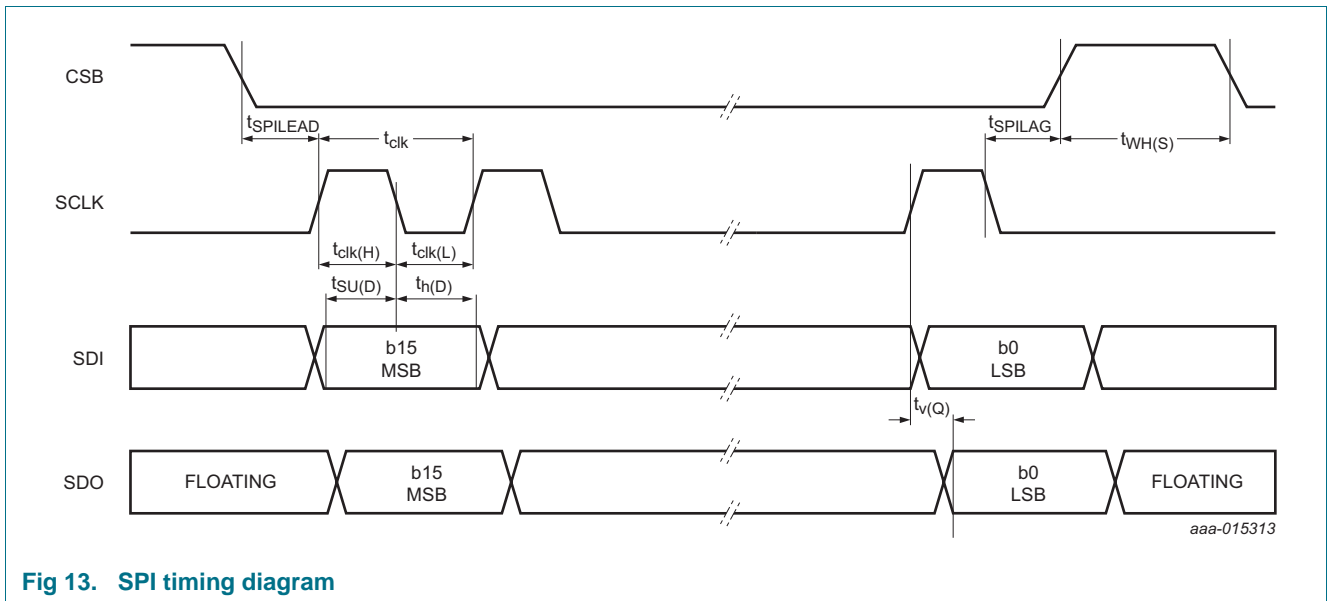
| Symbol   | Parameter   | Conditions                             | Min | Typ  | Max | Unit          |
|--|---|--|-----|------|-----|---------------|
| $f_{DCDC}$   | DC-to-DC converter frequency                          |  | 125 | -    | 700 | kHz           |
| $f_{(DCDC)acc}$  | DC-to-DC converter frequency accuracy                 | operating, trimmed                     | -5  | -    | +5  | %             |
| $f_{osc}$  | oscillator frequency                                  | internal oscillator, untrimmed         | 130 | -    | 250 | MHz           |
|  |   | target frequency for trimmed operation | -   | 180  | -   | MHz           |
| $t_{startup}$  | start-up time   | EN high until SPI is operational       | -   | -    | 150 | $\mu\text{s}$ |
| <b>Serial peripheral interface timing; pins CSB, SCLK, SDI and SDO</b> |   |  |     |      |     |               |
| $f_{clk(int)}/f_{SPI}$   | Internal clock frequency to SPI clock frequency ratio |  | -   | 20:1 | -   | 1             |
| $t_{cy}(clk)$  | clock cycle time                                      |  | 250 | -    | -   | ns            |
| $t_{SPILEAD}$  | SPI enable lead time                                  |  | 50  | -    | -   | ns            |
| $t_{SPILAG}$   | SPI enable lag time                                   |  | 50  | -    | -   | ns            |
| $t_{clk(H)}$   | clock HIGH time                                       |  | 125 | -    | -   | ns            |
| $t_{clk(L)}$   | clock LOW time  |  | 125 | -    | -   | ns            |
| $t_{su(D)}$  | data input set-up time                                |  | 50  | -    | -   | ns            |
| $t_{h(D)}$   | data input hold time                                  |  | 50  | -    | -   | ns            |
| $t_{v(Q)}$   | data output valid time                                | pin SDO; $C_L = 20\text{ pF}$          | -   | -    | 130 | ns            |

**Table 44. Dynamic characteristics ...continued**

Min and Max values are specified for the following conditions:  $V_{BAT} = 5.5\text{ V to }40\text{ V}$ ,  $V_{EN} = 4.5\text{ V to }5.5\text{ V}$ ,  $f_{osc} = 130\text{ MHz to }200\text{ MHz}$ ,  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , and  $T_j = -40\text{ }^\circ\text{C to }+175\text{ }^\circ\text{C}$ [1]. All voltages are defined with respect to ground. Positive currents flow into the IC. Typical values are given at  $V_{BAT} = 12\text{ V}$ ,  $V_{EN} = 5\text{ V}$ ,  $V_{CC} = 5\text{ V}$  and  $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

| Symbol                   | Parameter                    | Conditions  | Min | Typ  | Max | Unit          |
|--------------------------|------------------------------|---|-----|------|-----|---------------|
| $t_{WH(S)}$              | chip select pulse width HIGH |   | 250 | -    | -   | ns            |
| <b>Gate driver</b>       |                              |   |     |      |     |               |
| $t_{ch(g)}$              | gate charge time             | 20 % to 80 %; $V_{GG} = 7.5\text{ V}$ ; $C_{gate} = 2000\text{ pF}$ | -   | -    | 30  | ns            |
| $t_{dch(g)}$             | gate discharge time          | 80 % to 20 %; $V_{GG} = 7.5\text{ V}$ ; $C_{gate} = 2000\text{ pF}$ | -   | -    | 14  | ns            |
| <b>Regulated voltage</b> |                              |   |     |      |     |               |
| $t_{err(startup)}$       | start-up error time          | of VGG; $f_{osc} = 180\text{ MHz}$                                  | -   | 2.5  | -   | ms            |
| $t_{err}$                | error detection time         | for VGG during operation;<br>$f_{osc} = 180\text{ MHz}$             | -   | 31.5 | -   | $\mu\text{s}$ |
| $t_{ftr(ov)}$            | output voltage filter time   | for bit Vout1_ok and Vout2_ok;<br>$f_{osc} = 180\text{ MHz}$        | -   | 31.5 | -   | $\mu\text{s}$ |

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.



**Fig 13. SPI timing diagram**

### 13. Application information

Figure 14 provides an application example for the ASL4500SHN in a typical four-phase boost converter IC with 1 output voltage.

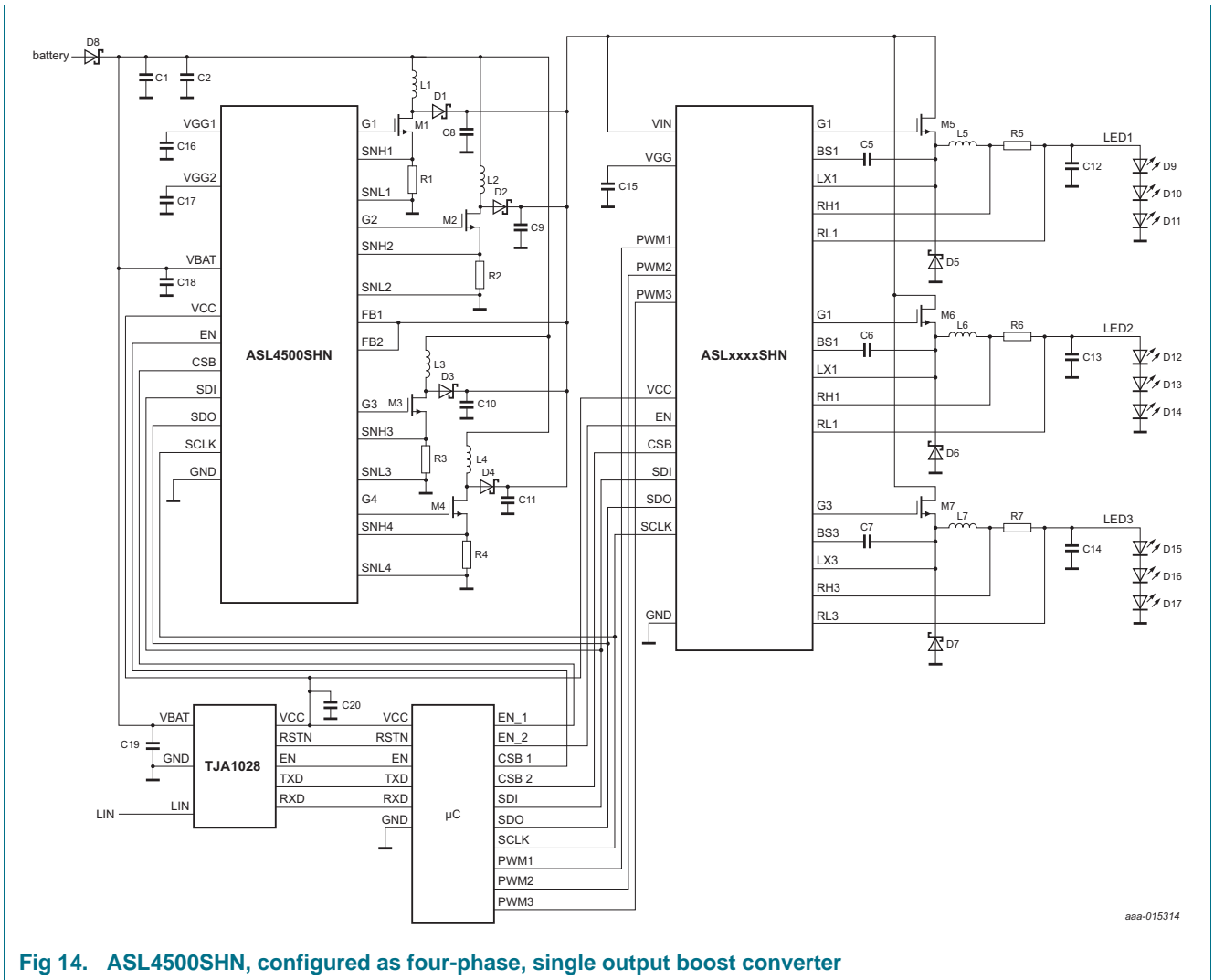


Fig 14. ASL4500SHN, configured as four-phase, single output boost converter

aaa-015314

## 14. Test information

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### 14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - *Failure mechanism-based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

SOT617-12

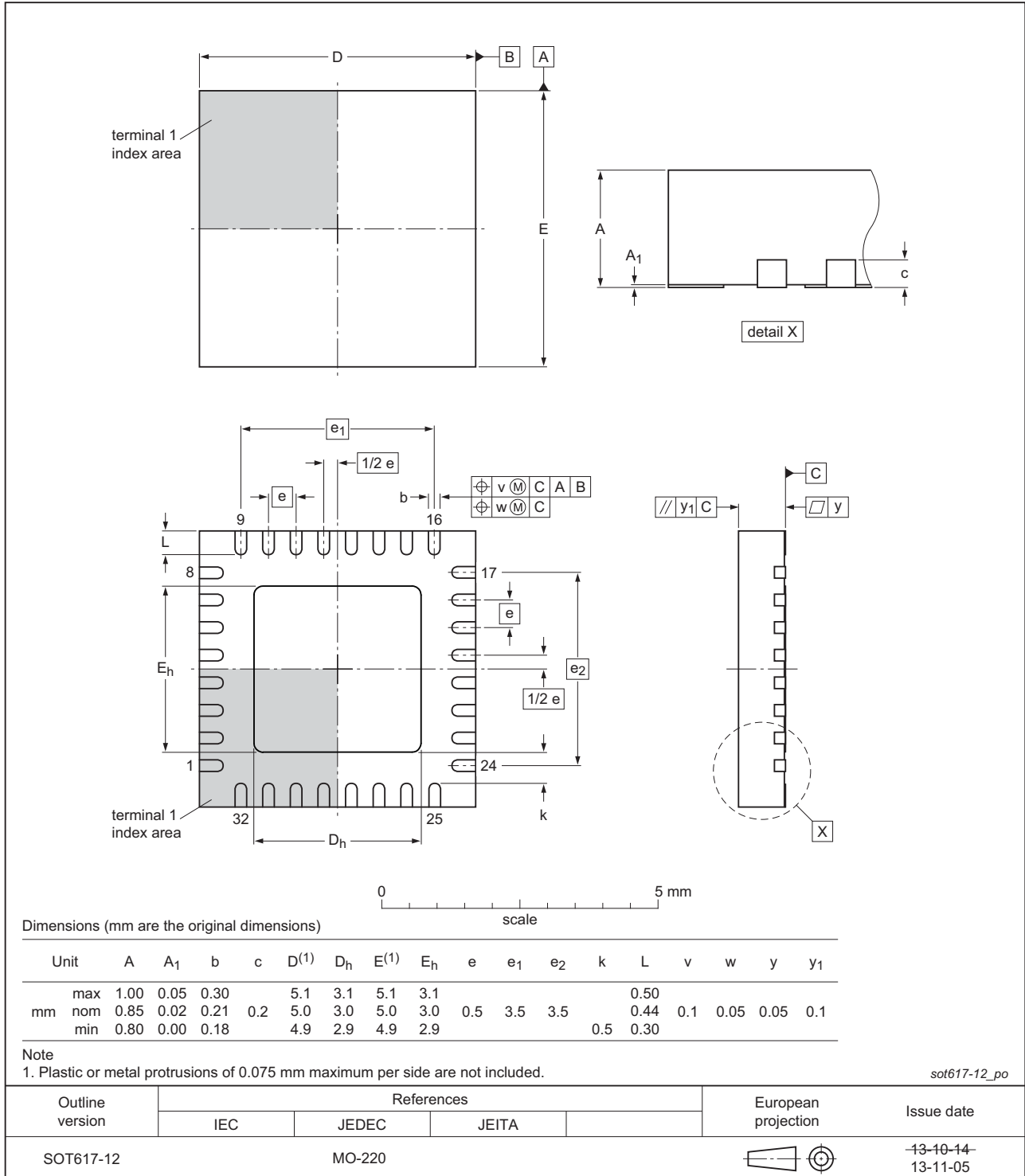


Fig 15. Package outline HVQFN32

## 16. Revision history

Table 45. Revision history

| Document ID    | Release date  | Data sheet status      | Change notice | Supersedes     |
|----------------|---|------------------------|---------------|----------------|
| ASL4500SHN v.6 | 20171026  | Product data sheet     | -             | ASL4500SHN v.5 |
| Modifications: | <ul style="list-style-type: none"> <li>• <a href="#">Section 8.7</a>: clarified exceeding of limiting values</li> <li>• Formula for voltage conversion updated</li> <li>• <a href="#">Table 43</a>: values of output voltage accuracy updated</li> <li>• <a href="#">Table 43</a>: values of regulator voltage accuracy on pin VGG updated</li> <li>• <a href="#">Table 44</a>: data output valid time updated</li> </ul> |                        |               |                |
| ASL4500SHN v.5 | 20160404  | Product data sheet     | -             | ASL4500SHN v.4 |
| Modifications: | <ul style="list-style-type: none"> <li>• Title and address of <a href="#">Table 24</a> corrected</li> </ul>   |                        |               |                |
| ASL4500SHN v.4 | 20160321  | Product data sheet     | -             | ASL4500SHN v.3 |
| Modifications: | <ul style="list-style-type: none"> <li>• Minor corrections made to Figure 3.</li> <li>• Text corrections made in accordance with the corrections to Figure 3.</li> <li>• New symbol added to Table 44.</li> </ul>   |                        |               |                |
| ASL4500SHN v.3 | 20150925  | Product data sheet     | -             | ASL4500SHN v.2 |
| Modifications: | <ul style="list-style-type: none"> <li>• Minor corrections made to Figure 1, Figure 3, Figure 6, Figure 7, Figure 10, Figure 11 and Figure 14.</li> <li>• Phase off and delay output 1 and output 2, bits reassigned in Table 38.</li> <li>• A number of symbols have been upgraded to NXP standards.</li> </ul>  |                        |               |                |
| ASL4500SHN v.2 | 20150305  | Preliminary data sheet | -             | ASL4500SHN v.1 |
| ASL4500SHN v.1 | 20150225  | Preliminary data sheet | -             | -              |

## 17. Legal information

### 17.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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