



**THE DATASHEET OF  
STP08CDC596M**





# STP08CDC596

## 8-Bit constant current Led sink driver with full outputs detection

### General features

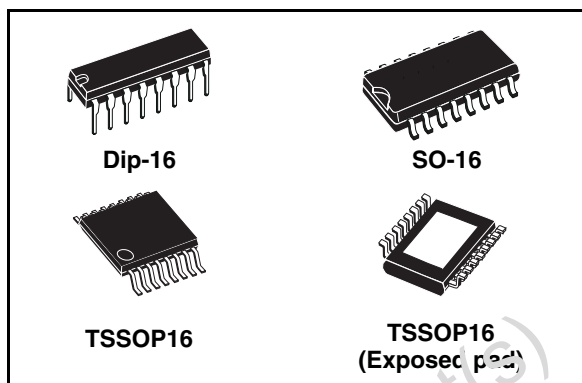
- 8 constant current output channels
- Adjustable output current through one external resistor
- Open and short line, short to GND, short to V-LED supply error detection
- Serial data in/parallel data out
- Serial out change state on the falling edges of clock
- Output current: 20-120mA
- 3.3V micro driver-able
- 25MHz clock frequency
- Available in high thermal TSSOP exposed pad.

### Description

The STP08CDC596 is a monolithic, medium-voltage, low current power 8-bit shift register designed for LED panel display. The STP08CDC596 contains a 8-bit serial-in, parallel-out shift register that feeds a 8-bit D-type storage register. In the output stage, eight regulated current sources were designed to provide 15-120mA constant current to drive the LEDs. The STP08CDC596 contains the built-IN error detection feature. The device performs this additional function without any increase of the pin number and any change of the pin function, if compared to the standard device without error detection. Consequently, choosing this device does not mean to change the footprint on the board.

### Order codes

Part Number	Temperature range	Package	Packaging
STP08CDC596B1	-40°C to 125°C	DIP-16	25 part per tube
STP08CDC596M	-40°C to 125°C	SO-16 (Tube)	50 parts per tube
STP08CDC596MTR	-40°C to 125°C	SO-16 (Tape & Reel)	2500 parts per reel
STP08CDC596TTR	-40°C to 125°C	TSSOP16 (Tape & Reel)	2500 parts per reel
STP08CDC596XTTR	-40°C to 125°C	TSSOP16 Exposed pad (Tape & Reel)	2500 parts per reel



To perform this functionality mode, the device needs a digital key coming from the Microprocessor. The STP08CDC596 is able to detect: open and short on the LED line, short to GND, short to LED voltage supply. The data mapping of output channels status detection is provided by a feedback from the serial output to the Microprocessor.

Through an external resistor, users may adjust the STP08CDC596 output current, controlling the light intensity of LEDs.

The STP08CDC596 guarantees 16V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 25 MHz, also satisfies the system requirement of high volume data transmission.

The device is offered in DIP-16, SO-16, TSSOP-16 and TSSOP-16 Exposed Pad packages.

The STP08CDC596 is well suitable for traffic display signs where the detection feature is strongly required.

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# 1 Summary description

Table 1. Current accuracy

Output voltage	Current accuracy		Output current
	Between bits	Between ICs	
≥0.7V	(Typ) ±3%	±10%	20 to 120mA

## 1.1 Pin connection and description

Figure 1. Connections diagram

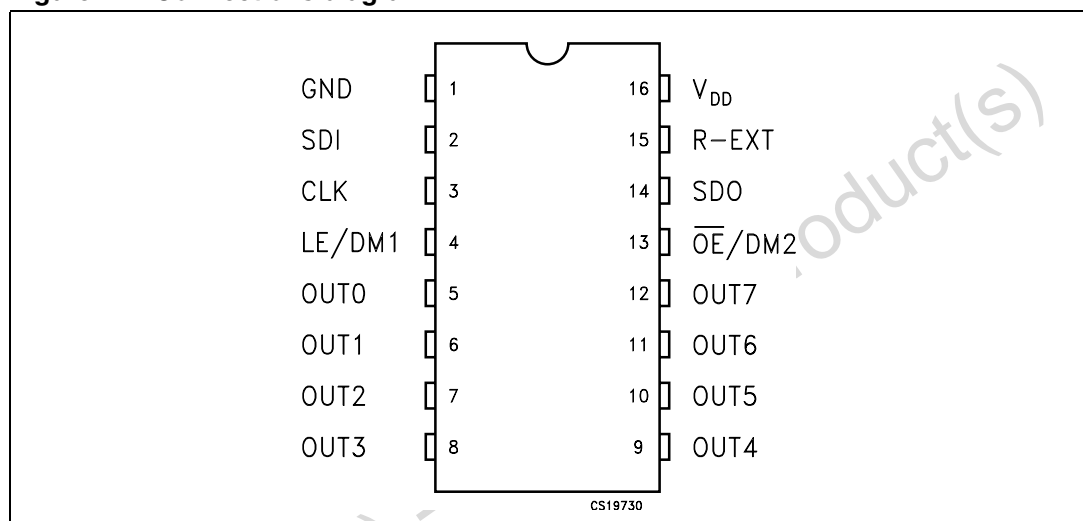
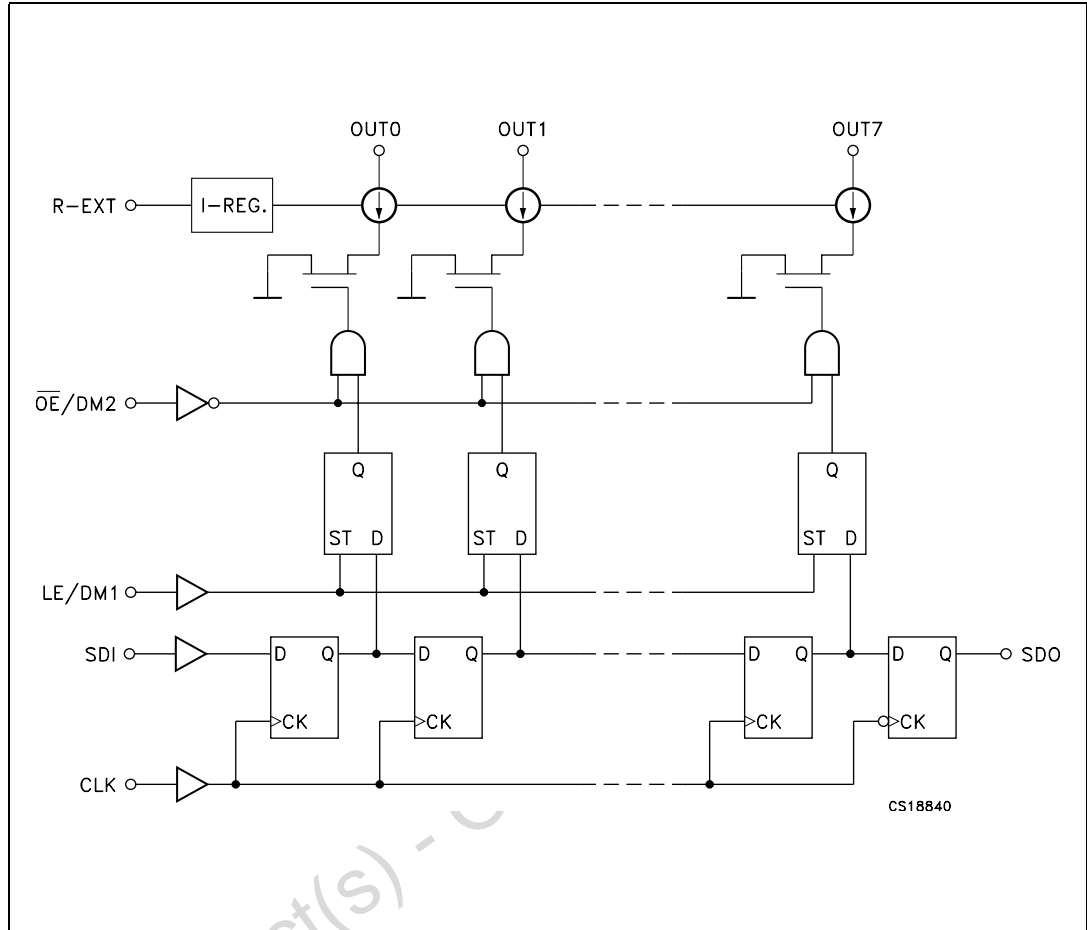


Table 2. Pin description

PIN N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE/DM1	Latch input terminal
5-12	OUT 0-7	Output terminal
13	$\overline{OE}/DM2$	Output enable input terminal (active low)
14	SDO	Serial data out terminal
15	R-EXT	Constant current programming
16	$V_{DD}$	5V Supply voltage terminal

## 2 Block diagram

Figure 2. Block diagram



### 3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

#### 3.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage $I_{GND}$	0 to 7	V
$V_O$	Output voltage	-0.5 to 16	V
$I_O$	Output current	120	mA
$V_I$	Input voltage	-0.4 to $V_{DD}+0.4$	V
$I_{GND}$	GND terminal current	980	mA
$f_{CLK}$	Clock frequency	25	MHz
$T_{OPR}$	Operating temperature range	-40 to +125	°C
$T_{STG}$	Storage temperature range	-55 to +150	°C

#### 3.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Package	Value	Unit
$R_{thJA}$	Thermal resistance junction-ambient	DIP-16	90	°C/W
		SO-16	125	
		TSSOP-16	140	
		TSSOP-16 Exposed Pad	38 <sup>(1)</sup>	

1. The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

### 3.3 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{DD}$	Supply voltage		3.3		5.5	V
$V_O$	Output voltage				16.0	V
$I_O$	Output current	OUTn	15		120	mA
$I_{OH}$	Output current	SERIAL-OUT			+1	mA
$I_{OL}$	Output current	SERIAL-OUT			-1	mA
$V_{IH}$	Input voltage		$0.7V_{DD}$		$V_{DD}+0.3$	V
$V_{IL}$	Input voltage		-0.3		$0.3V_{DD}$	V
$t_{wLAT}$	LE/DM1 pulse width	$V_{DD} = 3.0$ to $5.0V$		10	20	ns
$t_{wCLK}$	CLK pulse width			10	20	ns
$t_{wEN}$	$\overline{OE}/DM2$ pulse width <sup>(1)</sup>			120	400	ns
$t_{SETUP(D)}$	Setup time for DATA			5	20	ns
$t_{HOLD(D)}$	Hold time for DATA			4	15	ns
$t_{SETUP(L)}$	Setup time for LATCH			8	15	ns
$f_{CLK}$	Clock frequency <sup>(2)</sup>					25

1. If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

2. In normal mode the  $\overline{OE}/DM2$  must remain low at least two clock cycles.

## 4 Electrical characteristics

**Table 6. Electrical characteristics** ( $V_{DD} = 5V$ ,  $T = 25^{\circ}C$ , unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IH}$	Input voltage high level		$0.7V_{DD}$		$V_{DD}$	V
$V_{IL}$	Input voltage low level		GND		$0.3V_{DD}$	V
$I_{OH}$	Output leakage current	$V_{OH} = 16V$			10	$\mu A$
$V_{OL}$	Output voltage (Serial-OUT)	$I_{OL} = 1mA$			0.4	V
$V_{OH}$	Output voltage (Serial-OUT)	$I_{OH} = -1mA$	$V_{DD}-0.4V$			V
$I_{OL1}$	Output current	$V_O = 0.7V R_{EXT} = 910 \Omega$	18.8	20.9	24.00	mA
$I_{OL2}$		$V_O = 0.7V R_{EXT} = 360 \Omega$	46.00	51.5	56.5	mA
$\Delta I_{OL1}$	Output current error between bit (All Output ON)	$V_O = 0.7V R_{EXT} = 910 \Omega$		$\pm 2$	$\pm 5$	%
$\Delta I_{OL2}$		$V_O = 0.7V R_{EXT} = 360 \Omega$		$\pm 1$	$\pm 4$	%
$R_{SIN(up)}$	Pull-up resistor		150	300	600	K $\Omega$
$R_{SIN(down)}$	Pull-down resistor		100	200	400	K $\Omega$
$I_{DD(OFF1)}$	Supply current (OFF)	$R_{EXT} = OPEN$ OUT 0 to 7 = OFF		0.45	0.7	mA
$I_{DD(OFF2)}$		$R_{EXT} = 910 \Omega$ OUT 0 to 7 = OFF		3.0	6.0	
$I_{DD(OFF3)}$		$R_{EXT} = 360 \Omega$ OUT 0 to 7 = OFF		8.2	12.0	
$I_{DD(ON1)}$	Supply current (ON)	$R_{EXT} = 910 \Omega$ OUT 0 to 7 = ON		3.1	6.2	mA
$I_{DD(ON2)}$		$R_{EXT} = 360 \Omega$ OUT 0 to 7 = ON		8.4	12.8	

## 5 Switching characteristics

**Table 7. Switching Characteristics** ( $V_{DD} = 3.3V$  to  $5.5V$ ,  $T = 25^{\circ}C$ , unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	
$t_{PLH1}$	Propagation delay time, CLK- $\overline{OUTn}$ , $\overline{LE}/DM1 = H$ , $\overline{OE}/DM2 = L$	$V_{DD} = 3V$ $V_{IL} = GND$ $I_O = 40mA$ $R_{EXT} = 470\Omega$ $V_{IH} = V_{DD}$ $C_L = 13pF$ $V_L = 3V$ $R_L = 65\Omega$		180	280	ns	
$t_{PLH2}$	Propagation delay time, $\overline{LE}/DM1-\overline{OUTn}$ , $\overline{OE}/DM2 = L$			150	280	ns	
$t_{PLH3}$	Propagation delay time, $\overline{OE}/DM2-\overline{OUTn}$ , $\overline{LE}/DM1 = H$			140	280	ns	
$t_{PLH}$	Propagation delay time, CLK-SDO			25	35	ns	
$t_{PHL1}$	Propagation delay time, CLK- $\overline{OUTn}$ , $\overline{LE}/DM1 = H$ , $\overline{OE}/DM2 = L$			30	60	ns	
$t_{PHL2}$	Propagation delay time, $\overline{LE}/DM1-\overline{OUTn}$ , $\overline{OE}/DM2 = L$			30	50	ns	
$t_{PHL3}$	Propagation delay time, $\overline{OE}/DM2-\overline{OUTn}$ , $\overline{LE}/DM1 = H$			35	70	ns	
$t_{PHL}$	Propagation delay time, CLK-SDO			30	40	ns	
$t_r$	Output rise time				220		ns
$t_f$	Output fall time				20		ns

## 6 Equivalent circuit of inputs and outputs

Figure 3.  $\overline{OE}$  terminal

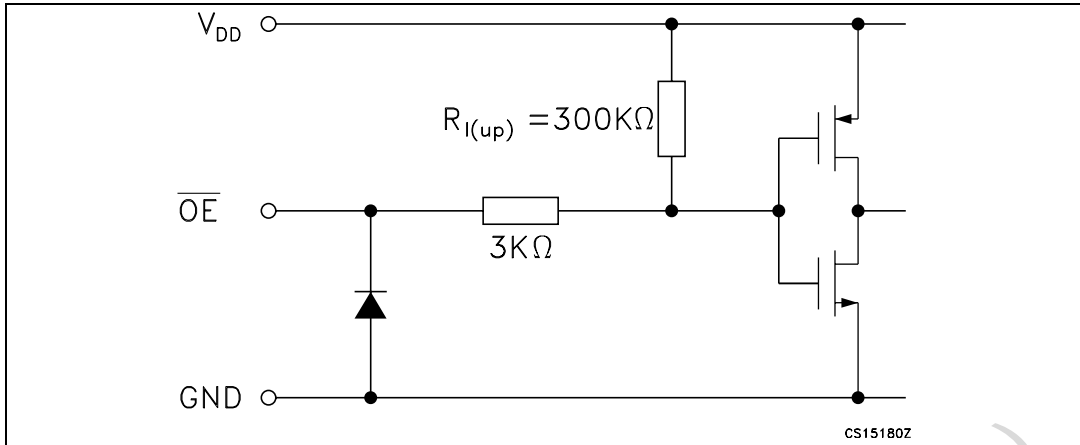


Figure 4. LE terminal

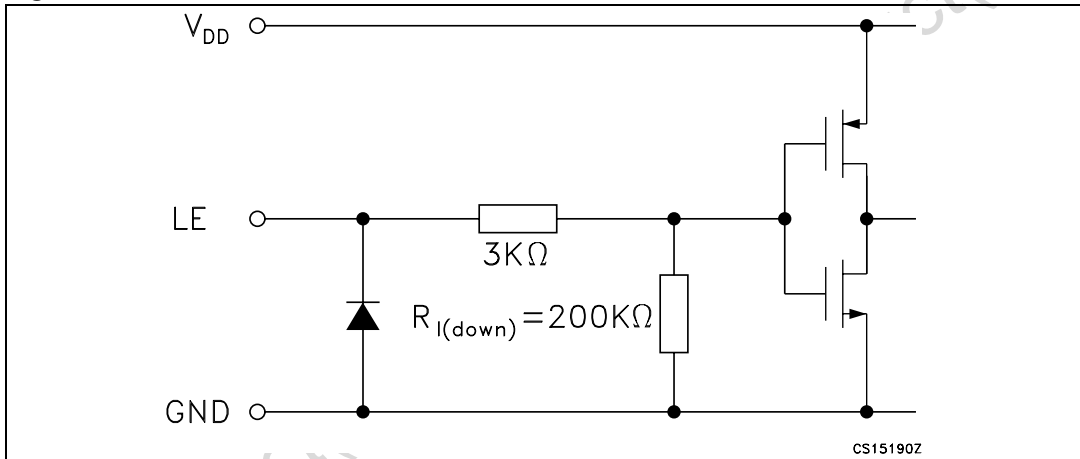


Figure 5. CLK, SDI terminal

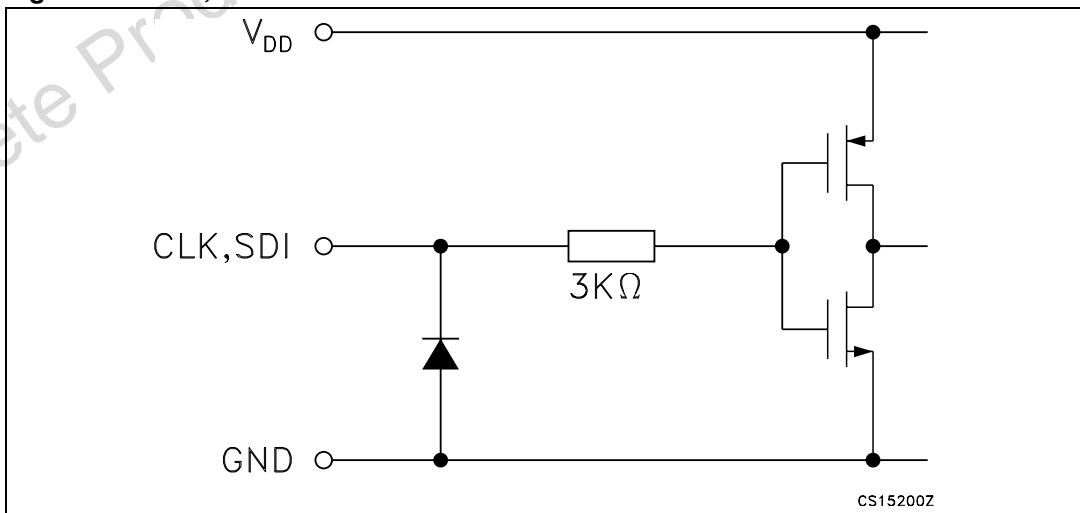
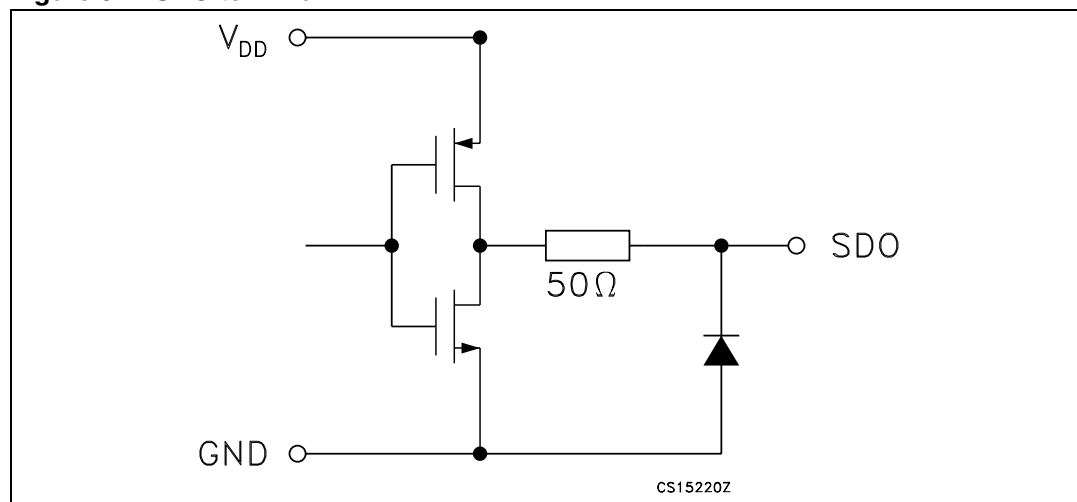


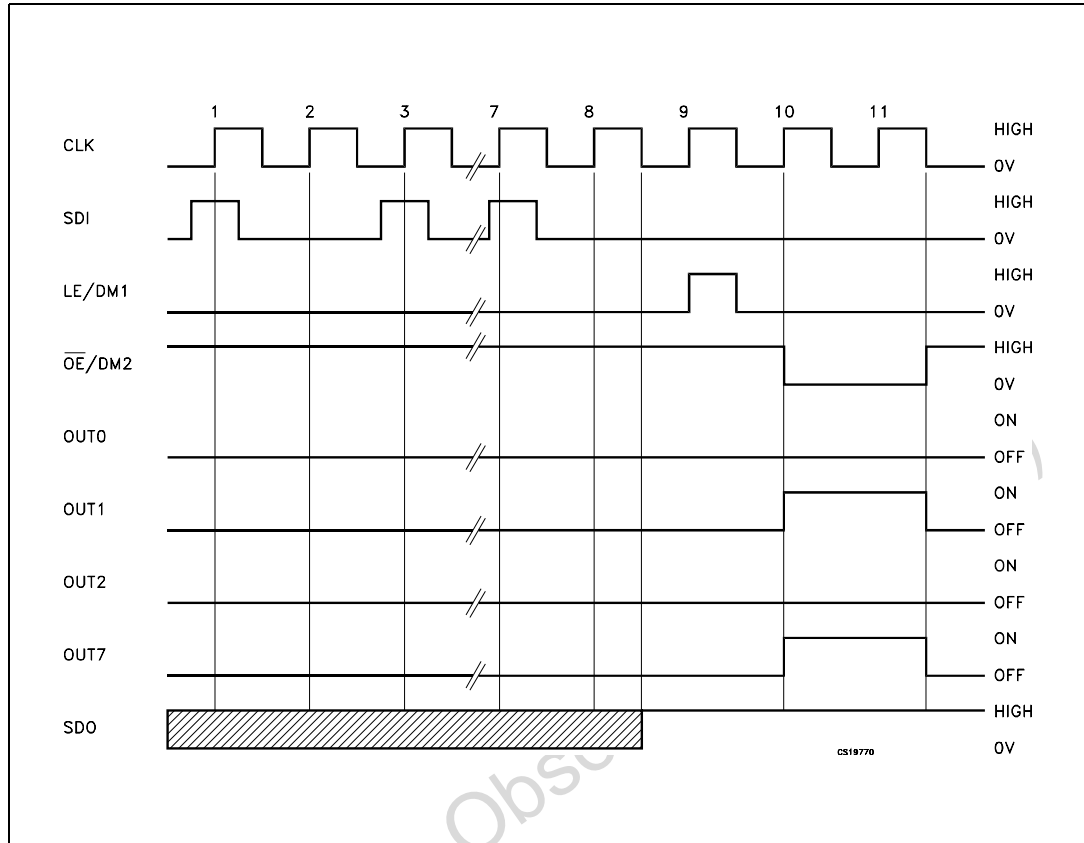
Figure 6. SDO terminal



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# 7 Timing diagram

Figure 7. Timing diagram



Note: In normal mode the  $\overline{OE}/DM2$  must remain low at least two clock cycles. In case of  $\overline{OE}$  signal enabled ( $\overline{OE} = LOW$ ) during no clock activity (clock stopped), after the CLK restarts, 3 full CLK cycles are necessary before disabling the  $\overline{OE}$  signal ( $\overline{OE} = High$ ).

Figure 8. Clock, serial-in, serial-out

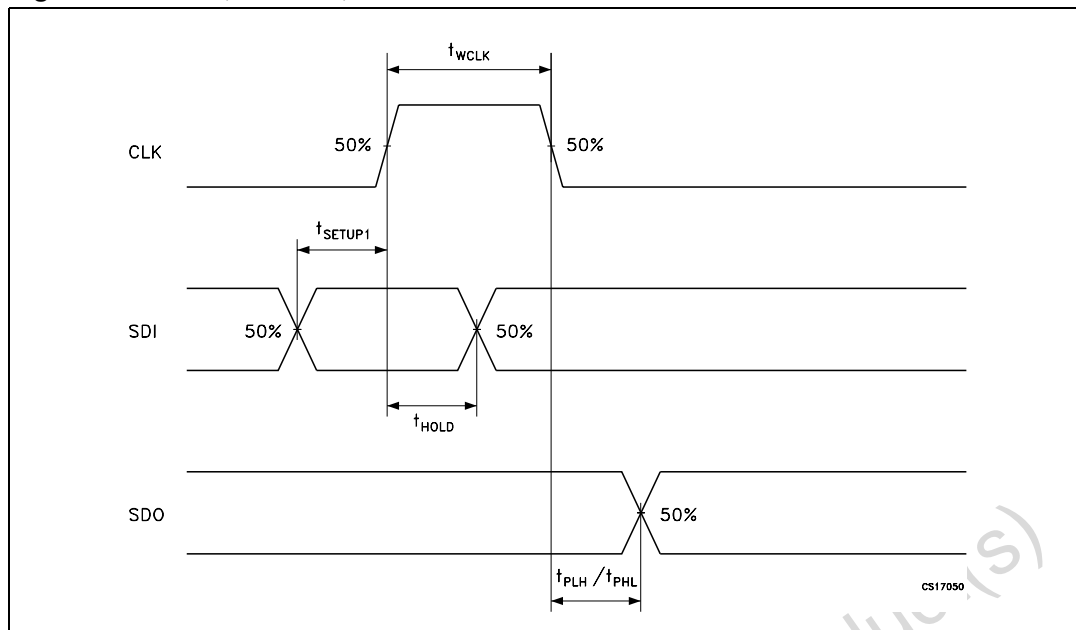


Figure 9. Clock, serial-in, latch, enable, outputs

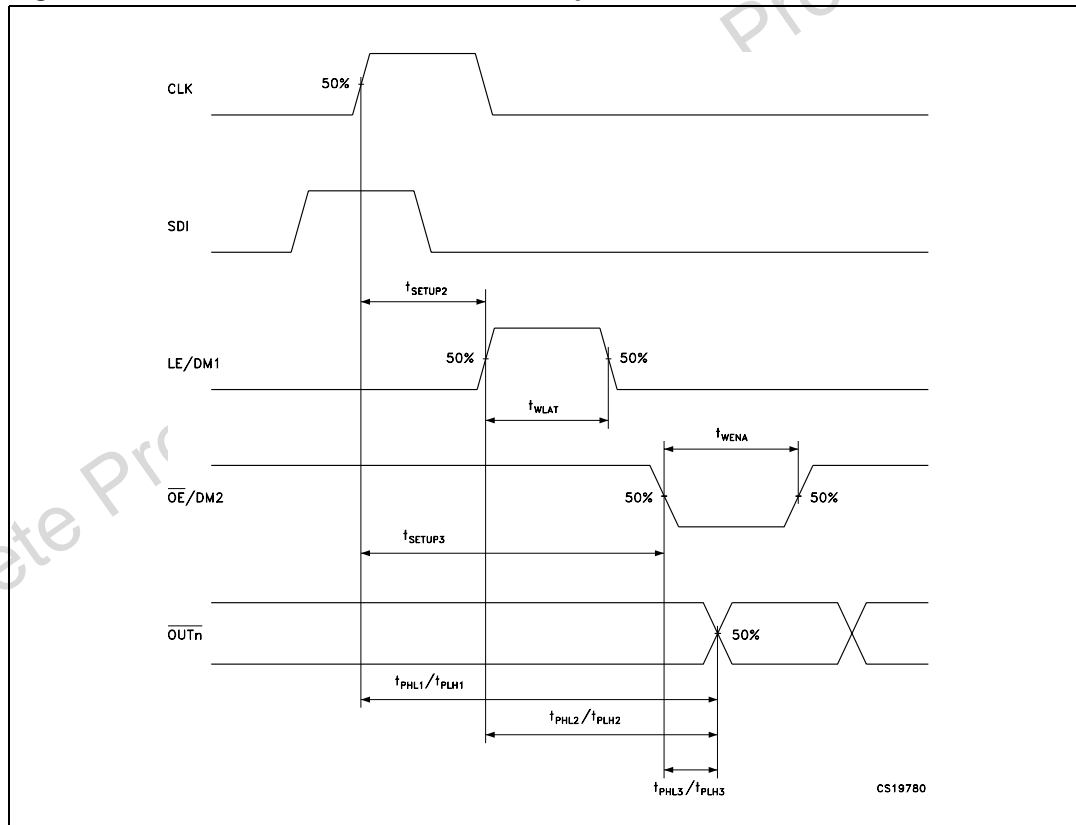
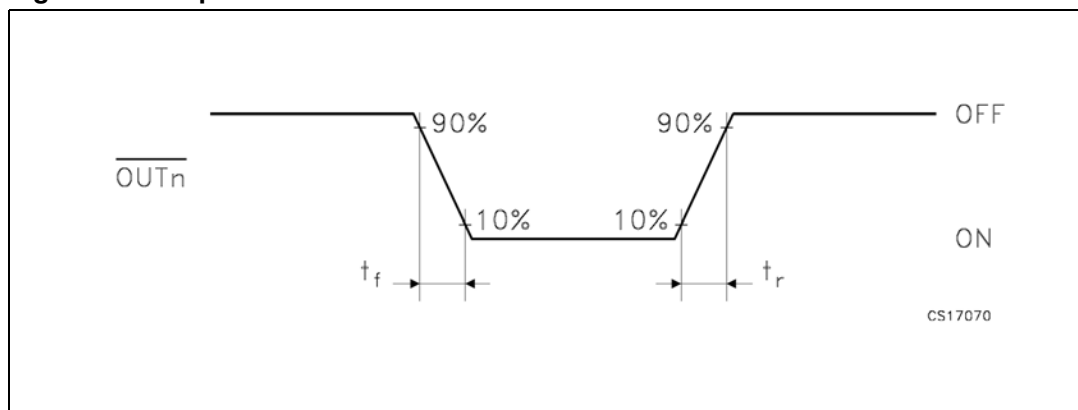


Figure 10. Outputs



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# 8 Test circuit

Figure 11. DC characteristics

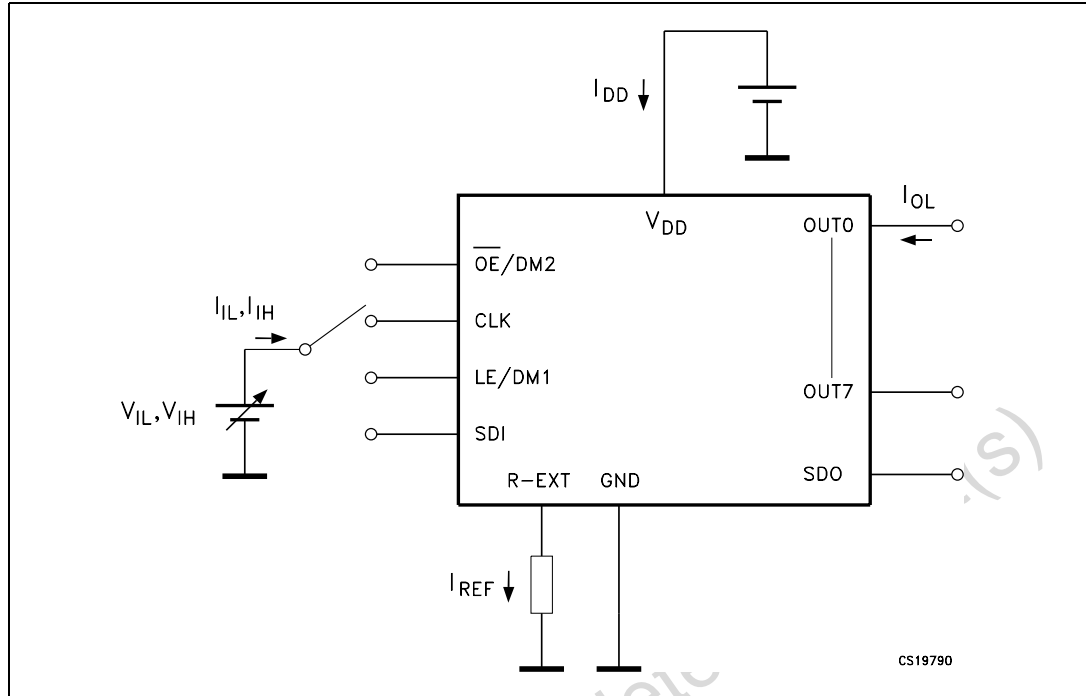


Figure 12. AC characteristics

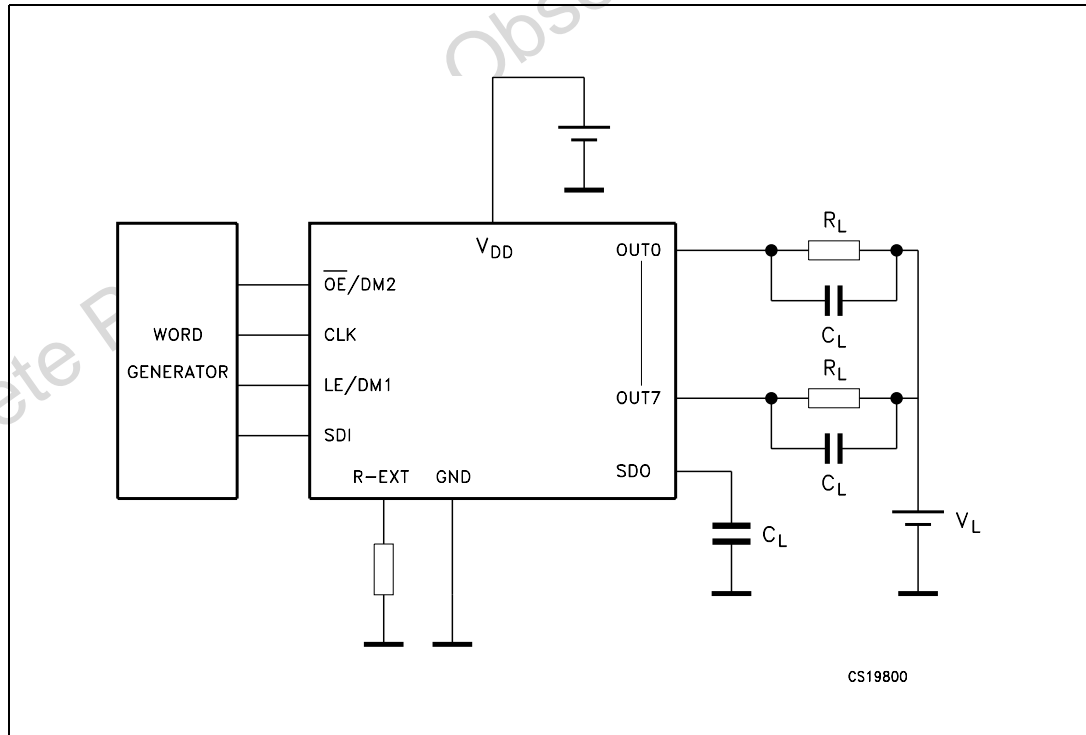
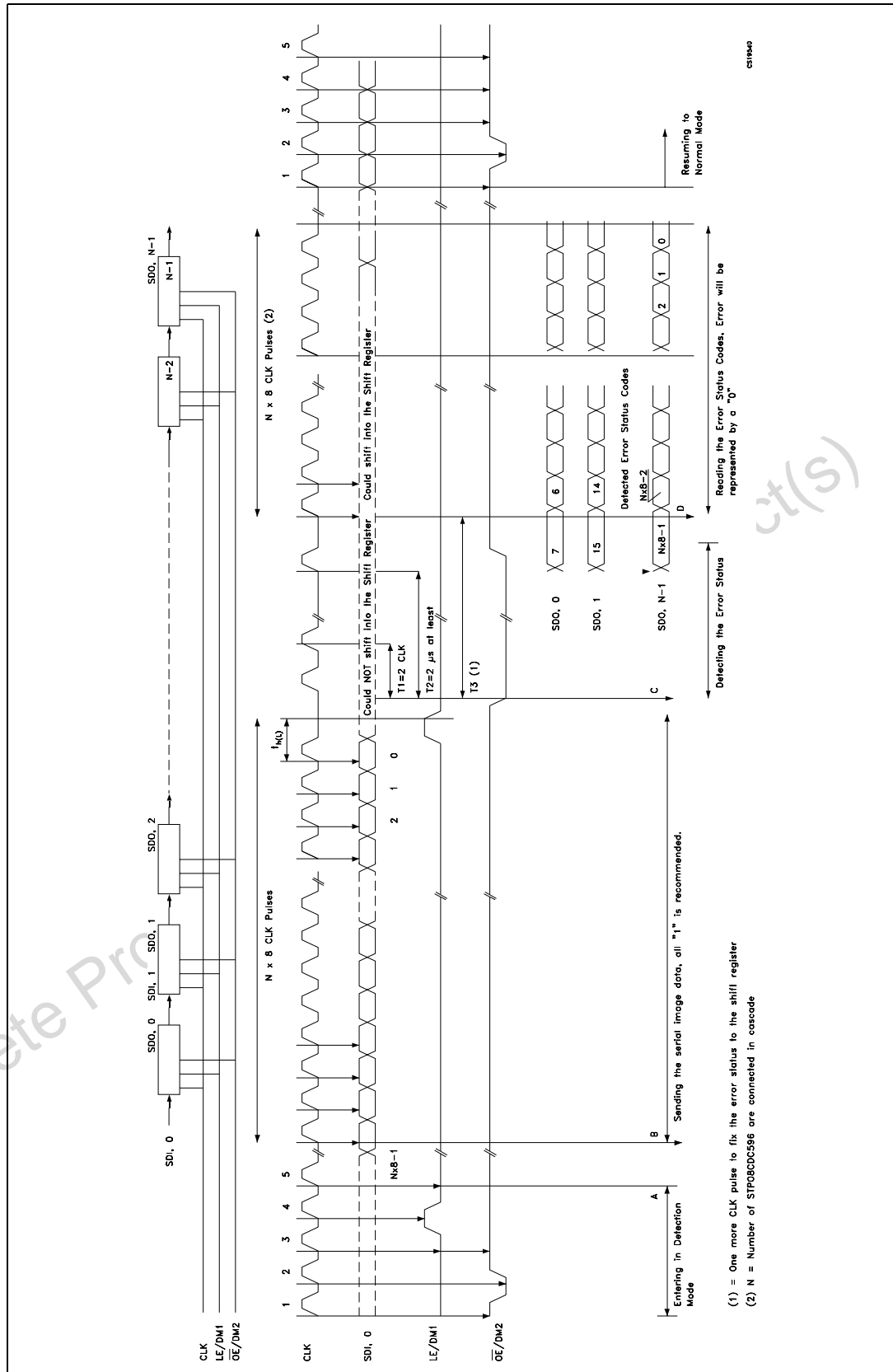


Figure 13. Timing example for open and/or short detection



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## 9 Running the detection mode

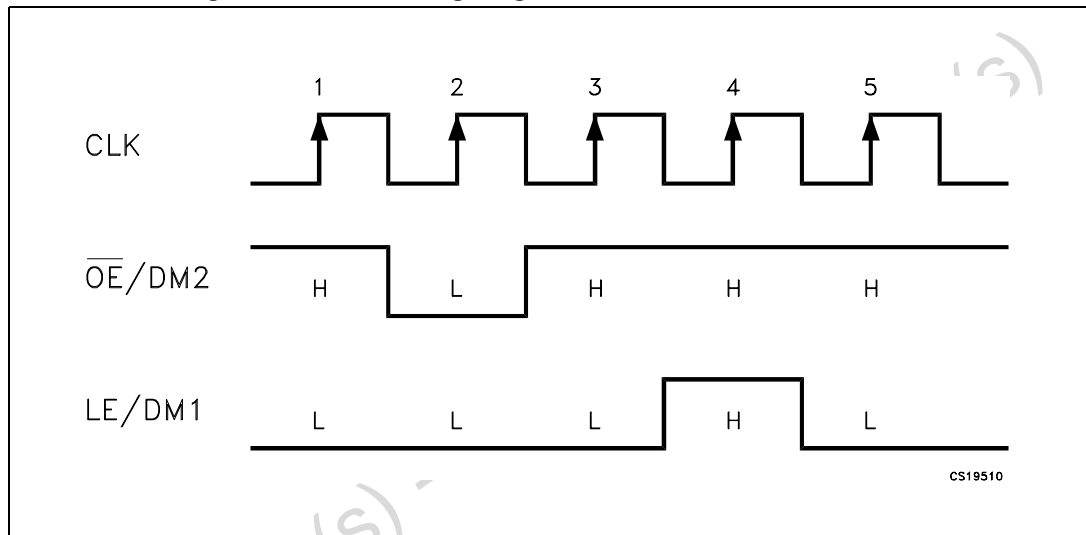
### 9.1 Phase one: “entering in detection mode“

From the “Normal Mode” condition the device can switch to the “Error Mode“ by a logic sequence on the OE/DM2 and LE/DM1 pins as showed in the following table and diagram:

**Table 8. Entering in detection truth table**

CLK	1°	2°	3°	4°	5°
OE/DM2	H	L	H	H	H
LE/DM1	L	L	L	H	L

**Table 9. Entering in detection timing diagram**

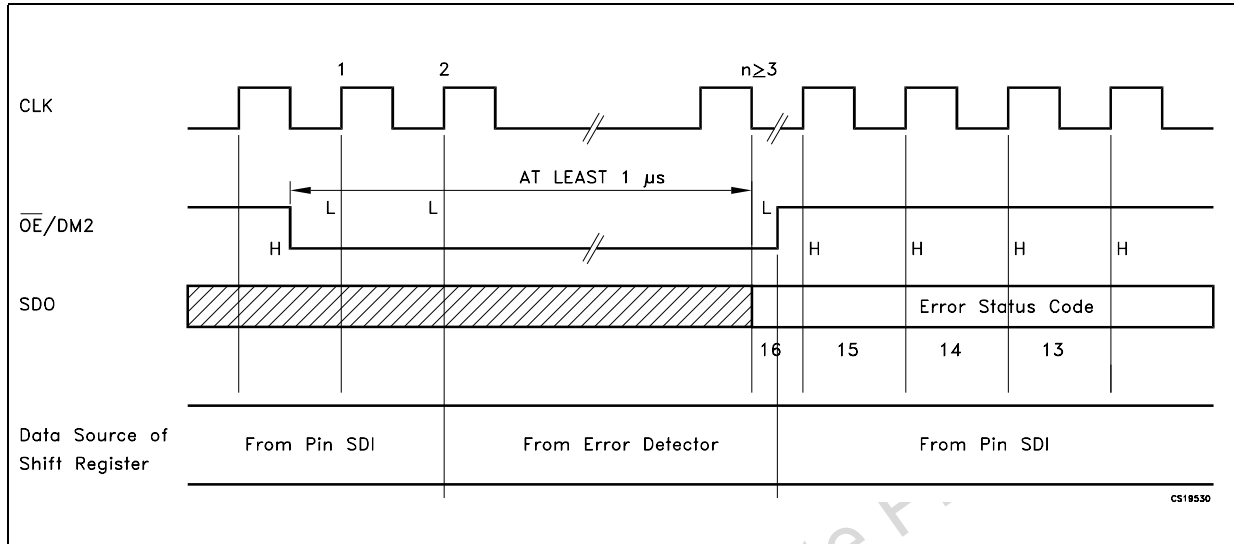


After these five CLK cycles the device goes into the “Error Detection Mode“ and at the 6<sup>th</sup> rise front of CLK the SDI data are ready for the sampling.

## 9.2 Phase two: “error detection“

The eight data bits must be set “1” in order to set ON all the outputs during the detection. The data are latched by LE/DM1 and after that the outputs are ready for the detection process. When the Micro controller switches the OE/DM2 to LOW, the device drives the LEDs in order to analyze if an OPEN or SHORT condition has occurred.

Table 10. Detection diagram



The LEDs status will be detected at least in 2 microseconds and after this time the microcontroller puts OE in HIGH state and the output data detection result will go to the microprocessor via SDO.

The detection data format is the same of data in normal mode. As soon as all the detection data bits are available on the serial line, the device may go back to normal mode operation.

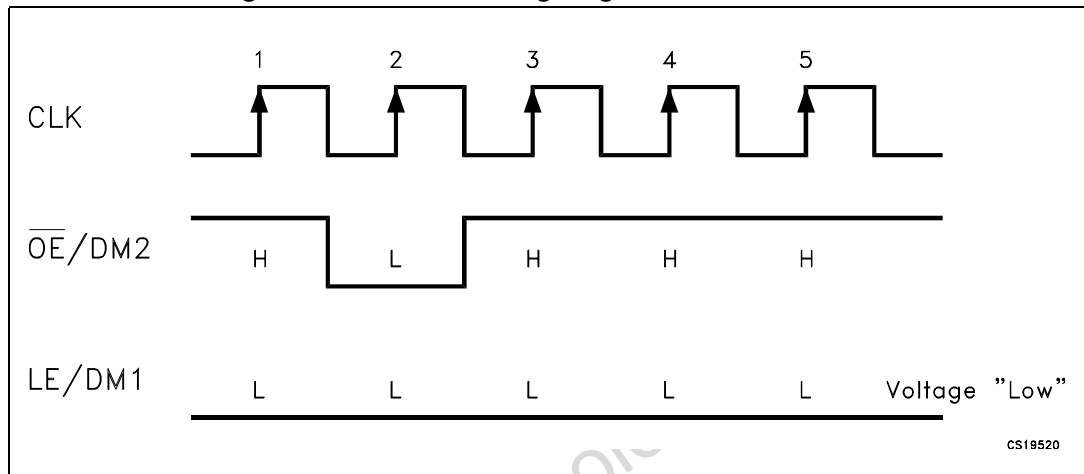
### 9.3 Phase three: “resuming to normal mode”

The sequence for re-entering in normal mode is showed in the following Table and diagram:

**Table 11. Resuming to normal mode timing diagram**

CLK	1°	2°	3°	4°	5°
OE/DM2	H	L	H	H	H
LE/DM1	L	L	L	L	L

**Table 12. Resuming to normal mode timing diagram**



*Note:* For proper device operation the "Entering in detection" sequence must be follow by a "Resume Mode" sequence, isn't possible to insert consecutive equal sequence.

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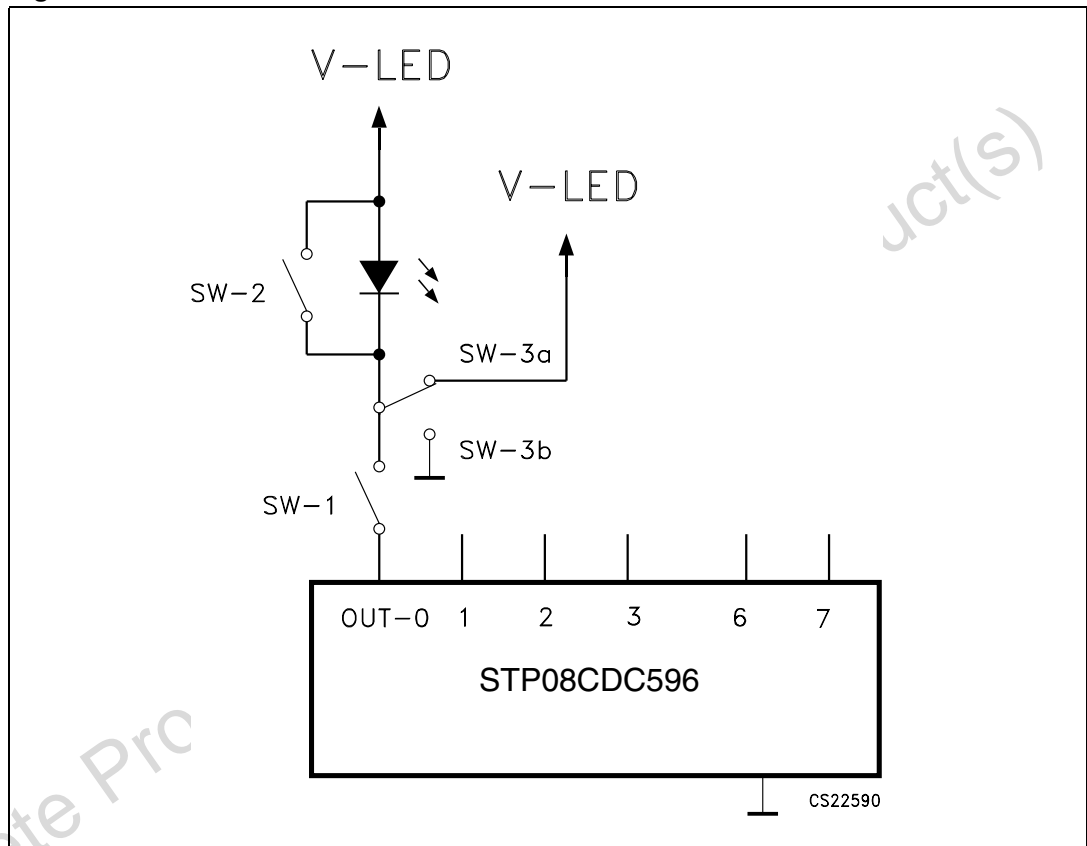
### 9.4 Condition in order to get a successfully detection condition

**Table 13. Detection condition** ( $V_{DD} = 3.3$  to  $5$  V Temp. Range  $-40$  to  $85^{\circ}\text{C}$ )

<b>SW-1 or SW-3b</b>	Open line or output short to GND detected	$\implies I_{ODEC} \leq 0.5 \times I_O$	No error detected	$\implies I_{ODEC} \geq 0.5 \times I_O$
<b>SW-2 or SW-3a</b>	Short on LED or short to V-LED detected	$\implies V_O \geq 2.4$ V	No error detected	$\implies V_O \leq 2.2$ V

*Note:* Where:  $I_O$  = the output current programmed by the  $R_{EXT}$ ,  $I_{ODEC}$  = the detected output current in detection mode.

**Figure 14. Detection circuit**



# 10 Typical characteristics

Figure 15. Output current-REXT resistor      Figure 16. Dropout voltage vs output current

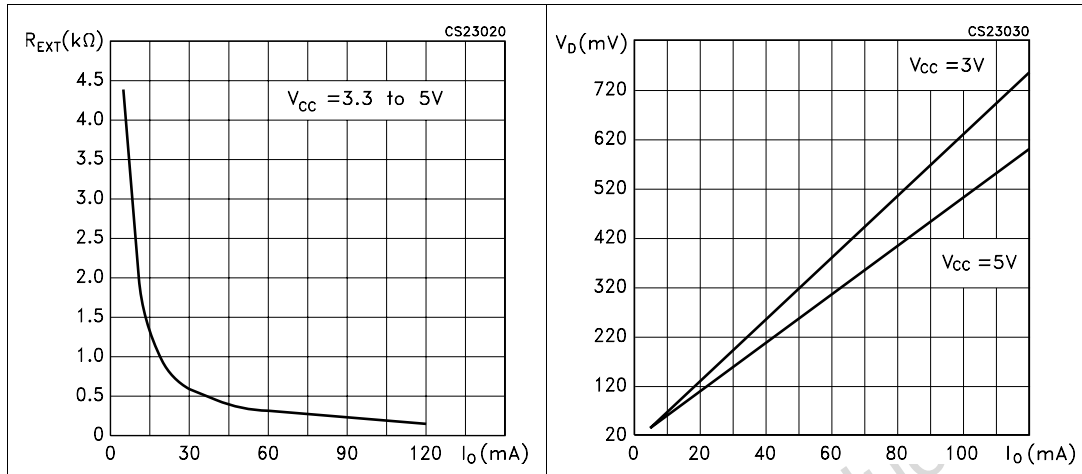


Figure 17. Power dissipation vs temperature package

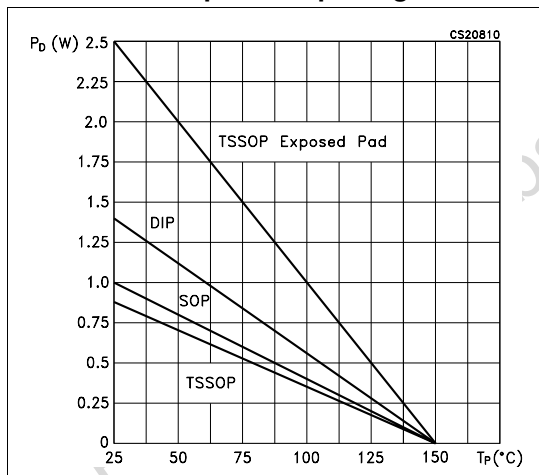
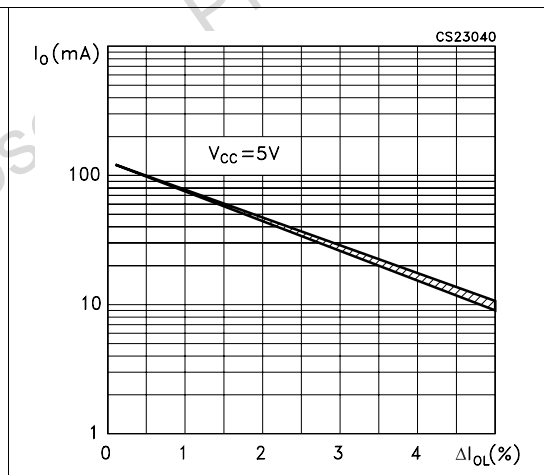


Figure 18. Output current vs  $\pm\Delta I_{OL}$  (%)



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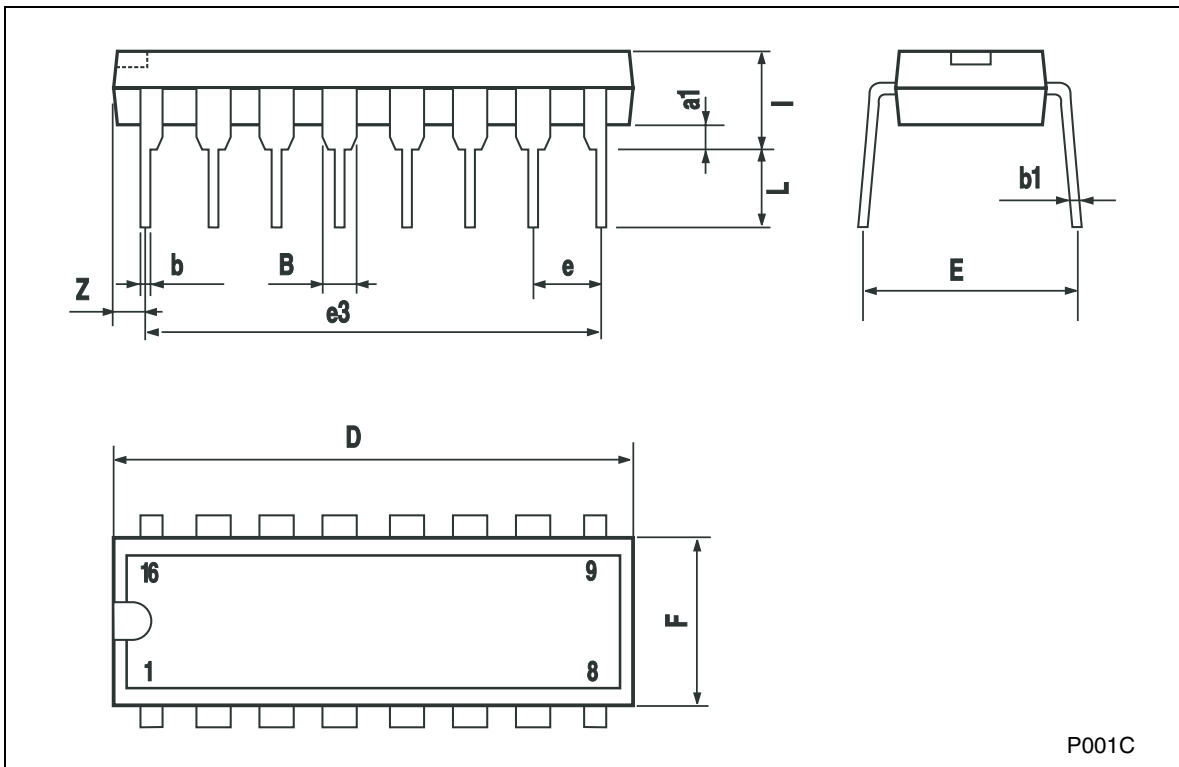
## 11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

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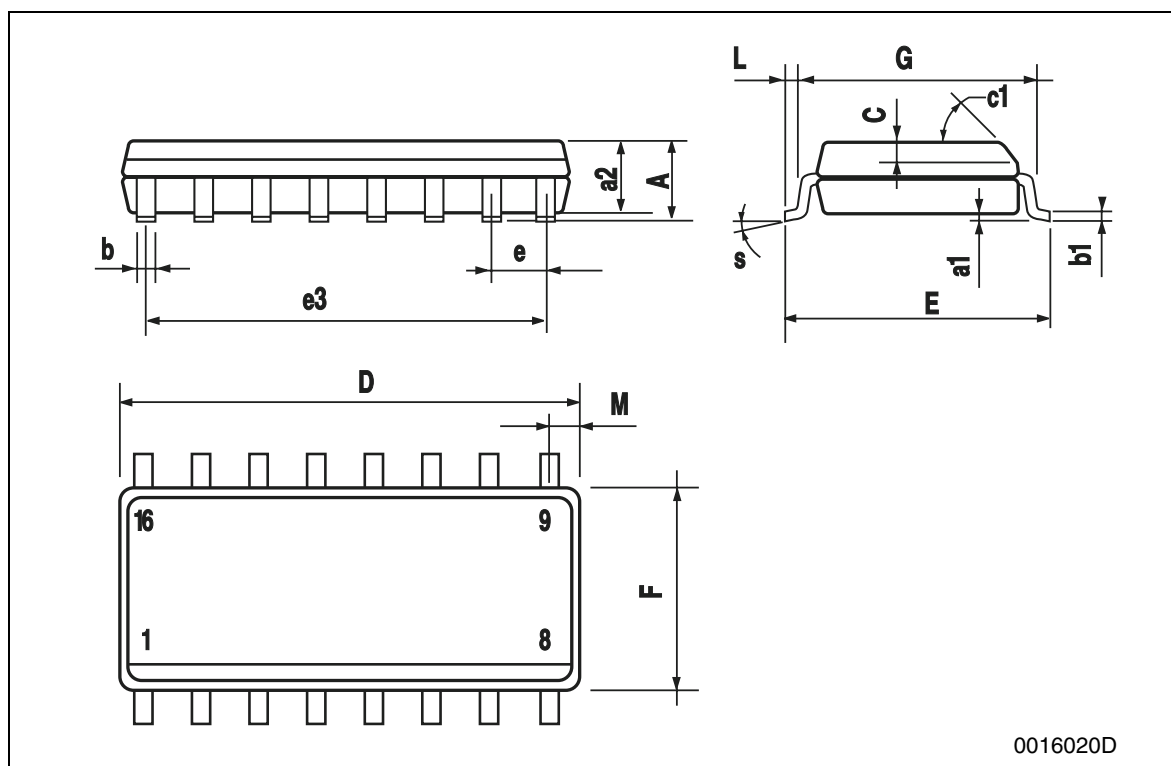
**Plastic DIP-16 (0.25) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



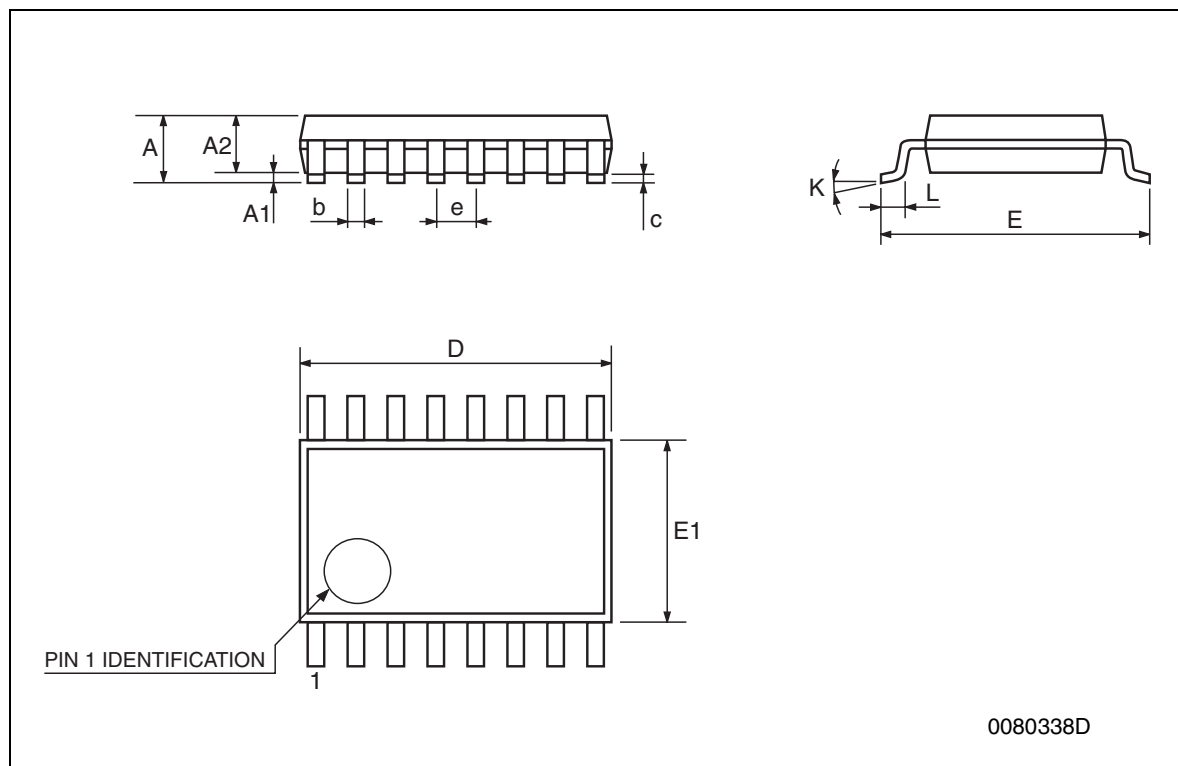
## SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



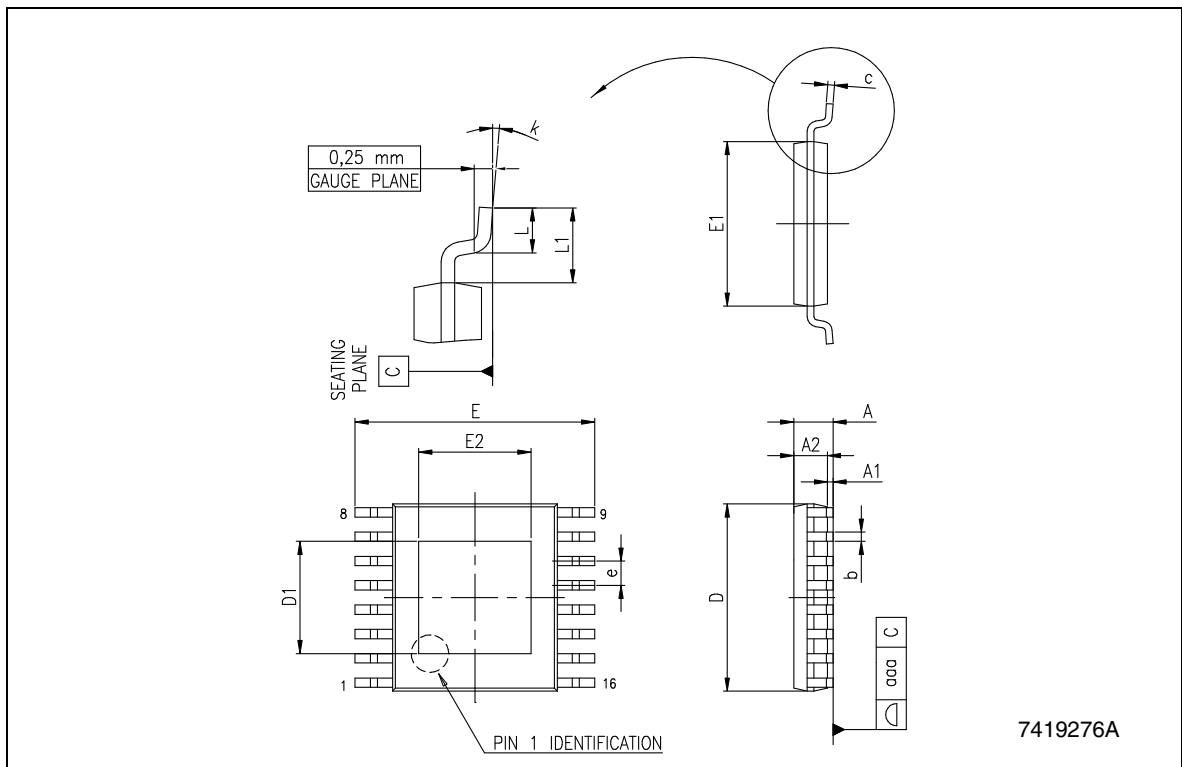
**TSSOP16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



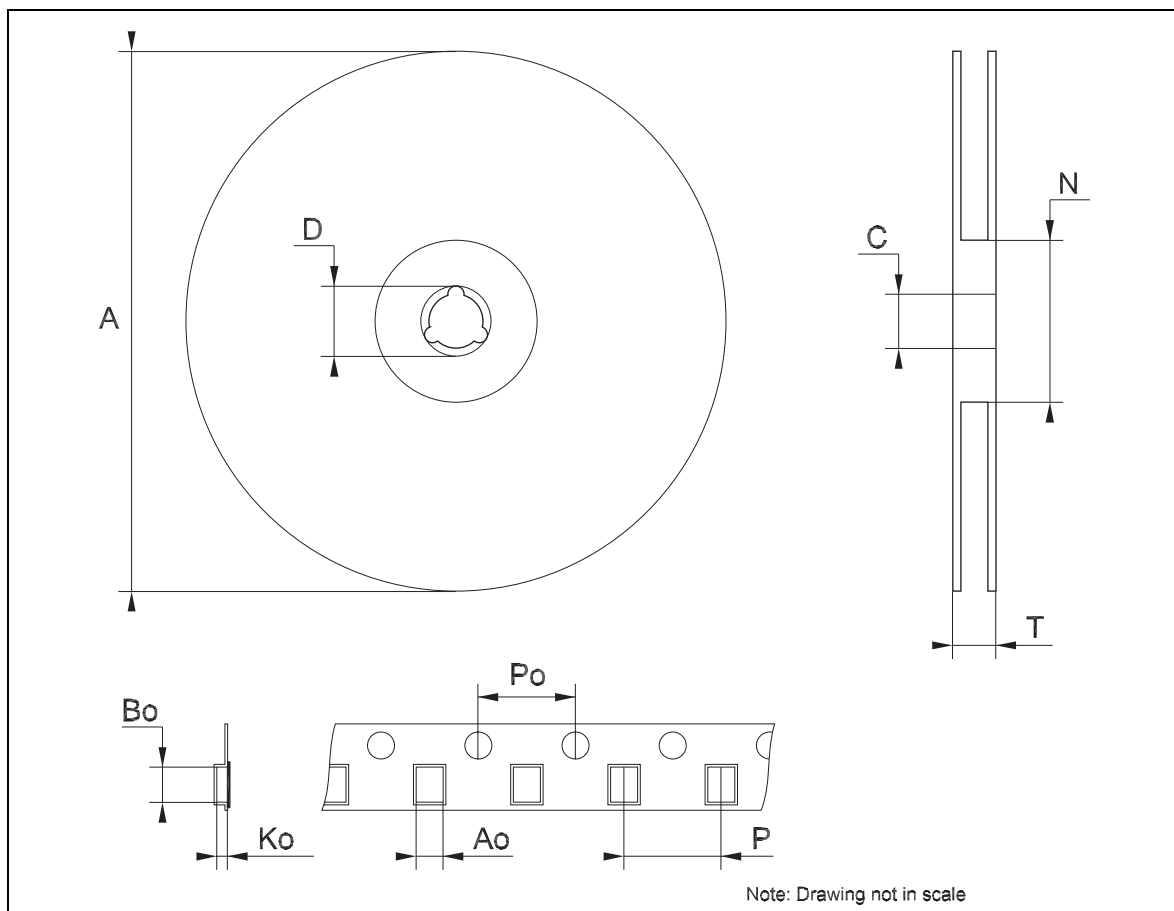
**TSSOP16 EXPOSED PAD MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
D1	1.7			0.067		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	1.5			0.059		
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



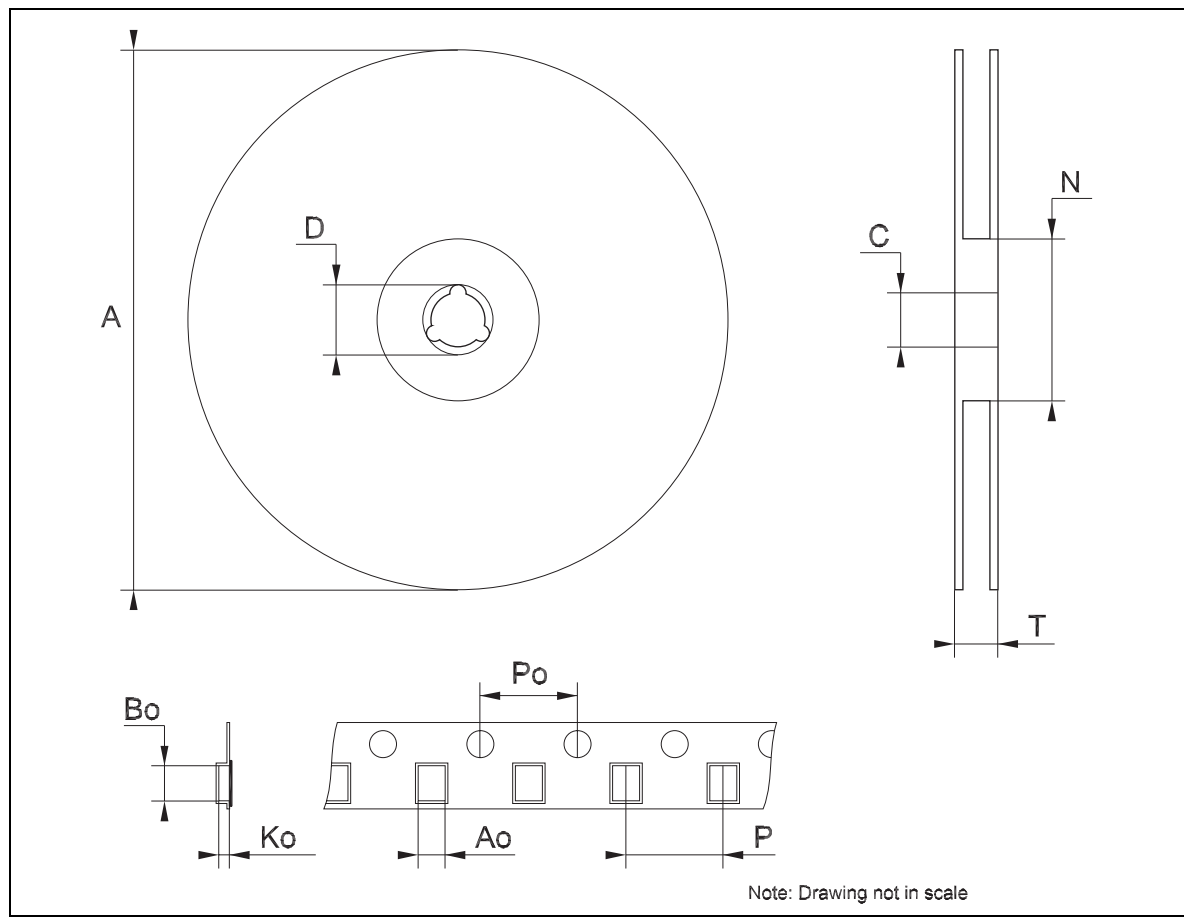
**Tape & Reel TSSOP16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



**Tape & Reel SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



## 12 Revision history

**Table 1. Revision history**

Date	Revision	Changes
15-Jun-2005	1	First release
11-Oct-2005	2	Minor revision, no content change
2-Aug-2006	3	New template, block diagram <a href="#">Figure 2 on page 4</a> and equivalent circuit <a href="#">Section 6 on page 9</a> updated, added TSSOP-16 Exposed Pad package.

Obsolete Product(s) - Obsolete Product(s)

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