



**THE DATASHEET OF  
LTC4353IMS#TRPBF**



## FEATURES

- Low Loss Replacement for Power Diodes
- Controls N-Channel MOSFETs
- 0V to 18V Supply ORing or Holdup
- 1 $\mu$ s Gate Turn-On and Turn-Off Time
- Enable Inputs
- MOSFET On-Status Outputs
- 16-Lead MSOP and DFN (4mm  $\times$  3mm) Packages

## APPLICATIONS

- Redundant Power Supplies
- Supply Holdup
- High Availability Systems and Servers
- Telecom and Network Infrastructure

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## DESCRIPTION

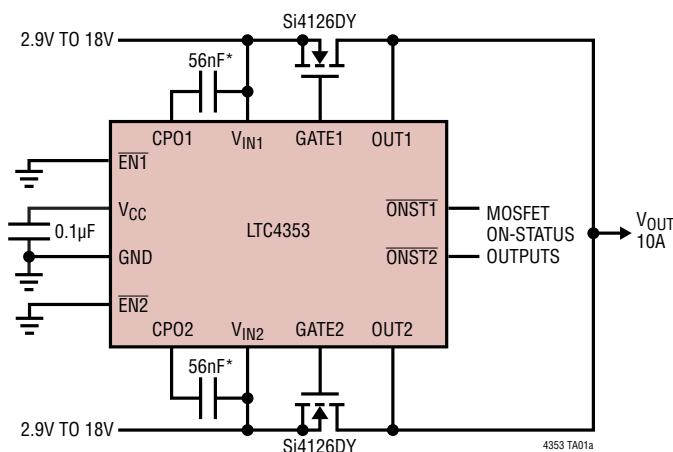
The LTC<sup>®</sup>4353 controls external N-channel MOSFETs to implement an ideal diode function. It replaces two high power Schottky diodes and their associated heat sinks, saving power and board area. The ideal diode function permits low loss power supply ORing and supply holdup applications.

The LTC4353 regulates the forward-voltage drop across the MOSFET to ensure smooth current transfer in diode-OR applications. A fast turn-on reduces the load voltage droop during supply switchover. If the input supply fails or is shorted, a fast turn-off minimizes reverse-current transients.

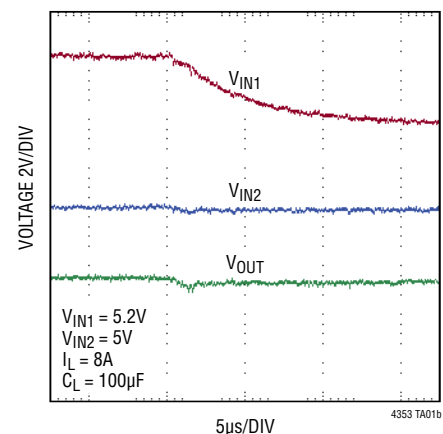
The controller operates with supplies from 2.9V to 18V. If both supplies are below 2.9V, an external supply is needed at the V<sub>CC</sub> pin. Enable inputs can be used to turn off the MOSFET and put the controller in a low current state. Status outputs indicate whether the MOSFETs are on or off.

## TYPICAL APPLICATION

2.9V to 18V, 10A Ideal Diode-OR



Output Maintained with Failing Input Supply



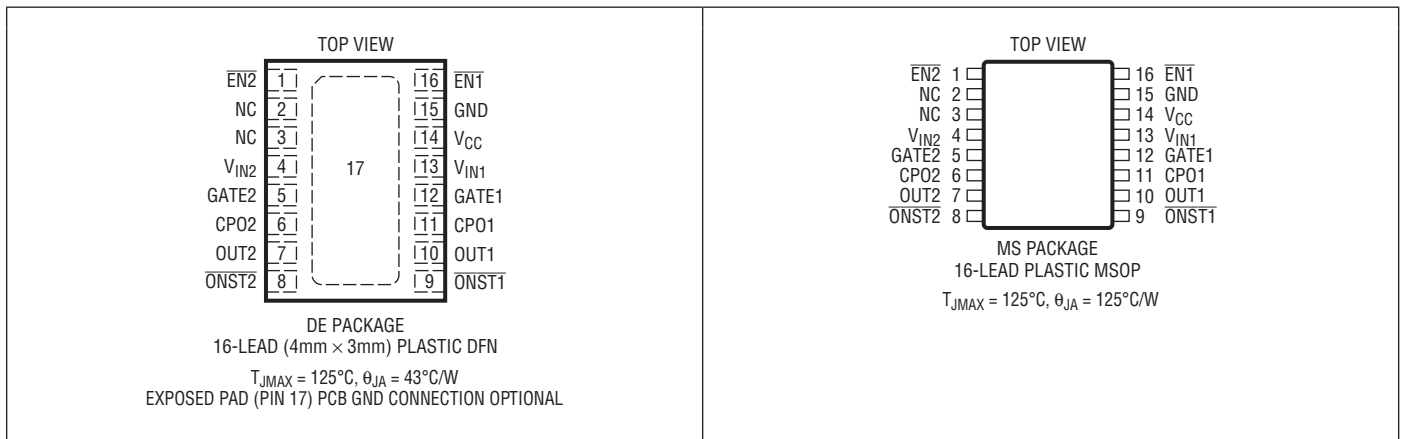
\*OPTIONAL FOR FAST TURN-ON

# LTC4353

## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

$V_{IN1}$ , $V_{IN2}$ , OUT1, OUT2 Voltages .....	-2V to 24V	Operating Ambient Temperature Range	
$V_{CC}$ Voltage .....	-0.3V to 6.5V	LTC4353C .....	0°C to 70°C
GATE1, GATE2 Voltages (Note 3) .....	-0.3V to 34V	LTC4353I .....	-40°C to 85°C
CPO1, CPO2 Voltages (Note 3) .....	-0.3V to 34V	Storage Temperature Range .....	-65°C to 150°C
$\overline{EN1}$ , $\overline{EN2}$ , $\overline{ONST1}$ , $\overline{ONST2}$ Voltages .....	-0.3V to 24V	Lead Temperature (Soldering, 10 sec)	
CPO1, CPO2 Average Current .....	10mA	MS Package .....	300°C
$\overline{ONST1}$ , $\overline{ONST2}$ Currents .....	5mA		

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4353CDE#PBF	LTC4353CDE#TRPBF	4353	16-Pin (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC4353IDE#PBF	LTC4353IDE#TRPBF	4353	16-Pin (4mm × 3mm) Plastic DFN	-40°C to 85°C
LTC4353CMS#PBF	LTC4353CMS#TRPBF	4353	16-Pin Plastic MSOP	0°C to 70°C
LTC4353IMS#PBF	LTC4353IMS#TRPBF	4353	16-Pin Plastic MSOP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes those specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN1} = V_{IN2} = 12\text{V}$ ,  $\text{OUT} = V_{IN}$ ,  $V_{CC}$  Open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Supplies</b>							
$V_{IN}$	$V_{IN1}$ , $V_{IN2}$ Operating Range	With External $V_{CC}$ Supply	●	2.9		18	V
			●	0		$V_{CC}$	V
$V_{CC(\text{EXT})}$	$V_{CC}$ External Supply Operating Range	$V_{IN1}$ , $V_{IN2} \leq V_{CC}$	●	2.9		6	V
$V_{CC(\text{REG})}$	$V_{CC}$ Regulated Voltage		●	4.5	5	5.5	V
$I_{IN}$	$V_{IN1}$ , $V_{IN2}$ Current Enabled, Higher Supply Enabled, Lower Supply Pull-Up Disabled	Other $V_{IN} = 11.7\text{V}$ , Both $\overline{\text{EN}} = 0\text{V}$ Other $V_{IN} = 12.3\text{V}$ , Both $\overline{\text{EN}} = 0\text{V}$ Both $V_{IN} = 0\text{V}$ , $V_{CC} = 5\text{V}$ , Both $\overline{\text{EN}} = 0\text{V}$ Both $\overline{\text{EN}} = 1\text{V}$	●		1.5	2.5	mA
			●		200	300	$\mu\text{A}$
			●		-45	-80	$\mu\text{A}$
			●		75	160	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Current Enabled Disabled	$V_{CC} = 5\text{V}$ , Both $V_{IN} = 1.2\text{V}$ , Both $\overline{\text{EN}} = 0\text{V}$ $V_{CC} = 5\text{V}$ , Both $V_{IN} = 1.2\text{V}$ , Both $\overline{\text{EN}} = 1\text{V}$	●		1.5	2.2	mA
			●		88	190	$\mu\text{A}$
$V_{CC(\text{UVLO})}$	$V_{CC}$ Undervoltage Lockout Threshold	$V_{CC}$ Rising	●	2.3	2.55	2.7	V
$\Delta V_{CC(\text{HYST})}$	$V_{CC}$ Undervoltage Lockout Hysteresis		●	40	120	300	mV
<b>Ideal Diode Control</b>							
$V_{FR}$	Forward Regulation Voltage ( $V_{IN} - \text{OUT}$ )	$V_{IN} = 1.2\text{V}$ , $V_{CC} = 5\text{V}$ $V_{IN} = 12\text{V}$	●	2	12	25	mV
			●	2	25	50	mV
$\Delta V_{\text{GATE}}$	MOSFET Gate Drive ( $\text{GATE} - V_{IN}$ )	$V_{\text{FWD}} = 0.2\text{V}$ ; $I = 0$ , $-1\mu\text{A}$ ; Highest $V_{IN} = 12\text{V}$ $V_{\text{FWD}} = 0.2\text{V}$ ; $I = 0$ , $-1\mu\text{A}$ ; Highest $V_{IN} = 2.9\text{V}$	●	10	12	14	V
			●	4.5	7	9	V
$t_{\text{ON}(\text{GATE})}$	GATE1, GATE2 Turn-On Propagation Delay	$V_{\text{FWD}} (= V_{IN} - \text{OUT})$ Step: $-0.3\text{V}$ to $0.3\text{V}$	●		0.4	1	$\mu\text{s}$
$t_{\text{OFF}(\text{GATE})}$	GATE1, GATE2 Turn-Off Propagation Delay	$V_{\text{FWD}}$ Step: $0.3\text{V}$ to $-0.3\text{V}$	●		0.3	1	$\mu\text{s}$
$I_{\text{GATE}}$	GATE1, GATE2 Fast Pull-Up Current GATE1, GATE2 Fast Pull-Down Current GATE1, GATE2 Off Pull-Down Current	$V_{\text{FWD}} = 0.4\text{V}$ , $\Delta V_{\text{GATE}} = 0\text{V}$ , $\text{CPO} = 17\text{V}$ $V_{\text{FWD}} = -0.8\text{V}$ , $\Delta V_{\text{GATE}} = 5\text{V}$ Corresponding $\overline{\text{EN}} = 1\text{V}$ , $\Delta V_{\text{GATE}} = 2.5\text{V}$	●	-0.9	-1.4	-1.9	A
			●	0.9	1.4	1.9	A
			●	65	110	160	$\mu\text{A}$
<b>Input/Output Pins</b>							
$V_{\text{EN}(\text{TH})}$	$\overline{\text{EN}}1$ , $\overline{\text{EN}}2$ Threshold Voltage	$\overline{\text{EN}}$ Falling	●	580	600	620	mV
$\Delta V_{\text{EN}(\text{TH})}$	$\overline{\text{EN}}1$ , $\overline{\text{EN}}2$ Threshold Hysteresis		●	2	8	20	mV
$I_{\overline{\text{EN}}}$	$\overline{\text{EN}}1$ , $\overline{\text{EN}}2$ Current	At $0.6\text{V}$	●		0	$\pm 1$	$\mu\text{A}$
$I_{\text{OUT}}$	OUT1, OUT2 Current Enabled Disabled	OUT $n = 0\text{V}$ , $12\text{V}$ ; Both $\overline{\text{EN}} = 0\text{V}$ Both $\overline{\text{EN}} = 1\text{V}$	●	-4		160	$\mu\text{A}$
			●		8	16	$\mu\text{A}$
$I_{\text{CPO}(\text{UP})}$	CPO1, CPO2 Pull-Up Current	$\text{CPO} = V_{IN}$	●	-40	-70	-115	$\mu\text{A}$
$V_{\text{OL}}$	$\overline{\text{ONST}}1$ , $\overline{\text{ONST}}2$ Output Low Voltage	$I = 1\text{mA}$ $I = 3\text{mA}$	●		0.14	0.4	V
			●		0.42	1.2	V
$V_{\text{OH}}$	$\overline{\text{ONST}}1$ , $\overline{\text{ONST}}2$ Output High Voltage	$I = -1\mu\text{A}$	●	$V_{CC} - 1.4$	$V_{CC} - 0.9$	$V_{CC} - 0.5$	V
$I_{\overline{\text{ONST}}}$	$\overline{\text{ONST}}1$ , $\overline{\text{ONST}}2$ Leakage Current	At $12\text{V}$	●		0	$\pm 1$	$\mu\text{A}$
$\Delta V_{\text{GATE}(\text{ON})}$	MOSFET On-Detect Threshold ( $\text{GATE} - V_{IN}$ )	$\overline{\text{ONST}}$ Pulls Low	●	0.28	0.7	1.1	V

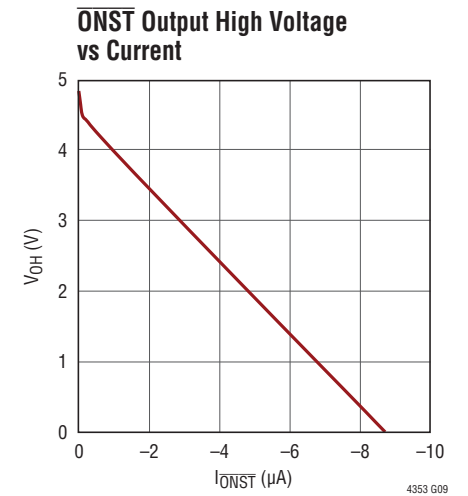
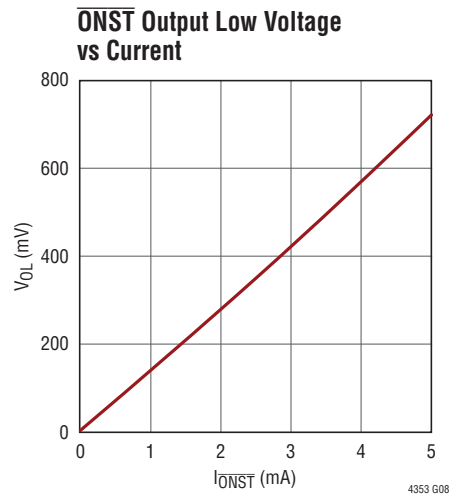
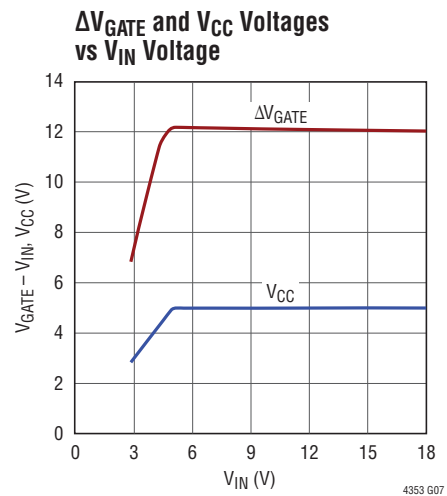
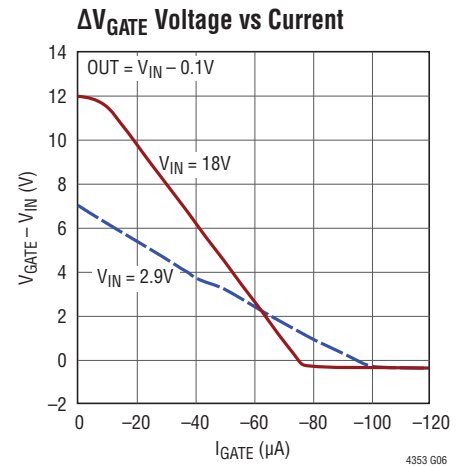
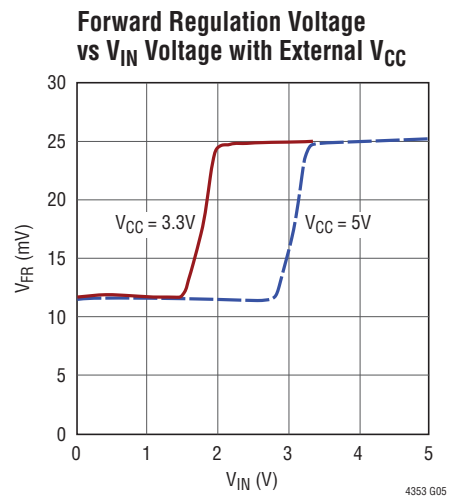
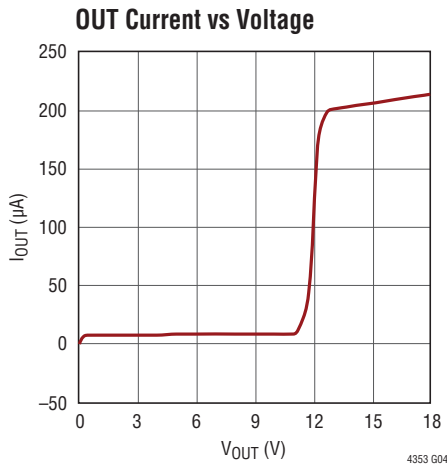
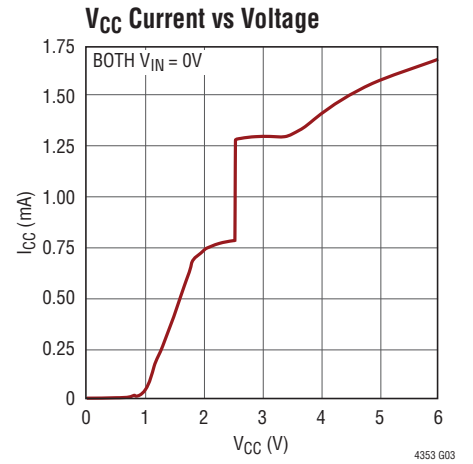
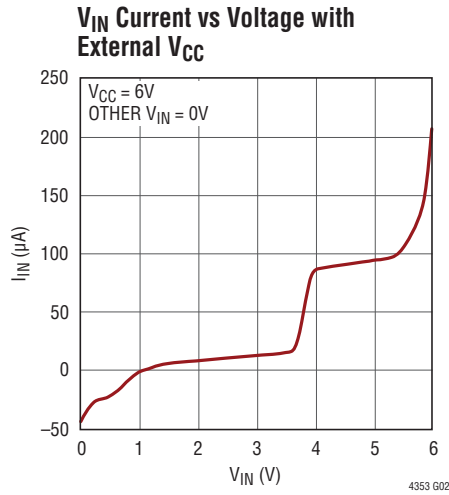
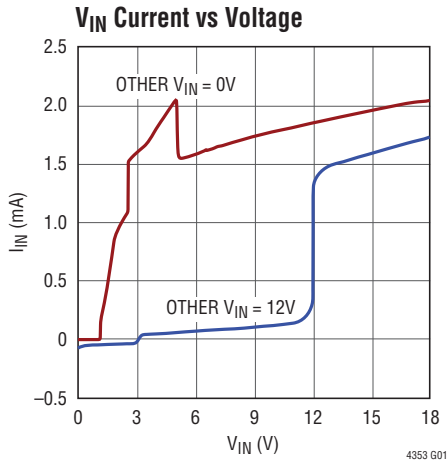
**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

**Note 3:** Internal clamps limit the GATE and CPO pins to a minimum of  $10\text{V}$  above, and a diode below the corresponding  $V_{IN}$  pin. Driving these pins to voltages beyond the clamp may damage the device.

## TYPICAL PERFORMANCE CHARACTERISTICS

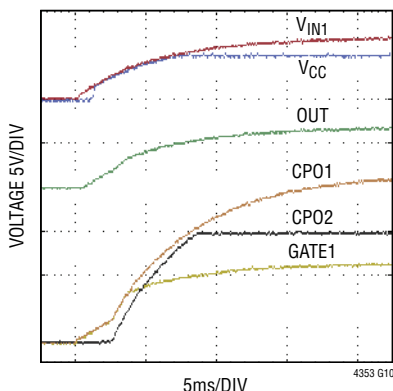
$T_A = 25^\circ\text{C}$ ,  $V_{IN1} = V_{IN2} = 12\text{V}$ ,  $\text{OUT} = V_{IN}$ ,  $V_{CC}$  open, unless otherwise noted.



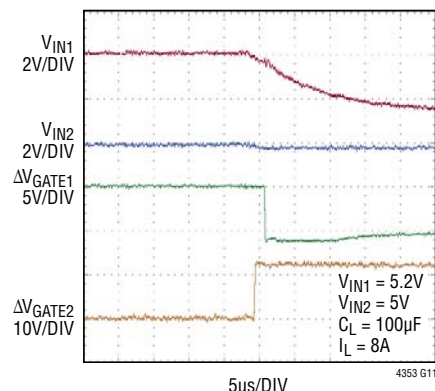
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{IN1} = V_{IN2} = 12\text{V}$ ,  $\text{OUT} = V_{IN}$ ,  $V_{CC}$  open, unless otherwise noted.

Start-Up Waveform on  $V_{IN1}$   
Power-Up



Fast Gate Switchover  
From Failing Supply



## PIN FUNCTIONS

**CPO1, CPO2:** Charge Pump Output. Connect a capacitor from this pin to the corresponding  $V_{IN}$  pin. The value of this capacitor should be approximately  $10\times$  the gate capacitance ( $C_{ISS}$ ) of the MOSFET switch. The charge stored on this capacitor is used to pull-up the gate during a fast turn-on. Leave this pin open if fast turn-on is not needed.

**$\overline{\text{EN1}}$ ,  $\overline{\text{EN2}}$ :** Enable Input. Keep this pin below 0.6V to enable diode control on the corresponding supply. Driving this pin high shuts off the MOSFET gate (current can still flow through its body diode). The comparator has a built-in hysteresis of 8mV. Having both  $\overline{\text{EN}}$  pins high lowers the current consumption of the controller.

**Exposed Pad (DE Package Only):** This pin may be left open or connected to device ground.

**GATE1, GATE2:** MOSFET Gate Drive Output. Connect this pin to the gate of the external N-channel MOSFET switch. An internal clamp limits the gate voltage to 12V above, and a diode below the input supply. During fast turn-on, a 1.4A pull-up current charges GATE from CPO. During fast turn-off, a 1.4A pull-down current discharges GATE to  $V_{IN}$ .

**GND:** Device Ground.

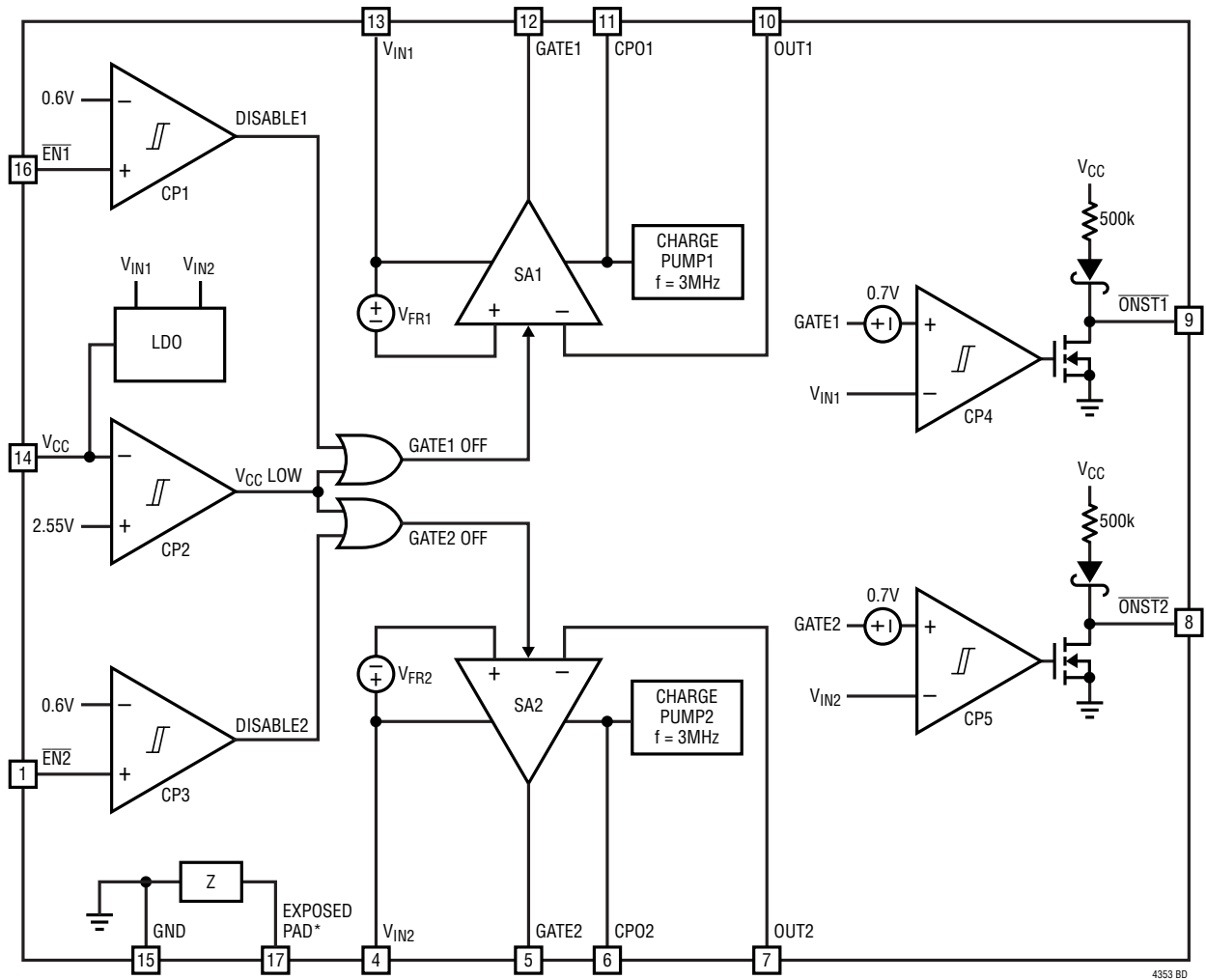
**$\overline{\text{ONST1}}$ ,  $\overline{\text{ONST2}}$ :** MOSFET Status Output. This pin is pulled low by an internal switch when GATE is more than 0.7V above  $V_{IN}$  to indicate an on MOSFET. An internal 500k resistor pulls this pin up to a diode below  $V_{CC}$ . It may be pulled above  $V_{CC}$  using an external pull-up. Tie to GND or leave open if unused.

**OUT1, OUT2:** Output Voltage Sense Input. Connect this pin to the load side of the MOSFET. The voltage sensed at this pin is used to control the MOSFET gate.

**$V_{CC}$ :** Low Voltage Supply. Connect a 0.1 $\mu\text{F}$  capacitor from this pin to ground. For  $V_{IN} \geq 2.9\text{V}$ , this pin provides decoupling for an internal regulator that generates a 5V supply. For applications where both  $V_{IN} < 2.9\text{V}$ , also connect an external supply voltage in the 2.9V to 6V range to this pin.

**$V_{IN1}$ ,  $V_{IN2}$ :** Voltage Sense and Supply Input. Connect this pin to the supply side of the MOSFET. The low voltage supply  $V_{CC}$  is generated from the higher of  $V_{IN1}$  and  $V_{IN2}$ . The voltage sensed at this pin is used to control the MOSFET gate.

FUNCTIONAL DIAGRAM



\*DE PACKAGE ONLY

4353 BD

## OPERATION

The LTC4353 controls N-channel MOSFETs to emulate two ideal diodes. When enabled, each servo amplifier (SA1, SA2) controls the gate of the external MOSFET to servo its forward voltage drop ( $V_{FWD} = V_{IN} - OUT$ ) to  $V_{FR}$ . The gate voltage rises to enhance the MOSFET if the load current causes the drop to exceed  $V_{FR}$ . For large output currents, the MOSFET gate is driven fully on and the voltage drop is equal to  $I_{FET} \cdot R_{DS(ON)}$ .

In the case of an input supply short-circuit, when the MOSFET is conducting, a large reverse current starts flowing from the load towards the input. SA detects this failure condition as soon as it appears, and turns off the MOSFET by rapidly pulling down its gate.

SA quickly pulls up the gate whenever it senses a large forward voltage drop. An external capacitor between the CPO and  $V_{IN}$  pins is needed for fast gate pull-up. This capacitor

is charged up, at device power-up, by the internal charge pump. The stored charge is used for the fast gate pull-up.

The GATE pin sources current from the CPO pin and sinks current to the  $V_{IN}$  and GND pins. Clamps limit the GATE and CPO voltages to 12V above and a diode below  $V_{IN}$ . Internal switches pull the  $\overline{ONST}$  pins low when the GATE to  $V_{IN}$  voltage exceeds 0.7V to indicate that power is passing through the MOSFET.

LDO is a low dropout regulator that generates a 5V supply at the  $V_{CC}$  pin from the highest  $V_{IN}$  input. When both  $V_{IN}$  are below 2.9V, an external supply in the 2.9V to 6V range is required at the  $V_{CC}$  pin.

$V_{CC}$  and  $\overline{EN}$  pin comparators, CP1 to CP3, control power passage. The MOSFET is held off whenever the  $\overline{EN}$  pin is above 0.6V, or the  $V_{CC}$  pin is below 2.55V. A high on both  $\overline{EN}$  pins lowers the current consumption of the device.

## APPLICATIONS INFORMATION

High availability systems often employ parallel connected power supplies or battery feeds to achieve redundancy and enhance system reliability. ORing diodes have been a popular means of connecting these supplies at the point of load. Diodes followed by storage capacitors also hold up supply voltages when an input voltage sags or has a brownout. The disadvantage of these approaches is the diode's significant forward-voltage drop and the resulting power loss. The LTC4353 solves these problems by using an external N-channel MOSFET as the pass element (see Figure 1). The MOSFET is turned on when power is being passed, allowing for a low voltage drop from the supply to the load. When the input source voltage drops below the output common supply voltage it turns off the MOSFET, thereby matching the function and performance of an ideal diode.

### Power Supply Configuration

The LTC4353 can operate with input supplies down to 0V. This requires powering the  $V_{CC}$  pin with an early external supply in the 2.9V to 6V range. In this range of operation  $V_{IN}$  should be lower than  $V_{CC}$ . If  $V_{CC}$  powers up after  $V_{IN}$  and backfeeding of  $V_{CC}$  by the internal 5V LDO is a concern, then a series resistor (few 100 $\Omega$ ) or Schottky diode limits device power dissipation and backfeeding of a low  $V_{CC}$  supply when any  $V_{IN}$  is high. A 0.1 $\mu$ F bypass capacitor should also be connected between the  $V_{CC}$  and GND pins, close to the device. Figure 2 illustrates this.

If either  $V_{IN}$  operates above 2.9V, the external supply at  $V_{CC}$  is not needed. The 0.1 $\mu$ F capacitor is still required for bypassing.

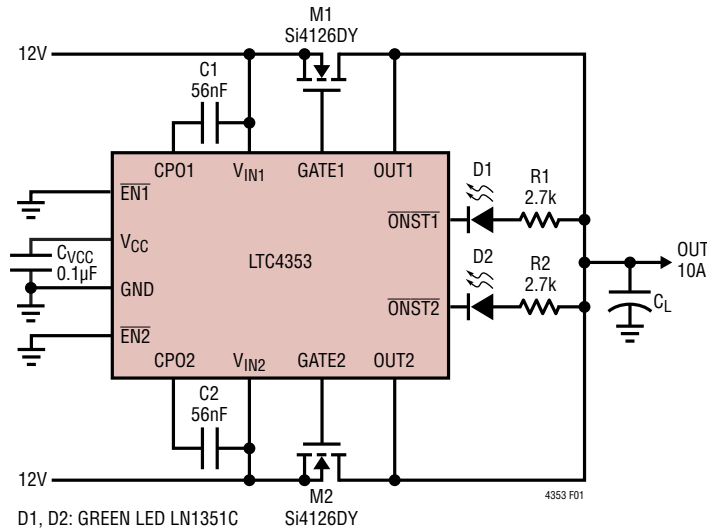


Figure 1. 12V Ideal Diode-OR with Status Lights

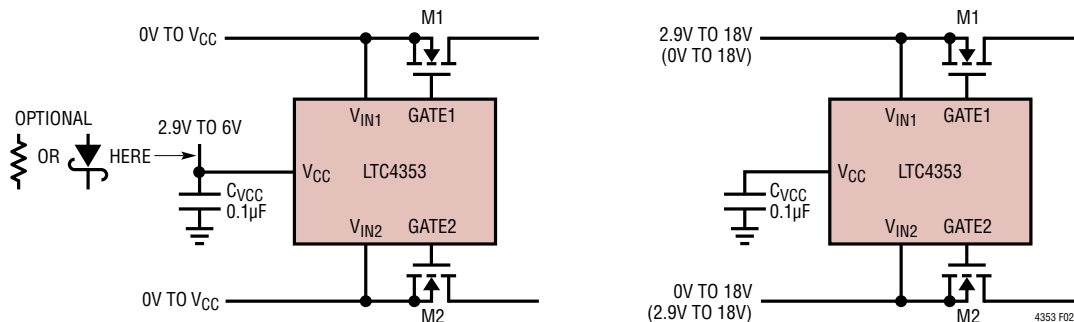


Figure 2. Power Supply Configurations

## APPLICATIONS INFORMATION

### MOSFET Selection

The LTC4353 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFET are its maximum drain-source voltage  $BV_{DSS}$ , maximum gate-source voltage  $V_{GS(MAX)}$ , and the on-resistance  $R_{DS(ON)}$ .

If an input is connected to ground, the full supply voltage can appear across the MOSFET. To survive this, the  $BV_{DSS}$  must be higher than the supply voltages. The  $V_{GS(MAX)}$  rating of the MOSFET should exceed 14V since that is the upper limit of the internal GATE to  $V_{IN}$  clamp. The  $R_{DS(ON)}$  of the MOSFET dictates the maximum voltage drop ( $I_L \cdot R_{DS(ON)}$ ) and the power dissipated ( $I_L^2 \cdot R_{DS(ON)}$ ) in the MOSFET. Note that the minimum MOSFET voltage drop is controlled by the servo amplifier regulation voltage, hence, picking a very low  $R_{DS(ON)}$  (below  $V_{FR}/I_L$ ) may not be beneficial.

### CPO Capacitor Selection

The recommended value of the capacitor between the CPO and  $V_{IN}$  pins is approximately  $10\times$  the input capacitance  $C_{ISS}$  of the MOSFET. A larger capacitor takes a correspondingly longer time to be charged by the internal charge pump. A smaller capacitor suffers more voltage drop during a fast gate turn-on event as it shares charge with the MOSFET gate capacitance.

### External CPO Supply

The internal charge pump takes milliseconds to charge up the CPO capacitor especially during device power-up. This time can be shortened by connecting an external supply to the CPO pin. A series resistor is needed to limit the current into the internal clamp between CPO and  $V_{IN}$  pins. The CPO supply should also be higher than the main input supply to meet the gate drive requirements of the MOSFET. Figure 3 shows such a 3.3V ideal diode application, where a 12V supply is connected to the CPO pins through a 1k resistor. The 1k limits the current into the CPO pin, when the  $V_{IN}$  pin is grounded. For the 8.7V gate drive ( $12V - 3.3V$ ), logic-level MOSFETs would be an appropriate choice for M1 and M2.

### Input Transient Protection

When the capacitances at the input and output are very small, rapid changes in current can cause transients that exceed the 24V absolute maximum rating of the  $V_{IN}$  and OUT pins. In ORing applications, one surge suppressor connected from OUT to ground clamps all the inputs. In the absence of a surge suppressor, an output capacitance of  $10\mu F$  is sufficient in most applications to prevent the transient from exceeding 24V.

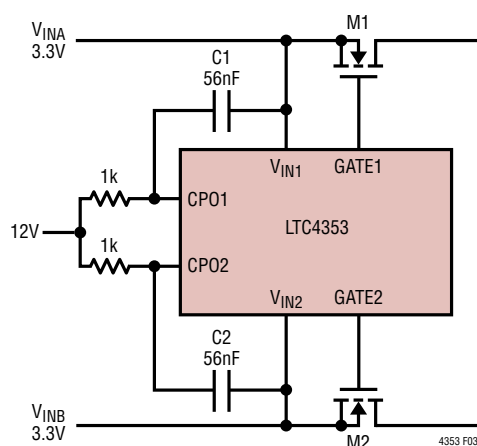


Figure 3. 3.3V Ideal Diode with External 12V Supply Powering CPO for Faster Start-Up and Refresh

## APPLICATIONS INFORMATION

### Design Example

The following design example demonstrates the calculations involved for selecting components in a 12V system with 10A maximum load current (see Figure 1).

First, calculate the  $R_{DS(ON)}$  of the MOSFET to achieve the desired forward drop at full load. Assuming a  $V_{DROP}$  of 30mV:

$$R_{DS(ON)} \leq \frac{V_{DROP}}{I_{LOAD}} = \frac{30mV}{10A} = 3m\Omega$$

The Si4126DY offers a good solution in a SO-8 sized package with a 2.8m $\Omega$  maximum  $R_{DS(ON)}$ , 30V  $BV_{DSS}$ , and 20V  $V_{GS(MAX)}$ . The maximum power dissipation in the MOSFET is:

$$P = I_{LOAD}^2 \cdot R_{DS(ON)} = (10A)^2 \cdot 2.8m\Omega = 0.3W$$

With a maximum steady-state thermal resistance  $\theta_{JA}$  of 35°C/W, 0.3W causes a modest 11°C rise in junction temperature of the Si4126DY above the ambient.

The input capacitance,  $C_{ISS}$ , of the Si4126DY is about 5500pF. Following the 10 $\times$  recommendation, a 56nF capacitor is selected for C1 and C2.

LEDs, D1 and D2, require around 3mA for good luminous intensity. Accounting for a 2V diode drop and 0.6V  $V_{OL}$ , R1 and R2 are set to 2.7k.

### PCB Layout Considerations

Connect the  $V_{IN}$  and OUT pin traces as close as possible to the MOSFET's terminals. Keep the traces to the MOSFET wide and short to minimize resistive losses. The PCB traces associated with the power path through the MOSFET should have low resistance (see Figure 4).

It is also important to put  $C_{VCC}$ , the bypass capacitor for the  $V_{CC}$  pin, as close as possible between  $V_{CC}$  and GND. Place C1 and C2 near the CPO and  $V_{IN}$  pins. Surge suppressors, when used, should be mounted close to the LTC4353 using short lead lengths.

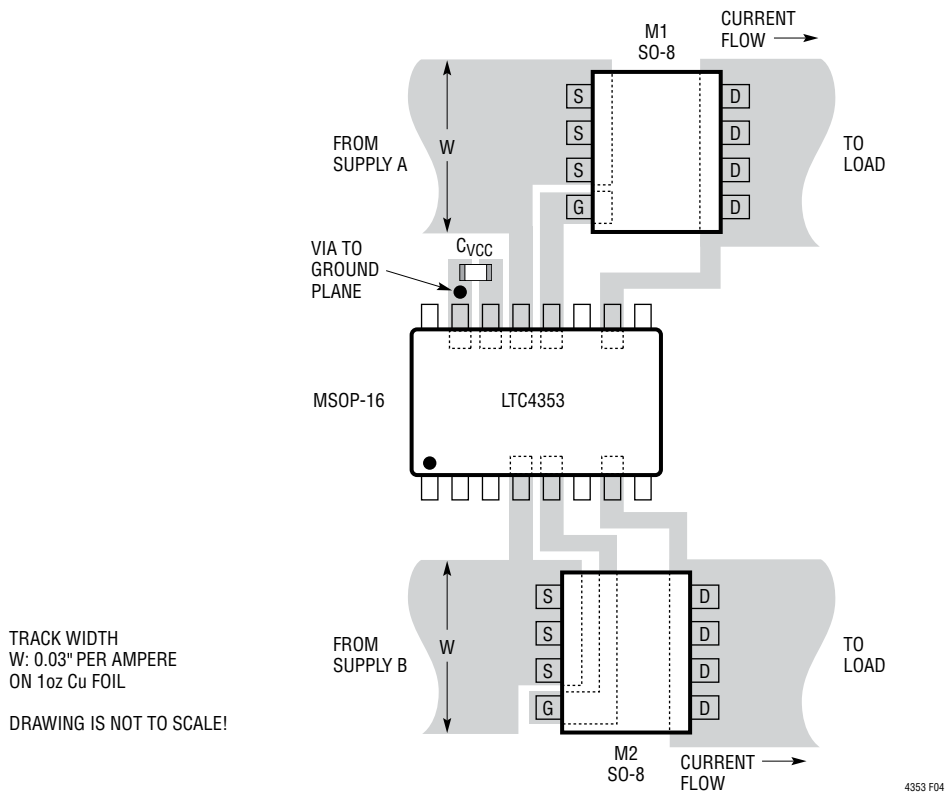
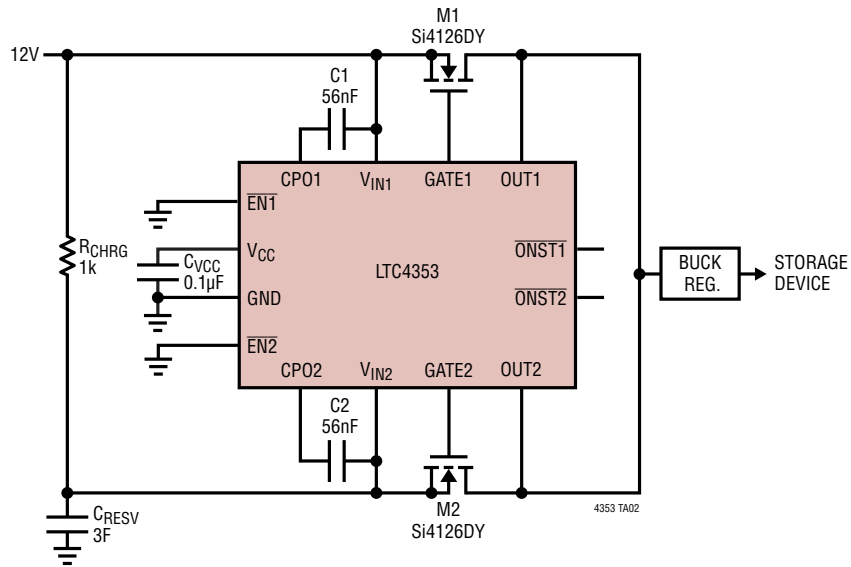


Figure 4. Recommended PCB Layout for M1, M2,  $C_{VCC}$

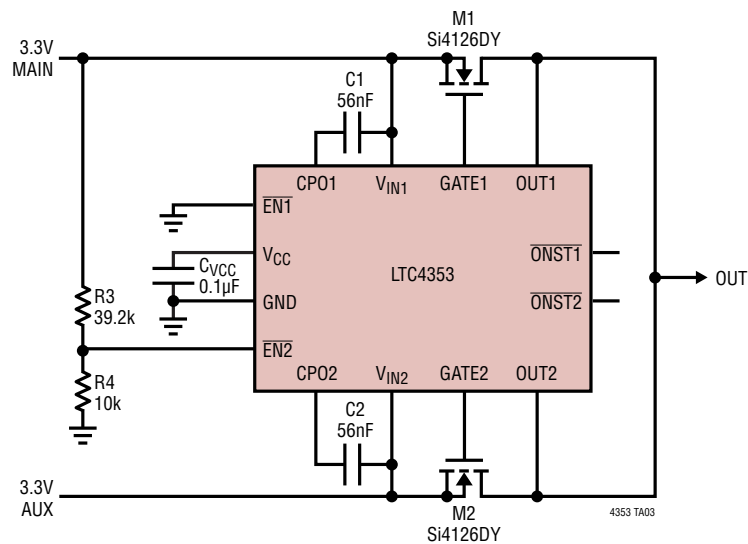
## TYPICAL APPLICATIONS

### 12V Supply with Capacitive Reservoir for Data Backup on Power Fail for Disk Drive and Solid-State Drive Applications



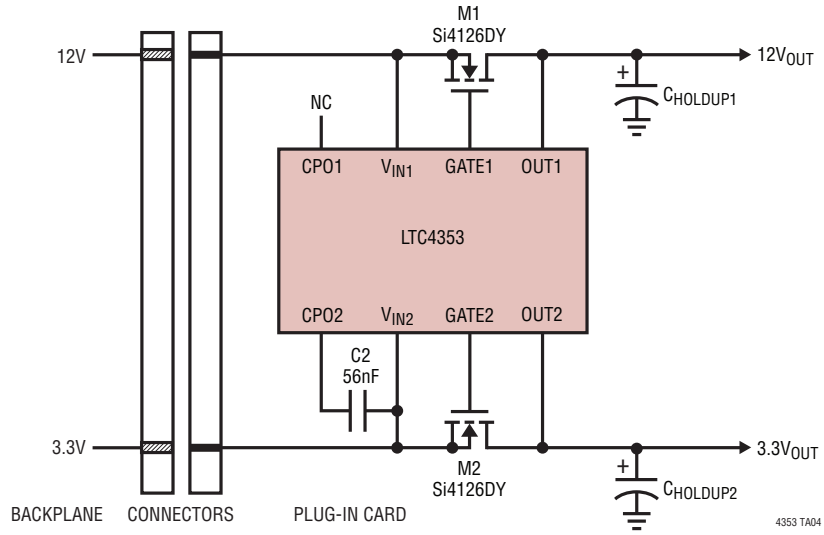
CRESV: 3 PARALLEL STRINGS, EACH WITH 3 SERIES PM-5R0V305-R

### 3.3V Main and Auxiliary Supply Diode-OR (Auxiliary Ideal Diode Disabled if Main Above 2.95V)



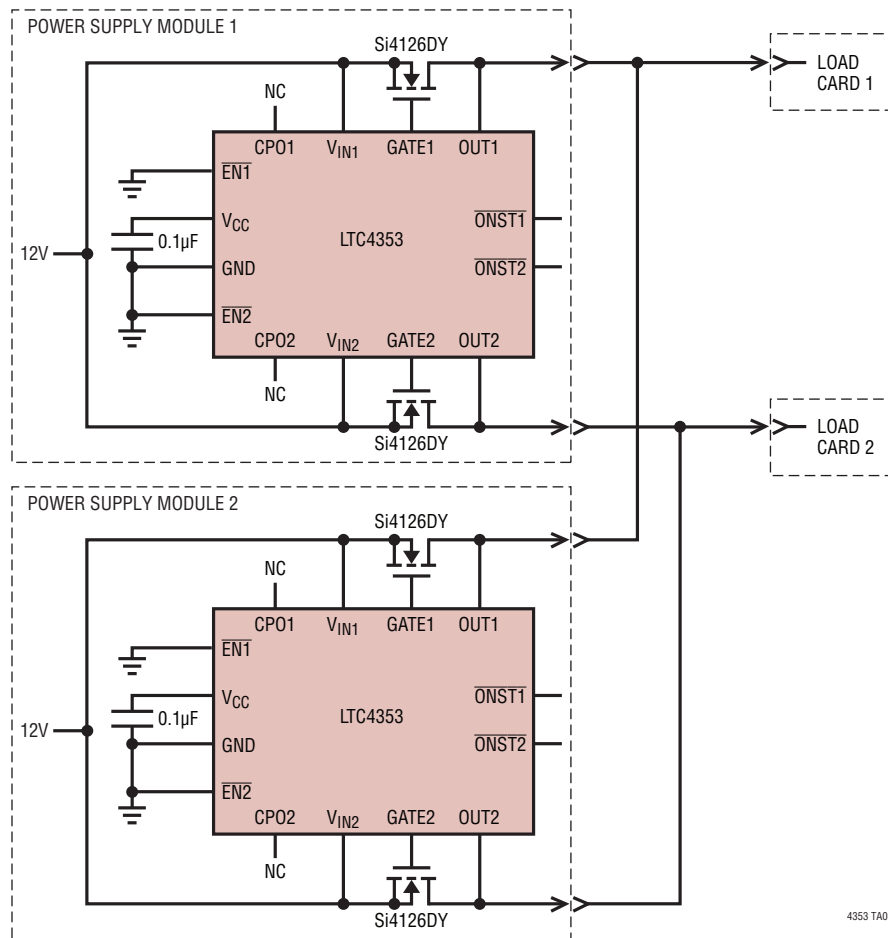
## TYPICAL APPLICATIONS

Plug-in Card Supply Holdup Using Ideal Diode at 12V and 3.3V Inputs



# TYPICAL APPLICATIONS

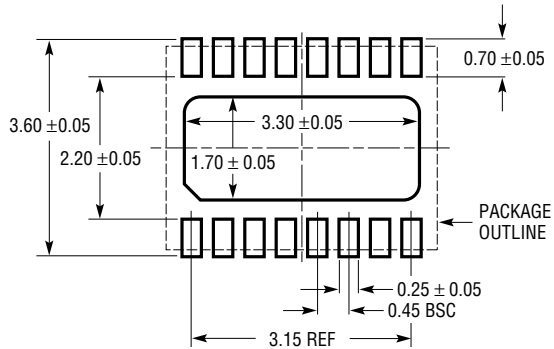
Redundant Power Supply System with ORing on Backplane, as in MicroTCA



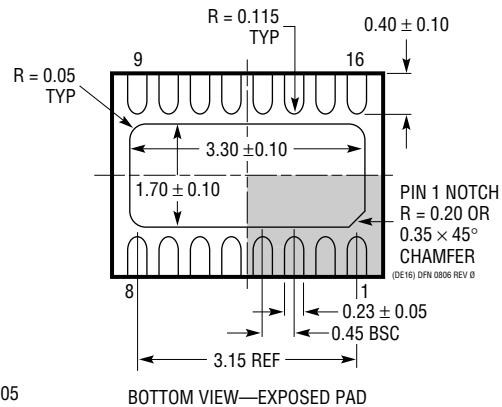
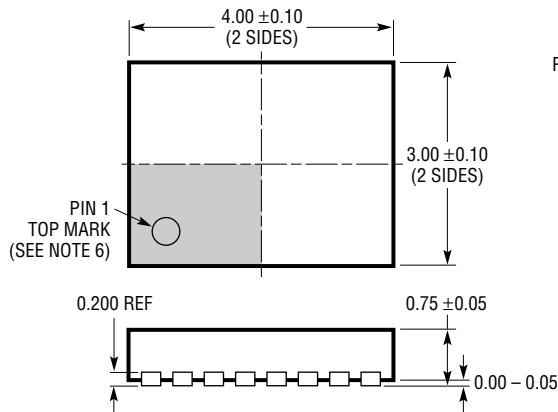
## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

**DE Package**  
**16-Lead Plastic DFN (4mm × 3mm)**  
 (Reference LTC DWG # 05-08-1732 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



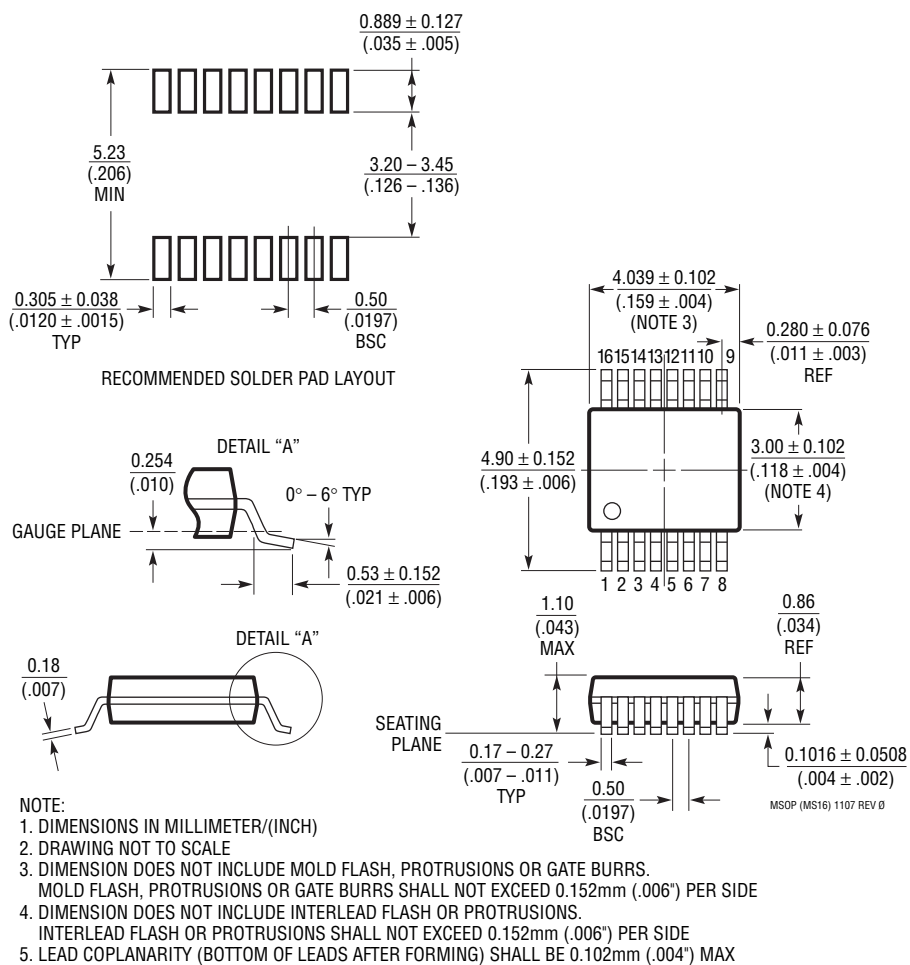
- NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

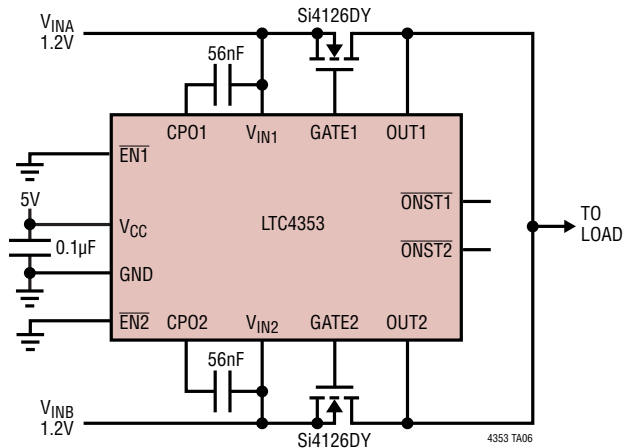
### MS Package 16-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1669 Rev 0)



## TYPICAL APPLICATION

## 1.2V Ideal Diode-OR



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1473/LTC1473L	Dual PowerPath™ Switch Driver	N-Channel, 4.75V to 30V/3.3V to 10V, SSOP-16 Package
LTC1479	PowerPath Controller for Dual Battery Systems	Three N-Channel Drivers, 6V to 28V, SSOP-36 Package
LTC4352	Low Voltage Ideal Diode Controller with Monitoring	N-Channel, 0V to 18V, UV, OV, MSOP-12 and DFN-12 Packages
LTC4354	Negative Voltage Diode-OR Controller and Monitor	Dual N-Channel, -4.5V to -80V, SO-8 and DFN-8 Packages
LTC4355	Positive High Voltage Ideal Diode-OR with Supply and Fuse Monitors	Dual N-Channel, 9V to 80V, SO-16 and DFN-14 Packages
LTC4357	Positive High Voltage Ideal Diode Controller	N-Channel, 9V to 80V, MSOP-8 and DFN-6 Packages
LTC4358	5A Ideal Diode	Internal N-Channel, 9V to 26.5V, TSSOP-16 and DFN-14 Packages
LTC4370	Two-Supply Diode-OR Current Sharing Controller	Dual N-Channel, 0V to 18V, MSOP-16 and DFN-16 Packages
LTC4411	2.6A Low Loss Ideal Diode in ThinSOT™	Internal P-Channel, 2.6V to 5.5V, 40µA I <sub>Q</sub> , SOT-23 Package
LTC4412/LTC4412HV	Low Loss PowerPath Controller in ThinSOT	P-Channel, 2.5V to 28V/36V, 11µA I <sub>Q</sub> , SOT-23 Package
LTC4413/LTC4413-1	Dual 2.6A, 2.5V to 5.5V, Ideal Diodes in DFN-10	Dual Internal P-Channel, 2.5V to 5.5V, DFN-10 Package
LTC4414	36V Low Loss PowerPath Controller for Large P-Channel MOSFETs	P-Channel, 3V to 36V, 30µA I <sub>Q</sub> , MSOP-8 Package
LTC4415	Dual 4A Ideal Diodes with Adjustable Current Limit	Dual P-Channel 50mΩ Ideal Diodes, 1.7V to 5.5V, 15mV Forward Drop, MSOP-16 and DFN-16 Packages
LTC4416/LTC4416-1	36V Low Loss Dual PowerPath Controller for Large P-Channel MOSFETs	Dual P-Channel, 3.6V to 36V, 70µA I <sub>Q</sub> , MSOP-10 Package

## Looking for pricing, stock, or lifecycle information?

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- ⊖ [Analog Devices Inc. Information](#)

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