



# THE DATASHEET OF BTS4300SGAXUMA1



# BTS4300SGA

Smart High-Side Power Switch

Automotive Power



Never stop thinking

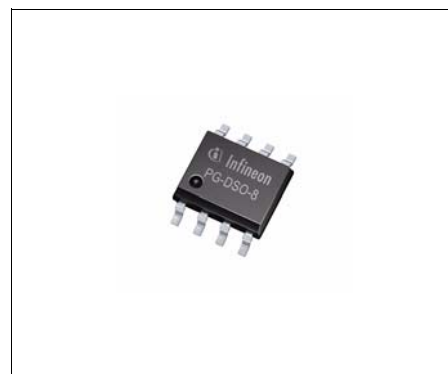
<b>1</b>	<b>Overview</b>	<b>3</b>
<b>2</b>	<b>Block Diagram</b>	<b>5</b>
<b>3</b>	<b>Pin Configuration</b>	<b>6</b>
3.1	Pin Assignment	6
3.2	Pin Definitions and Functions	6
3.3	Voltage and Current Definition	7
<b>4</b>	<b>General Product Characteristics</b>	<b>8</b>
4.1	Absolute Maximum Ratings	8
4.2	Functional Range	9
4.3	Thermal Resistance	9
<b>5</b>	<b>Power Stage</b>	<b>10</b>
5.1	Output ON-State Resistance	10
5.2	Turn ON / OFF Characteristics	10
5.3	Inductive Output Clamp	11
5.4	Electrical Characteristics Power Stage	12
<b>6</b>	<b>Protection Mechanisms</b>	<b>13</b>
6.1	Undervoltage Protection	13
6.2	Overvoltage Protection	13
6.3	Reverse Polarity Protection	14
6.4	Overload Protection	14
6.5	Electrical Characteristics Protection Functions	16
<b>7</b>	<b>Diagnostic Mechanism</b>	<b>17</b>
7.1	ST Pin	17
7.2	ST Signal in Case of Failures	17
7.2.1	Diagnostic in Open Load, Channel OFF	17
7.2.2	ST Signal in case of Over Temperature	19
7.3	Electrical Characteristics Diagnostic Functions	20
<b>8</b>	<b>Input Pin</b>	<b>21</b>
8.1	Input Circuitry	21
8.2	Electrical Characteristics	21
<b>9</b>	<b>Application Information</b>	<b>22</b>
9.1	Further Application Information	22
<b>10</b>	<b>Package Outlines</b>	<b>23</b>
<b>11</b>	<b>Revision History</b>	<b>24</b>



## 1 Overview

### Basic Features

- Fit for 12V application
- One Channel device
- Very Low Stand-by Current
- CMOS Compatible Inputs
- Electrostatic Discharge Protection (ESD)
- Optimized Electromagnetic Compatibility
- Logic ground independent from load ground
- Very low leakage current from OUT to the load in OFF state
- Green Product (RoHS compliant)
- AEC Qualified


**PG-DSO-8-24**

### Description

The BTS4300SGA is a single channel Smart High-Side Power Switch. It is embedded in a PG-DSO-8-24 package, providing protective functions and diagnostics. The power transistor is built by a N-channel power MOSFET with charge pump. The device is monolithically integrated in Smart technology. It is specially designed to drive Relay or LED in the harsh automotive environment.

**Table 1 Electrical Parameters (short form)**

Parameter	Symbol	Value
Operating voltage range	$V_{SOP}$	5V .... 34V
Over voltage protection	$V_{S(AZ)}$	41V
Maximum ON State resistance at $T_j = 150^{\circ}\text{C}$	$R_{DS(ON)}$	600m $\Omega$
Nominal load current	$I_{L(nom)}$	0.4A
Minimum current limitation	$I_{L\_SCR}$	0.4A
Standby current for the whole device with load	$I_{S(off)}$	26 $\mu\text{A}$
Maximum reverse battery voltage	$-V_{S(REV)}$	32V

### Diagnostic Feature

- Open drain diagnostic output
- Open load detection in OFF state

Type	Package	Marking
BTS4300SGA	PG-DSO-8-24	4300SGA

**Protection Functions**

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown with restart
- Overvoltage protection (including load dump)
- Loss of ground and loss of battery protection
- Electrostatic discharge protection (ESD)

**Application**

- All types of relays, resistive and capacitive loads

## 2 Block Diagram

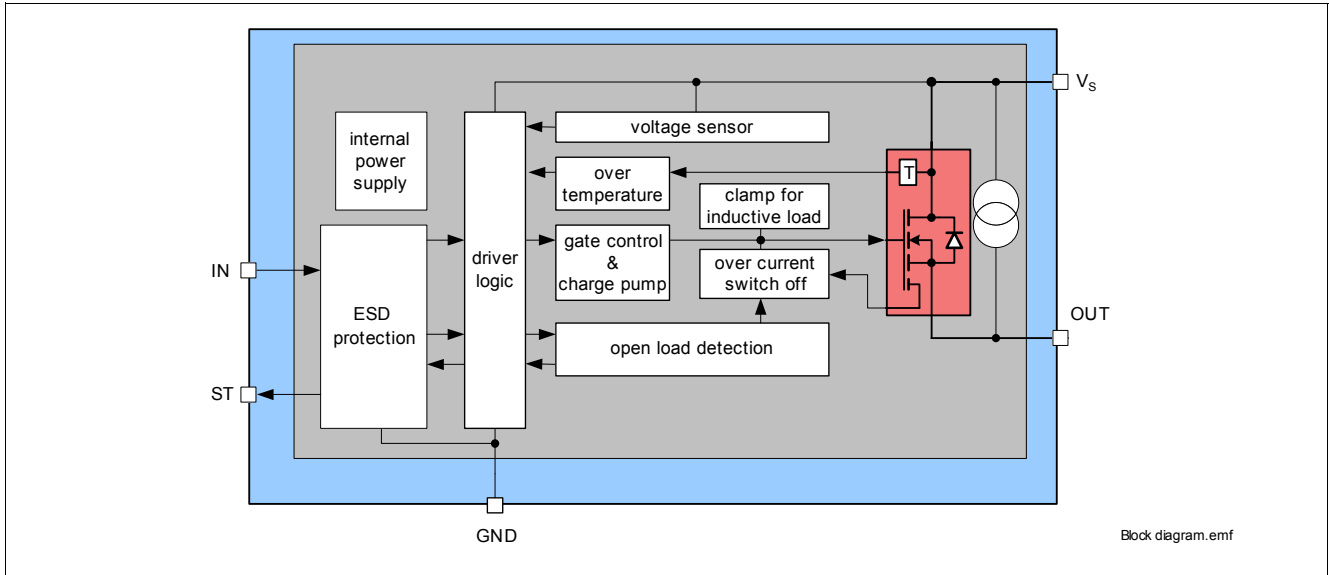


Figure 1 Block diagram for the BTS4300SGA

### 3 Pin Configuration

#### 3.1 Pin Assignment

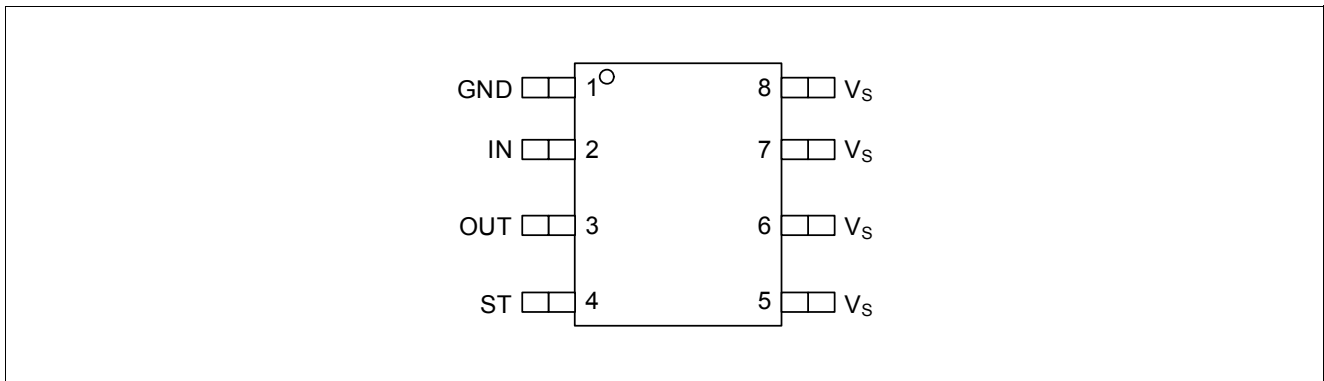


Figure 2 Pin Configuration

#### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	<b>Ground;</b> Ground connection
2	IN	<b>Input channel;</b> Input signal. Activate the channel in case of logic high level
3	OUT	<b>Output;</b> Protected High side power output channel
4	ST	<b>Diagnostic feedback;</b> of channel. Open drain.
5, 6, 7, 8	V <sub>S</sub>	<b>Battery voltage;</b> Design the wiring for the simultaneous max. short circuit current and also for low thermal resistance

### 3.3 Voltage and Current Definition

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

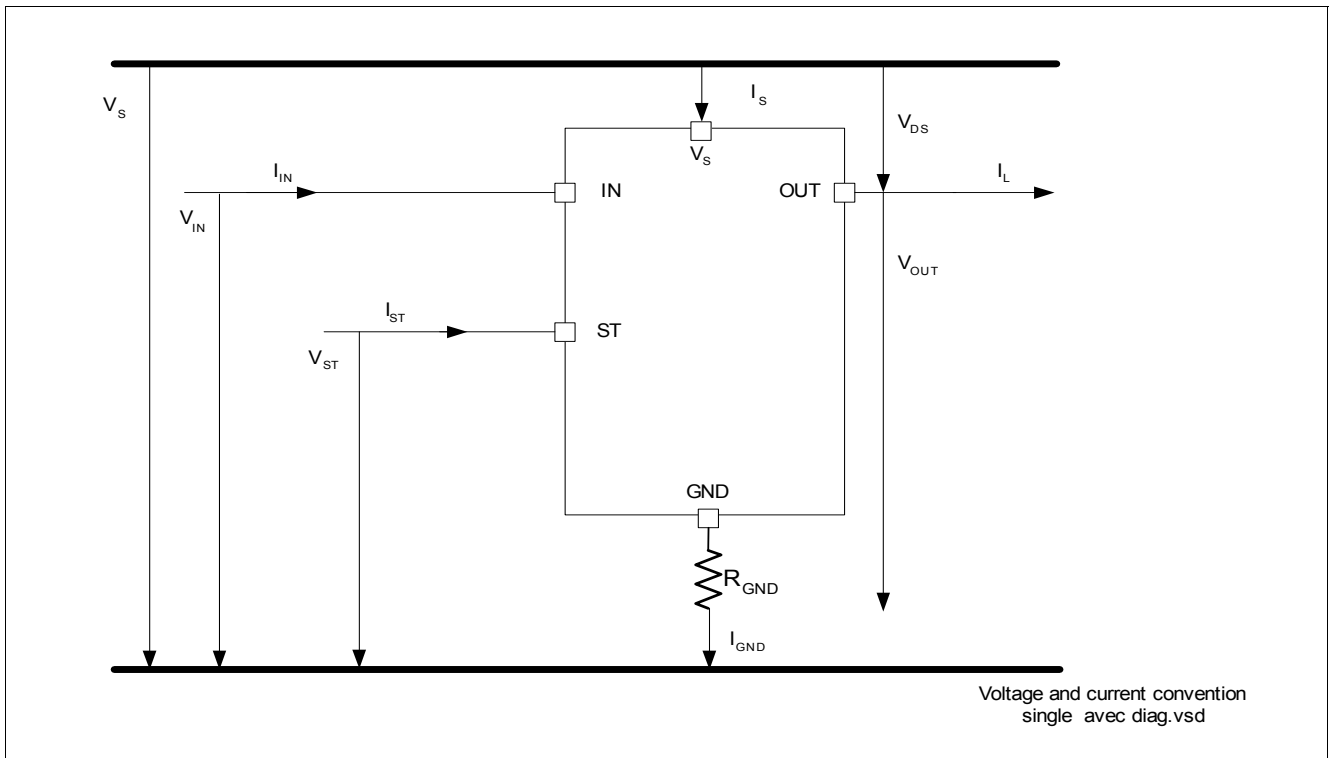


Figure 3 Voltage and current definition

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = 25\text{ °C}$ ; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
<b>Voltages</b>						
4.1.1	Supply voltage	$V_S$	–	40	V	–
4.1.2	Reverse polarity Voltage	$-V_{S(REV)}$	0	32	V	–
4.1.3	Supply voltage for short circuit protection	$V_{bat(SC)}$	0	28	V	$R_{ECU} = 20\text{m}\Omega$ , $R_{Cable} = 16\text{m}\Omega/\text{m}$ , $L_{Cable} = 1\mu\text{H}/\text{m}$ , $\ell = 0$ or $5\text{m}$ <sup>2)</sup> see <a href="#">Chapter 6</a>
<b>Input pins</b>						
4.1.4	Voltage at INPUT pins	$V_{IN}$	-10	16	V	–
4.1.5	Current through INPUT pins	$I_{IN}$	-5	5	mA	–
<b>Power stage</b>						
4.1.6	Load current	$ I_L $	–	$I_{L(LIM)}$	A	–
4.1.7	Power dissipation (DC),	$P_{TOT}$	–	0.8	W	$T_A = 85\text{ °C}$ , $T_j < 150\text{ °C}$
4.1.8	Inductive load switch off energy dissipation, Single pulse	$E_{AS}$	–	800	mJ	$T_j = 150\text{ °C}$ , $V_S = 13.5\text{V}$ , $I_L = 0.3\text{A}$
<b>Temperatures</b>						
4.1.9	Junction Temperature	$T_j$	-40	150	°C	–
4.1.10	Storage Temperature	$T_{stg}$	-55	150	°C	–
<b>ESD Susceptibility</b>						
4.1.11	ESD Resistivity IN pin	$V_{ESD}$	-1	1	kV	HBM <sup>3)</sup>
4.1.12	ESD Resistivity all other pins	$V_{ESD}$	-5	5	kV	HBM <sup>3)</sup>

1) Not subject to production test, specified by design

2) In accordance to AEC Q100-012 and AEC Q101-006

3) ESD susceptibility HBM according to EIA/JESD 22-A 114B

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Operating Voltage	$V_{SOP}$	5	34	V	$V_{IN} = 4.5V$ , $R_L = 47\Omega$ , $V_{DS} < 0.5V$
4.2.2	Undervoltage shutdown	$V_{SUV}$	–	5	V	–
4.2.3	Undervoltage restart of charge pump	$V_{S(u\ cp)}$	–	5.5	V	–
4.2.4	Operating current	$I_{GND}$		1.3	mA	$V_{IN} = 5V$
4.2.5	Standby current	$I_{S(OFF)}$	–	26	$\mu A$	$T_J = 150^\circ C$ , $V_{IN} = 0V$

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Soldering Point	$R_{thJC}$	–	–	15	K/W	– <sup>1)</sup>
4.3.2	Junction to Ambient: channel active	$R_{thJA}$	–	83	–	K/W	with 6cm <sup>2</sup> cooling area <sup>1)</sup>

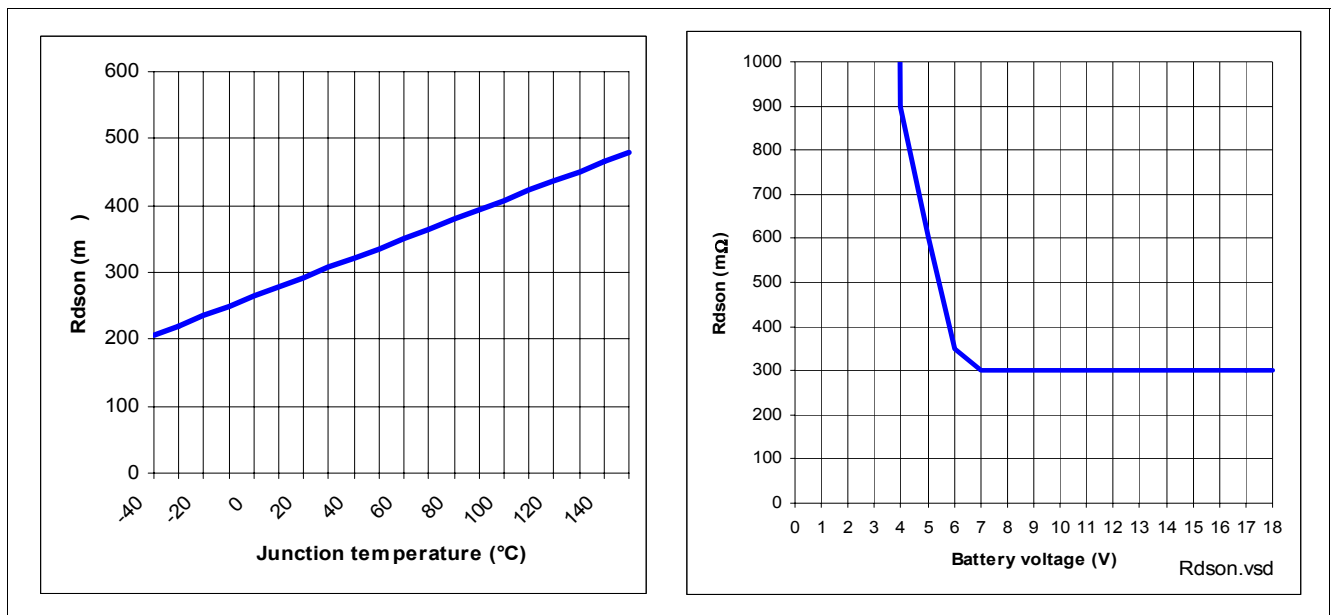
1) Not subject to production test, specified by design

## 5 Power Stage

The power stage is built by an N-channel vertical power MOSFET (DMOS) with charge pump.

### 5.1 Output ON-State Resistance

The ON-state resistance  $R_{DS(ON)}$  depends on the supply voltage as well as the junction temperature  $T_j$ . **Figure 4** shows the dependencies for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.3**.

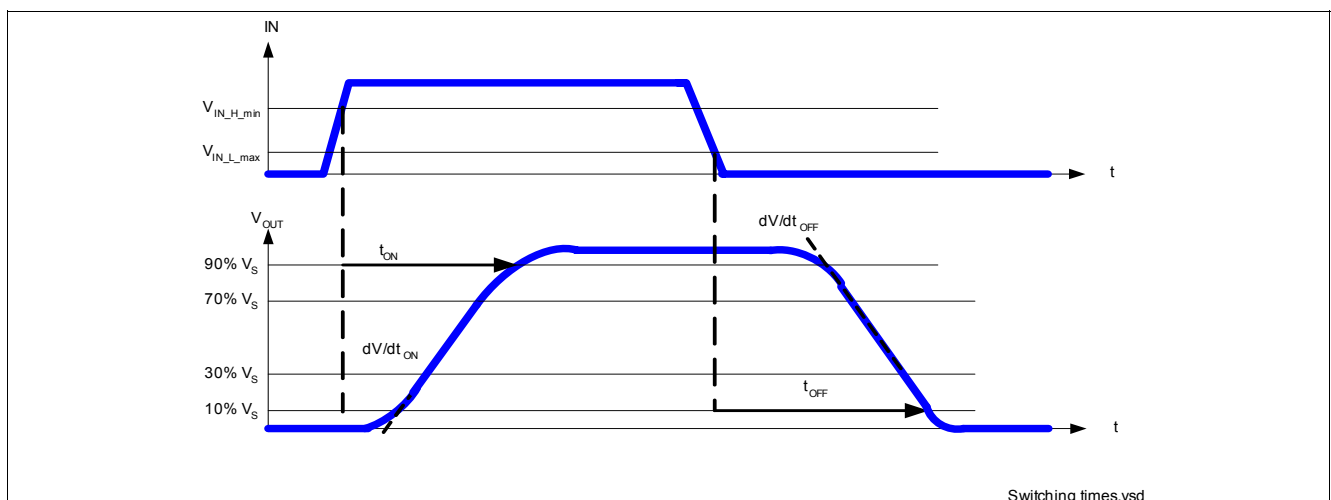


**Figure 4** Typical ON-state resistance

A high signal (See **Chapter 8**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

### 5.2 Turn ON / OFF Characteristics

**Figure 5** shows the typical timing when switching a resistive load.



**Figure 5** Turn ON/OFF (resistive) timing

### 5.3 Inductive Output Clamp

When switching OFF inductive loads with high side switches, the voltage  $V_{OUT}$  drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, there is a voltage clamp mechanism implemented that keeps the negative output voltage at a certain level ( $V_S - V_{DS(AZ)}$ ). Please refer to [Figure 6](#) and [Figure 7](#) for details. Nevertheless, the maximum allowed load inductance is limited.

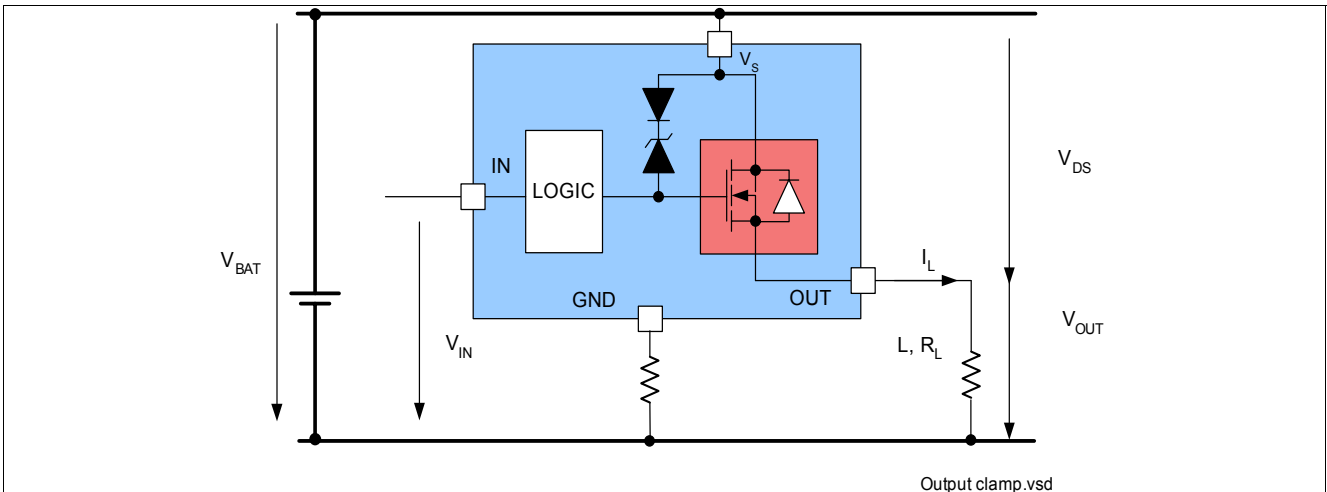


Figure 6 Output clamp

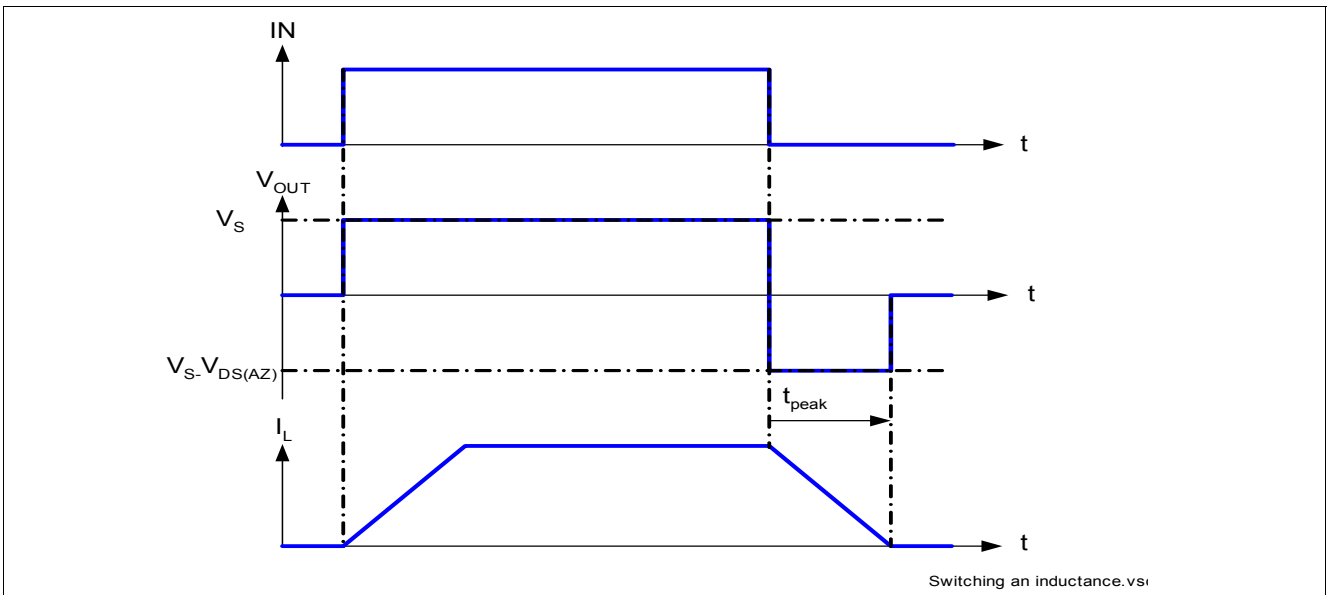


Figure 7 Switching in inductance timing

#### Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTS4300SGA. This energy can be calculated with following equation:

$$E = V_{DS(AZ)} \times \frac{L}{R_L} \times \left[ \frac{V_S - V_{DS(AZ)}}{R_L} + \ln\left(\frac{R_L \times I_L}{V_S - V_{DS(AZ)}}\right) + I_L \right]$$

Following equation simplifies under the assumption of  $R_L = 0\Omega$ .

$$E = \frac{1}{2} \times LI^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right)$$

The energy, which is converted into heat, is limited by the thermal design of the component.

## 5.4 Electrical Characteristics Power Stage

### Electrical Characteristics: Power stage

$V_S = 13.5V$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $+150\text{ }^\circ\text{C}$ , (unless otherwise specified). Typical values are given at  $T_j = 25\text{ }^\circ\text{C}$

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	ON-state resistance per channel	$R_{DS(ON)}$	–	300	–	m $\Omega$	$T_j = 25\text{ }^\circ\text{C}$ , <sup>1)</sup> $I_L = 0.3A$ , $V_{BB} = 9\text{...}40V$ $V_{IN} = 5V$ , See <a href="#">Figure 4</a>
			–	480	600		
5.4.2	Nominal load current	$I_{L(nom)}$	0.4	–	–	A	$T_A = 85\text{ }^\circ\text{C}$ <sup>1)</sup> , $T_j < 150\text{ }^\circ\text{C}$
5.4.3	Drain to Source Clamping Voltage $V_{DS(AZ)} = V_S - V_{OUT}$	$V_{DS(AZ)}$	41	47	–	V	$I_{DS} = 4mA$ <sup>2)</sup>
5.4.4	Output leakage current	$I_{L(OFF)}$	–	–	12	$\mu A$	$V_{IN} = 0V$ , $V_{OUT} = 0V$
5.4.5	Slew rate ON 10% to 30% $V_{OUT}$	$dV/dt_{ON}$	–	–	2	V/ $\mu s$	$R_L = 47\Omega$ , $V_S = 13.5V$ , See <a href="#">Figure 5</a>
5.4.6	Slew rate OFF 70% to 40% $V_{OUT}$	$-dV/dt_{OFF}$	–	–	2	V/ $\mu s$	
5.4.7	Turn-ON time to 90% $V_{OUT}$ Includes propagation delay	$t_{ON}$	–	–	140	$\mu s$	
5.4.8	Turn-OFF time to 10% $V_{OUT}$ Includes propagation delay	$t_{OFF}$	–	–	170	$\mu s$	

1) Not subject to production test, specified by design

2) Voltage is measured by forcing  $I_{DS}$ .

## 6 Protection Mechanisms

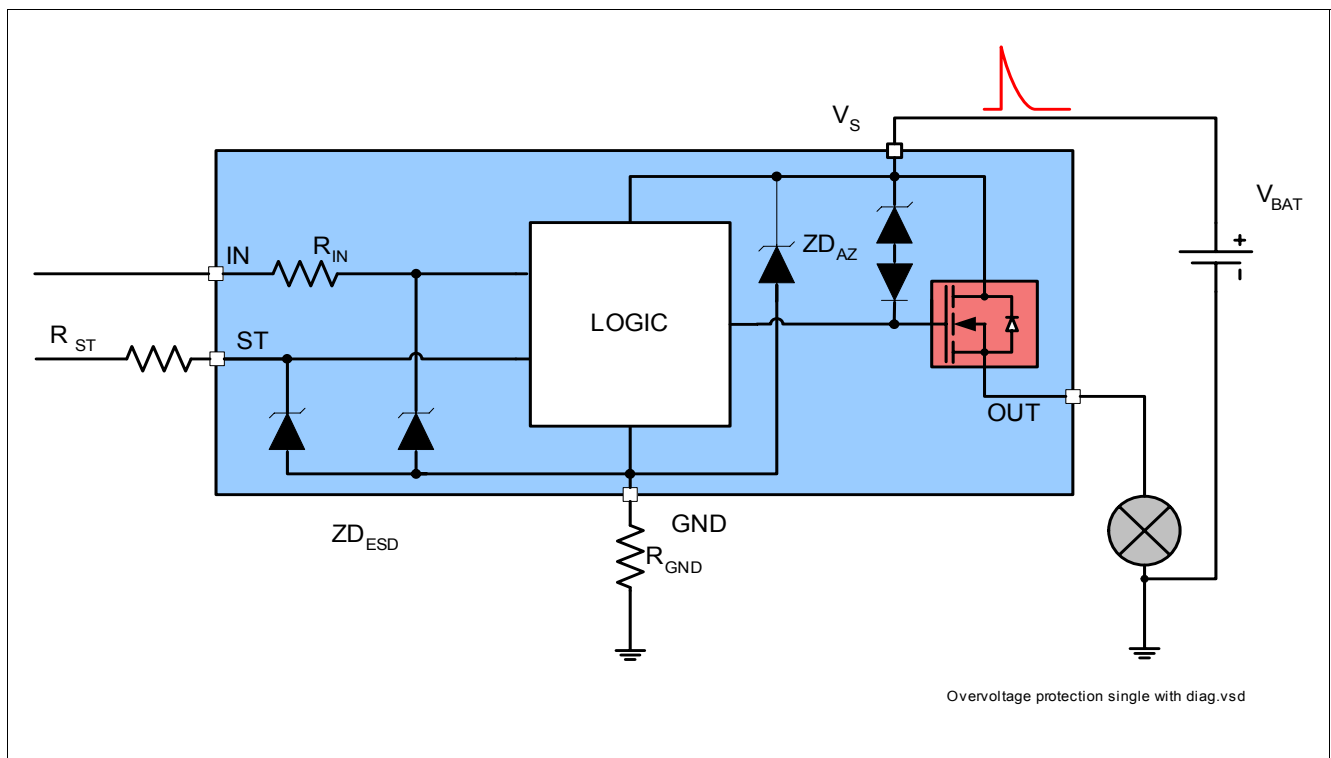
The device provides embedded protective functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

### 6.1 Undervoltage Protection

Below  $V_{SOP\_min}$ , the under voltage mechanism is met. If the supply voltage is below the under voltage mechanism, the device is OFF (turns OFF). As soon as the supply voltage is above the under voltage mechanism, then the device can be switched ON and the protection functions are operational.

### 6.2 Overvoltage Protection

There is a clamp mechanism for over voltage protection. To guarantee this mechanism operates properly in the application, the current in the zener diode  $Z_{DAZ}$  has to be limited by a ground resistor. **Figure 8** shows a typical application to withstand overvoltage issues. In case of supply greater than  $V_{S(AZ)}$ , the power transistor switches ON and the voltage across logic section is clamped. As a result, the internal ground potential rises to  $V_S - V_{S(AZ)}$ . Due to the ESD zener diodes, the potential at pin IN rises almost to that potential, depending on the impedance of the connected circuitry. Integrated resistors are provided at the IN pin to protect the input circuitry from excessive current flow during this condition.



**Figure 8 Over voltage protection with external components**

In the case the supply voltage is in between of  $V_{S(SC) max}$  and  $V_{DS(AZ)}$ , the output transistor is still operational and follow the input. If the channel is in ON state, parameters are no longer warranted and lifetime is reduced compared to normal mode. This specially impacts the short circuit robustness, as well as the maximum energy  $E_{AS}$  the device can handle.

### 6.3 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logical pins has to be limited to the maximum current described in [Chapter 4.1](#), sometimes with an external resistor. [Figure 9](#) shows a typical application. The  $R_{GND}$  resistor is used to limit the current in the zener protection of the device. Resistors  $R_{IN}$  and  $R_{ST}$  is used to limit the current in the logic of the device and in the ESD protection stage. The recommended value for  $R_{GND}$  is  $150\Omega$ , for  $R_{ST\ 0/1} = 15k\Omega$ . In case the over voltage is not considered in the application,  $R_{GND}$  can be replaced by a Shottky diode.

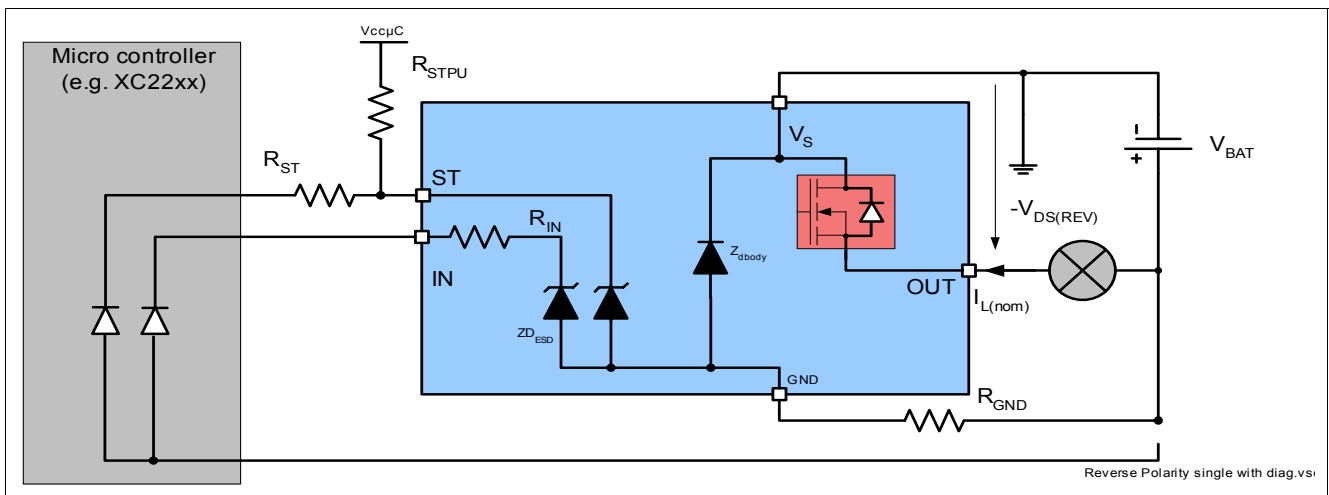


Figure 9 Reverse polarity protection with external components

### 6.4 Overload Protection

In case of overload, or short circuit to ground, the BTS4300SGA offers two protections mechanisms.

#### Current limitation

At first step, the instantaneous power in the switch is maintained to a safe level by limiting the current to the maximum current allowed in the switch  $I_{L(LIM)}$ . During this time, the DMOS temperature is increasing, which affects the current flowing in the DMOS.

#### Thermal protection

At thermal shutdown, the device turns OFF and cools down. A restart mechanism is used, after cooling down, the device restarts and limits the current to  $I_{L(SCR)}$ . [Figure 10](#) shows the behavior of the current limitation as a function of time.

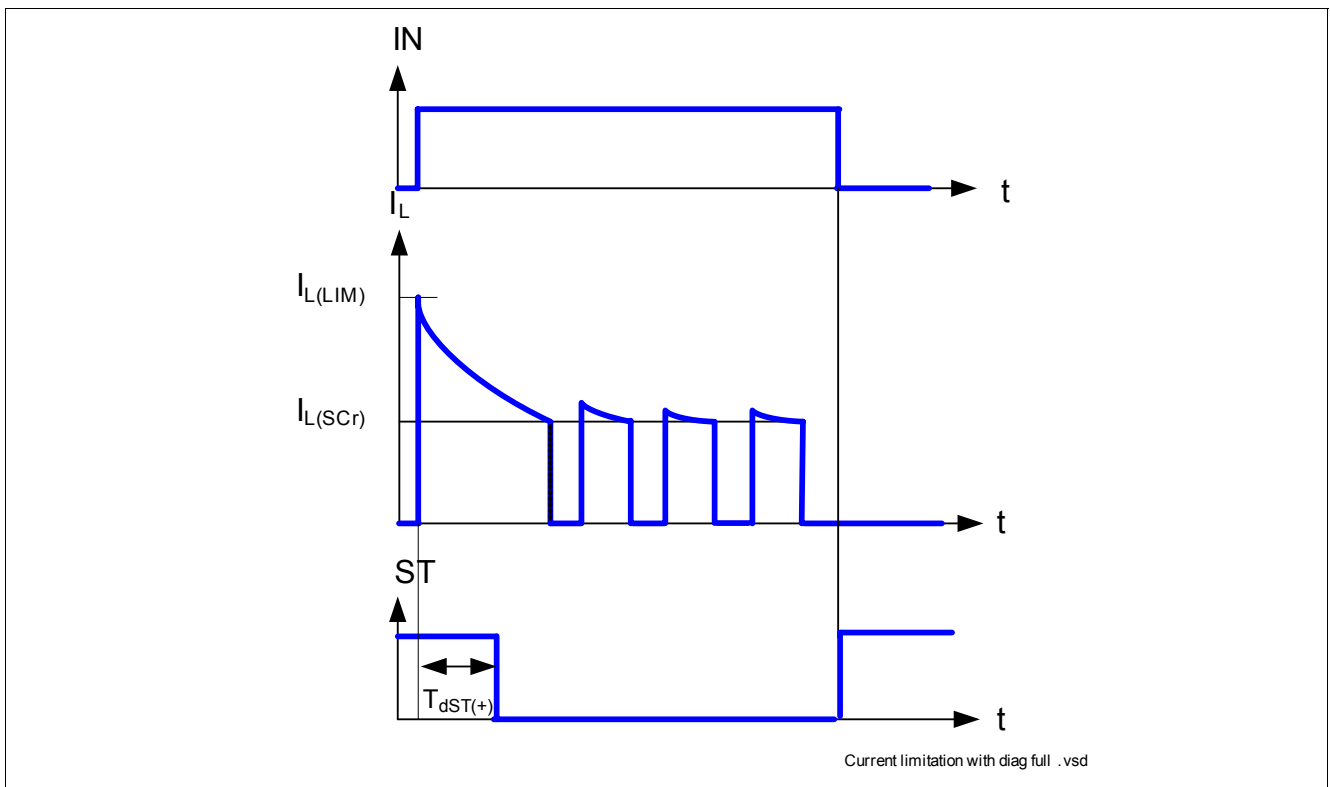


Figure 10 Current limitation function of the time

## 6.5 Electrical Characteristics Protection Functions

### Electrical Characteristics: Protection

$V_S = 13.5V$ ,  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ . Typical values are given at  $T_j = 25\text{ °C}$

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Reverse polarity</b>							
6.5.1	Drain source diode voltage during reverse polarity	$-V_{DS(REV)}$	–	600	–	mV	$T_j = 150\text{ °C}$
<b>Overvoltage</b>							
6.5.2	Over voltage protection	$V_{S(AZ)}$	41	–	–	V	$I_s = 4mA$
<b>Overload condition</b>							
6.5.3	Load current limitation	$I_{L(LIM)}$	– – 0.4	– 1.2 –	2 – –	A	$T_j = -40\text{ °C}$ , $T_j = 25\text{ °C}$ , $T_j = 150\text{ °C}$ , $V_S = 20V$
6.5.4	Repetitive short circuit current limitation	$I_{L(SCR)}$	–	1	–	A	<sup>1)</sup>
6.5.5	Thermal shutdown temperature	$T_{jSC}$	150	–	–	°C	<sup>1)</sup>
6.5.6	Thermal shutdown hysteresis	$\Delta T_{JT}$	–	10	–	K	<sup>1)</sup>

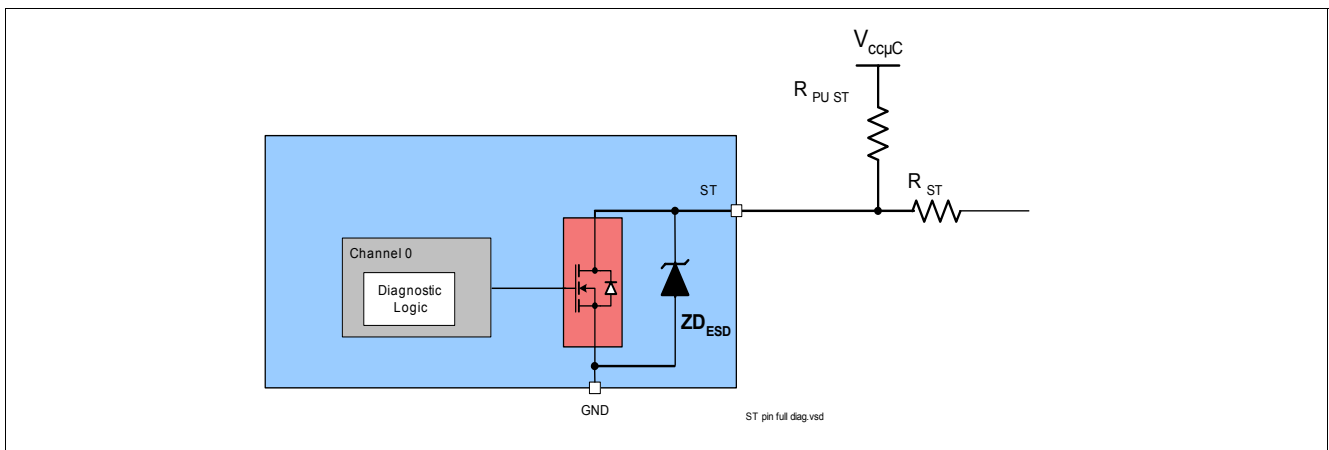
1) Not subject to production test, but specified by design

## 7 Diagnostic Mechanism

For diagnosis purpose, the BTS4300SGA provides a status pin.

### 7.1 ST Pin

BTS4300SGA status pin is an open drain, active low circuit. **Figure 11** shows the equivalent circuitry. As long as no “hard” failure mode occurs (Short circuit to GND / Over temperature or open load in OFF), the signal is permanently high, and due to a required external pull-up to the logic voltage will exhibit a logic high in the application. A suggested value for the  $R_{PU\ ST}$  is 15k $\Omega$ .



**Figure 11** Status output circuitry

### 7.2 ST Signal in Case of Failures

**Table 3** gives a quick reference for the logical state of the ST pin during device operation.

**Table 3** ST pin truth table

Device operation	IN	OUT	ST
Normal operation	L	L	H
	H	H	H
Open Load channel	L	H	L
	H	H	H
Over temp channel	L	L	H
	H	L	L
Short circuit to GND	L	L	H
	H	L <sup>1)</sup>	L

1)  $V_{out} < 2V$  typ.

#### 7.2.1 Diagnostic in Open Load, Channel OFF

For open load diagnosis in OFF-state, an external output pull-up resistor ( $R_{OL}$ ) is recommended. For calculation of the pull-up resistor value, the leakage currents and the open load threshold voltage  $V_{OL(OFF)}$  has to be taken into account. **Figure 12** gives a sketch of the situation and **Figure 13** shows the typical timing diagram.

$I_{leakage}$  defines the leakage current in the complete system, including  $I_{L(OFF)}$  (see **Chapter 5.4**) and external leakages e.g due to humidity, corrosion, etc... in the application.

To reduce the stand-by current of the system, an open load resistor switch  $S_{OL}$  is recommended.

If the channel is OFF, the output is no longer pulled down by the load and  $V_{OUT}$  voltage rises to nearly  $V_S$ . This is recognized by the device as open load. The voltage threshold is given by  $V_{OL(OFF)}$ . In that case, the ST signal is switched to a logical low  $V_{STL}$ .

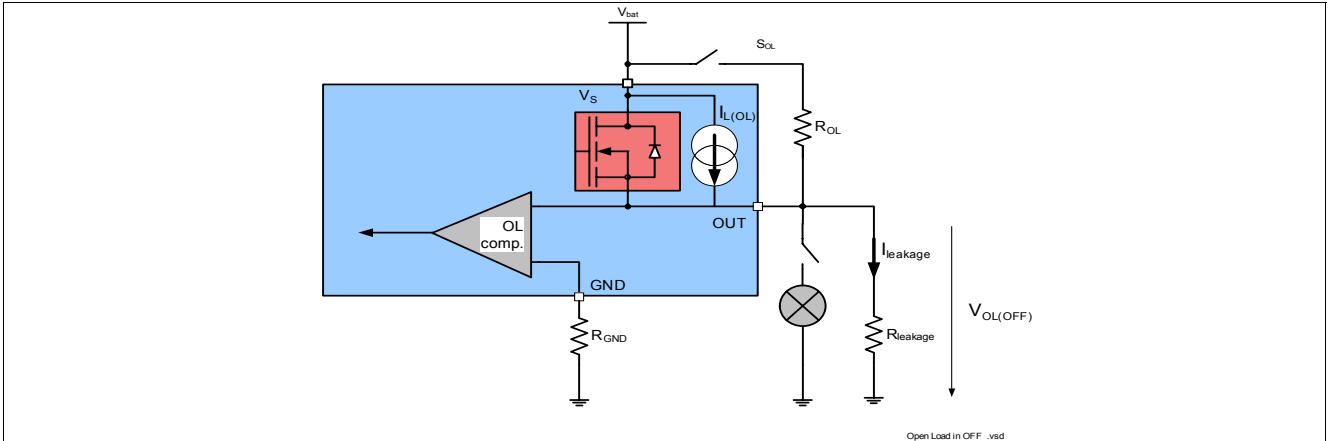


Figure 12 Open load detection in OFF electrical equivalent circuit

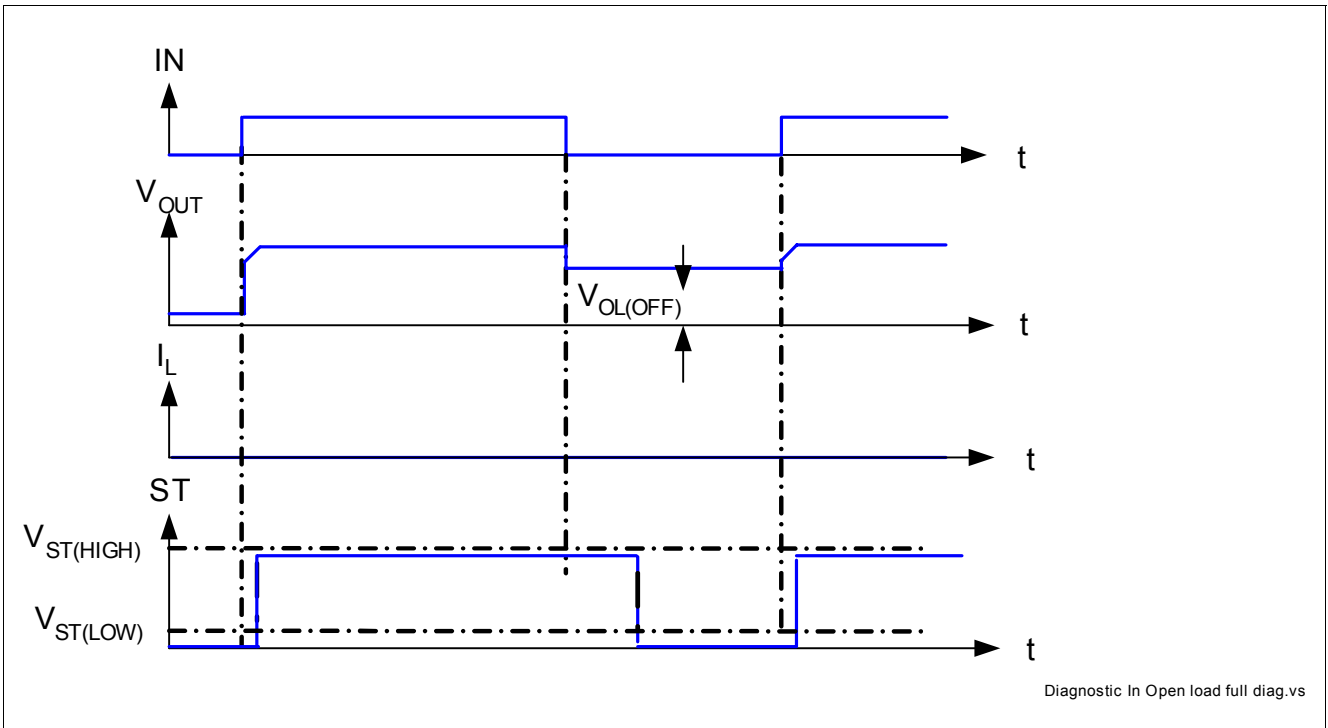


Figure 13 ST in open load condition



### 7.3 Electrical Characteristics Diagnostic Functions

#### Electrical Characteristics: Diagnostics

$V_S = 13.5V$ ,  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ , (unless otherwise specified) Typical values are given at  $V_S = 13.5V$ ,  $T_j = 25\text{ °C}$

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Load condition threshold for diagnostic</b>							
7.3.1	Open Load detection voltage	$V_{OL(OFF)}$	–	3.0	–	V	$V_{IN} = 0V$
7.3.1	Open load detection current	$I_{L(OL)}$	–	5	–	μA	included in the standby current $I_{S(OFF)}$
<b>ST pin</b>							
7.3.2	Status output (open drain) High level; Zener limit voltage	$V_{ST(HIGH)}$	5.4	6.1	–	V	$I_{ST} = +1,6mA^{1)}$ , Zener Limit voltage
7.3.3	Status output (open drain) Low level	$V_{ST(LOW)}$	–	–	0.6	V	$I_{ST} = +1,6mA^{1)}$
<b>Diagnostic timing</b>							
7.3.4	Status invalid after positive input slope	$t_{dST(+)}$	–	300	600	μs	– <sup>2)</sup>
7.3.5	Short circuit detection voltage	$V_{OUT(SC)}$	–	2.8	–	V	–

1) If ground resistor  $R_{GND}$  is used, the voltage drop across this resistor has to be added

2) Not subject to production test, specified by design

## 8 Input Pin

### 8.1 Input Circuitry

The input circuitry is CMOS compatible. The concept of the Input pin is to react to voltage transition and not to voltage threshold. With the Schmidt trigger, it is impossible to have the device in an un-defined state, if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in an linear or undefined state. The input circuitry is compatible with PWM applications. **Figure 15** shows the electrical equivalent input circuitry. The pull down current source ensures the channel is OFF with a floating input.

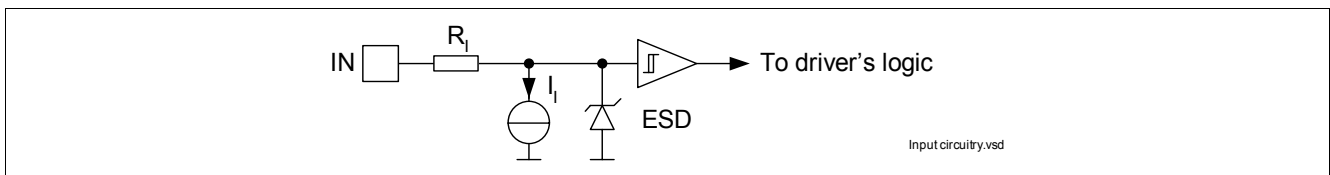


Figure 15 Input pin circuitry

### 8.2 Electrical Characteristics

#### Electrical Characteristics: Diagnostics

$V_S = 13.5V$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $+150\text{ }^\circ\text{C}$ , Typical values are given at  $V_S = 13.5V$ ,  $T_j = 25\text{ }^\circ\text{C}$

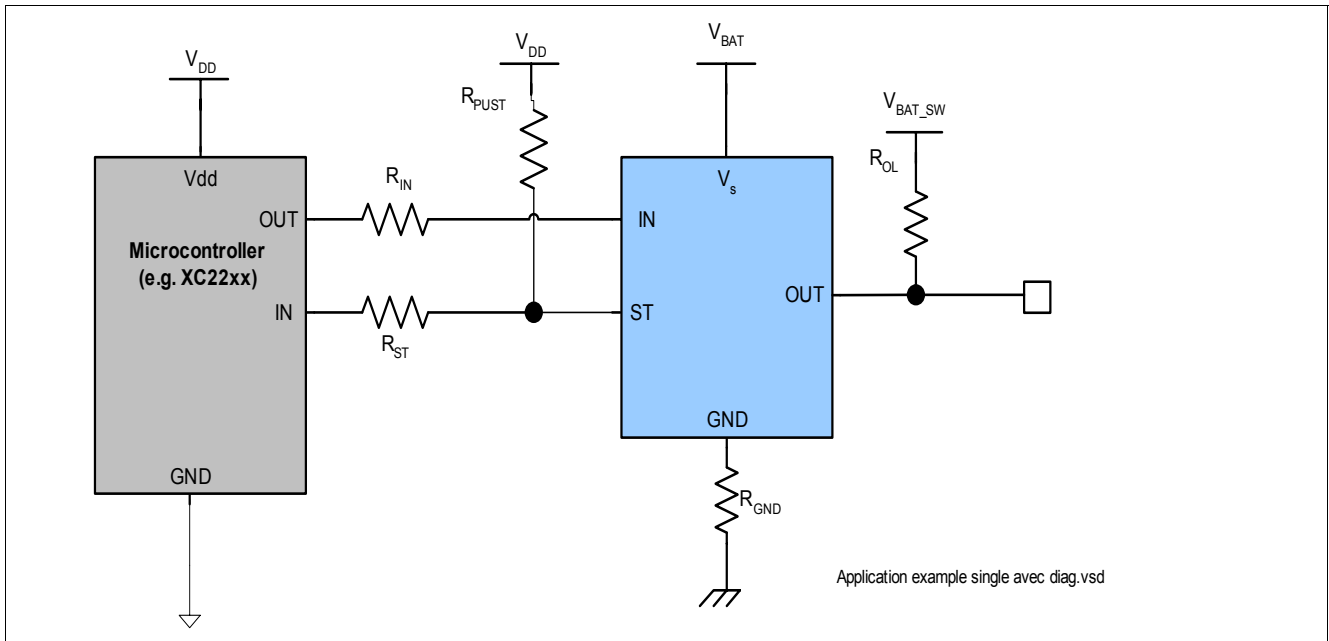
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Input pins characteristics</b>							
8.2.1	Low level input voltage	$V_{IN(L)}$	–	–	0.8	V	– <sup>1)</sup>
8.2.2	High level input voltage	$V_{IN(H)}$	2.2	–	–	V	– <sup>1)</sup>
8.2.3	Input voltage hysteresis	$V_{IN(HYS)}$	–	0.3	–	V	– <sup>2)</sup>
8.2.4	Low level input current	$I_{IN(L)}$	1	–	30	$\mu\text{A}$	$V_{IN} = 0.7V$
8.2.5	High level input current	$I_{IN(H)}$	1	–	30	$\mu\text{A}$	$V_{IN} = 5V$
8.2.6	Input resistance	$R_i$	1.5	3.5	5	$\text{k}\Omega$	See <b>Figure 15</b>

1) If ground resistor  $R_{GND}$  is used, the voltage drop across this resistor has to be added

2) Not subject to production test, specified by design

## 9 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 16** Application diagram with BTS4300SGA

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

### 9.1 Further Application Information

- For further information you may visit <http://www.infineon.com/>

## 10 Package Outlines

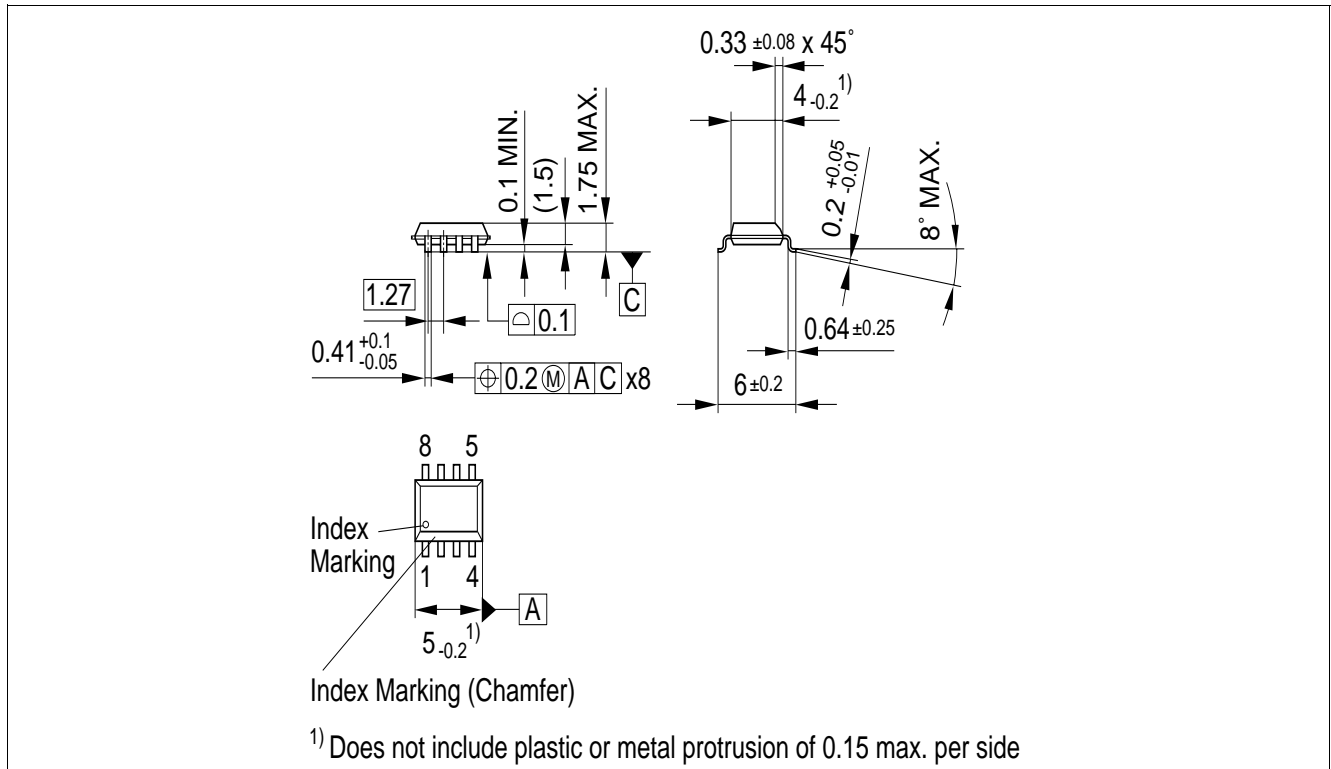


Figure 17 PG-DSO-8-24 (Plastic Dual Small Outline Package)

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## 11 Revision History

Version	Date	Changes
1.0	2008-03-18	Creation of the data sheet

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