



**THE DATASHEET OF  
CY7C1399BN-12VXC**



# 256K (32K x 8) Static RAM

## Features

- **Temperature Ranges**
  - Industrial:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-A:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- **Single 3.3V power supply**
- **Ideal for low-voltage cache memory applications**
- **High speed: 12 ns**
- **Low active power**
  - 180 mW (max.)
- **Low-power alpha immune 6T cell**
- **Available in Pb-free and non Pb-free Plastic SOJ and TSOP I packages**

## Functional Description<sup>[1]</sup>

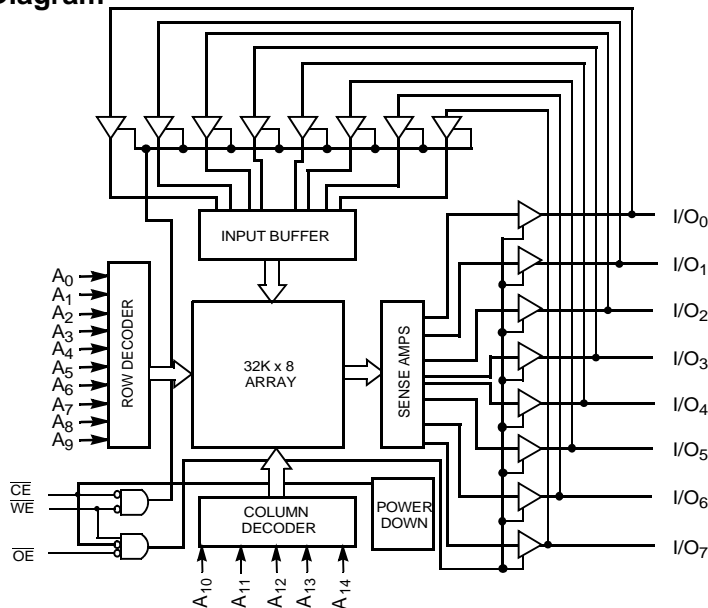
The CY7C1399BN is a high-performance 3.3V CMOS Static RAM organized as 32,768 words by 8 bits. Easy memory

expansion is provided by an active LOW Chip Enable ( $\overline{\text{CE}}$ ) and active LOW Output Enable ( $\overline{\text{OE}}$ ) and tristate drivers. The device has an automatic power-down feature, reducing the power consumption by more than 95% when deselected.

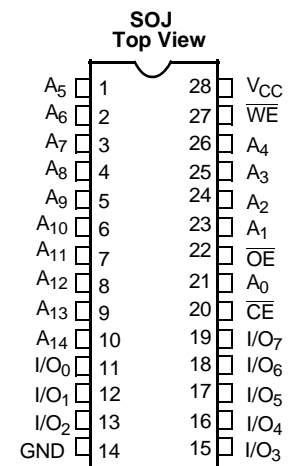
An active LOW Write Enable signal ( $\overline{\text{WE}}$ ) controls the writing/reading operation of the memory. When  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  inputs are both LOW, data on the eight data input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) is written into the memory location addressed by the address present on the address pins ( $\text{A}_0$  through  $\text{A}_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  active LOW, while  $\overline{\text{WE}}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ( $\overline{\text{WE}}$ ) is HIGH. The CY7C1399BN is available in 28-pin standard 300-mil-wide SOJ and TSOP Type I packages.

## Logic Block Diagram



## Pin Configurations



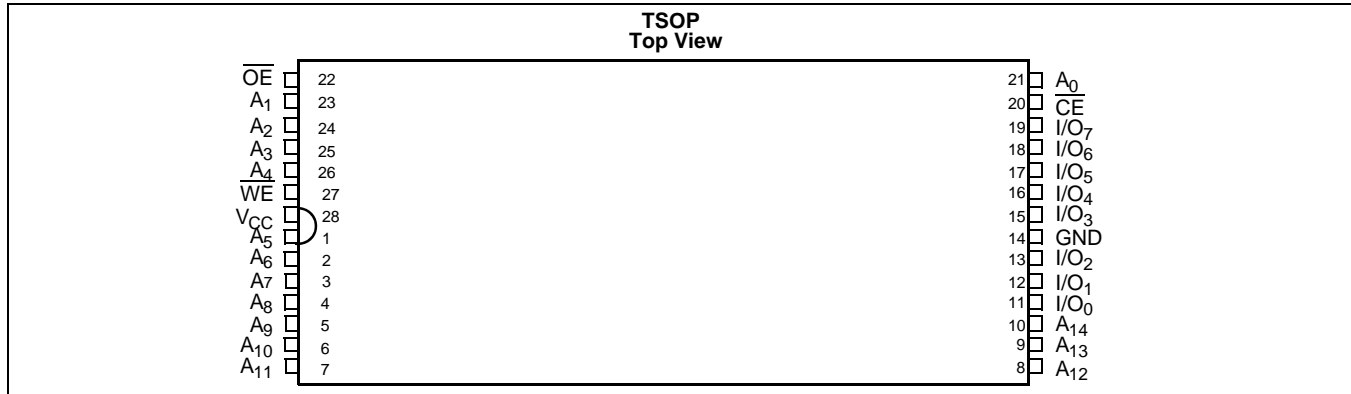
## Selection Guide

		-12	-15
Maximum Access Time (ns)		12	15
Maximum Operating Current (mA)		55	50
Maximum CMOS Standby Current ( $\mu\text{A}$ )	Commercial	500	
	Commercial (L)	50	
	Industrial	500	500
	Automotive-A		500

### Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> .... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- Output Current into Outputs (LOW) ..... 20 mA
- Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ±300 mV
Industrial	-40°C to +85°C	
Automotive-A	-40°C to +85°C	

Electrical Characteristics Over the Operating Range<sup>[1]</sup>

Parameter	Description	Test Conditions	-12		-15		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Leakage Current		-1	+1	-1	+1	µA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	µA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		55		50	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> , or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Comm'l	5			mA
			Comm'l (L)	4			mA
			Ind'l	5		5	mA
			Auto-A			5	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs <sup>[3]</sup>	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, WE ≥ V <sub>CC</sub> - 0.3V or WE ≤ 0.3V, f = f <sub>MAX</sub>	Comm'l	500			µA
			Comm'l (L)	50			µA
			Ind'l	500		500	µA
			Auto-A			500	µA

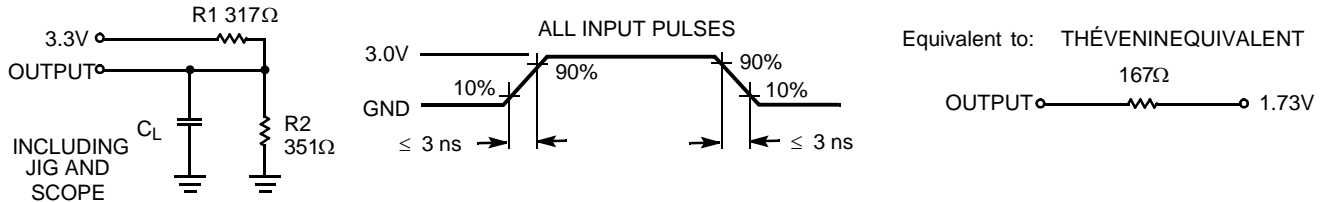
Notes:

- 2. Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
- 3. Device draws low standby current regardless of switching on the addresses.

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub> : Addresses	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	5	pF
C <sub>IN</sub> : Controls			6	pF
C <sub>OUT</sub>	Output Capacitance		6	pF

**AC Test Loads and Waveforms<sup>[5]</sup>**



**Switching Characteristics Over the Operating Range<sup>[5]</sup>**

Parameter	Description	-12		-15		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	12		15		ns
t <sub>AA</sub>	Address to Data Valid		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		6	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		5		6	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15	ns
<b>Write Cycle<sup>[8, 9]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	8		10		ns
t <sub>AW</sub>	Address Set-Up to Write End	8		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	8		10		ns
t <sub>SD</sub>	Data Set-Up to Write End	7		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[8]</sup>		7		7	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		ns

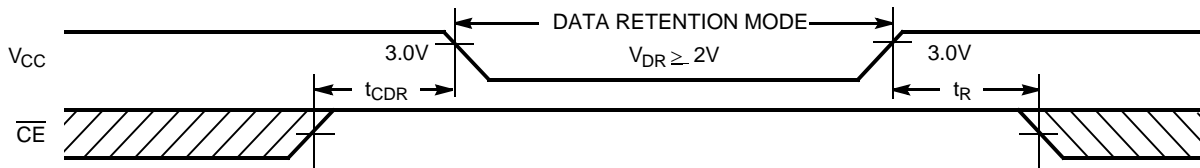
**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and capacitance C<sub>L</sub> = 30 pF.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Data Retention Characteristics** (Over the Operating Range - L version only)

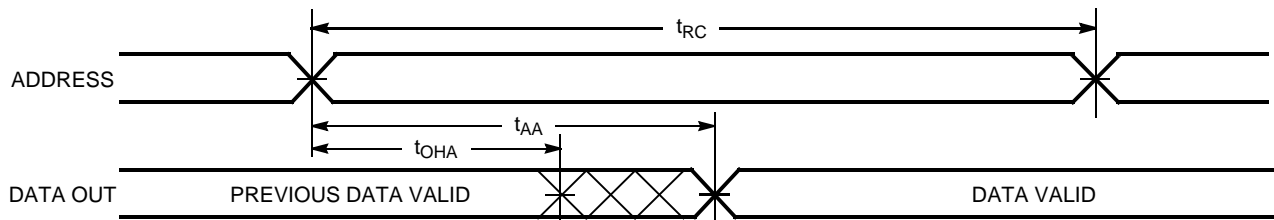
Parameter	Description	Conditions	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$ , $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0	20	$\mu A$
$t_{CDR}$	Chip Deselect to Data Retention Time		0		ns
$t_R$	Operation Recovery Time		$t_{RC}$		ns

**Data Retention Waveform**

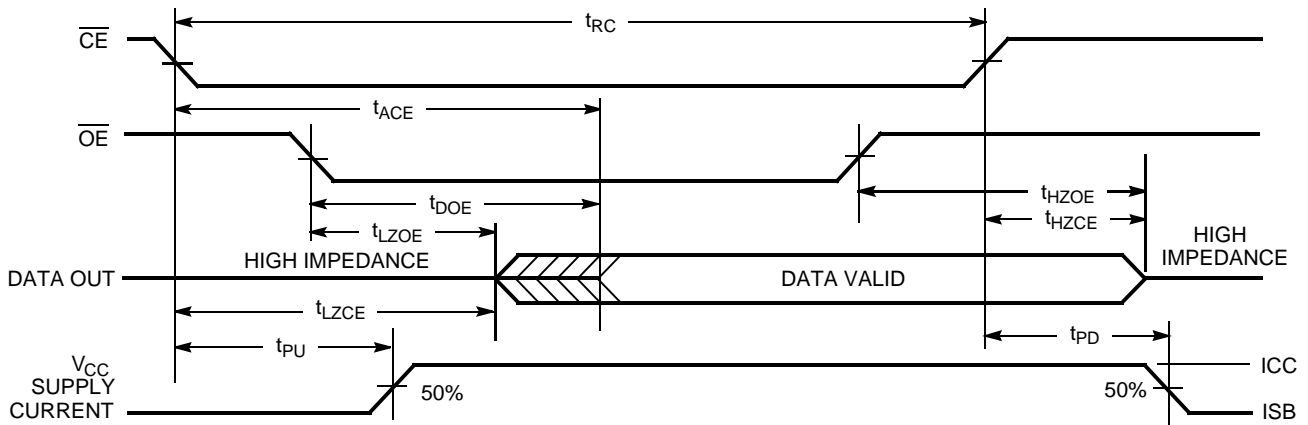


**Switching Waveforms**

**Read Cycle No. 1**<sup>[10, 11]</sup>



**Read Cycle No. 2**<sup>[11, 12]</sup>

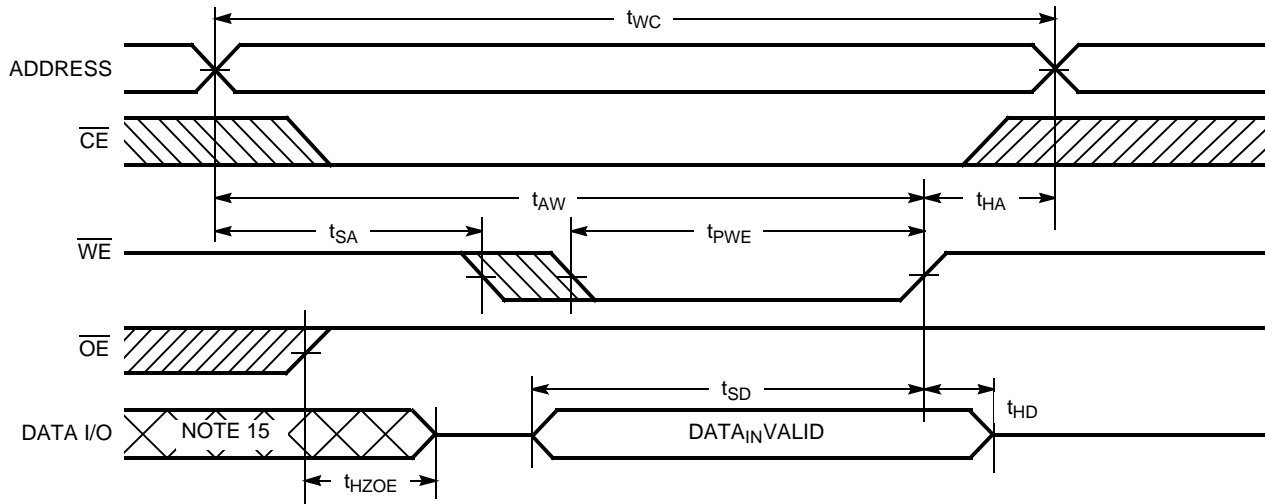


**Notes:**

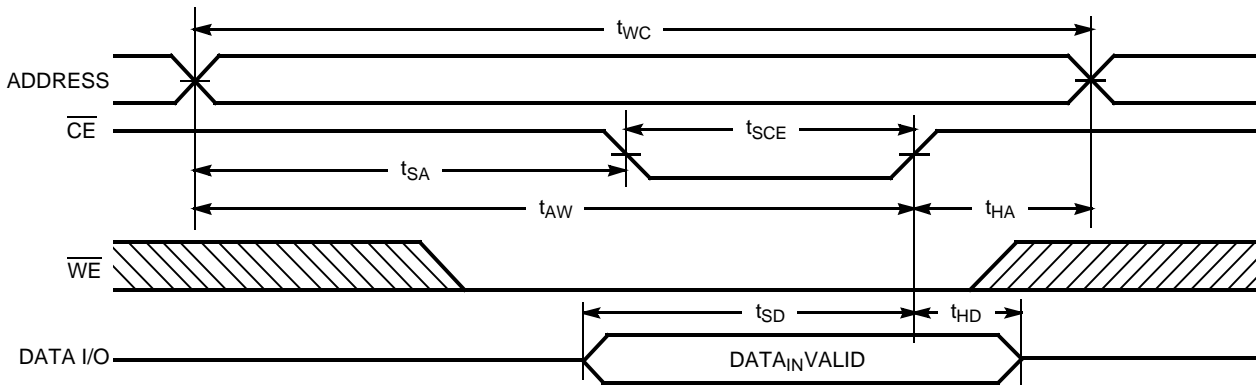
- 10. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
- 11.  $\overline{WE}$  is HIGH for read cycle.
- 12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

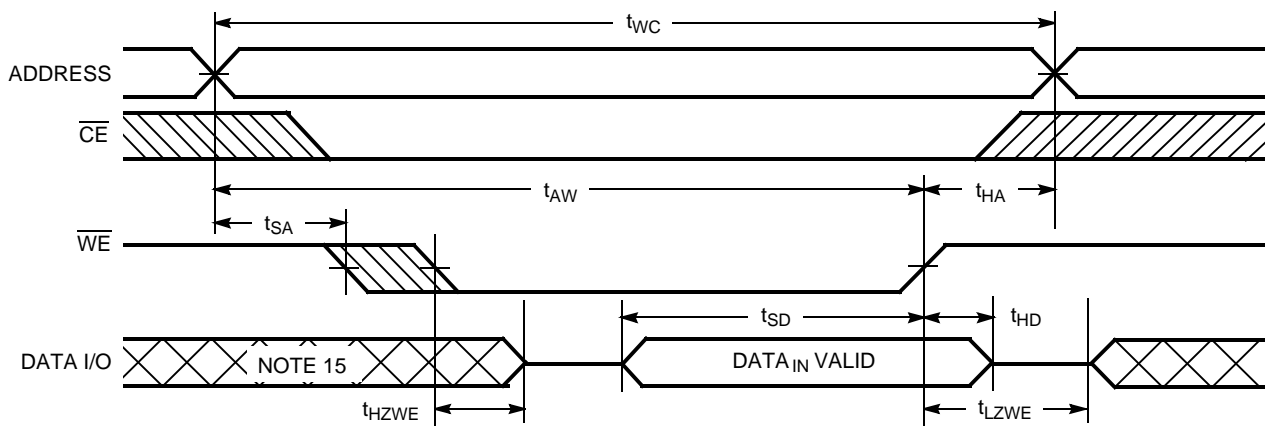
Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[8, 13, 14]</sup>



Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[8, 13, 14]</sup>



Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[9, 14]</sup>



- Notes:**
- 13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
  - 14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
  - 15. During this period, the I/Os are in the output state and input signals should not be applied.

**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

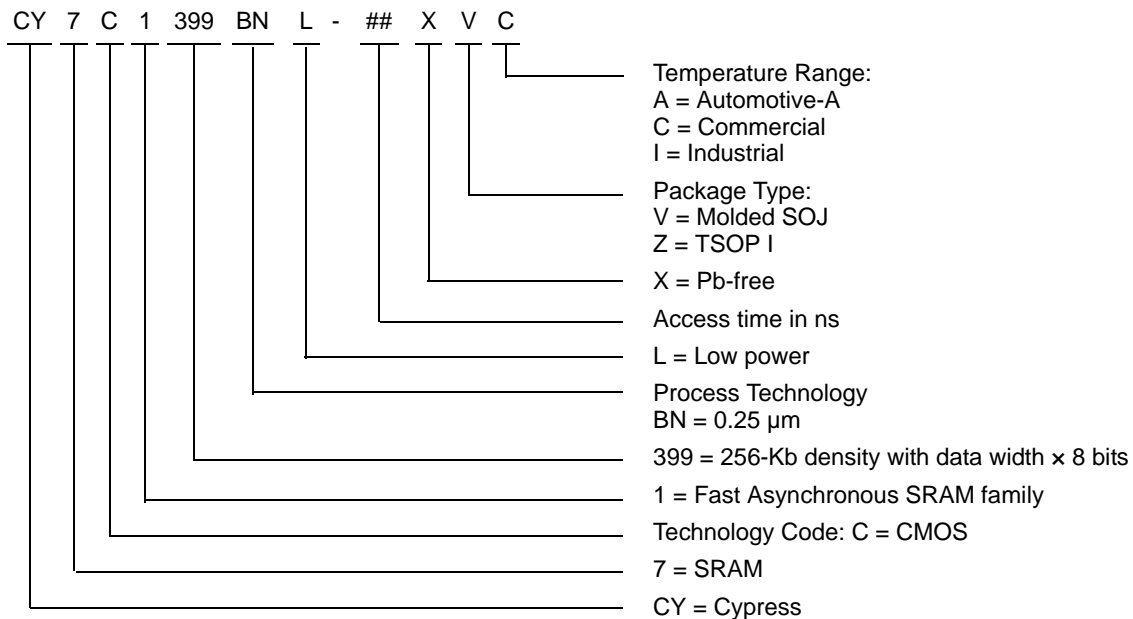
For a complete listing of all options, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1399BN-12VXC	51-85031	28-Lead Molded SOJ (Pb-free)	Commercial
	CY7C1399BN-12ZXC	51-85071	28-Lead TSOP I (Pb-free)	
	CY7C1399BNL-12ZXC		28-Lead TSOP I (Pb-free)	
	CY7C1399BN-12VXI	51-85031	28-Lead Molded SOJ (Pb-free)	Industrial
15	CY7C1399BN-15ZXI	51-85071	28-Lead TSOP I (Pb-free)	Industrial
	CY7C1399BN-15VXA	51-85031	28-Lead Molded SOJ (Pb-free)	Automotive-A

Please contact local sales representative regarding availability of these parts.

**Ordering Code Definitions**

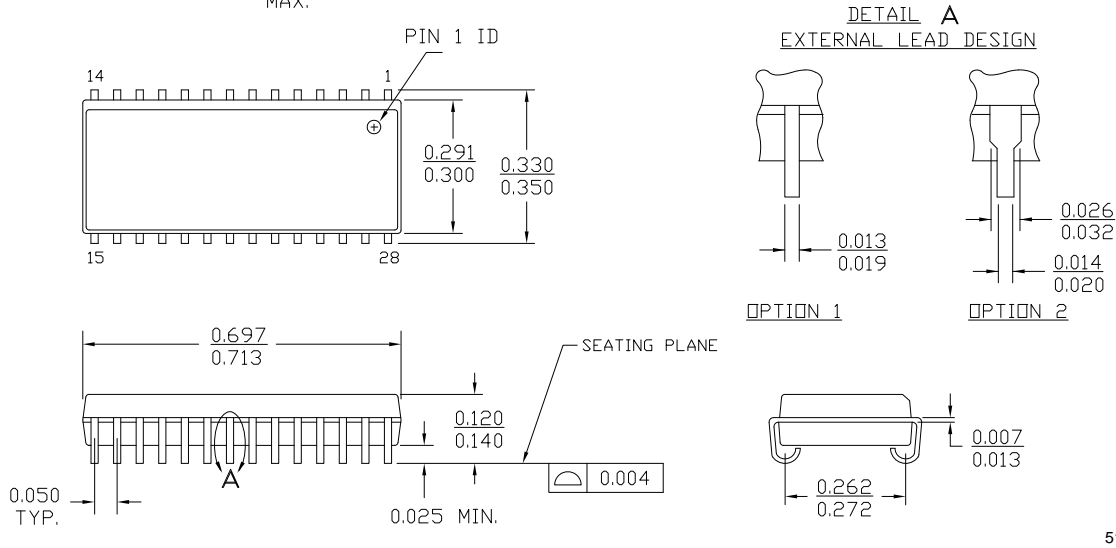


**Package Diagrams**

**28-Lead (300-Mil) Molded SOJ (51-85031)**

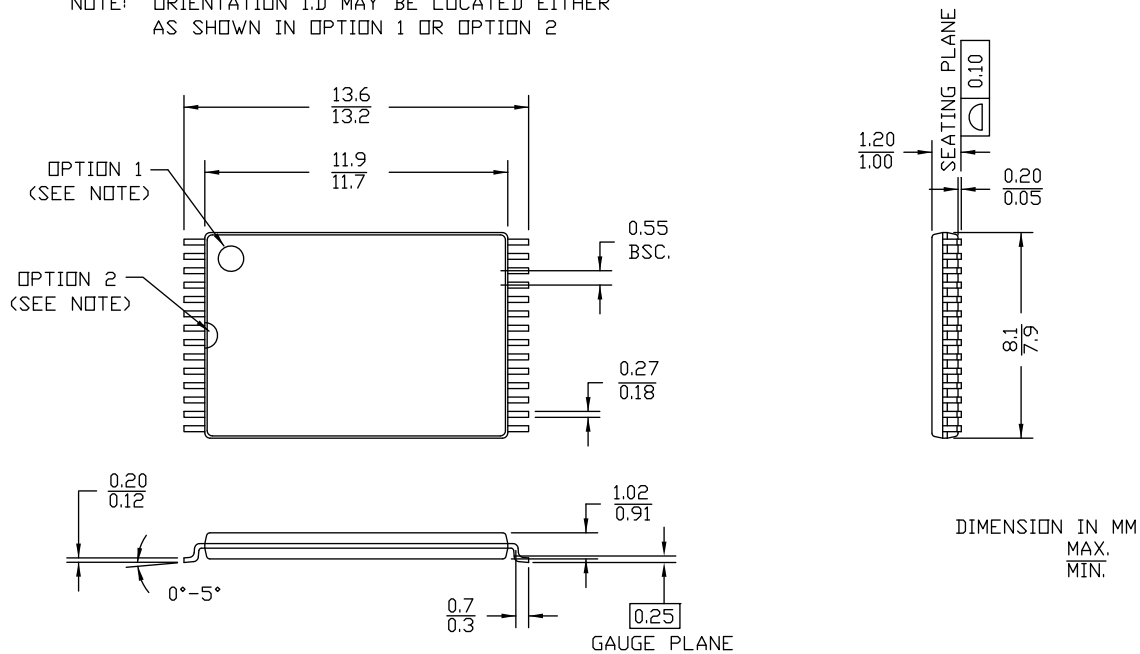
NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.  
MAX.



**28-Lead TSOP 1 (8x13.4 mm) (51-85071)**

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2





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**Document History Page**

Document Title: CY7C1399BN 256K (32K x 8) Static RAM Document Number: 001-06490				
REV.	ECN NO.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
**	423877	See ECN	NXR	New Data Sheet
*A	498575	See ECN	NXR	Added Automotive-A range Removed I <sub>OS</sub> parameter from DC Electrical Characteristics table Updated Ordering Information table.
*B	2896382	03/19/2010	AJU	Removed obsolete part numbers from Ordering Information table and updated package diagrams.
*C	3053362	10/08/2010	PRAS	Removed pruned part numbers CY7C1399BNL-15VXC and CY7C1399BNL-15VXCT. Added Ordering Code Definitions.

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