THE DATASHEET OF

CY7C1361B-100AC

www.win-source.net 0086-755-83957316

CY7C1361B
CY7C1363B

9-Mbit (256K x 36/512K x 18) Flow-Through SRAM

Features

- **Supports 133-MHz bus operations**
- **256K X 36/512K X 18 common I/O**
- **3.3V –5% and +10% core power supply (V_{DD})**
- **2.5V or 3.3V I/O supply (V_{DDQ})**
- **Fast clock-to-output times**
  - **6.5 ns (133-MHz version)**
  - **7.5 ns (117-MHz version)**
  - **8.5 ns (100-MHz version)**
- **Provide high-performance 2-1-1-1 access rate**
- **User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Asynchronous output enable**
- **Offered in JEDEC-standard 100-pin TQFP, 119-ball BGA and 165-ball fBGA packages**
  - **Both 2 and 3 Chip Enable Options for TQFP**
- **JTAG boundary scan for BGA and fBGA packages**
- **"ZZ" Sleep Mode option**

Functional Description[1]

The CY7C1361B/CY7C1363B is a 3.3V, 256K x 36 and 512K x 18 Synchronous Flow through SRAMs, respectively designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133-MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE_1}$), depth-expansion Chip Enables (CE_2 and $\overline{CE_3}$[2]), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW_x}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

The CY7C1361B/CY7C1363B allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe ($\overline{ADSP}$) or the cache Controller Address Strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the Address Advancement ($\overline{ADV}$) input.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

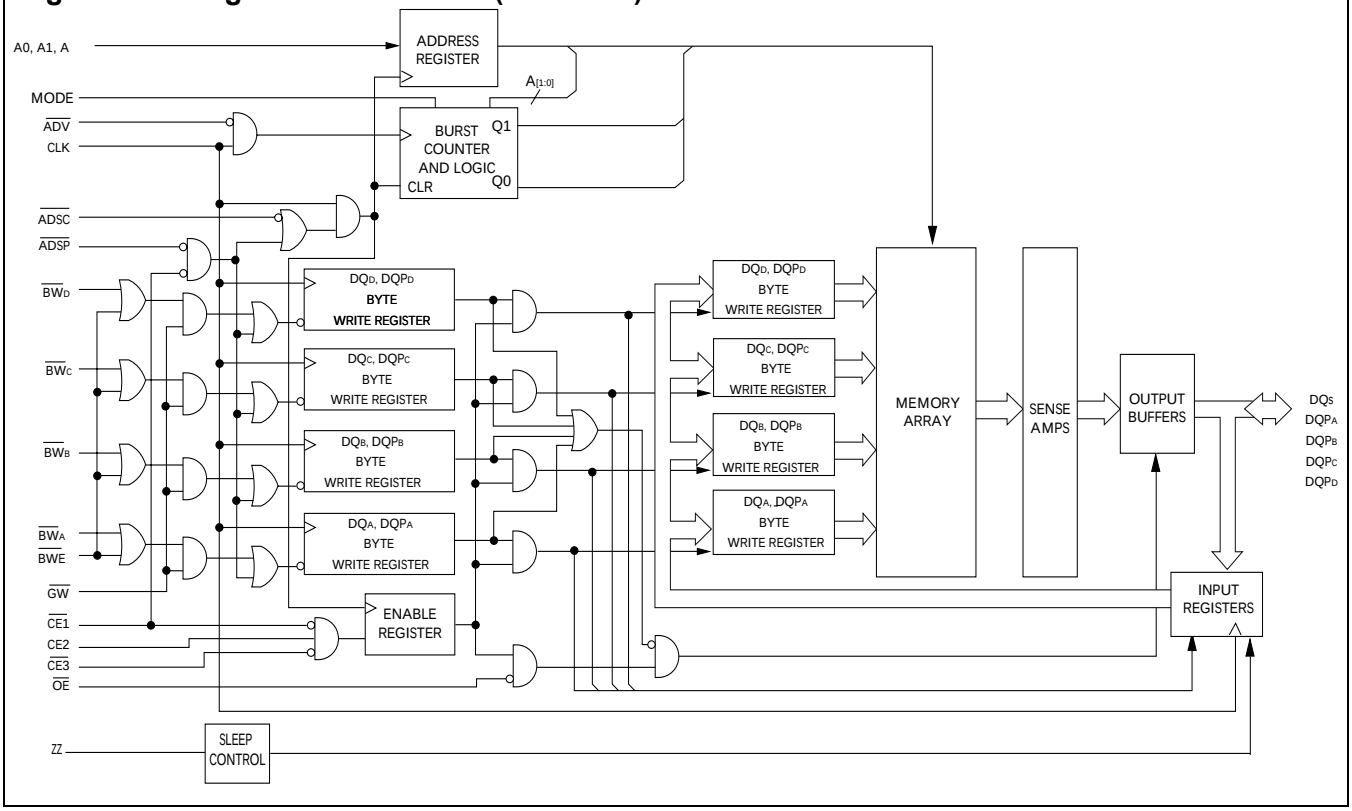
The CY7C1361B/CY7C1363B operates from a +3.3V core power supply while all outputs may operate with either a +2.5 or +3.3V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

Selection Guide

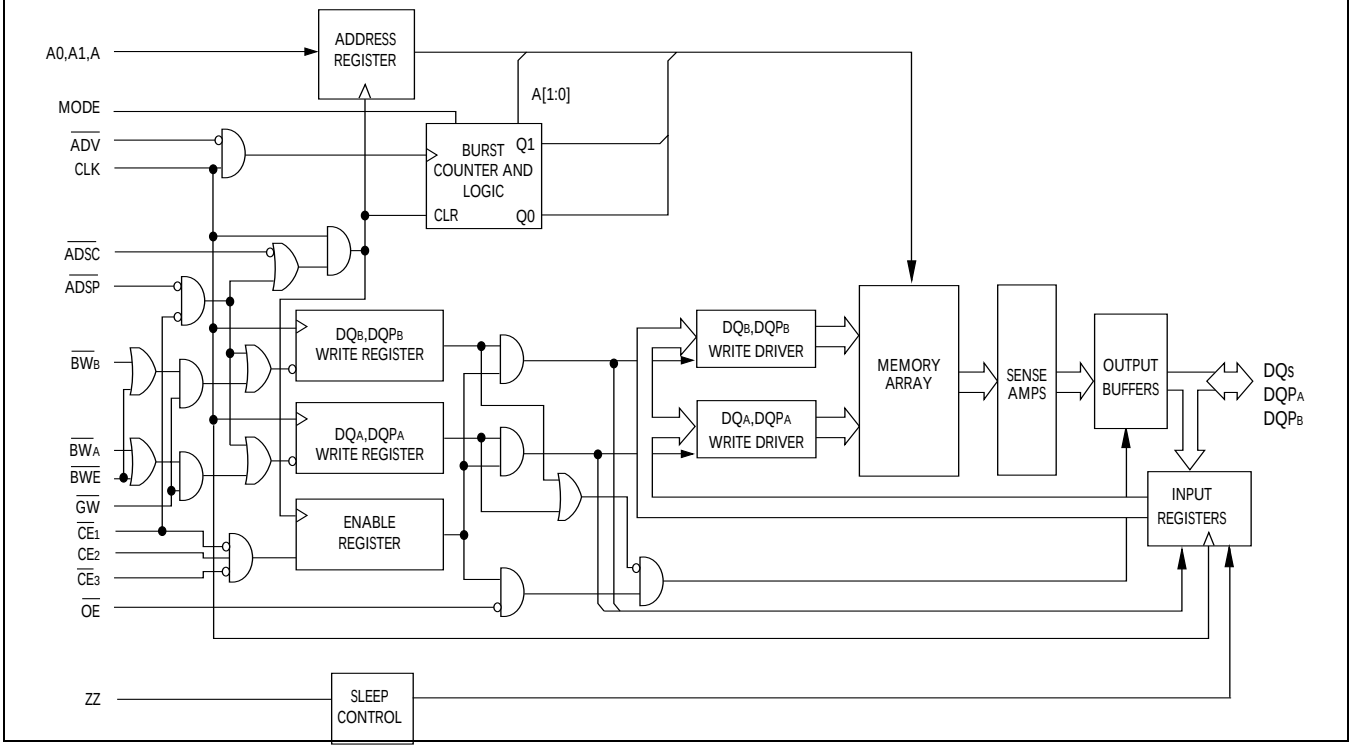
	133 MHz	117 MHz	100 MHz	Unit
Maximum Access Time	6.5	7.5	8.5	ns
Maximum Operating Current	250	220	180	mA
Maximum CMOS Standby Current	30	30	30	mA

Notes:
1. For best–practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.
2. $\overline{CE_3}$ is for A version of TQFP (3 Chip Enable Option) and 165 fBGA package only. 119 BGA is offered only in 2 Chip Enable.

Logic Block Diagram – CY7C1361B (256K x 36)

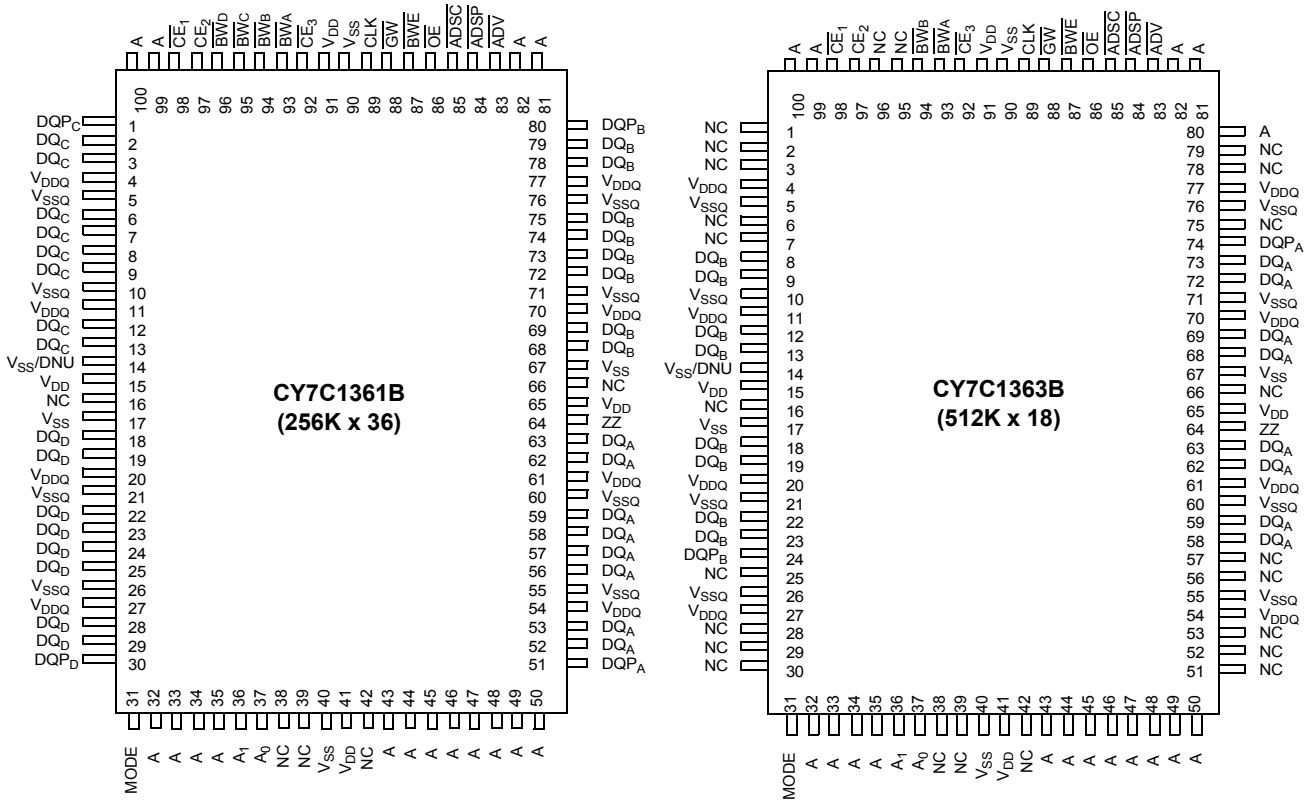


Logic Block Diagram – CY7C1363B (512K x 18)



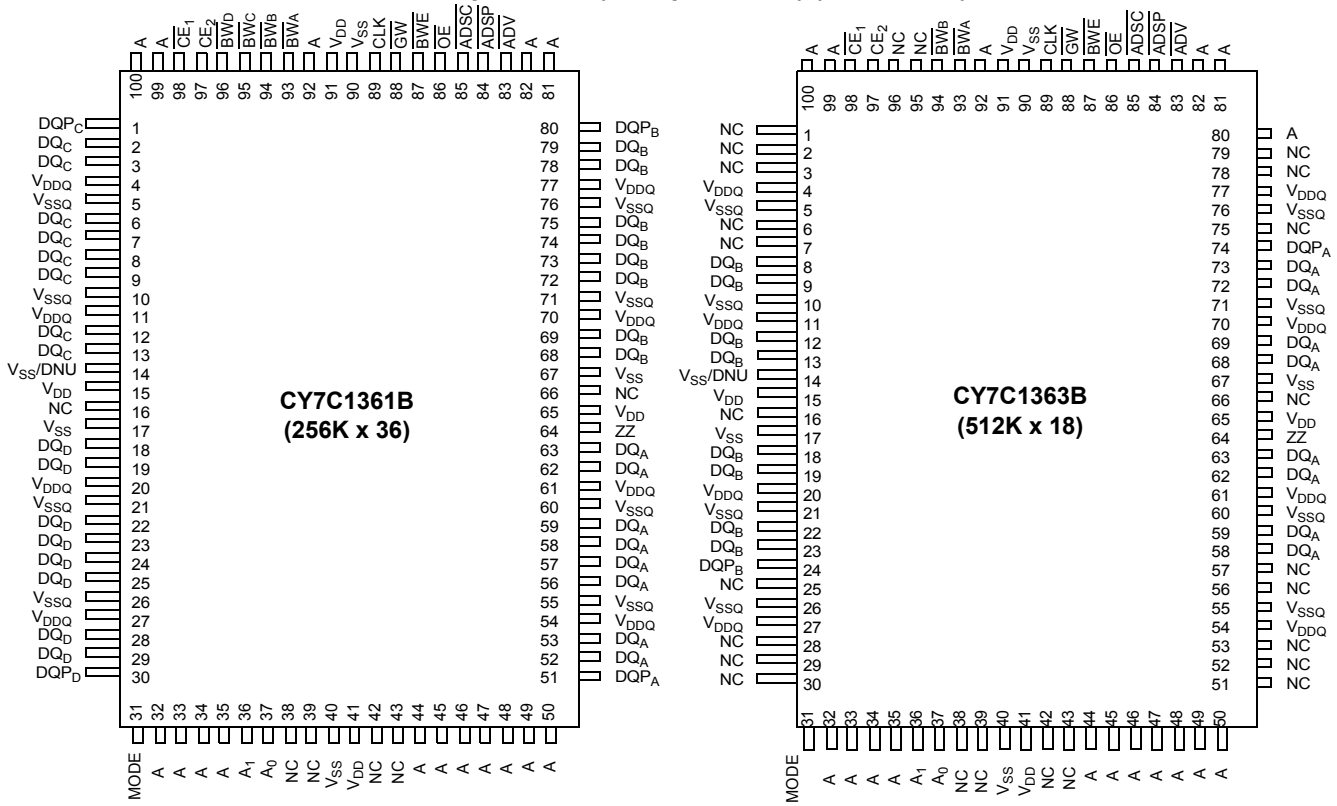
Pin Configurations

100-pin TQFP Pinout (3 Chip Enables) (A version)



Pin Configurations (continued)

100-pin TQFP (2 Chip Enables) (AJ Version)



Pin Configurations (continued)

119-ball BGA (2 Chip Enables with JTAG)

CY7C1361B (256K x 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CE_2	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE}_1$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW}_C$	$\overline{ADV}$	$\overline{BW}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW}_D$	NC	$\overline{BW}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BWE}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1363B (512K x 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CE_2	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_B	NC	V_{SS}	NC	V_{SS}	DQP_A	NC
E	NC	DQ_B	V_{SS}	$\overline{CE}_1$	V_{SS}	NC	DQ_A
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_A	V_{DDQ}
G	NC	DQ_B	$\overline{BW}_B$	$\overline{ADV}$	V_{SS}	NC	DQ_A
H	DQ_B	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_A	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_B	V_{SS}	CLK	V_{SS}	NC	DQ_A
L	DQ_B	NC	V_{SS}	NC	$\overline{BW}_A$	DQ_A	NC
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	DQ_B	NC	V_{SS}	A1	V_{SS}	DQ_A	NC
P	NC	DQP_B	V_{SS}	A0	V_{SS}	NC	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

165-ball fBGA (3 Chip Enable)

CY7C1361B (256K x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC / 288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC	A	CE_2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC / 144M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	NC / 18M	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC / 72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC / 36M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1363B (512K x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC / 288M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC	A	CE_2	NC	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC / 144M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_A
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A
H	V_{SS}	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC
N	DQP_B	NC	V_{DDQ}	V_{SS}	NC	NC / 18M	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	NC / 72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	NC / 36M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1361B–Pin Definitions

Name	TQFP (3-Chip Enable)	TQFP (2-Chip Enable)	BGA (2-Chip Enable)	fBGA (3-Chip Enable)	I/O	Description
A_0, A_1, A	37,36,32,33, 34,35,43,44, 45,46,47,48, 49,50,81,82, 99,100	37,36,32,33, 34,35,44,45, 46,47,48,49, 50,81,82,92, 99,100	P4,N4,A2, C2,R2,A3, B3,C3,T3, T4,A5,B5, C5,T5,A6, B6,C6,R6	R6,P6,A2, A10,B2,B10, P3,P4,P8, P9,P10,P11, R3,R4,R8, R9,R10,R11	Input-Synchronous	**Address Inputs used to select one of the 256K address location**s. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE_1}$, CE_2, and $\overline{CE_3}$[2] are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW_A}$,$\overline{BW_B}$ $\overline{BW_C}$,$\overline{BW_D}$	93,94,95,96	93,94,95,96	L5,G5,G3, L3	B5,A5,A4, B4	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	88	88	H4	B7	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $BW_{[A:D]}$and $\overline{BWE}$).
CLK	89	89	K4	B6	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE_1}$	98	98	E4	A3	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$[2] to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.
CE_2	97	97	B2	B3	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$[2] to select/deselect the device.
$\overline{CE_3}$[2]	92	–	–	A6	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device.
$\overline{OE}$	86	86	F4	B8	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	83	83	G4	A9	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	84	84	A4	B9	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE_1}$ is deasserted HIGH.

CY7C1361B–Pin Definitions (continued)

Name	TQFP (3-Chip Enable)	TQFP (2-Chip Enable)	BGA (2-Chip Enable)	fBGA (3-Chip Enable)	I/O	Description
$\overline{ADSC}$	85	85	B4	A8	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW.** When asserted LOW, addresses presented to the device are captured in the address registers. A[1:0] are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
$\overline{BWE}$	87	87	M4	A7	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	64	64	T7	H11	Input-Asynchronous	**ZZ "sleep" Input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQ_s	52,53,56,57, 58,59,62,63, 68,69,72,73, 74,75,78,79, 2,3,6,7,8,9, 12,13,18,19, 22,23,24,25, 28,29	52,53,56,57, 58,59,62,63, 68,69,72,73, 74,75,78,79, 2,3,6,7,8,9, 12,13,18,19, 22,23,24,25, 28,29	K6,L6,M6, N6,K7,L7, N7,P7,E6, F6,G6,H6, D7,E7,G7, H7,D1,E1, G1,H1,E2, F2,G2,H2, K1,L1,N1, P1,K2,L2, M2,N2	M11,L11, K11,J11, J10,K10, L10,M10, D10,E10, F10,G10, D11,E11, F11,G11, D1,E1,F1, G1,D2,E2, F2,G2,J1, K1,L1,M1, J2,K2,L2 M2,	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and $DQP_{[A:D]}$ are placed in a three-state condition.The outputs are automatically three-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
$DQP_{[A:D]}$	51,80,1,30	51,80,1,30	P6,D6,D2, P2	N11,C11,C1, N1	I/O-Synchronous	**Bidirectional Data Parity I/O Lines**. Functionally, these signals are identical to DQ_s. During write sequences, $DQP_{[A:D]}$ is controlled by $\overline{BW}_{[A:D]}$ correspondingly.
MODE	31	31	R3	R1	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
V_{DD}	15,41,65,91	15,41,65,91	J2,C4,J4, R4,J6	D4,D8,E4, E8,F4,F8, G4,G8, H4,H8,J4, J8,K4,K8, L4,L8,M4, M8	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	4,11,20,27, 54,61,70,77	4,11,20,27, 54,61,70,77	A1,F1,J1, M1,U1, A7,F7,J7, M7,U7	C3,C9,D3, D9,E3,E9, F3,F9,G3, G9,J3,J9, K3,K9,L3, L9,M3,M9, N3,N9	I/O Power Supply	**Power supply for the I/O circuitry**.

CY7C1361B–Pin Definitions (continued)

Name	TQFP (3-Chip Enable)	TQFP (2-Chip Enable)	BGA (2-Chip Enable)	fBGA (3-Chip Enable)	I/O	Description
V_{SS}	17,40,67,90	17,40,67,90	H2,D3,E3, F3,H3,K3, M3,N3, P3,D5,E5, F5,H5,K5, M5,N5,P5	C4,C5,C6, C7,C8,D5, D6,D7,E5, E6,E7,F5, F6,F7,G5, G6,G7,H5, H6,H7,J5, J6,J7,K5,K6, K7,L5,L6,L7, M5,M6,M7, N4,N8	Ground	**Ground for the core of the device**.
V_{SSQ}	5,10,21,26, 55,60,71,76	5,10,21,26, 55,60,71,76	–	–	I/O Ground	**Ground for the I/O circuitry**.
TDO	–	–	U5	P7	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be left unconnected. This pin is not available on TQFP packages.
TDI	–	–	U3	P5	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be left floating or connected to V_{DD} through a pull up resistor. This pin is not available on TQFP packages.
TMS	–	–	U2	R5	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	–	–	U4	R7	JTAG-Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not being utilized, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	16,38,39,42, 66	16,38,39,42, 43,66	B1,C1,R1, T1,T2,J3, D4,L4,J5, R5,T6,U6, B7,C7,R7	A1,A11,B1, B11,C2,C10, H1,H3,H9, H10,N2,N5, N6,N7,N10, P1,P2,R2	–	**No Connects**. Not internally connected to the die. 18M, 36M, 72M, 144M and 288M are address expansion pins are not internally connected to the die.
V_{SS}/DNU	14	14	-	-	Ground/DNU	This pin can be connected to Ground or should be left floating.

CY7C1363B: Pin Definitions

Name	TQFP (3-Chip Enable)	TQFP (2-Chip Enable)	BGA (2-Chip Enable)	fBGA (3-Chip Enable)	I/O	Description
A_0, A_1, A	37,36,32,33, 34,35,43,44, 45,46,47,48, 49,50,80,81, 82,99,100	37,36,32,33, 34,35,44,45, 46,47,48,49, 50,80,81,82, 92,99,100	P4,N4,A2, C2,R2,T2, A3,B3,C3, T3,A5,B5, C5,T5,A6, B6,C6,R6, T6	R6,P6,A2, A10,A11,B2, B10,P3,P4, P8,P9,P10, P11,R3,R4, R8,R9,R10, R11	Input-Synchronous	**Address Inputs used to select one of the 512K address locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$[2] are sampled active. $A_{[1:0]}$ feed the 2-bit counter.

CY7C1363B: Pin Definitions (continued)

Name	TQFP (3-Chip Enable)	TQFP (2-Chip Enable)	BGA (2-Chip Enable)	fBGA (3-Chip Enable)	I/O	Description
$\overline{BW}_A$, $\overline{BW}_B$	93,94	93,94	L5,G3	B5,A4	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	88	88	H4	B7	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[A:B]}$ and $\overline{BWE}$).
$\overline{BWE}$	87	87	M4	A7	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	89	89	K4	B6	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	98	98	E4	A3	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$[2] to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.
CE_2	97	97	B2	B3	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$[2] to select/deselect the device.
$\overline{CE}_3$[2]	92	–	–	A6	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	86	86	F4	B8	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	83	83	G4	A9	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	84	84	A4	B9	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.

CY7C1363B: Pin Definitions (continued)

Name	TQFP (3-Chip Enable)	TQFP (2-Chip Enable)	BGA (2-Chip Enable)	fBGA (3-Chip Enable)	I/O	Description
$\overline{ADSC}$	85	85	B4	A8	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized·
ZZ	64	64	T7	H11	Input-Asynchronous	**ZZ "sleep" Input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQ_s	58,59,62,63, 68,69,72,73, 8,9,12,13, 18,19,22,23	58,59,62,63, 68,69,72,73, 8,9,12,13, 18,19,22,23	P7,K7,G7, E7,F6,H6, L6,N6,D1, H1,L1,N1, E2,G2,K2, M2	J10,K10, L10,M10, D11,E11, F11,G11,J1, K1,L1,M1, D2,E2,F2, G2	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and $DQP_{[A:B]}$ are placed in a three-state condition.The outputs are automatically three-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
$DQP_{[A:B]}$	74,24	74,24	D6,P2	C11,N1	I/O-Synchronous	**Bidirectional Data Parity I/O Lines.** Functionally, these signals are identical to DQ_s. During write sequences, $DQP_{[A:B]}$ is controlled by $\overline{BW}_{[A:B]}$ correspondingly.
MODE	31	31	R3	R1	Input-Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
V_{DD}	15,41,65,91	15,41,65,91	C4,J2,J4, J6,R4	D4,D8,E4, E8,F4,F8, G4,G8, H4,H8,J4, J8,K4,K8, L4,L8,M4, M8	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	4,11,20,27, 54,61,70,77	4,11,20,27, 54,61,70,77	A1,A7,F1, F7,J1,J7, M1,M7,U1 ,U7	C3,C9,D3, D9,E3,E9, F3,F9,G3, G9,J3,J9, K3,K9,L3, L9,M3,M9, N3,N9	I/O Power Supply	**Power supply for the I/O circuitry**.

CY7C1363B: Pin Definitions (continued)

Name	TQFP (3-Chip Enable)	TQFP (2-Chip Enable)	BGA (2-Chip Enable)	fBGA (3-Chip Enable)	I/O	Description
V_{SS}	17,40,67,90	17,40,67,90	D3,D5,E3, E5,F3,F5, G5,H3, H5,K3,K5, L3,M3, M5,N3, N5,P3,P5	C4,C5,C6, C7,C8,D5, D6,D7,E5, E6,E7,F5, F6,F7,G5, G6,G7,H1, H2,H5,H6, H7,J5,J6,J7, K5,K6,K7,L5 ,L6,L7,M5, M6,M7,N4, N8	Ground	**Ground for the core of the device**.
V_{SSQ}	5,10,21,26, 55,60,71,76,	5,10,21,26, 55,60,71,76,	–	–	I/O Ground	**Ground for the I/O circuitry**.
TDO	–	–	U5	P7	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be left unconnected. This pin is not available on TQFP packages.
TDI	–	–	U3	P5	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be left floating or connected to V_{DD} through a pull up resistor. This pin is not available on TQFP packages.
TMS	–	–	U2	R5	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	–	–	U4	R7	JTAG-Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not being utilized, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	1,2,3,6,7,16, 25,28,29,30, 38,39,42,51, 52,53,56,57, 66,75,78,79, 95,96	1,2,3,6,7,16, 25,28,29,30, 38,39,42,43, 51,52,53,56, 57,66,75,78, 79,95,96	B1,B7,C1, C7,D2,D4, D7,E1,E6, H2,F2,G1, G6,H7,J3, J5,K1,K6, L4,L2,L7, M6,N2,N7 ,L7,P1,P6, R1,R5,R7, T1,T4,U6	A1,A5,B1, B4,B11,C1, C2,C10,D1, D10,E1,E10, F1,F10,G1, G10,H3,H9, H10,J2,J11, K2,K11,L2, L11,M2,M11, N2,N5,N6, N7,N10,N11, P1,P2,R2	–	**No Connects**. Not internally connected to the die. 18M, 36M, 72M, 144M and 288M are address expansion pins are not internally connected to the die.
V_{SS}/DNU	14	14	–	–	Ground/DNU	This pin can be connected to Ground or should be left floating.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{C0}) is 6.5 ns (133-MHz device).

The CY7C1361B/CY7C1363B supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium® and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}$X) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$[2]) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$[2] are all asserted active, and (2) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW (if the access is initiated by $\overline{ADSC}$, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data will be available at the data outputs a maximum to t_{CDV} after clock rise. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, $\overline{CE}_3$[2] are all asserted active, and (2) $\overline{ADSP}$ is asserted LOW. The addresses presented are loaded into the address register and the burst inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_X$)are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the appropriate data will be latched and written into the device.Byte writes are allowed. All I/Os are three-stated during a byte write.Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be three-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are three-stated once a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$[2] are all asserted active, (2) $\overline{ADSC}$ is asserted LOW, (3) $\overline{ADSP}$ is deasserted HIGH, and (4) the write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_X$) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to $DQ_{[A:D]}$ will be written into the specified address location. Byte writes are allowed. All I/Os are three-stated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be three-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are three-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1361B/CY7C1363B provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE will select an interleaved burst order. Leaving MODE unconnected will cause the device to default to a interleaved burst sequence.

Interleaved Burst Address Table (MODE = Floating or VDD)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$[2], $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	ZZ ≥ V_{DD} – 0.2V		35	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2V		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2V	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to snooze current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit snooze current	This parameter is sampled	0		ns

Truth Table[3, 4, 5, 6, 7]

Cycle Description	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	three-state
Deselected Cycle, Power-down	None	L	L	X	L	L	X	X	X	X	L-H	three-state
Deselected Cycle, Power-down	None	L	X	H	L	L	X	X	X	X	L-H	three-state
Deselected Cycle, Power-down	None	L	L	X	L	H	L	X	X	X	L-H	three-state
Deselected Cycle, Power-down	None	X	X	X	L	H	L	X	X	X	L-H	three-state
Snooze Mode, Power-down	None	X	X	X	H	X	X	X	X	X	X	three-state
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	three-state
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	three-state
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	three-state
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	three-state
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	three-state
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	three-state
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes:

3. X="Don't Care." H = Logic HIGH, L = Logic LOW.
4. $\overline{WRITE}$ = L when any one or more Byte Write enable signals and $\overline{BWE}$ = L or $\overline{GW}$= L. $\overline{WRITE}$ = H when all Byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
5. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of GW, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to three-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are three-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Partial Truth Table for Read/Write[3, 8]

Function (CY7C1361B)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte (A, DQP_A)	H	L	H	H	H	L
Write Byte (B, DQP_B)	H	L	H	H	L	H
Write Bytes (B, A, DQP_A, DQP_B)	H	L	H	H	L	L
Write Byte (C, DQP_C)	H	L	H	L	H	H
Write Bytes (C, A, DQP_C, DQP_A)	H	L	H	L	H	L
Write Bytes (C, B, DQP_C, DQP_B)	H	L	H	L	L	H
Write Bytes (C, B, A, DQP_C, DQP_B, DQP_A)	H	L	H	L	L	L
Write Byte (D, DQP_D)	H	L	L	H	H	H
Write Bytes (D, A, DQP_D, DQP_A)	H	L	L	H	H	L
Write Bytes (D, B, DQP_D, DQP_A)	H	L	L	H	L	H
Write Bytes (D, B, A, DQP_D, DQP_B, DQP_A)	H	L	L	H	L	L
Write Bytes (D, B, DQP_D, DQP_B)	H	L	L	L	H	H
Write Bytes (D, B, A, DQP_D, DQP_C, DQP_A)	H	L	L	L	H	L
Write Bytes (D, C, A, DQP_D, DQP_B, DQP_A)	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Truth Table for Read/Write[3]

Function (CY7C1363B)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	L	H
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

Note:
8. Table only lists a partial listing of the byte write combinations. Any Combination of $\overline{BW}_X$ is valid Appropriate write will be done based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

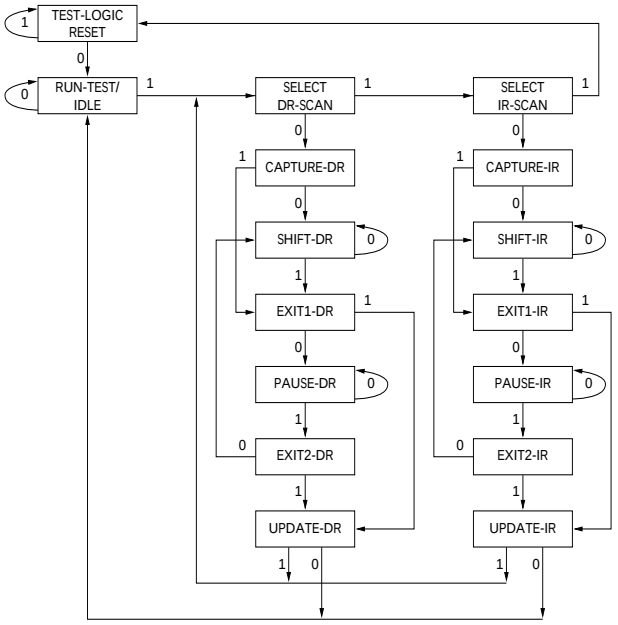
The CY7C1361B/CY7C1363B incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3V or 2.5V I/O logic levels.

The CY7C1361B/CY7C1363B contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW(V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

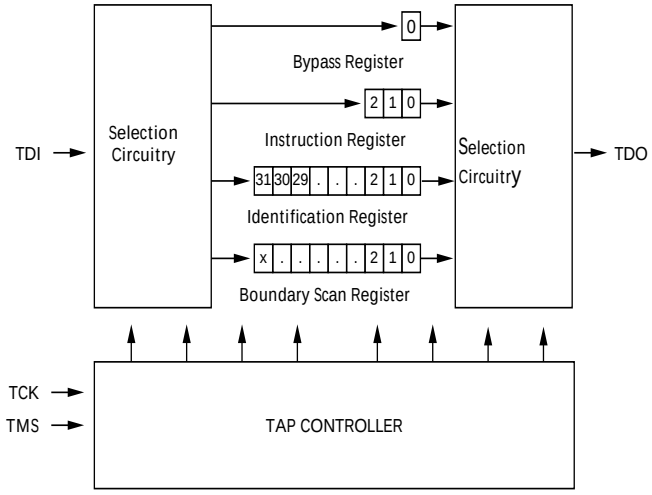
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure . TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Tap Controller Block Diagram.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Tap Controller State Diagram.)

TAP Controller Block Diagram



Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the Tap Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The SRAM has a 71-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller’s capture setup plus hold time (t_{CS} plus t_{CH}).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still

possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

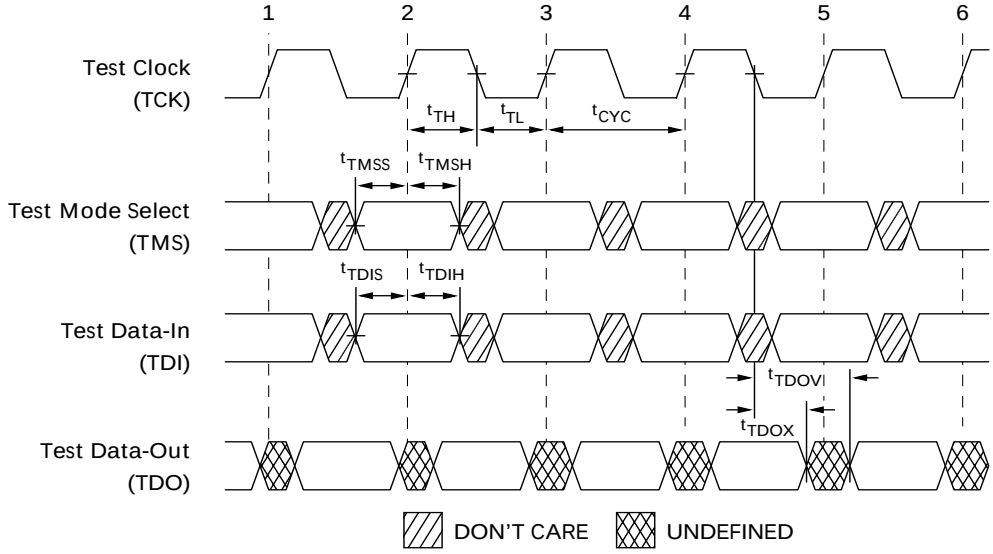
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



TAP AC Switching Characteristics Over the operating Range[9, 10]

Parameter	Description	Min.	Max.	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH time	25		ns
t_{TL}	TCK Clock LOW time	25		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		5	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Setup Times				
t_{TMSS}	TMS Set-Up to TCK Clock Rise	5		ns
t_{TDIS}	TDI Set-Up to TCK Clock Rise	5		ns
t_{CS}	Capture Set-Up to TCK Rise	5		
Hold Times				
t_{TMSH}	TMS hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

Notes:
9. ^{t}CS and ^{t}CH refer to the setup and hold time requirements of latching data from the boundary scan register.
10. Test conditions are specified using the load in TAP AC test Conditions. T_R/t_F = 1ns

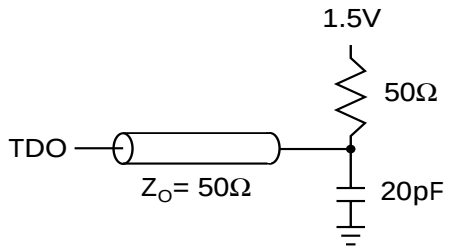
3.3V TAP AC Test Conditions

Input pulse levels ....VSS to 3.3V
Input rise and fall times 1ns
Input timing reference levels 1.5V
Output reference levels 1.5V
Test load termination supply voltage 1.5V

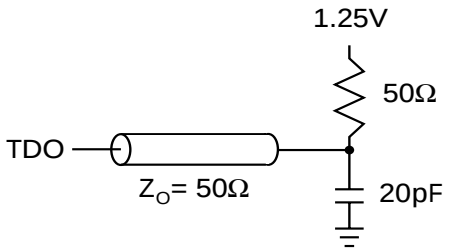
2.5V TAP AC Test Conditions

Input pulse levels ..... VSS to 2.5V
Input rise and fall time 1ns
Input timing reference levels..... .....1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

3.3V TAP AC Output Load Equivalent



2.5V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics And Operating Conditions

(0°C < TA < +70°C; V_{DD} = 3.3V ±0.165V unless otherwise noted)[11]

Parameter	Description	DESCRIPTION	CONDITIONS	MIN	MAX	UNIT
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA	V_{DDQ} = 3.3V	2.4		V
		I_{OH} = –1.0 mA	V_{DDQ} = 2.5V	2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3V	2.9		V
			V_{DDQ} = 2.5V	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3V		0.4	V
		I_{OL} = 8.0 mA	V_{DDQ} = 2.5V		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3V		0.2	V
			V_{DDQ} = 2.5V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3V	–0.5	0.7	V
			V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note:
11. All voltages referenced to VSS (GND).

Identification Register Definitions

Instruction Field	CY7C1361B (256Kx36)	CY7C1363B (512Kx18)	Description
Revision Number (31:29)	001	001	Describes the version number.
Device Depth (28:24)	01010	01010	Reserved for Internal Use
Device Width (23:18)	000000	000000	Defines memory type and architecture
Cypress Device ID (17:12)	100110	010110	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order	71	71

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

119-Ball BGA Boundary Scan Order

CY7C1361B (256K x 36)							CY7C1363B (512K x 18)					
BIT#	BALL ID	Signal Name	BIT#	BALL ID	Signal Name		BIT#	BALL ID	Signal Name	BIT#	BALL ID	Signal Name
1	K4	CLK	37	P4	A0		1	K4	CLK	37	P4	A0
2	H4	$\overline{GW}$	38	N4	A1		2	H4	$\overline{GW}$	38	N4	A1
3	M4	$\overline{BWE}$	39	R6	A		3	M4	$\overline{BWE}$	39	R6	A
4	F4	$\overline{OE}$	40	T5	A		4	F4	$\overline{OE}$	40	T5	A
5	B4	$\overline{ADSC}$	41	T3	A		5	B4	$\overline{ADSC}$	41	T3	A
6	A4	$\overline{ADSP}$	42	R2	A		6	A4	$\overline{ADSP}$	42	R2	A
7	G4	$\overline{ADV}$	43	R3	MODE		7	G4	$\overline{ADV}$	43	R3	MODE
8	C3	A	44	P2	DQP_D		8	C3	A	44	Internal	Internal
9	B3	A	45	P1	DQ_D		9	B3	A	45	Internal	Internal
10	D6	DQP_B	46	L2	DQ_D		10	T2	A	46	Internal	Internal
11	H7	DQ_B	47	K1	DQ_D		11	Internal	Internal	47	Internal	Internal
12	G6	DQ_B	48	N2	DQ_D		12	Internal	Internal	48	P2	DQP_B
13	E6	DQ_B	49	N1	DQ_D		13	Internal	Internal	49	N1	DQ_B
14	D7	DQ_B	50	M2	DQ_D		14	D6	DQP_A	50	M2	DQ_B
15	E7	DQ_B	51	L1	DQ_D		15	E7	DQ_A	51	L1	DQ_B
16	F6	DQ_B	52	K2	DQ_D		16	F6	DQ_A	52	K2	DQ_B
17	G7	DQ_B	53	Internal	Internal		17	G7	DQ_A	53	Internal	Internal
18	H6	DQ_B	54	H1	DQ_C		18	H6	DQ_A	54	H1	DQ_B
19	T7	ZZ	55	G2	DQ_C		19	T7	ZZ	55	G2	DQ_B
20	K7	DQ_A	56	E2	DQ_C		20	K7	DQ_A	56	E2	DQ_B
21	L6	DQ_A	57	D1	DQ_C		21	L6	DQ_A	57	D1	DQ_B
22	N6	DQ_A	58	H2	DQ_C		22	N6	DQ_A	58	Internal	Internal
23	P7	DQ_A	59	G1	DQ_C		23	P7	DQ_A	59	Internal	Internal
24	N7	DQ_A	60	F2	DQ_C		24	Internal	Internal	60	Internal	Internal
25	M6	DQ_A	61	E1	DQ_C		25	Internal	Internal	61	Internal	Internal
26	L7	DQ_A	62	D2	DQP_C		26	Internal	Internal	62	Internal	Internal
27	K6	DQ_A	63	C2	A		27	Internal	Internal	63	C2	A
28	P6	DQP_A	64	A2	A		28	Internal	Internal	64	A2	A
29	T4	A	65	E4	$\overline{CE_1}$		29	T6	A	65	E4	$\overline{CE_1}$
30	A3	A	66	B2	CE_2		30	A3	A	66	B2	CE_2
31	C5	A	67	L3	$\overline{BW_D}$		31	C5	A	67	Internal	Internal
32	B5	A	68	G3	$\overline{BW_C}$		32	B5	A	68	Internal	Internal
33	A5	A	69	G5	$\overline{BW_B}$		33	A5	A	69	G3	$\overline{BW_B}$
34	C6	A	70	L5	$\overline{BW_A}$		34	C6	A	70	L5	$\overline{BW_A}$
35	A6	A	71	Internal	Internal		35	A6	A	71	Internal	Internal
36	B6	A					36	B6	A			

165-Ball fBGA Boundary Scan Order

CY7C1361B (256K x 36)							CY7C1363B (512K x 18)					
BIT#	BALL ID	Signal Name	BIT#	BALL ID	Signal Name		BIT#	BALL ID	Signal Name	BIT#	BALL ID	Signal Name
1	B6	CLK	37	R6	A0		1	B6	CLK	37	R6	A0
2	B7	$\overline{GW}$	38	P6	A1		2	B7	$\overline{GW}$	38	P6	A1
3	A7	$\overline{BWE}$	39	R4	A		3	A7	$\overline{BWE}$	39	R4	A
4	B8	$\overline{OE}$	40	P4	A		4	B8	$\overline{OE}$	40	P4	A
5	A8	$\overline{ADSC}$	41	R3	A		5	A8	$\overline{ADSC}$	41	R3	A
6	B9	$\overline{ADSP}$	42	P3	A		6	B9	$\overline{ADSP}$	42	P3	A
7	A9	$\overline{ADV}$	43	R1	MODE		7	A9	$\overline{ADV}$	43	R1	MODE
8	B10	A	44	N1	DQP_D		8	B10	A	44	Internal	Internal
9	A10	A	45	L2	DQ_D		9	A10	A	45	Internal	Internal
10	C11	DQP_B	46	K2	DQ_D		10	A11	A	46	Internal	Internal
11	E10	DQ_B	47	J2	DQ_D		11	Internal	Internal	47	Internal	Internal
12	F10	DQ_B	48	M2	DQ_D		12	Internal	Internal	48	N1	DQP_B
13	G10	DQ_B	49	M1	DQ_D		13	Internal	Internal	49	M1	DQ_B
14	D10	DQ_B	50	L1	DQ_D		14	C11	DQP_A	50	L1	DQ_B
15	D11	DQ_B	51	K1	DQ_D		15	D11	DQ_A	51	K1	DQ_B
16	E11	DQ_B	52	J1	DQ_D		16	E11	DQ_A	52	J1	DQ_B
17	F11	DQ_B	53	Internal	Internal		17	F11	DQ_A	53	Internal	Internal
18	G11	DQ_B	54	G2	DQ_C		18	G11	DQ_A	54	G2	DQ_B
19	H11	ZZ	55	F2	DQ_C		19	H11	ZZ	55	F2	DQ_B
20	J10	DQ_A	56	E2	DQ_C		20	J10	DQ_A	56	E2	DQ_B
21	K10	DQ_A	57	D2	DQ_C		21	K10	DQ_A	57	D2	DQ_B
22	L10	DQ_A	58	G1	DQ_C		22	L10	DQ_A	58	Internal	Internal
23	M10	DQ_A	59	F1	DQ_C		23	M10	DQ_A	59	Internal	Internal
24	J11	DQ_A	60	E1	DQ_C		24	Internal	Internal	60	Internal	Internal
25	K11	DQ_A	61	D1	DQ_C		25	Internal	Internal	61	Internal	Internal
26	L11	DQ_A	62	C1	DQP_C		26	Internal	Internal	62	Internal	Internal
27	M11	DQ_A	63	B2	A		27	Internal	Internal	63	B2	A
28	N11	DQP_A	64	A2	A		28	Internal	Internal	64	A2	A
29	R11	A	65	A3	$\overline{CE_1}$		29	R11	A	65	A3	$\overline{CE_1}$
30	R10	A	66	B3	CE_2		30	R10	A	66	B3	CE_2
31	P10	A	67	B4	$\overline{BW_D}$		31	P10	A	67	Internal	Internal
32	R9	A	68	A4	$\overline{BW_C}$		32	R9	A	68	Internal	Internal
33	P9	A	69	A5	$\overline{BW_B}$		33	P9	A	69	A4	$\overline{BW_B}$
34	R8	A	70	B5	$\overline{BW_A}$		34	R8	A	70	B5	$\overline{BW_A}$
35	P8	A	71	A6	$\overline{CE_3}$		35	P8	A	71	A6	$\overline{CE_3}$
36	P11	A					36	P11	A			

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND..... –0.5V to +4.6V

DC Voltage Applied to Outputs in three-state ..... –0.5V to V_{DDQ} + 0.5V

DC Input Voltage.....–0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V – 5%/+10%	2.5V – 5% to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics Over the Operating Range [12, 13]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	V_{DDQ} = 3.3V		3.135	V_{DD}	V
		V_{DDQ} = 2.5V		2.375	2.625	V
V_{OH}	Output HIGH Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OH} = –4.0 mA		2.4		V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OL} = 8.0 mA			0.4	V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OL} = 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage[12]	V_{DDQ} = 3.3V		2.0	V_{DD} + 0.3V	V
		V_{DDQ} = 2.5V		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[12]	V_{DDQ} = 3.3V		–0.3	0.8	V
		V_{DDQ} = 2.5V		–0.3	0.7	V
I_X	Input Load	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DD}, Output Disabled		–5	5	µA
I_{OS}	Output Short Circuit Current	V_{DD} = Max., V_{OUT} = GND			-300	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	7.5-ns cycle, 133 MHz		250	mA
			8.8-ns cycle, 117 MHz		220	mA
			10-ns cycle, 100 MHz		180	
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, inputs switching	All speeds		40	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All speeds		30	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{DDQ} – 0.3V or V_{IN} ≤ 0.3V, f = f_{MAX}, inputs switching	All speeds		40	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All Speeds		40	mA

Notes:
12. Overshoot: $V_{IH}(AC) < V_{DD}$ +1.5V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2V$ (Pulse width less than $t_{CYC}/2$).
13. $T_{Power\text{-}up}$: Assumes a linear ramp from 0v to V_{DD}(min.) within 200ms. During this time $V_{IH} \le V_{DD}$ and $V_{DDQ} \le V_{DD}$

Thermal Resistance[14]

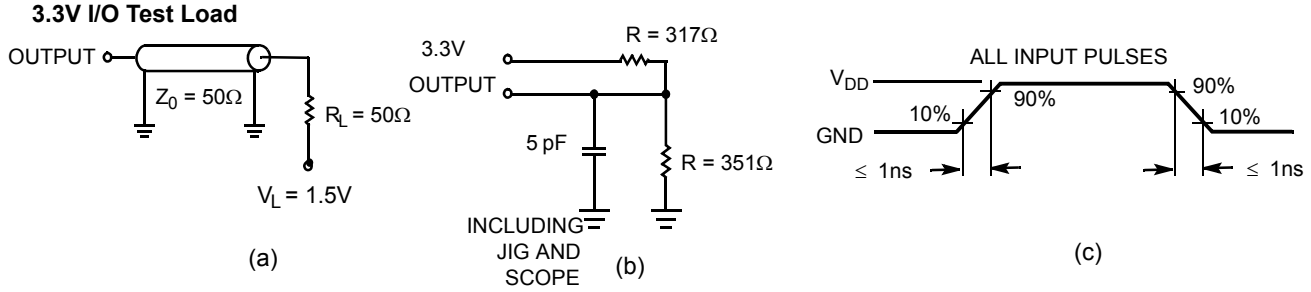
Parameter	Description	Test Conditions	TQFP Package	BGA Package	fBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	25	25	27	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		9	6	6	°C/W

Capacitance[14]

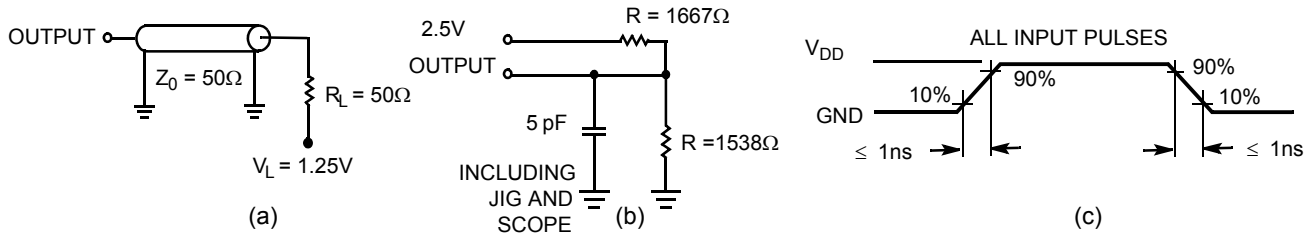
Parameter	Description	Test Conditions	TQFP Package	BGA Package	fBGA Package	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V. V_{DDQ} = 2.5V	5	5	5	pF
C_{CLK}	Clock Input Capacitance		5	5	5	pF
$C_{I/O}$	Input/Output Capacitance		5	7	7	pF

AC Test Loads and Waveforms

3.3V I/O Test Load



2.5V I/O Test Load



Note:
14. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics Over the Operating Range[19, 20]

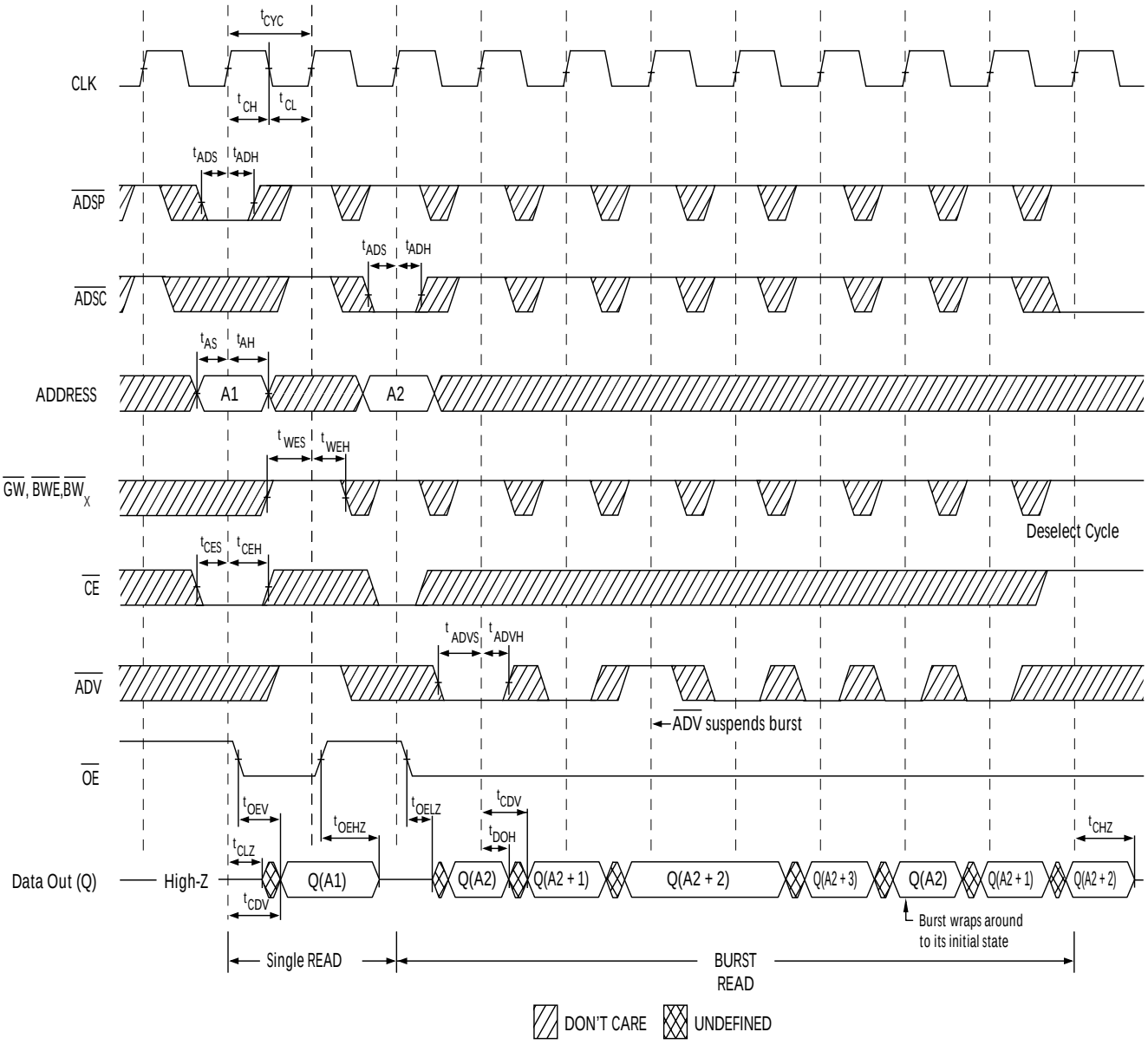
Parameter	Description	133 MHz		117 MHz		100 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{POWER}	V_{DD}(Typical) to the first Access[15]	1		1		1		ms
Clock								
t_{CYC}	Clock Cycle Time	7.5		8.5		10		ns
t_{CH}	Clock HIGH	3.0		3.2		4.0		ns
t_{CL}	Clock LOW	3.0		3.2		4.0		ns
Output Times								
t_{CDV}	Data Output Valid After CLK Rise		6.5		7.5		8.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.0		2.0		2.0		ns
t_{CLZ}	Clock to Low-Z[16, 17, 18]	0		0		0		ns
t_{CHZ}	Clock to High-Z[16, 17, 18]	0	3.5	0	3.5	0	3.5	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		3.5		3.5		3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z[16, 17, 18]	0		0		0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z[16, 17, 18]		3.5		3.5		3.5	ns
Set-up Times								
t_{AS}	Address Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{ADVS}	$\overline{ADV}$ Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{CES}	Chip Enable Set-up	1.5		1.5		1.5		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WEH}	$\overline{GW}$,$\overline{BWE}$, $\overline{BW}_{[A:D]}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		0.5		ns

Notes:

15. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially, before a read or write operation can be initiated.
16. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
17. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions
18. This parameter is sampled and not 100% tested.
19. Timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ} = 2.5V.
20. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

Timing Diagrams

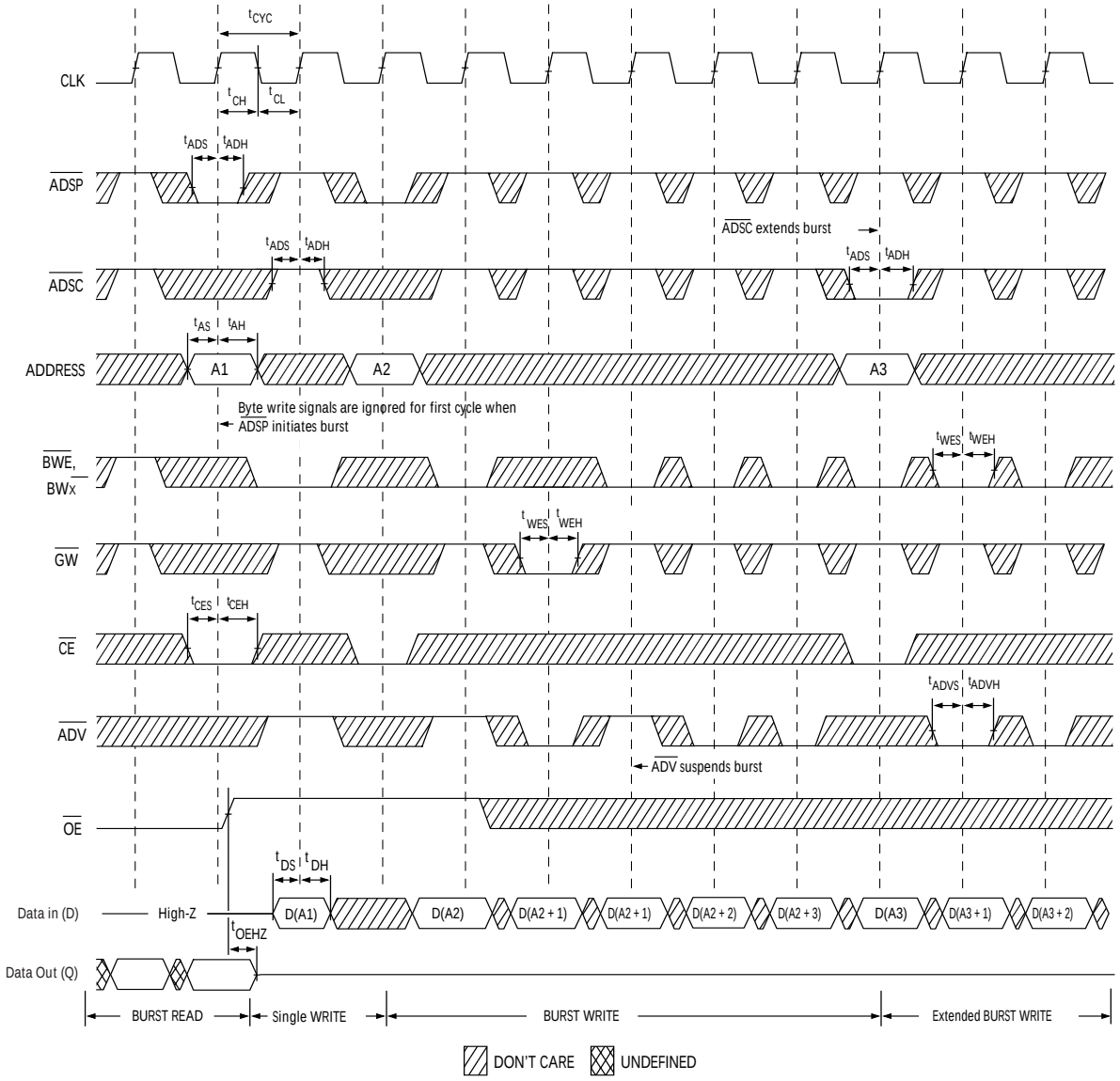
Read Cycle Timing[21]



Note:
21. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Timing Diagrams (continued)

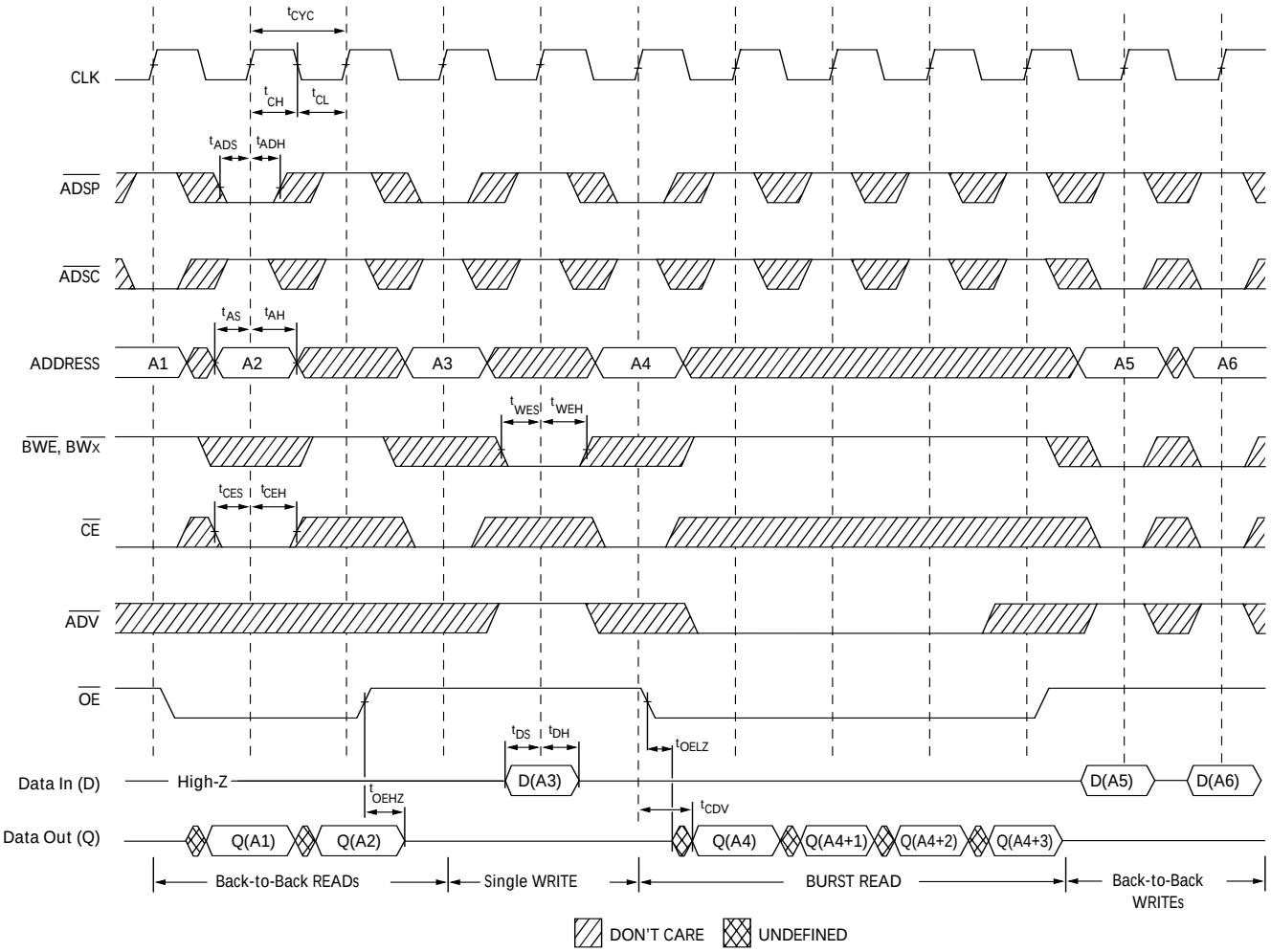
Write Cycle Timing[21, 22]



Notes:
22. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

Timing Diagrams (continued)

Read/Write Cycle Timing[21, 23, 24]

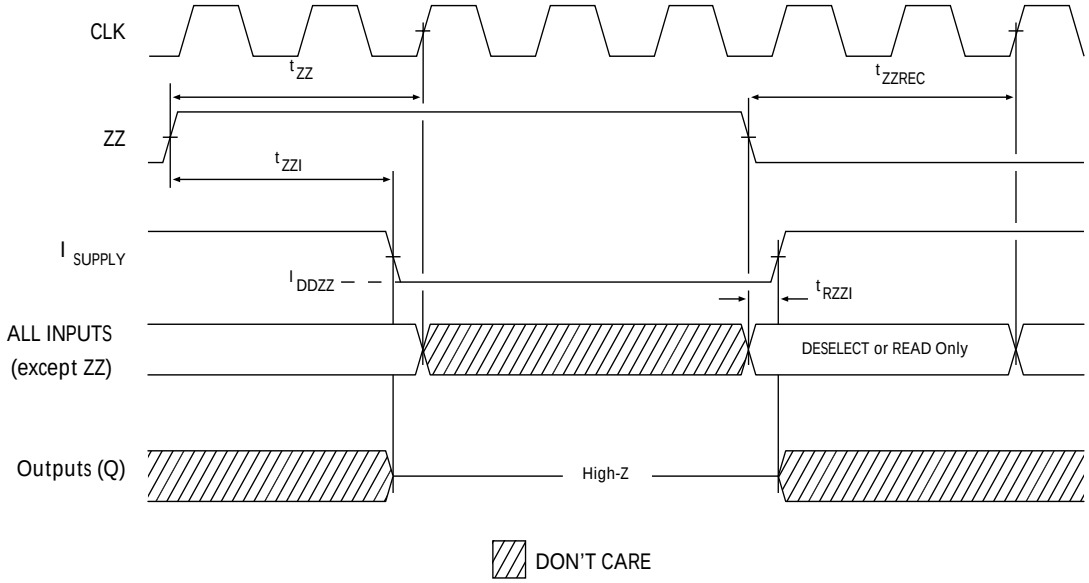


Notes:

23. The data bus (Q) remains in high-Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
24. $\overline{GW}$ is HIGH.
25. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
26. DQs are in high-Z when exiting ZZ sleep mode.

Timing Diagrams (continued)

ZZ Mode Timing[25, 26]



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Part and Package Type	Operating Range
133	CY7C1361B-133AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) 3 Chip Enables	Commercial
	CY7C1363B-133AC			
	CY7C1361B-133AI	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) 3 Chip Enables	Industrial
	CY7C1363B-133AI			
	CY7C1361B-133AJC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) 2 Chip Enables	Commercial
	CY7C1363B-133AJC			
	CY7C1361B-133AJI	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) 2 Chip Enables	Industrial
	CY7C1363B-133AJI			
	CY7C1361B-133BGC	BG119	119-ball (14 x 22 x 2.4 mm) BGA 3 Chip Enables and JTAG	Commercial
	CY7C1363B-133BGC			
	CY7C1361B-133BGI	BG119	119-ball (14 x 22 x 2.4 mm) BGA 3 Chip Enables and JTAG	Industrial
	CY7C1363B-133BGI			
	CY7C1361B-133BZC	BB165A	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.2 mm) 3 Chip Enables and JTAG	Commercial
	CY7C1363B-133BZC			
	CY7C1361B-133BZI	BB165A	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.2 mm) 3 Chip Enables and JTAG	Industrial
	CY7C1363B-133BZI			

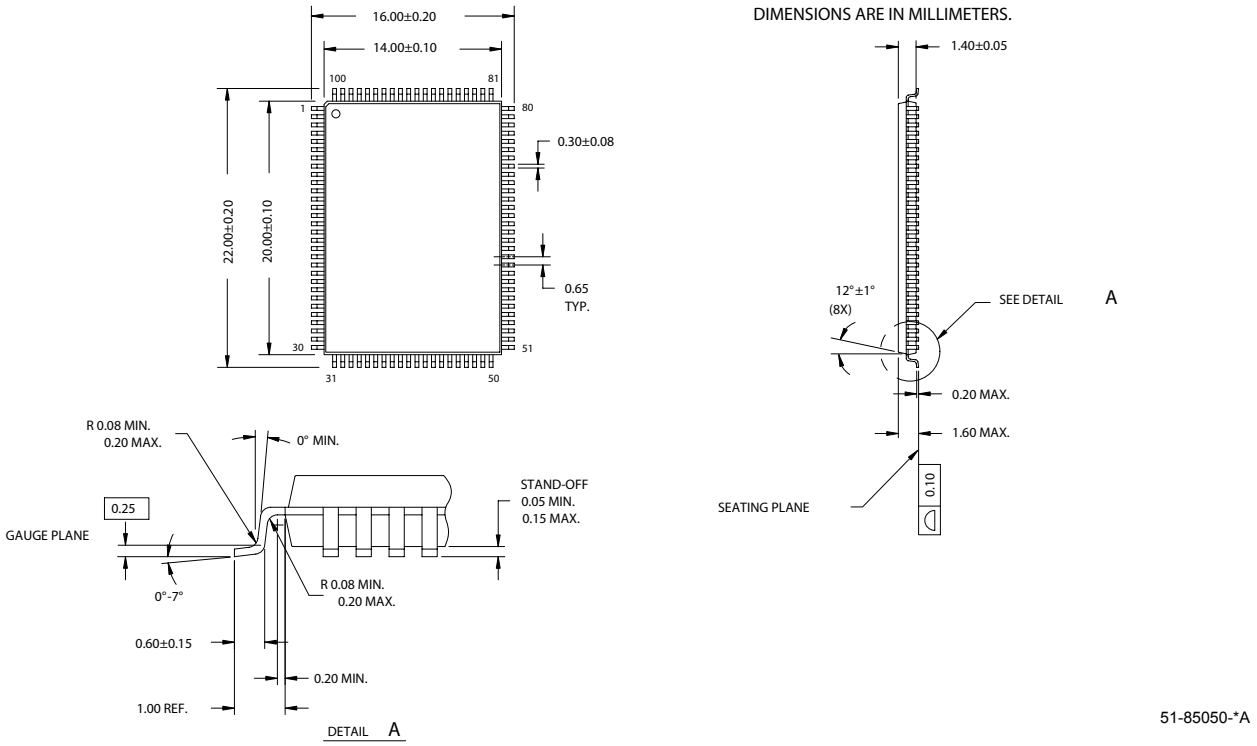
Ordering Information (continued)

Speed (MHz)	Ordering Code	Package Name	Part and Package Type	Operating Range
117	CY7C1361B-117AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4mm) 3 Chip Enables	Commercial
	CY7C1363B-117AC			
	CY7C1361B-117AI	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4mm) 3 Chip Enables	Industrial
	CY7C1363B-117AI			
	CY7C1361B-117AJC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4mm) 2 Chip Enables	Commercial
	CY7C1363B-117AJC			
	CY7C1361B-117AJI	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4mm) 2 Chip Enables	Industrial
	CY7C1363B-117AJI			
	CY7C1361B-117BGC	BG119	119-ball (14 x 22 x 2.4 mm) BGA 3 Chip Enables and JTAG	Commercial
	CY7C1363B-117BGC			
	CY7C1361B-117BGI	BG119	119-ball (14 x 22 x 2.4 mm) BGA 3 Chip Enables and JTAG	Industrial
	CY7C1363B-117BGI			
	CY7C1361B-117BZC	BB165A	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.2mm) 3 Chip Enables and JTAG	Commercial
	CY7C1363B-117BZC			
	CY7C1361B-117BZI	BB165A	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.2mm) 3 Chip Enables and JTAG	Industrial
	CY7C1363B-117BZI			
100	CY7C1361B-100AC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4mm) 3 Chip Enables	Commercial
	CY7C1363B-100AC			
	CY7C1361B-100AI	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4mm) 3 Chip Enables	Industrial
	CY7C1363B-100AI			
	CY7C1361B-100AJC	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4mm) 2 Chip Enables	Commercial
	CY7C1363B-100AJC			
	CY7C1361B-100AJI	A101	100-lead Thin Quad Flat Pack (14 x 20 x 1.4mm) 2 Chip Enables	Industrial
	CY7C1363B-100AJI			
	CY7C1361B-100BGC	BG119	119-ball (14 x 22 x 2.4 mm) BGA 3 Chip Enables and JTAG	Commercial
	CY7C1363B-100BGC			
	CY7C1361B-100BGI	BG119	119-ball (14 x 22 x 2.4 mm) BGA 3 Chip Enables and JTAG	Industrial
	CY7C1363B-100BGI			
	CY7C1361B-100BZC	BB165A	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.2mm) 3 Chip Enables and JTAG	Commercial
	CY7C1363B-100BGC			
	CY7C1361B-100BZI	BB165A	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.2mm) 3 Chip Enables and JTAG	Industrial
	CY7C1363B-100BGI			

Shaded areas contain advance information. Please contact your local sales representative for availability of these parts.

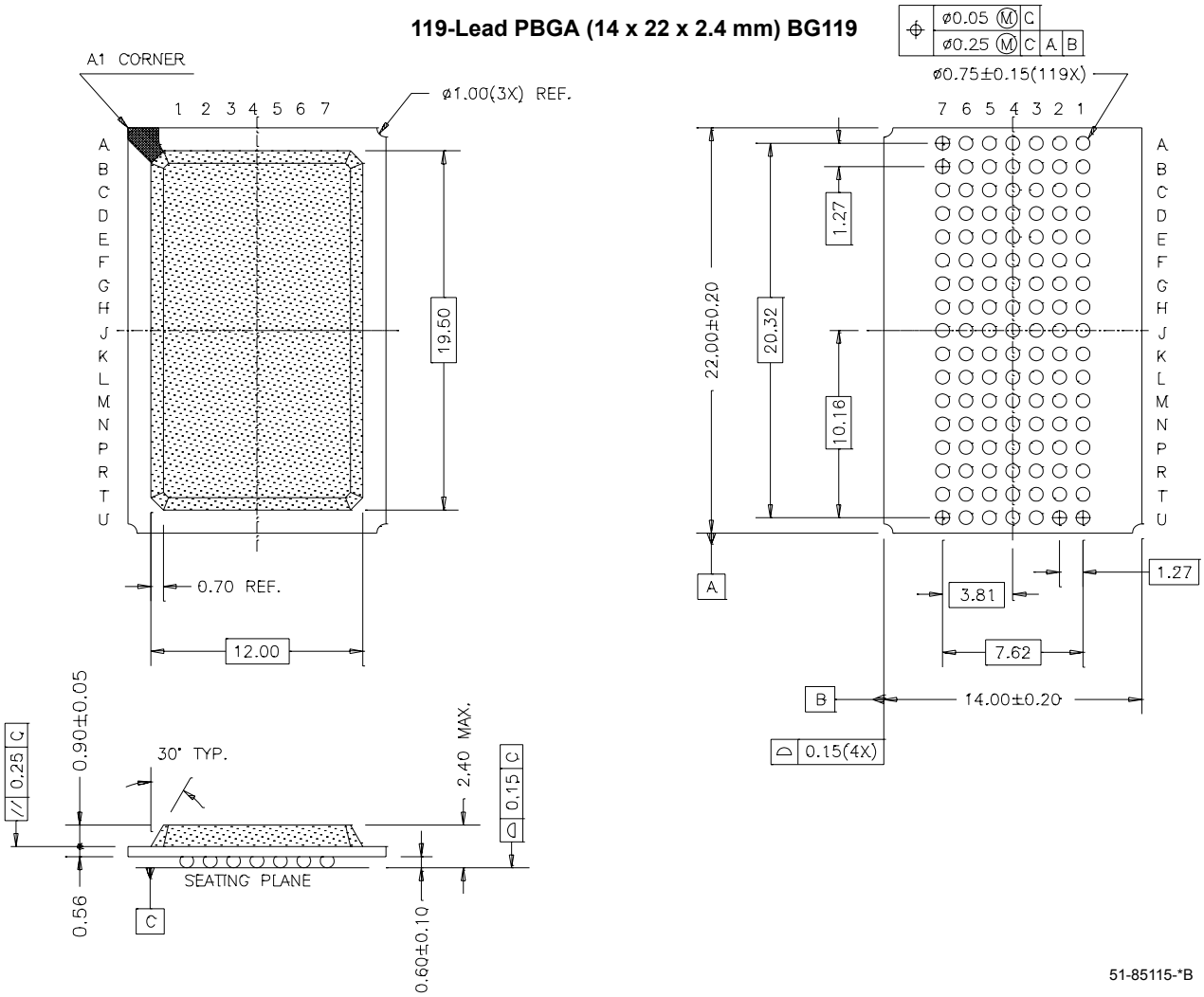
Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



Package Diagrams (continued)

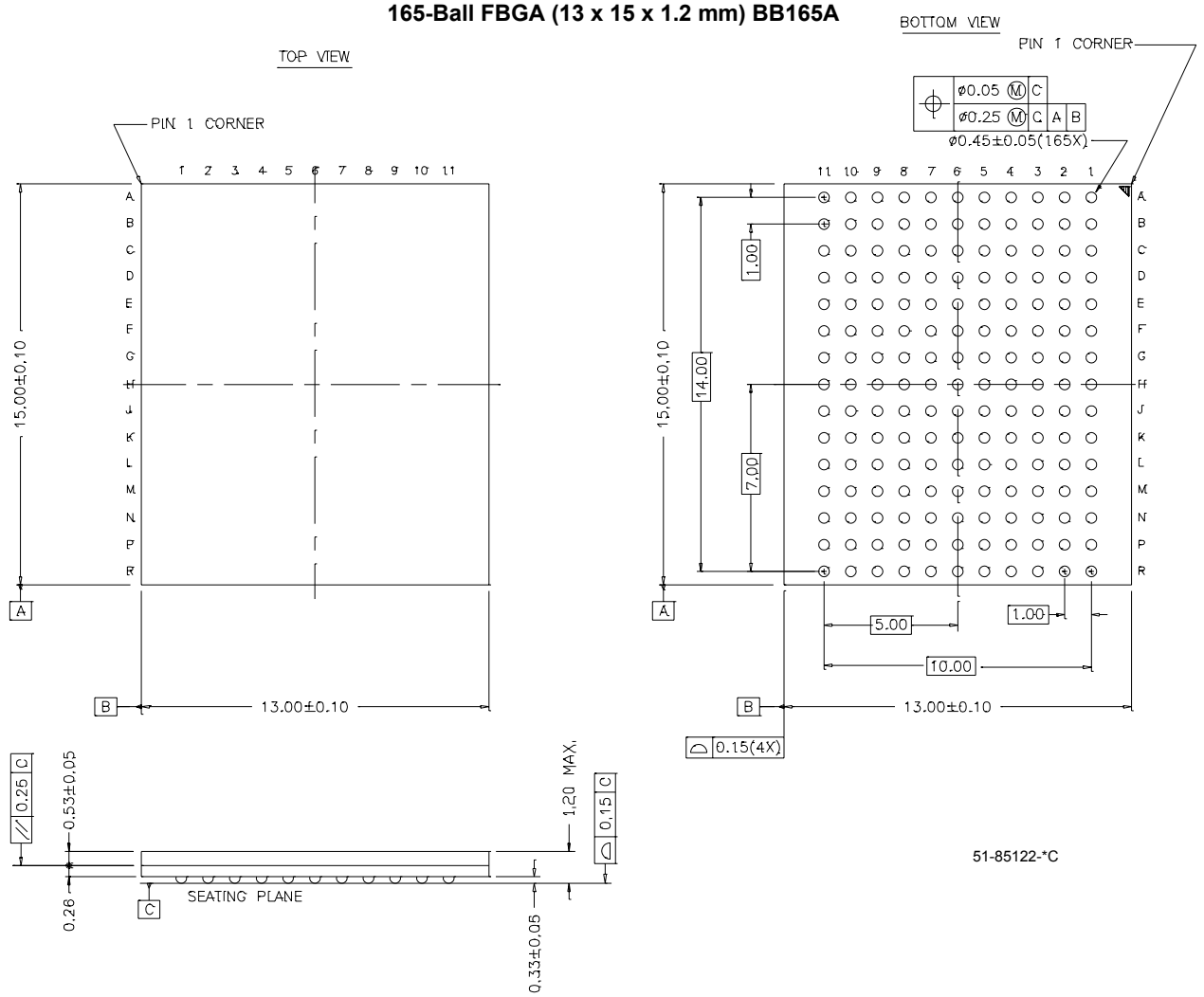
119-Lead PBGA (14 x 22 x 2.4 mm) BG119



51-85115-*B

Package Diagrams (continued)

165-Ball FBGA (13 x 15 x 1.2 mm) BB165A



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Document History Page

Document Title: CY7C1361B/CY7C1363B 9-Mbit (256K x 36/512K x 18) Flow-Through SRAM Document #: 38-05302 Rev. *B				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	116857	06/24/02	RCS	New Data Sheet
*A	206502	See ECN	NJY	Removed Preliminary status Updated Functional Block Diagrams Updated Pin Definitions Added JTAG boundary scan orders Updated timing diagrams
*B	225181	See ECN	VBL	Update Ordering Info section: unshade active part number

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