



**THE DATASHEET OF  
CY7C131-55JXI**



# 1 K × 8 Dual-Port Static RAM

## Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 1 K × 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 15 ns
- Low operating power:  $I_{CC} = 110$  mA (maximum)
- Fully asynchronous operation
- Automatic power-down
- Master CY7C130/130A/CY7C131/131A easily expands data bus width to 16 or more bits using slave CY7C140/CY7C141
- $\overline{BUSY}$  output flag on CY7C130/130A/CY7C131/131A;  $\overline{BUSY}$  input on CY7C140/CY7C141
- $\overline{INT}$  flag for port-to-port communication
- Available in 48-pin DIP (CY7C130/130A/140), 52-pin PLCC, 52-pin TQFP
- Pb-free packages available

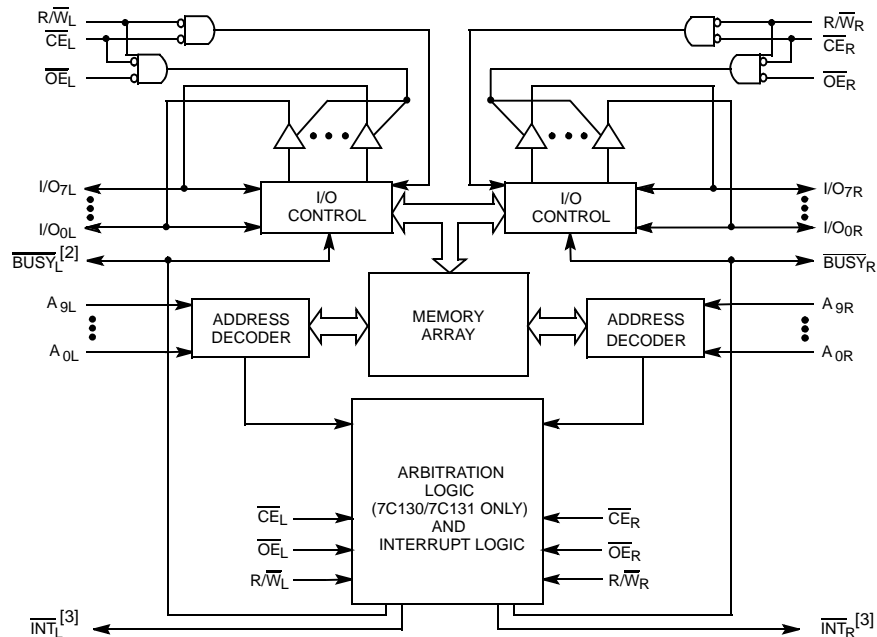
## Functional Description

The CY7C130/130A/CY7C131/131A/CY7C140<sup>[1]</sup> and CY7C141 are high speed CMOS 1 K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/130A/CY7C131/131A can be used as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multi-processor designs.

Each port has independent control pins; chip enable ( $\overline{CE}$ ), write enable ( $R/\overline{W}$ ), and output enable ( $\overline{OE}$ ). Two flags are provided on each port,  $\overline{BUSY}$  and  $\overline{INT}$ .  $\overline{BUSY}$  signals that the port is trying to access the same location currently being accessed by the other port.  $\overline{INT}$  is an interrupt flag indicating that data is placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power down feature is controlled independently on each port by the chip enable ( $\overline{CE}$ ) pins.

The CY7C130/130A and CY7C140 are available in 48-pin DIP. The CY7C131/131A and CY7C141 are available in 52-pin PLCC, 52-pin Pb-free PLCC, 52-pin PQFP, and 52-pin Pb-free PQFP.

## Logic Block Diagram



### Notes

1. CY7C130 and CY7C130A are functionally identical; CY7C131 and CY7C131A are functionally identical.
2. CY7C130/130A/CY7C131/131A (Master):  $\overline{BUSY}$  is open drain output and requires pull-up resistor.  
CY7C140/CY7C141 (Slave):  $\overline{BUSY}$  is input.
3. Open drain outputs: pull-up resistor required.

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## Pin Configurations

Figure 1. Pin Diagram - DIP (Top View)

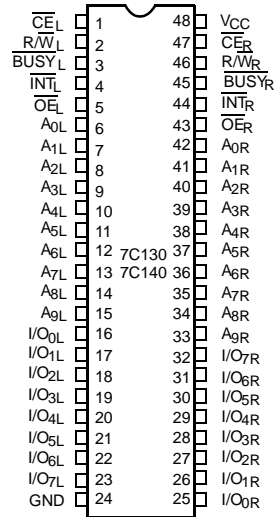


Figure 2. Pin Diagram - PLCC (Top View)

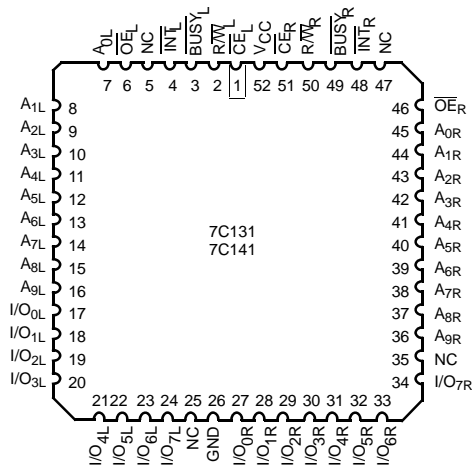
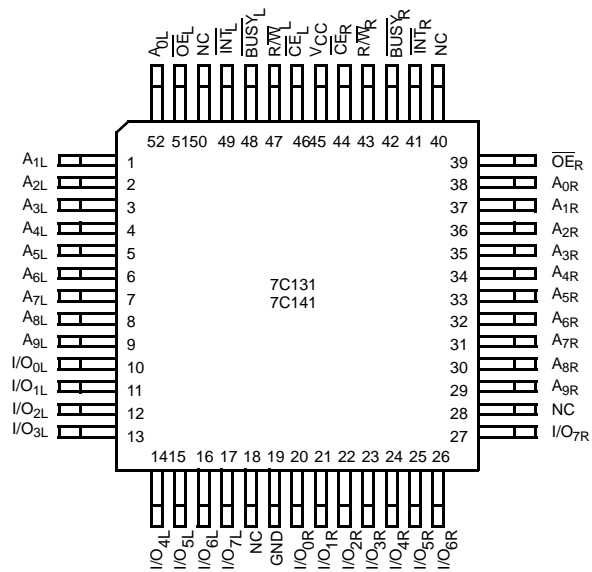


Figure 3. Pin Diagram - PQFP (Top View)



## Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/write enable
$\overline{OE}_L$	$\overline{OE}_R$	Output enable
$A_{0L}-A_{11/12L}$	$A_{0R}-A_{11/12R}$	Address
$I/O_{0L}-I/O_{15/17L}$	$I/O_{0R}-I/O_{15/17R}$	Data bus input/output
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy flag
$V_{CC}$		Power
GND		Ground

## Selection Guide

Parameter		7C131-15 <sup>[4]</sup> 7C131A-15 7C141-15	7C131-25 <sup>[4]</sup> 7C141-25	7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55	Unit
Maximum access time		15	25	30	35	45	55	ns
Maximum operating current	Commercial/ Industrial	190	170	170	120	120	110	mA
Maximum standby current	Commercial/ Industrial	75	65	65	45	45	35	mA

Shaded areas contain preliminary information.

### Note

4. 15 and 25 ns version available only in PLCC/PQFP packages.

## Maximum Ratings<sup>[5]</sup>

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Ambient temperature with power applied ..... -55 °C to +125 °C  
 Supply voltage to ground potential (pin 48 to pin 24) ..... -0.5 V to +7.0 V  
 DC voltage applied to outputs in high Z State ..... -0.5 V to +7.0 V

DC input voltage ..... -3.5 V to +7.0 V  
 Output current into outputs (LOW) ..... 20 mA  
 Static discharge voltage ..... > 2001 V (per MIL-STD-883, method 3015)  
 Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	-40 °C to +85 °C	5 V ± 10%
Military <sup>[6]</sup>	-55 °C to +125 °C	5 V ± 10%

## Electrical Characteristics

Over the Operating Range<sup>[7]</sup>

Parameter	Description	Test Conditions	7C131-15 <sup>[4]</sup> 7C131A-15 7C141-15		7C130-30 <sup>[4]</sup> 7C130A-30 7C131-25,30 7C140-30 7C141-25,30		7C130-35,45 7C131-35,45 7C140-35,45 7C141-35,45		7C130-55 7C131-55 7C140-55 7C141-55		Unit	
			Min	Max	Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	2.4	-	2.4	-	2.4	-	V	
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 4.0 mA	-	0.4	-	0.4	-	0.4	-	0.4	V	
		I <sub>OL</sub> = 16.0 mA <sup>[8]</sup>	-	0.5	-	0.5	-	0.5	-	0.5	V	
V <sub>IH</sub>	Input HIGH voltage		2.2	-	2.2	-	2.2	-	2.2	-	V	
V <sub>IL</sub>	Input LOW voltage		-	0.8	-	0.8	-	0.8	-	0.8	V	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	-5	+5	µA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled	-5	+5	-5	+5	-5	+5	-5	+5	µA	
I <sub>OS</sub>	Output short circuit current <sup>[9, 10]</sup>	V <sub>CC</sub> = Max, V <sub>OUT</sub> = GND	-	-350	-	-350	-	-350	-	-350	mA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	CE = V <sub>IL</sub> , outputs open, f = f <sub>MAX</sub> <sup>[11]</sup>	Commercial	-	190	-	170	-	120	-	110	mA
I <sub>SB1</sub>	Standby current both ports, TTL inputs	CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub> <sup>[11]</sup>	Commercial	-	75	-	65	-	45	-	35	mA
I <sub>SB2</sub>	Standby current one port, TTL inputs	CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>IH</sub> , active port outputs open, f = f <sub>MAX</sub> <sup>[11]</sup>	Commercial	-	135	-	115	-	90	-	75	mA
I <sub>SB3</sub>	Standby current both ports, CMOS inputs	Both ports CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0	Commercial	-	15	-	15	-	15	-	15	mA
I <sub>SB4</sub>	Standby current one port, CMOS inputs	One port CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, active port outputs open, f = f <sub>MAX</sub> <sup>[11]</sup>	Commercial	-	125	-	105	-	85	-	70	mA

Shaded areas contain preliminary information.

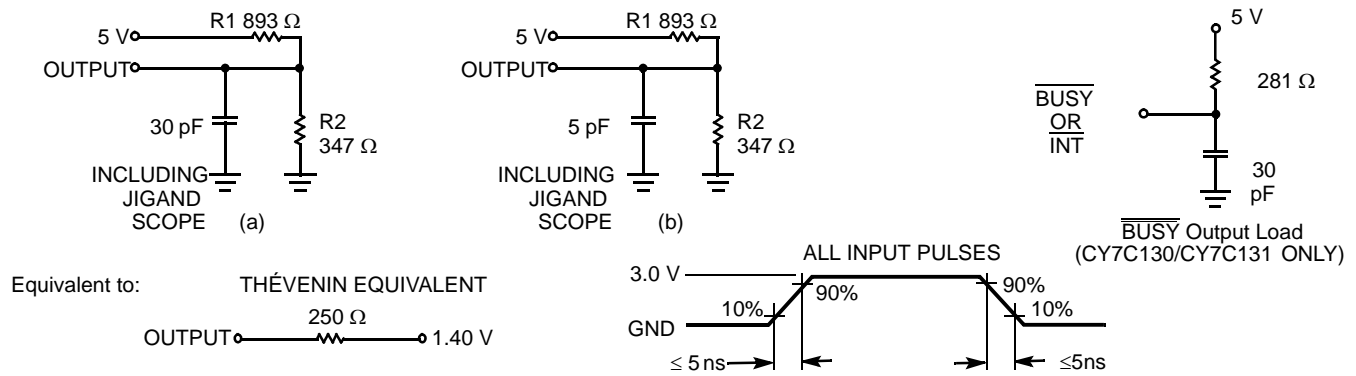
### Notes

- The voltage on any input or I/O pin cannot exceed the power pin during power up.
- T<sub>A</sub> is the "instant on" case temperature
- See the last page of this specification for Group A subgroup testing information.
- BUSY and INT pins only.
- Duration of the short circuit should not exceed 30 seconds.
- This parameter is guaranteed but not tested.
- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency of read cycle of 1/t<sub>RC</sub> and using AC Test Waveforms input levels of GND to 3 V.

**Capacitance<sup>[10]</sup>**

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$	15	pF
$C_{OUT}$	Output capacitance		10	pF

**Figure 4. AC Test Loads and Waveforms**



## Switching Characteristics

Over the Operating Range<sup>[12, 13]</sup>

Parameter	Description	7C131-15 <sup>[14]</sup> 7C131A-15 7C141-15		7C130-25 <sup>[14]</sup> 7C131-25 7C140-25 7C141-25		7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30		Unit
		Min	Max	Min	Max	Min	Max	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read cycle time	15	–	25	–	30	–	ns
t <sub>AA</sub>	Address to data valid <sup>[15]</sup>	–	15	–	25	–	30	ns
t <sub>OHA</sub>	Data hold from address change	0	–	0	–	0	–	ns
t <sub>ACE</sub>	CE LOW to data valid <sup>[15]</sup>	–	15	–	25	–	30	ns
t <sub>DOE</sub>	OE LOW to data valid <sup>[15]</sup>	–	10	–	15	–	20	ns
t <sub>LZOE</sub>	OE LOW to low Z <sup>[16, 17, 18]</sup>	3	–	3	–	3	–	ns
t <sub>HZOE</sub>	OE HIGH to high Z <sup>[16, 17, 18]</sup>	–	10	–	15	–	15	ns
t <sub>LZCE</sub>	CE LOW to low Z <sup>[16, 17, 18]</sup>	3	–	5	–	5	–	ns
t <sub>HZCE</sub>	CE HIGH to high Z <sup>[16, 17, 18]</sup>	–	10	–	15	–	15	ns
t <sub>PU</sub>	CE LOW to power-up <sup>[16]</sup>	0	–	0	–	0	–	ns
t <sub>PD</sub>	CE HIGH to power-down <sup>[16]</sup>	–	15	–	25	–	25	ns
<b>Write Cycle<sup>[19]</sup></b>								
t <sub>WC</sub>	Write cycle time	15	–	25	–	30	–	ns
t <sub>SCE</sub>	CE LOW to write end	12	–	20	–	25	–	ns
t <sub>AW</sub>	Address setup to write end	12	–	20	–	25	–	ns
t <sub>HA</sub>	Address hold from write end	2	–	2	–	2	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	0	–	0	–	ns
t <sub>PWE</sub>	R/W pulse width	12	–	15	–	25	–	ns
t <sub>SD</sub>	Data setup to write end	10	–	15	–	15	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	0	–	0	–	ns
t <sub>HZWE</sub>	R/W LOW to high Z <sup>[18]</sup>	–	10	–	15	–	15	ns
t <sub>LZWE</sub>	R/W HIGH to low Z <sup>[18]</sup>	0	–	0	–	0	–	ns

Shaded areas contain preliminary information.

### Notes

12. See the last page of this specification for Group A subgroup testing information.
13. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
14. 15 and 25 ns version available only in PLCC/PQFP packages.
15. AC Test Conditions use V<sub>OH</sub> = 1.6 V and V<sub>OL</sub> = 1.4 V.
16. This parameter is guaranteed but not tested.
17. At any given temperature and voltage condition for any given device, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> and t<sub>HZOE</sub> is less than t<sub>LZOE</sub>.
18. t<sub>LZCE</sub>, t<sub>LZWE</sub>, t<sub>HZOE</sub>, t<sub>LZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
19. The internal write time of the memory is defined by the overlap of CS LOW and R/W LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

## Switching Characteristics

Over the Operating Range<sup>[12, 13]</sup> (continued)

Parameter	Description	7C131-15 <sup>[14]</sup> 7C131A-15 7C141-15		7C130-25 <sup>[14]</sup> 7C131-25 7C140-25 7C141-25		7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30		Unit
		Min	Max	Min	Max	Min	Max	
<b>Busy/Interrupt Timing</b>								
t <sub>BLA</sub>	BUSY LOW from address match	–	15	–	20	–	20	ns
t <sub>BHA</sub>	BUSY HIGH from address mismatch <sup>[20]</sup>	–	15	–	20	–	20	ns
t <sub>BLC</sub>	BUSY LOW from CE LOW	–	15	–	20	–	20	ns
t <sub>BHC</sub>	BUSY HIGH from CE HIGH <sup>[20]</sup>	–	15	–	20	–	20	ns
t <sub>PS</sub>	Port set-up for priority	5	–	5	–	5	–	ns
t <sub>WB</sub> <sup>[21]</sup>	R/W LOW after BUSY LOW	0	–	0	–	0	–	ns
t <sub>WH</sub>	R/W HIGH after BUSY HIGH	13	–	20	–	30	–	ns
t <sub>BDD</sub>	BUSY HIGH to valid data	–	15	–	25	–	30	ns
t <sub>DDD</sub>	Write data valid to read data valid	–	Note 22	–	Note 22	–	Note 22	ns
t <sub>WDD</sub>	Write pulse to data delay	–	Note 22	–	Note 22	–	Note 22	ns
<b>Interrupt Timing</b>								
t <sub>WINS</sub>	R/W to INTERRUPT set time	–	15	–	25	–	25	ns
t <sub>EINS</sub>	CE to INTERRUPT set time	–	15	–	25	–	25	ns
t <sub>INS</sub>	Address to INTERRUPT set time	–	15	–	25	–	25	ns
t <sub>OINR</sub>	OE to INTERRUPT reset time <sup>[20]</sup>	–	15	–	25	–	25	ns
t <sub>EINR</sub>	CE to INTERRUPT reset time <sup>[20]</sup>	–	15	–	25	–	25	ns
t <sub>INR</sub>	Address to INTERRUPT reset time <sup>[20]</sup>	–	15	–	25	–	25	ns

Shaded areas contain preliminary information.

### Notes

20. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.

21. CY7C140/CY7C141 only.

22. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:

BUSY on Port B goes HIGH.

Port B's address is toggled.

CE for Port B is toggled.

R/W for Port B is toggled during valid read.

## Switching Characteristics

Over the Operating Range<sup>[23, 24]</sup>

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min	Max	Min	Max	Min	Max	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read cycle time	35	–	45	–	55	–	ns
t <sub>AA</sub>	Address to data valid <sup>[25]</sup>	–	35	–	45	–	55	ns
t <sub>OHA</sub>	Data hold from address change	0	–	0	–	0	–	ns
t <sub>ACE</sub>	CE LOW to data valid <sup>[25]</sup>	–	35	–	45	–	55	ns
t <sub>DOE</sub>	OE LOW to data valid <sup>[25]</sup>	–	20	–	25	–	25	ns
t <sub>LZOE</sub>	OE LOW to low Z <sup>[26, 27, 28]</sup>	3	–	3	–	3	–	ns
t <sub>HZOE</sub>	OE HIGH to high Z <sup>[26, 27, 28]</sup>	–	20	–	20	–	25	ns
t <sub>LZCE</sub>	CE LOW to low Z <sup>[26, 27, 28]</sup>	5	–	5	–	5	–	ns
t <sub>HZCE</sub>	CE HIGH to high Z <sup>[26, 27, 28]</sup>	–	20	–	20	–	25	ns
t <sub>PU</sub>	CE LOW to power-up <sup>[26]</sup>	0	–	0	–	0	–	ns
t <sub>PD</sub>	CE HIGH to power-down <sup>[26]</sup>	–	35	–	35	–	35	ns
<b>Write Cycle</b> <sup>[29]</sup>								
t <sub>WC</sub>	Write cycle time	35	–	45	–	55	–	ns
t <sub>SCE</sub>	CE LOW to write end	30	–	35	–	40	–	ns
t <sub>AW</sub>	Address set-up to write end	30	–	35	–	40	–	ns
t <sub>HA</sub>	Address hold from write end	2	–	2	–	2	–	ns
t <sub>SA</sub>	Address set-up to write start	0	–	0	–	0	–	ns
t <sub>PWE</sub>	R/W pulse width	25	–	30	–	30	–	ns
t <sub>SD</sub>	Data set-up to write end	15	–	20	–	20	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	0	–	0	–	ns
t <sub>HZWE</sub>	R/W LOW to high Z <sup>[28]</sup>	–	20	–	20	–	25	ns
t <sub>LZWE</sub>	R/W HIGH to low Z <sup>[28]</sup>	0	–	0	–	0	–	ns

### Notes

23. See the last page of this specification for Group A subgroup testing information.

24. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.

25. AC Test Conditions use V<sub>OH</sub> = 1.6 V and V<sub>OL</sub> = 1.4 V.

26. This parameter is guaranteed but not tested.

27. At any given temperature and voltage condition for any given device, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> and t<sub>HZOE</sub> is less than t<sub>LZOE</sub>.

28. t<sub>LZCE</sub>, t<sub>LZWE</sub>, t<sub>HZOE</sub>, t<sub>LZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.

29. The internal write time of the memory is defined by the overlap of CS LOW and R/W LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

## Switching Characteristics

Over the Operating Range<sup>[23, 24]</sup> (continued)

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min	Max	Min	Max	Min	Max	
<b>Busy/Interrupt Timing</b>								
t <sub>BLA</sub>	BUSY LOW from address match	–	20	–	25	–	30	ns
t <sub>BHA</sub>	BUSY HIGH from address mismatch <sup>[30]</sup>	–	20	–	25	–	30	ns
t <sub>BLC</sub>	BUSY LOW from CE LOW	–	20	–	25	–	30	ns
t <sub>BHC</sub>	BUSY HIGH from CE HIGH <sup>[30]</sup>	–	20	–	25	–	30	ns
t <sub>PS</sub>	Port set-up for priority	5	–	5	–	5	–	ns
t <sub>WB</sub> <sup>[31]</sup>	R/W LOW after BUSY LOW	0	–	0	–	0	–	ns
t <sub>WH</sub>	R/W HIGH after BUSY HIGH	30	–	35	–	35	–	ns
t <sub>BDD</sub>	BUSY HIGH to valid data	–	35	–	45	–	45	ns
t <sub>DDD</sub>	Write data valid to read data valid	–	Note 32	–	Note 32	–	Note 32	ns
t <sub>WDD</sub>	Write pulse to data delay	–	Note 32	–	Note 32	–	Note 32	ns
<b>Interrupt Timing</b>								
t <sub>WINS</sub>	R/W to INTERRUPT set time	–	25	–	35	–	45	ns
t <sub>EINS</sub>	CE to INTERRUPT set time	–	25	–	35	–	45	ns
t <sub>INS</sub>	Address to INTERRUPT set time	–	25	–	35	–	45	ns
t <sub>OINR</sub>	OE to INTERRUPT reset time <sup>[20]</sup>	–	25	–	35	–	45	ns
t <sub>EINR</sub>	CE to INTERRUPT reset time <sup>[20]</sup>	–	25	–	35	–	45	ns
t <sub>INR</sub>	Address to INTERRUPT reset time <sup>[20]</sup>	–	25	–	35	–	45	ns

### Notes

30. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.

31. CY7C140/CY7C141 only.

32. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:

BUSY on Port B goes HIGH.

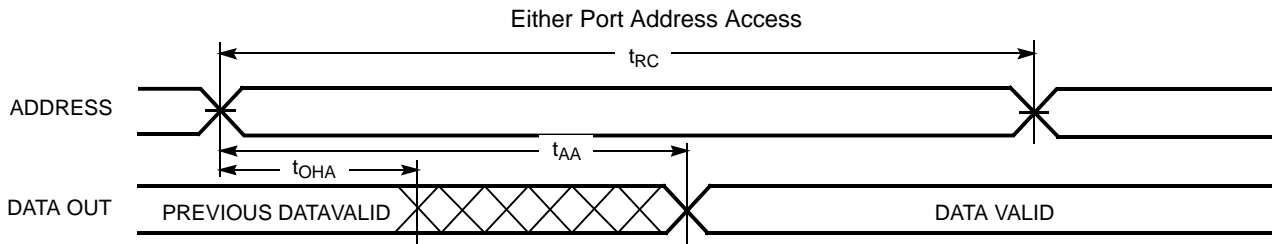
Port B's address is toggled.

CE for Port B is toggled.

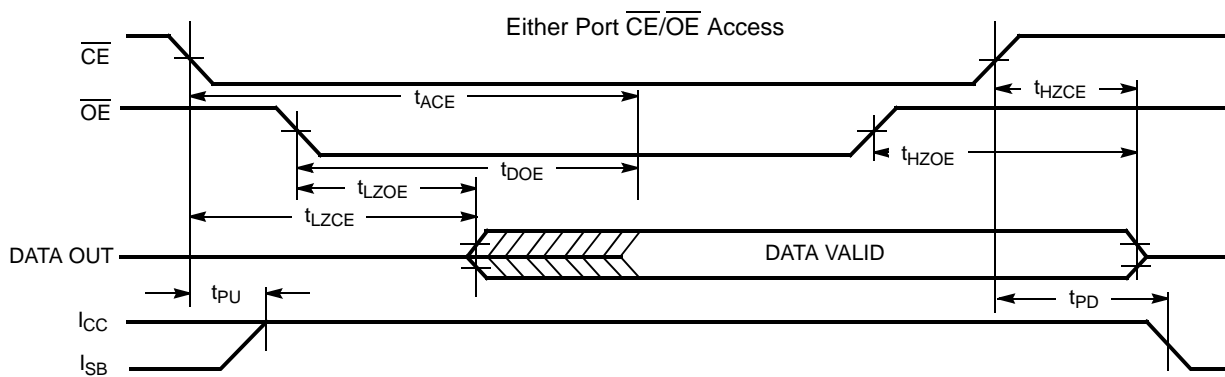
R/W for Port B is toggled during valid read.

## Switching Waveforms

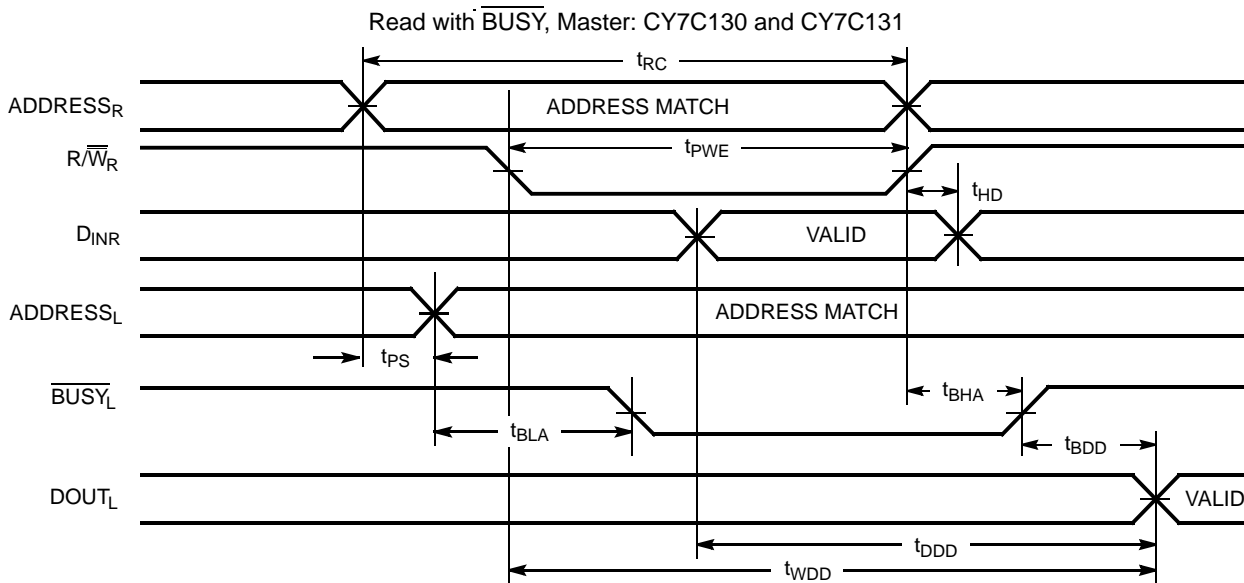
**Figure 5. Read Cycle No. 1<sup>[33, 34]</sup>**



**Figure 6. Read Cycle No. 2<sup>[33, 35]</sup>**



**Figure 7. Read Cycle No. 3<sup>[34]</sup>**



### Notes

- 33.  $\overline{RW}$  is HIGH for read cycle.
- 34. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
- 35. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (OE Three-States Data I/Os—Either Port)<sup>[36, 37]</sup>

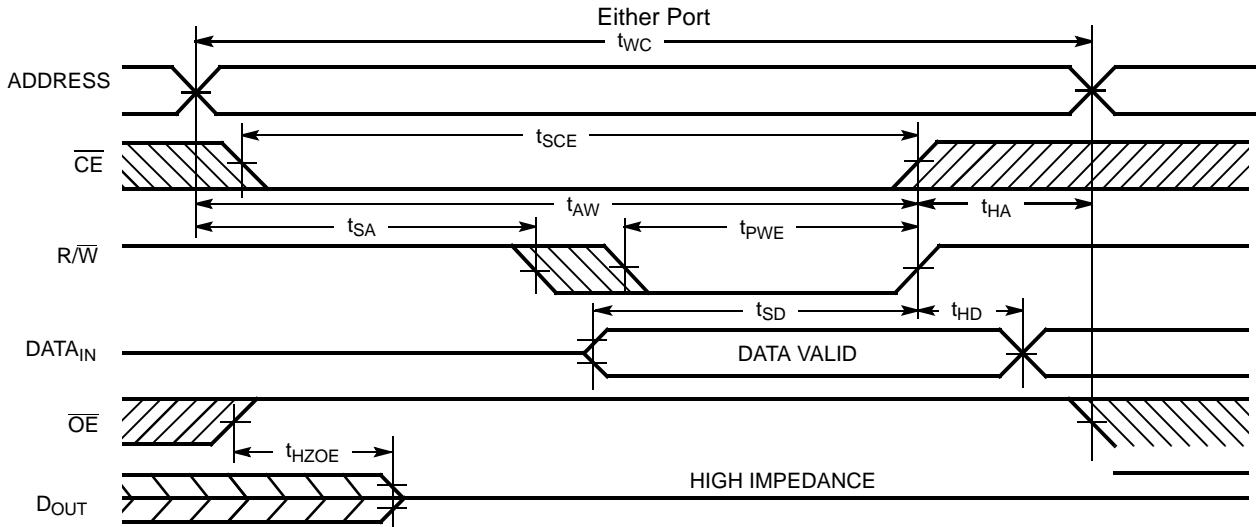
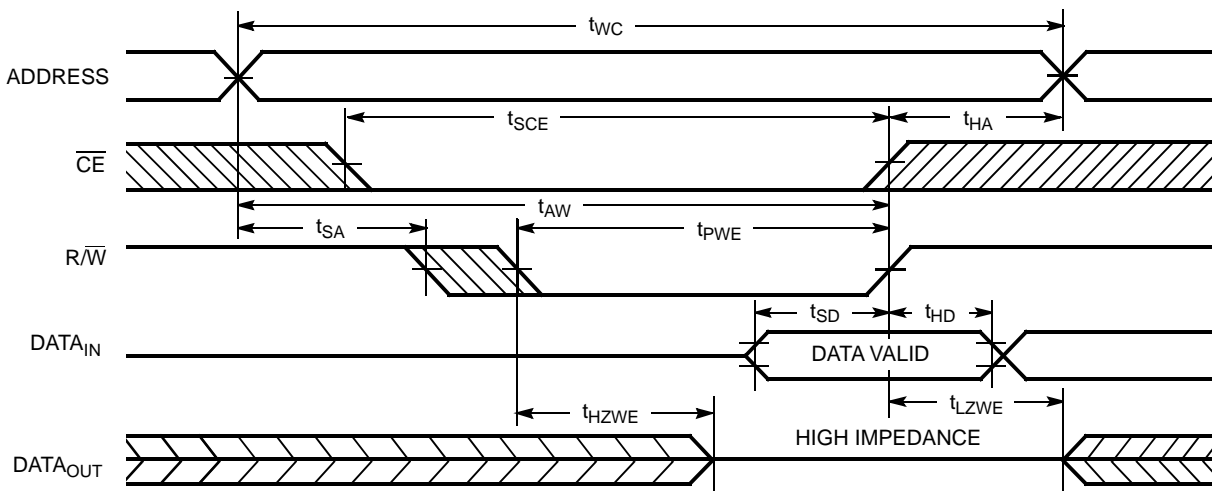


Figure 9. Write Cycle No. 2 (R/W Three-States Data I/Os—Either Port)<sup>[38, 39]</sup>



Notes

36. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{R/W}$  LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
37. If  $\overline{OE}$  is LOW during a  $\overline{R/W}$  controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or  $t_{HZWE} + t_{SD}$  to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required  $t_{SD}$ .
38. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
39. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the  $\overline{R/W}$  LOW transition, the outputs remain in the high impedance state.

Switching Waveforms (continued)

Figure 10. Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration)

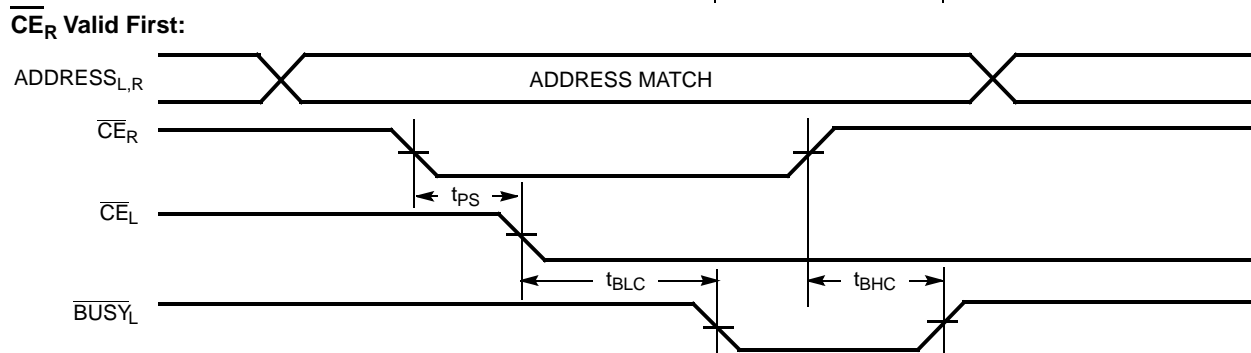
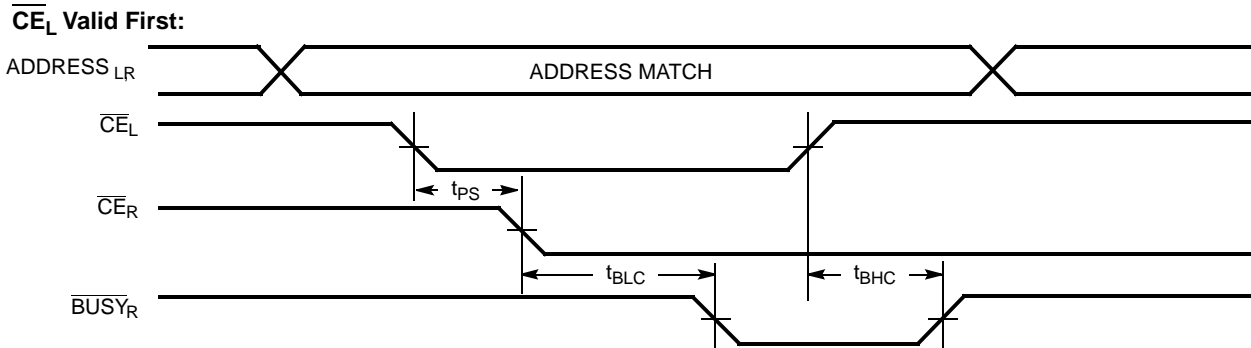
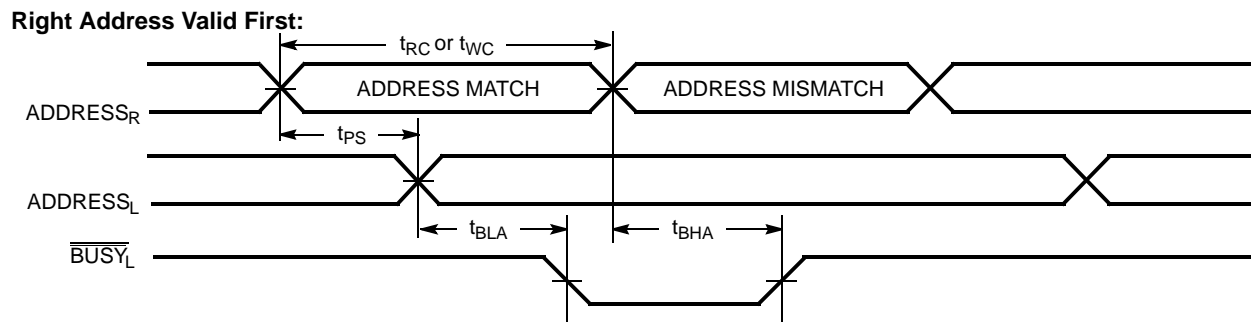
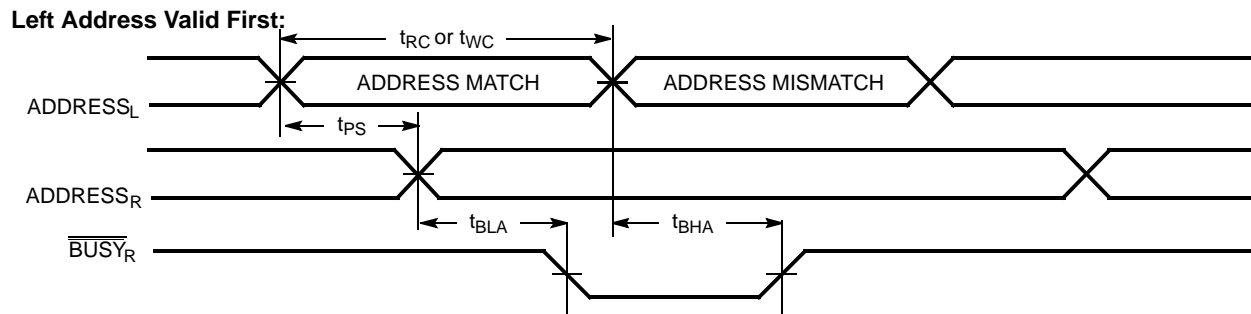
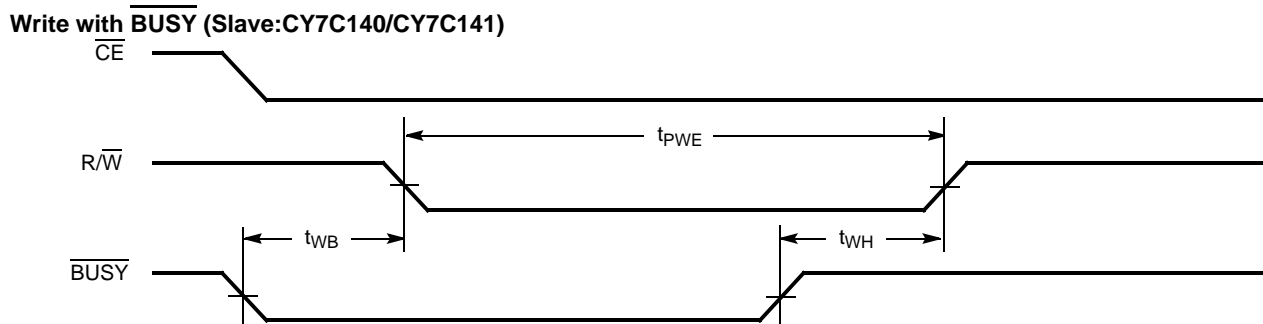


Figure 11. Busy Timing Diagram No. 2 (Address Arbitration)



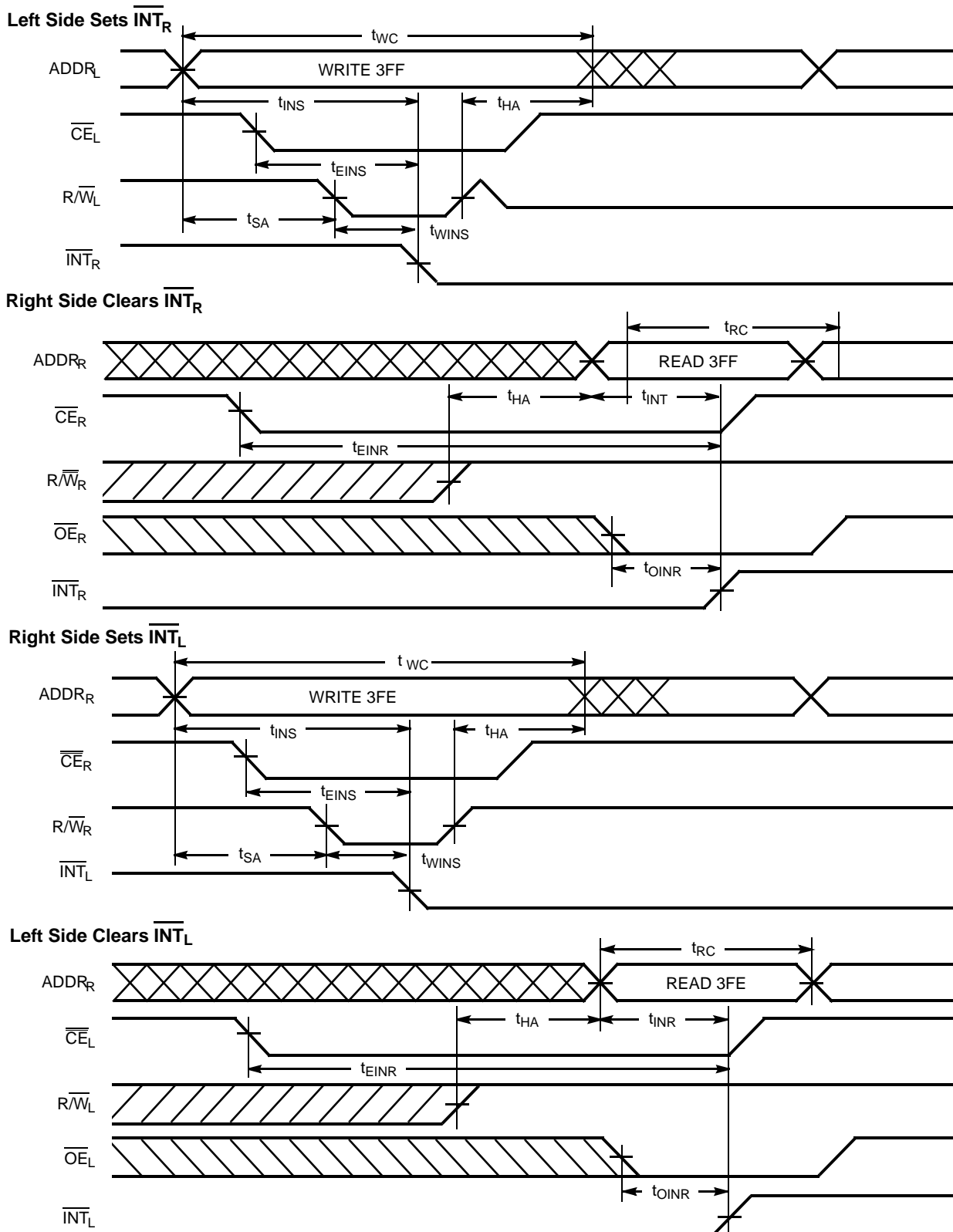
Switching Waveforms (continued)

Figure 12. Busy Timing Diagram No. 3

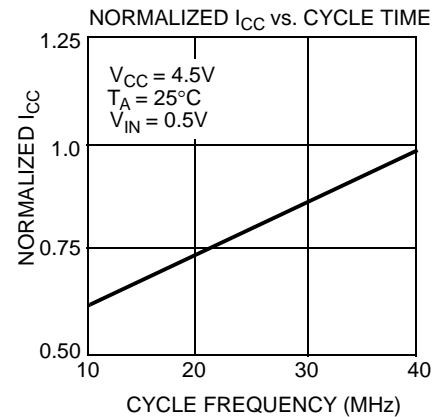
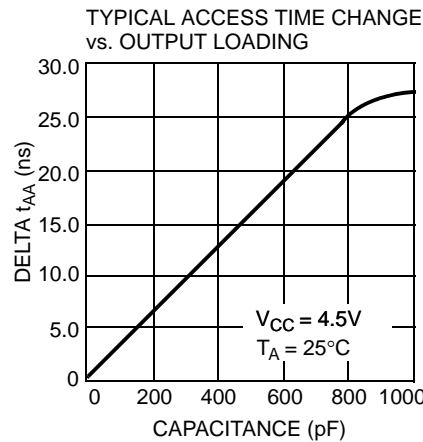
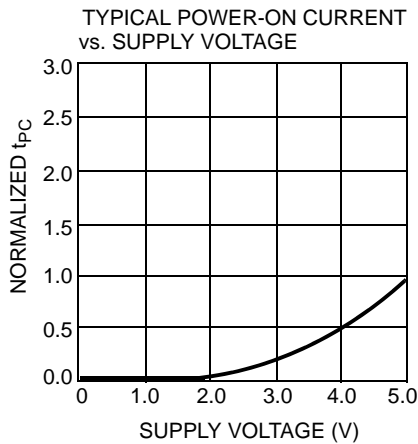
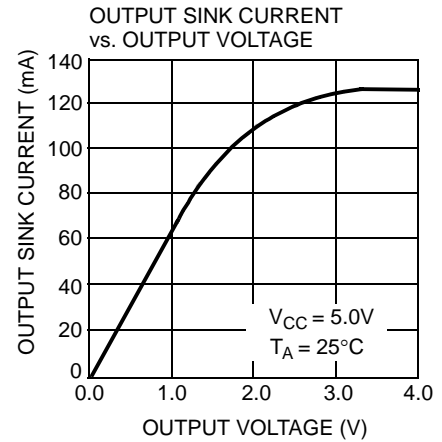
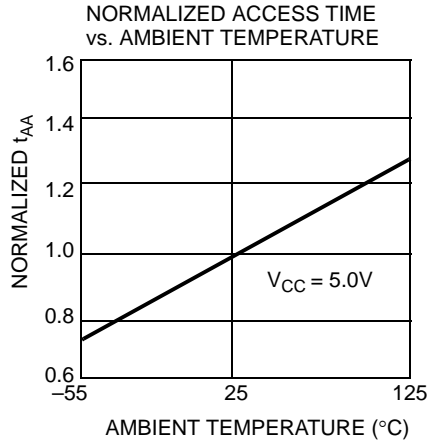
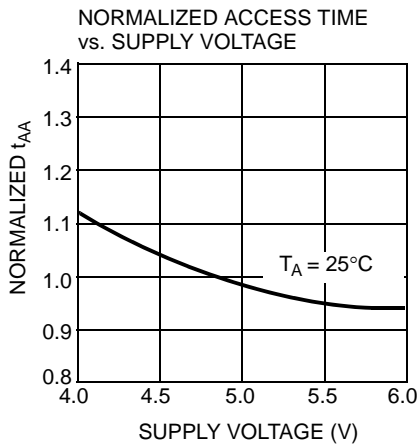
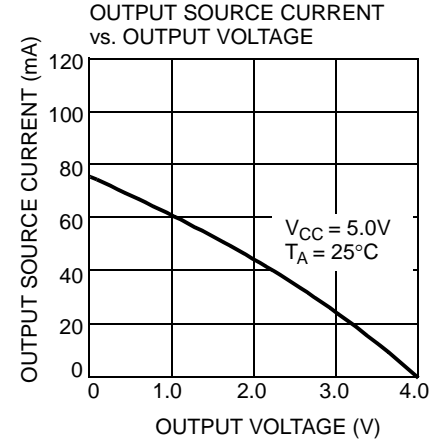
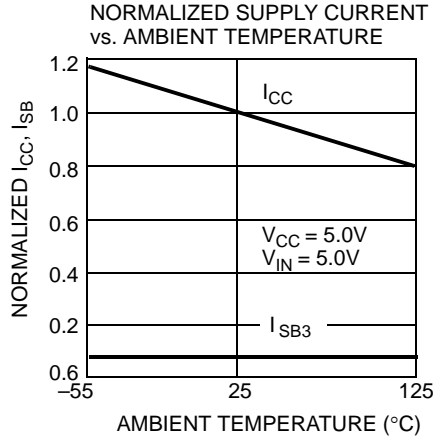
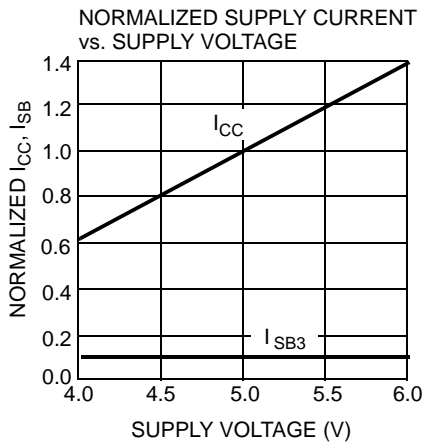


Switching Waveforms (continued)

Figure 13. Interrupt Timing Diagrams



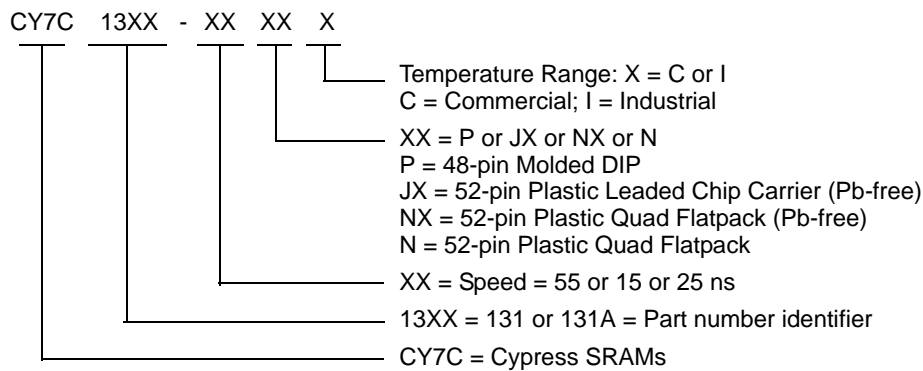
**Typical DC and AC Characteristics**



### Ordering Information

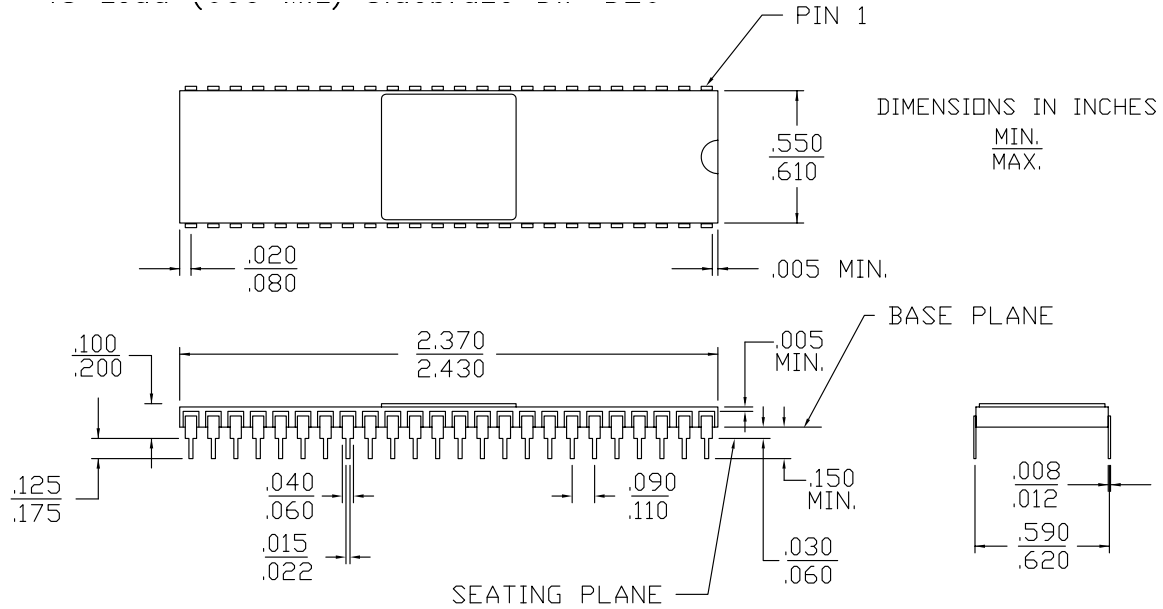
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY7C130-55PC	P25	48-pin (600 Mil) Molded DIP	Commercial
15	CY7C131A-15JXI	J69	52-pin Pb-free Plastic Leaded Chip Carrier	Industrial
	CY7C131-15NXI	N52	52-pin Pb-free Plastic Quad Flatpack	
25	CY7C131-25JXC	J69	52-pin Pb-free Plastic Leaded Chip Carrier	Commercial
	CY7C131-25NXC	N52	52-pin Pb-free Plastic Quad Flatpack	
55	CY7C131-55JXC	J69	52-pin Pb-free Plastic Leaded Chip Carrier	Commercial
	CY7C131-55NXC	N52	52-pin Pb-free Plastic Quad Flatpack	
	CY7C131-55JXI	J69	52-pin Pb-free Plastic Leaded Chip Carrier	Industrial
	CY7C131-55NXI	N52	52-pin Pb-free Plastic Quad Flatpack	

### Ordering Code Definitions



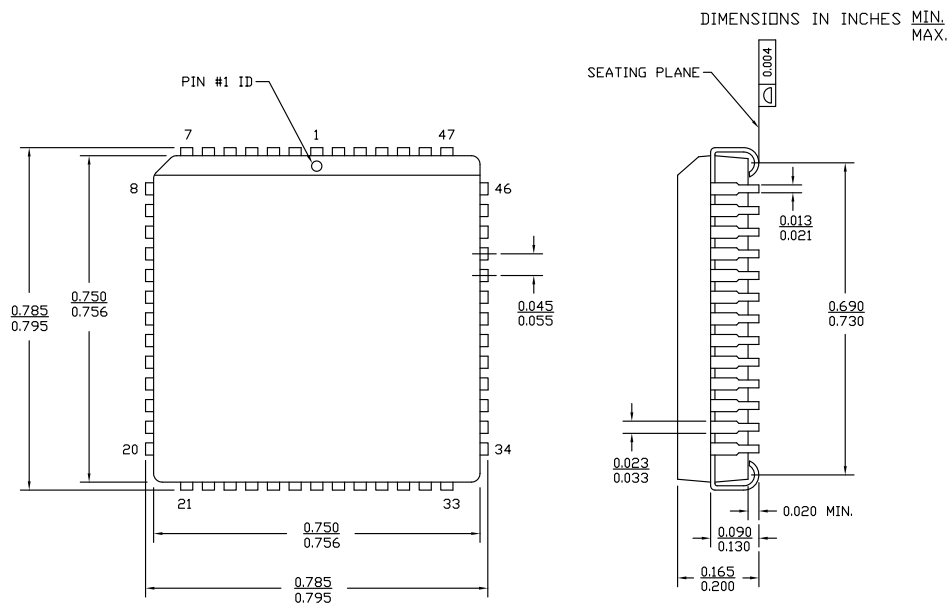
**Package Diagrams**

**Figure 14. 48-pin (600 Mil) Sidebrazed DIP D26**



51-80044 \*B

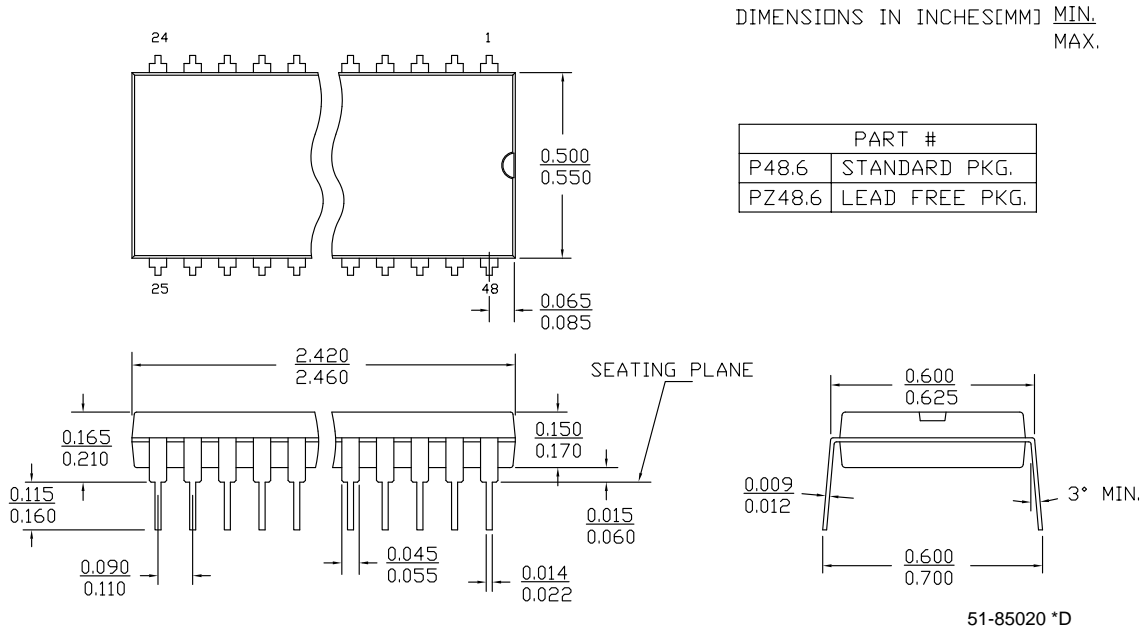
**Figure 15. 52-pin Pb-free Plastic Leaded Chip Carrier J69**



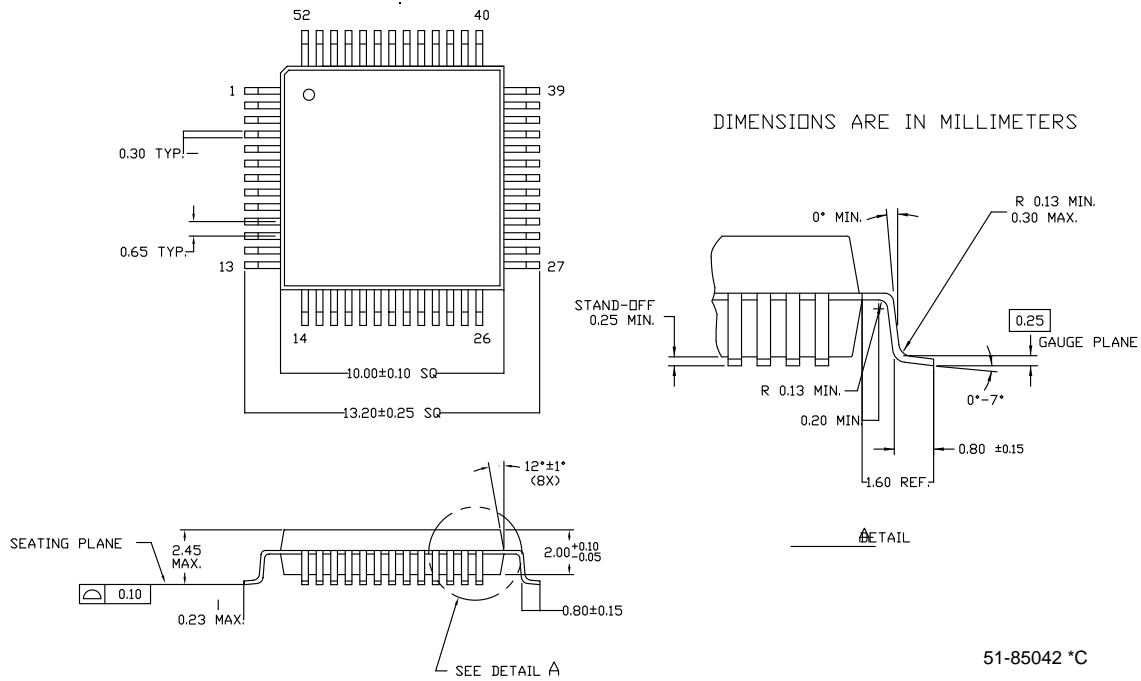
51-85004 \*C

**Package Diagrams** (continued)

**Figure 16. 48-pin (600 Mil) Molded DIP P25**



**Figure 17. 52-pin Pb-free Plastic Quad Flatpack N52**



## Acronyms

Acronym	Description
CE	chip enable
CMOS	complementary metal oxide semiconductor
DIP	dual in-line package
I/O	input/output
OE	output enable
PLCC	plastic leaded chip carrier
PQFP	plastic quad flat pack
SRAM	static random access memory
TQFP	thin quad flat pack
TTL	Transistor–transistor logic

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celcius
MHz	megahertz
μA	microamperes
mA	milliamperes
ms	milliseconds
mV	millivolts
ns	nanoseconds
pF	picofarad
V	volts
W	watts

## Document History Page

Document Title: CY7C130/CY7C130A/CY7C131/CY7C131A 1K x 8 Dual-Port Static RAM				
Document Number: 38-06002				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110169	SZV	09/29/01	Change from Spec number: 38-00027 to 38-06002
*A	122255	RBI	12/26/02	Power up requirements added to Maximum Ratings Information
*B	236751	YDT	See ECN	Removed cross information from features section
*C	325936	RUJ	See ECN	Added pin definitions table, 52-pin PQFP package diagram and Pb-free information
*D	393153	YIM	See ECN	Added CY7C131-15JI to ordering information Added Pb-Free parts to ordering information: CY7C131-15JXI
*E	2623540	VKN/PYRS	12/17/08	Added CY7C130A and CY7C131A parts Removed military information Updated ordering information table
*F	2897217	RAME	03/22/2010	Updated Ordering Information Updated Package Diagrams
*G	3054633	ADMU	10/11/2010	Updated <a href="#">Ordering Information</a> and added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Minor edits and updated in new template.
*H	3402163	ADMU	10/12/2011	Removed pruned part CY7C131-25NC from <a href="#">Ordering Information</a> Updated <a href="#">Package Diagrams</a> .

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