



**THE DATASHEET OF  
CY7C1021DV33-10ZSXI**



## Features

- Temperature ranges
  - Industrial: -40 °C to 85 °C
  - Automotive-A: -40 °C to 85 °C
- Pin-and function-compatible with CY7C1021CV33
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 60 \text{ mA @ } 10 \text{ ns}$
- Low CMOS standby power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide molded SOJ, 44-pin TSOP II and 48-ball VFBGA packages

## Functional Description

The CY7C1021DV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

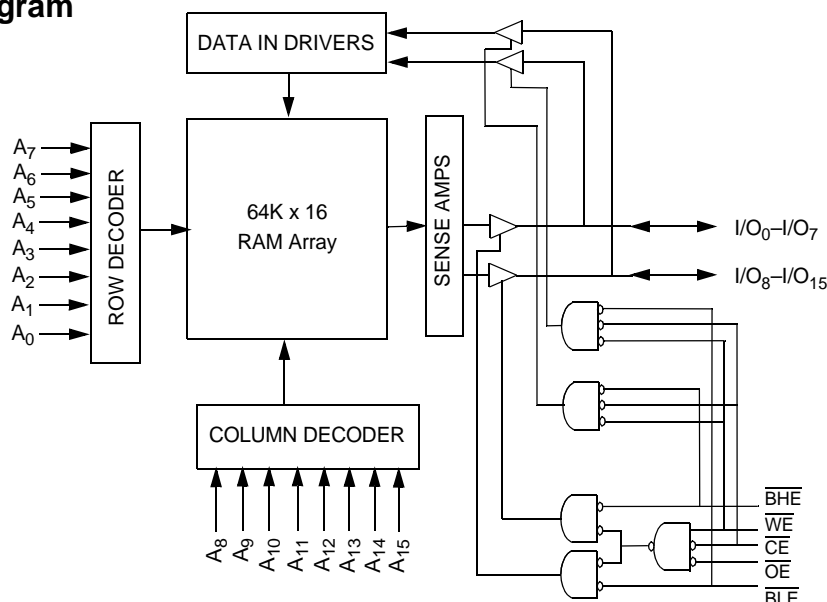
Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a Write operation ( $\overline{CE}$  LOW, and WE LOW).

The CY7C1021DV33 is available in Pb-free 44-pin 400-Mil wide Molded SOJ, 44-pin TSOP II and 48-ball VFBGA packages.

For a complete list of related resources, [click here](#).

## Logic Block Diagram



## Contents

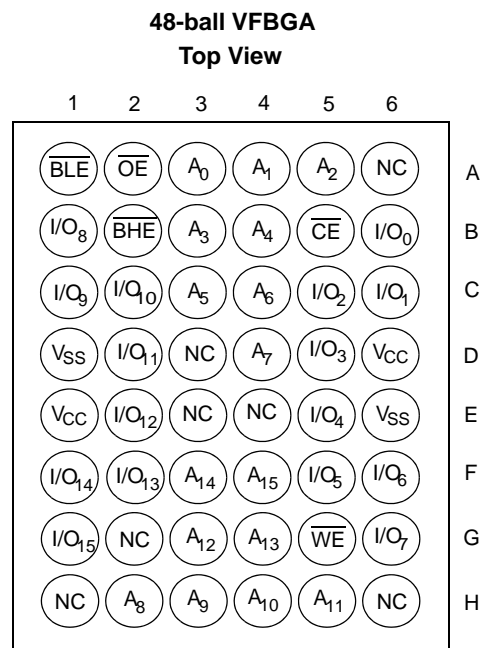
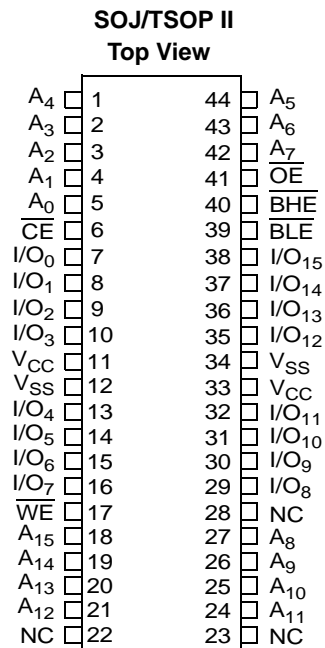
<b>Selection Guide</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>12</b>
<b>Pin Configurations</b> .....	<b>3</b>	Ordering Code Definitions .....	12
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagrams</b> .....	<b>13</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>15</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>15</b>
DC Electrical Characteristics .....	4	Units of Measure .....	15
<b>Capacitance</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>16</b>
<b>Thermal Resistance</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>18</b>
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	Worldwide Sales and Design Support .....	18
<b>Data Retention Characteristics</b> .....	<b>6</b>	Products .....	18
<b>Data Retention Waveform</b> .....	<b>6</b>	PSoC® Solutions .....	18
<b>Switching Characteristics</b> .....	<b>7</b>	Cypress Developer Community .....	18
<b>Switching Waveforms</b> .....	<b>8</b>	Technical Support .....	18
<b>Truth Table</b> .....	<b>11</b>		

### Selection Guide

Description	-10 (Industrial / Automotive-A)	Unit
Maximum access time	10	ns
Maximum operating current	60	mA
Maximum CMOS standby current	3	mA

### Pin Configurations

SOJ, TSOP II and VFBGA pinouts are as follows. [1]



**Note**

1. NC pins are not connected on the die.

**Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

- Storage temperature ..... -65 °C to +150 °C
- Ambient temperature with power applied ..... -55 °C to +125 °C
- Supply voltage on V<sub>CC</sub> to Relative GND [2] ..... -0.3 V to +4.6 V
- DC Voltage applied to outputs in high Z State [2] ..... -0.3 V to V<sub>CC</sub> + 0.3 V
- DC input voltage [2] ..... -0.3 V to V<sub>CC</sub> + 0.3 V

- Current into outputs (LOW) ..... 20 mA
- Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V
- Latch-up current ..... > 200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>	Speed
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V	10 ns
Automotive-A	-40 °C to +85 °C		10 ns

**Electrical Characteristics**

Over the Operating Range

**DC Electrical Characteristics**

Over the Operating Range

Parameter	Description	Test Conditions	-10 (Industrial / Automotive-A)		Unit	
			Min	Max		
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	V	
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA	-	0.4	V	
V <sub>IH</sub>	Input HIGH voltage		2.0	V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW voltage [2]		-0.3	0.8	V	
I <sub>Ix</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA	
I <sub>Oz</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	100 MHz	-	60	mA
			83 MHz	-	55	mA
			66 MHz	-	45	mA
			40 MHz	-	30	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current – TTL Inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	10	mA	
I <sub>SB2</sub>	Automatic CE Power-Down Current – CMOS Inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3 V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0	-	3	mA	

**Note**

2. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 1 V for pulse durations of less than 5 ns.

### Capacitance

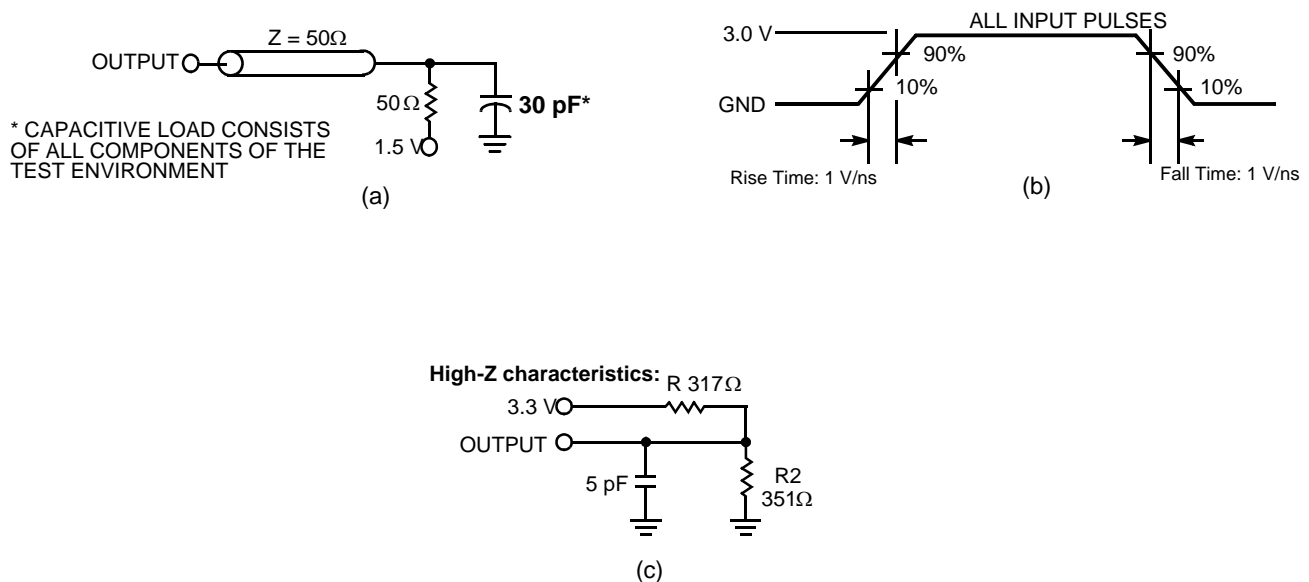
Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	8	pF
C <sub>OUT</sub>	Output capacitance		8	pF

### Thermal Resistance

Parameter <sup>[3]</sup>	Description	Test Conditions	SOJ	TSOP II	VFBGA	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	59.52	53.91	36	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		36.75	21.24	9	°C/W

### AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms <sup>[4]</sup>



**Notes**

- 3. Tested initially and after any design or process changes that may affect these parameters.
- 4. AC characteristics (except High Z) are tested using the load conditions shown in Figure 1 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 1 (c).

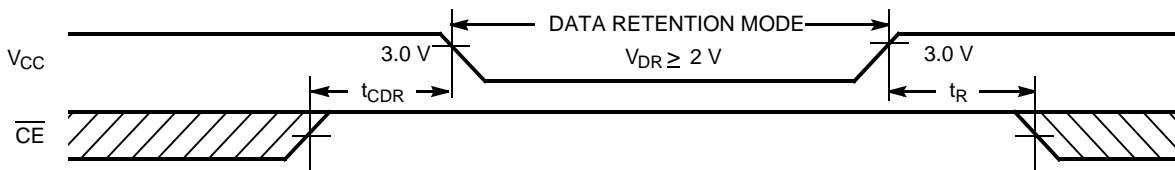
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	3	mA
$t_{CDR}^{[5]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[6]}$	Operation recovery time		$t_{RC}$	–	ns

## Data Retention Waveform

Figure 2. Data Retention Waveform



### Notes

5. Tested initially and after any design or process changes that may affect these parameters.
6. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\ \mu\text{s}$ .

## Switching Characteristics

Over the Operating Range

Parameter <sup>[7]</sup>	Description	-10 (Industrial / Automotive-A)		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}^{[8]}$	$V_{CC}$ (typical) to the first access	100	–	$\mu$ s
$t_{RC}$	Read cycle time	10	–	ns
$t_{AA}$	Address to data valid	–	10	ns
$t_{OHA}$	Data hold from address change	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	10	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[9]</sup>	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[9, 10]</sup>	–	5	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[9]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[9, 10]</sup>	–	5	ns
$t_{PU}^{[11]}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}^{[11]}$	$\overline{CE}$ HIGH to power-down	–	10	ns
$t_{DBE}$	Byte Enable to data valid	–	5	ns
$t_{LZBE}$	Byte Enable to low Z	0	–	ns
$t_{HZBE}$	Byte Disable to high Z	–	6	ns
<b>Write Cycle <sup>[12, 13]</sup></b>				
$t_{WC}$	Write cycle time	10	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	8	–	ns
$t_{AW}$	Address set-up to write end	8	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address set-up to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	ns
$t_{SD}$	Data set-up to write end	5	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[9]</sup>	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[9, 10]</sup>	–	5	ns
$t_{BW}$	Byte enable to end of write	7	–	ns

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in (c) of [Figure 1 on page 5](#). Transition is measured when the outputs enter a high impedance state.
- This parameter is guaranteed by design and is not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a Write and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

### Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [14, 15]

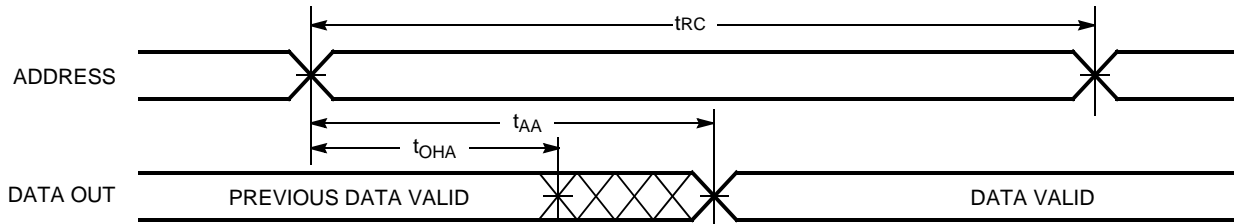
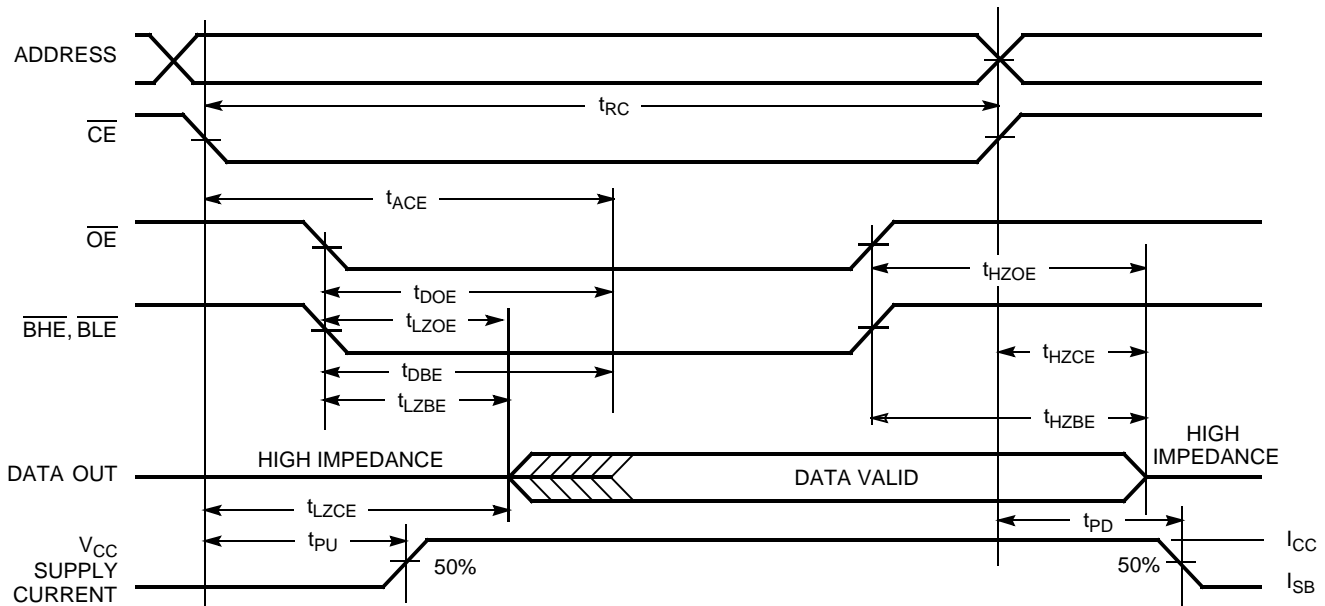


Figure 4. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [15, 16]



**Notes**

- 14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
- 15.  $\overline{WE}$  is HIGH for Read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [17, 18]

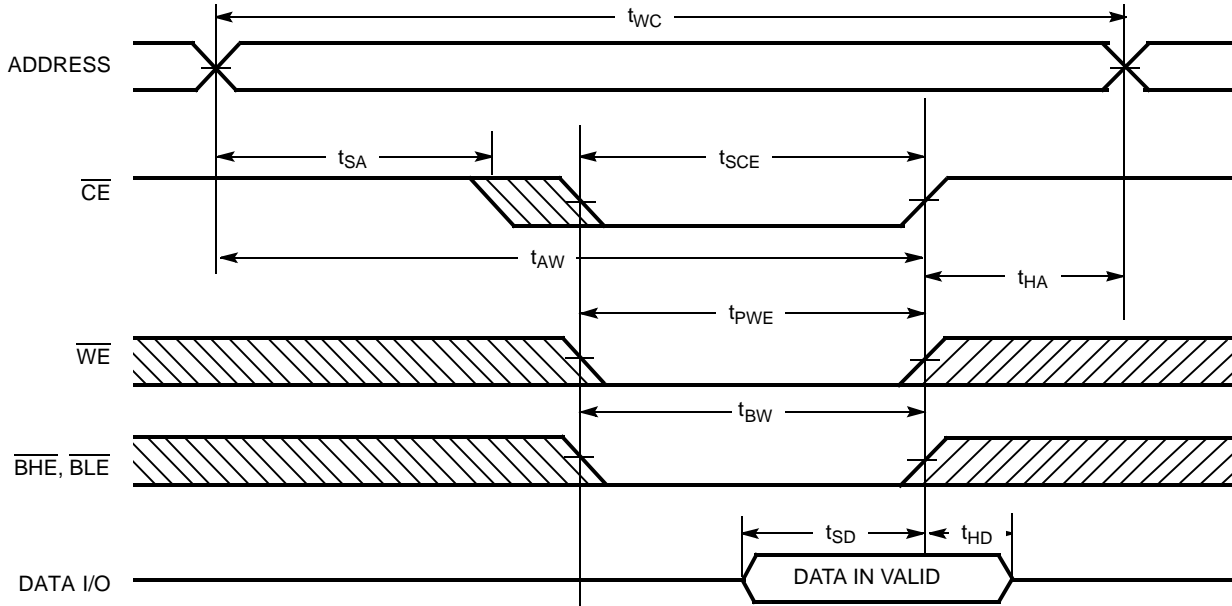
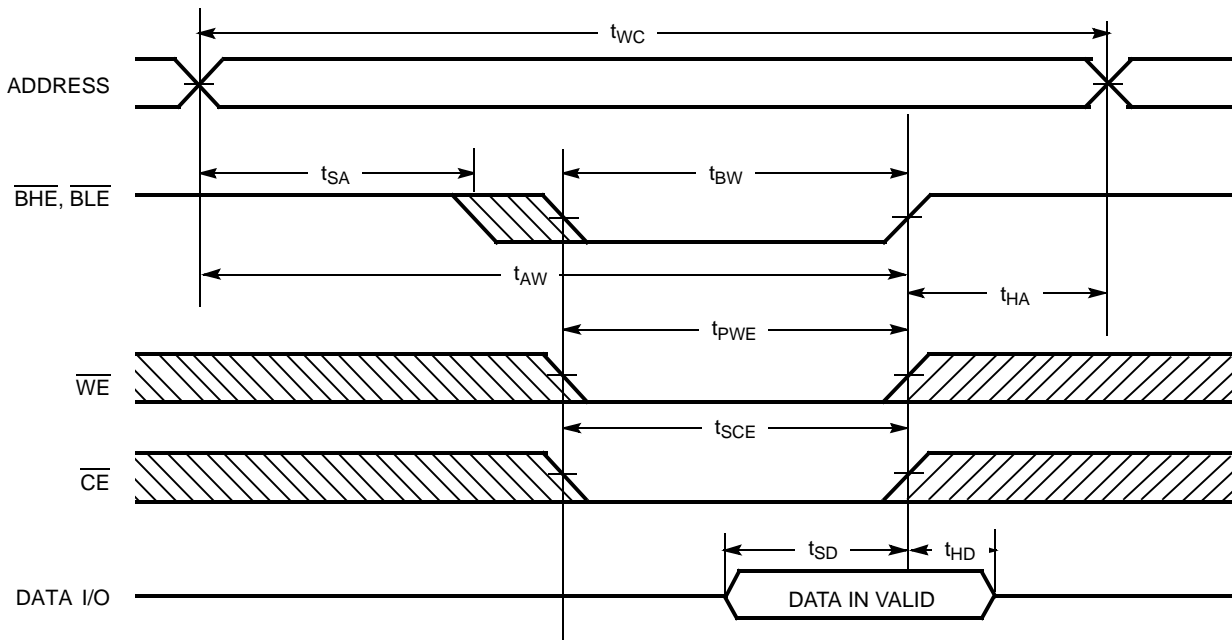


Figure 6. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)

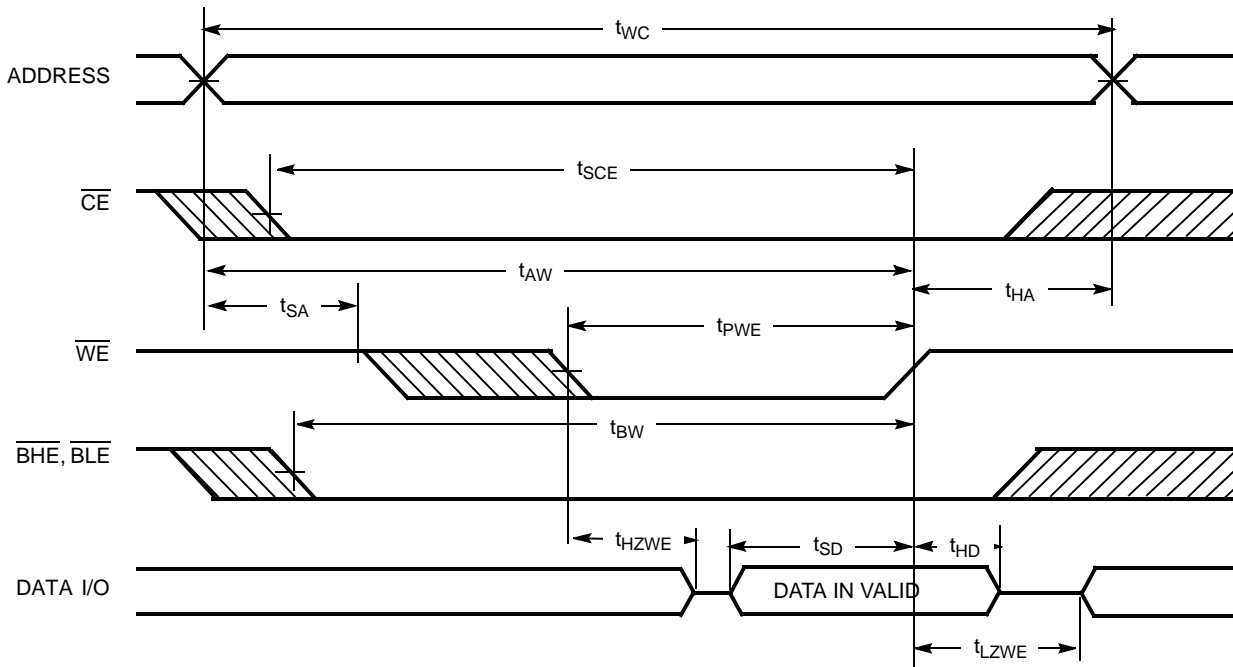


Notes

- 17. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 18. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[19]</sup>



Note

19. The minimum write pulse width should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

**Truth Table**

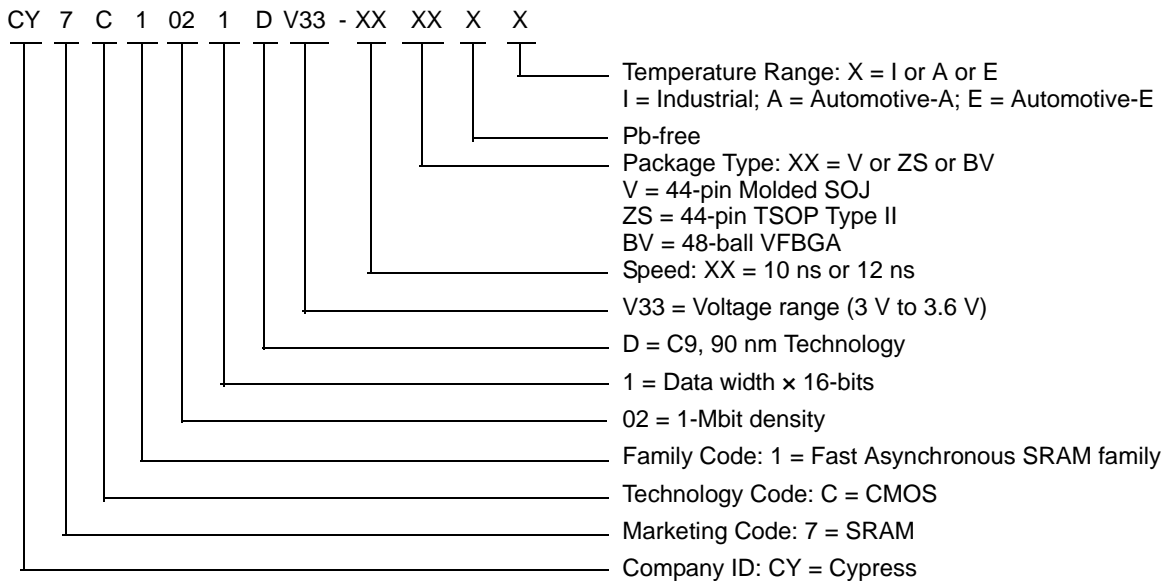
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I <sub>CC</sub> )
			L	H	Data Out	High-Z	Read – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High-Z	Data Out	Read – Upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I <sub>CC</sub> )
			L	H	Data In	High-Z	Write – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High-Z	Data In	Write – Upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1021DV33-10VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1021DV33-10ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021DV33-10BVXI	51-85150	48-ball VFBGA (Pb-free)	
10	CY7C1021DV33-10ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A

Please contact your local Cypress sales representative for availability of these parts.

**Ordering Code Definitions**



Package Diagrams

Figure 8. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082

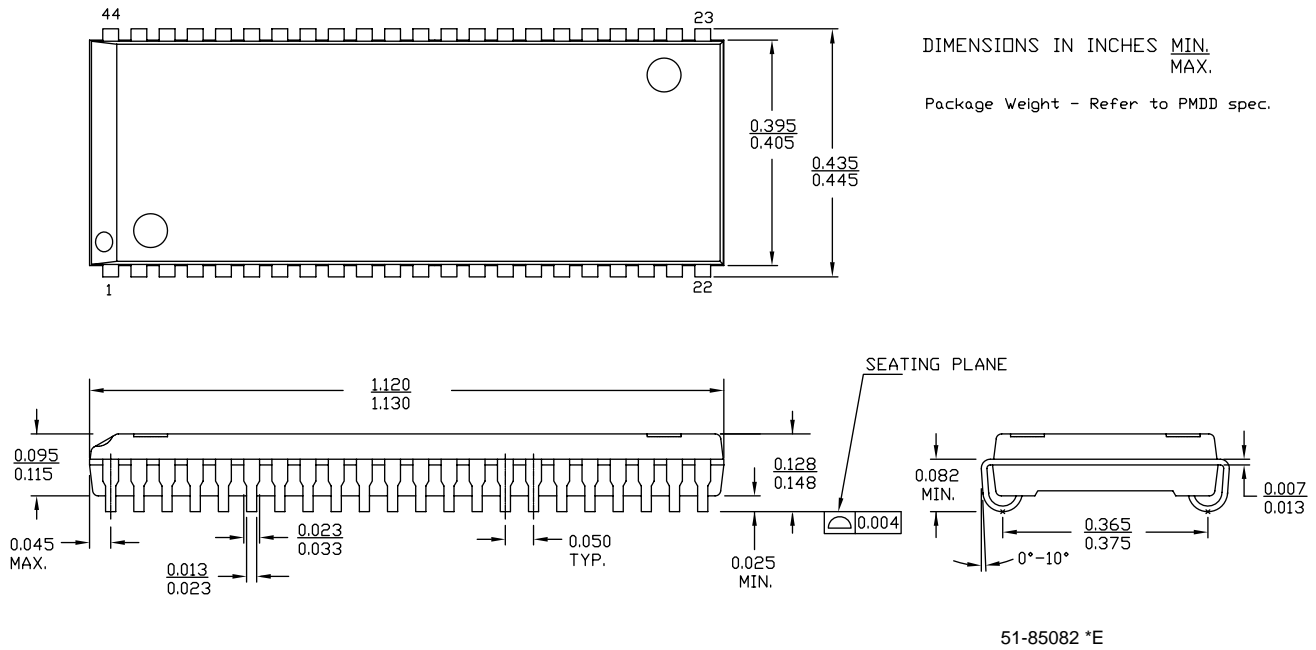
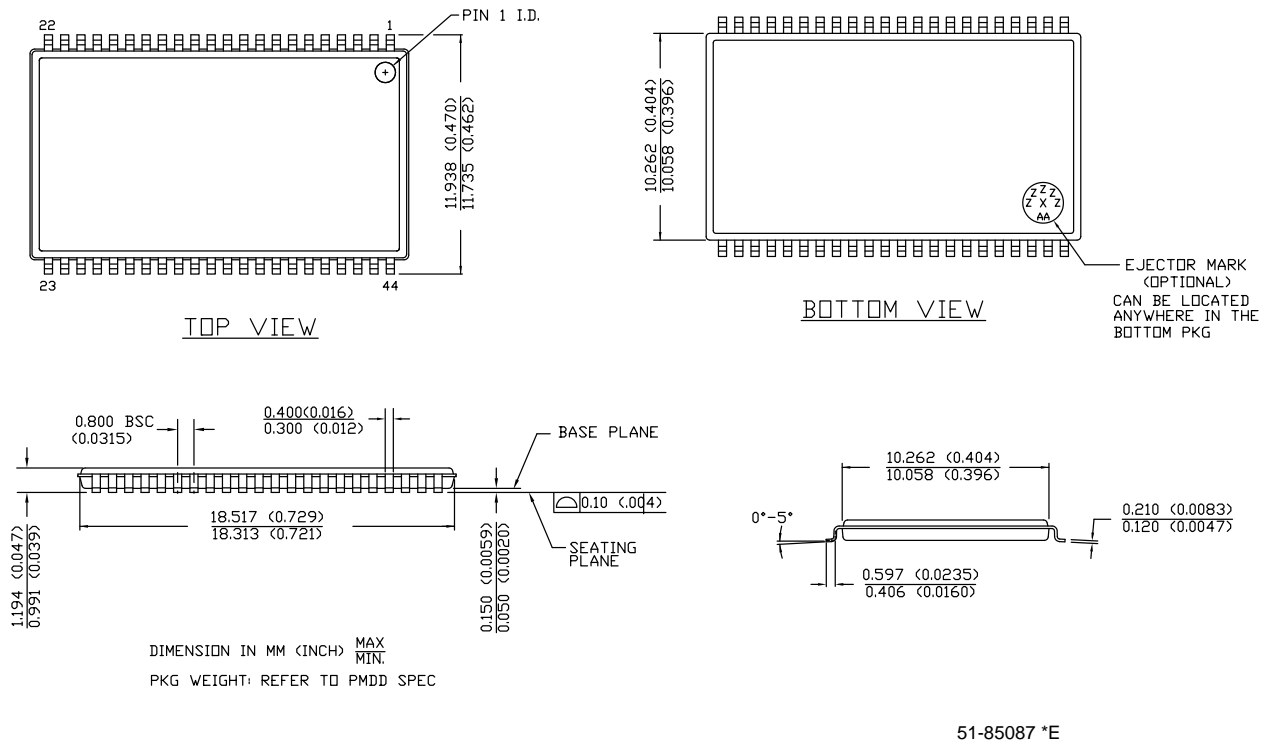
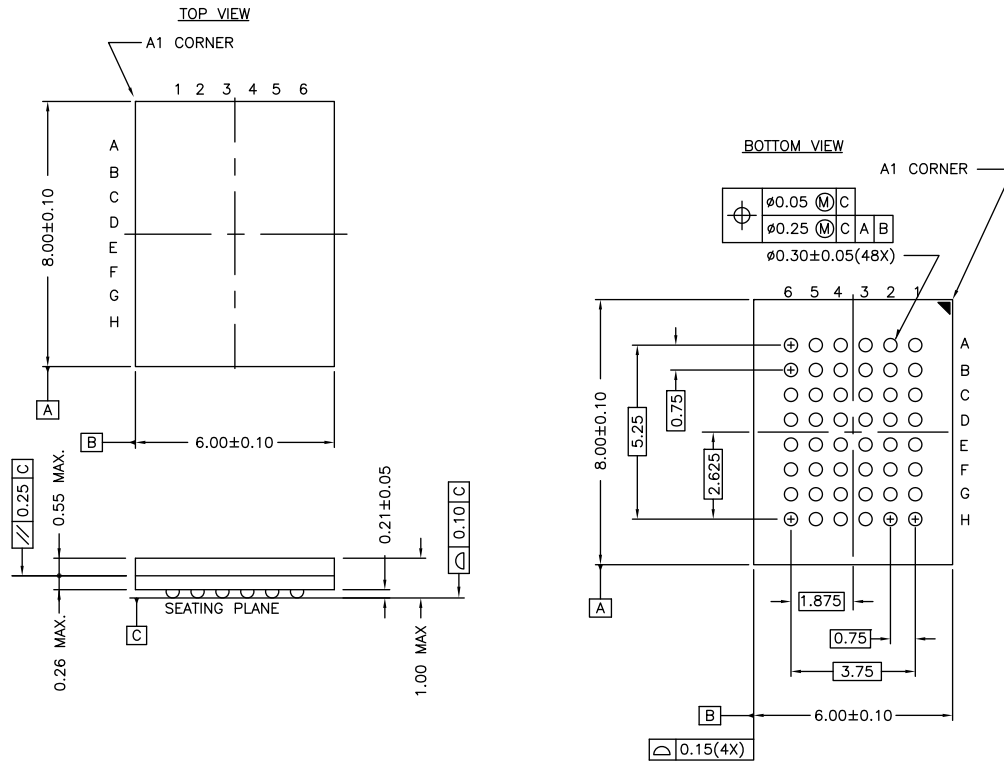


Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



Package Diagrams (continued)

Figure 10. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:  
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOJ	Small-Outline J-leaded
SRAM	Static Random Access Memory
TSOP	Thin Small-Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1021DV33, 1-Mbit (64 K × 16) Static RAM Document Number: 38-05460				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP.
*A	233693	See ECN	RKF	Updated <a href="#">Electrical Characteristics</a> (modified as per Eros (Spec # 01-02165)). Updated <a href="#">Ordering Information</a> (included Pb-free offering).
*B	263769	See ECN	RKF	Updated <a href="#">Functional Description</a> (Changed I/O <sub>1</sub> –I/O <sub>16</sub> to I/O <sub>0</sub> –I/O <sub>15</sub> ). Updated <a href="#">Pin Configurations</a> (Changed I/O <sub>1</sub> –I/O <sub>16</sub> to I/O <sub>0</sub> –I/O <sub>15</sub> ). Added <a href="#">Data Retention Characteristics</a> and <a href="#">Data Retention Waveform</a> . Updated <a href="#">Switching Characteristics</a> (Added T <sub>power</sub> parameter and its details). Updated <a href="#">Ordering Information</a> (Added shade, no change in part numbers).
*C	307601	See ECN	RKF	Updated <a href="#">Selection Guide</a> (Reduced Speed bins to -8 and -10 ns (Removed -12 and -15 speed bins related information)). Updated <a href="#">Electrical Characteristics</a> (Reduced Speed bins to -8 and -10 ns (Removed -12 and -15 speed bins related information)). Updated <a href="#">Switching Characteristics</a> (Reduced Speed bins to -8 and -10 ns (Removed -12 and -15 speed bins related information)). Updated <a href="#">Ordering Information</a> (Updated part numbers).
*D	520652	See ECN	VKN	Changed status from Preliminary to Final. Updated <a href="#">Features</a> (Removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information). Updated <a href="#">Selection Guide</a> (Removed -8 speed bin related information and included -12 speed bin related information). Updated <a href="#">Operating Range</a> (Removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information). Updated <a href="#">Electrical Characteristics</a> (Updated <a href="#">DC Electrical Characteristics</a> (Removed -8 speed bin related information and included -12 speed bin related information, removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information), Updated Note 2 (Changed V <sub>IH(max)</sub> from V <sub>CC</sub> + 2 V to V <sub>CC</sub> + 1 V), added I <sub>CC</sub> parameter values for the frequencies 83 MHz, 66 MHz and 40 MHz). Updated <a href="#">Thermal Resistance</a> (Replaced TBD with values for all packages). Updated <a href="#">Switching Characteristics</a> (Removed -8 speed bin related information and included -12 speed bin related information, removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information). Updated <a href="#">Data Retention Characteristics</a> (Removed Commercial Operating range related information and included Automotive-A, Automotive-E Operating range related information). Updated <a href="#">Ordering Information</a> (Updated part numbers).
*E	2898399	03/24/2010	AJU	Updated <a href="#">Package Diagrams</a> .
*F	3109897	12/14/2010	AJU	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> .

Document History Page (continued)

Document Title: CY7C1021DV33, 1-Mbit (64 K × 16) Static RAM				
Document Number: 38-05460				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*G	3421856	10/25/2011	TAVA	<p>Updated <a href="#">Features</a> (Removed Automotive-E Operating range related information).</p> <p>Updated <a href="#">Selection Guide</a> (Removed Automotive-E Operating range related information, removed -12 speed bin related information).</p> <p>Updated <a href="#">Operating Range</a> (Removed Automotive-E Operating range related information, removed -12 speed bin related information).</p> <p>Updated <a href="#">Electrical Characteristics</a> (Updated <a href="#">DC Electrical Characteristics</a> (Removed Automotive-E Operating range related information, removed -12 speed bin related information)).</p> <p>Updated <a href="#">Switching Characteristics</a> (Removed Automotive-E Operating range related information, removed -12 speed bin related information).</p> <p>Updated <a href="#">Data Retention Characteristics</a> (Removed Automotive-E Operating range related information).</p> <p>Updated <a href="#">Switching Waveforms</a>.</p> <p>Updated <a href="#">Ordering Information</a> (Updated part numbers).</p> <p>Updated <a href="#">Package Diagrams</a>.</p> <p>Updated to new template.</p>
*H	4578364	11/24/2014	MEMJ	<p>Updated <a href="#">Functional Description</a>:</p> <p>Added "For a complete list of related resources, <a href="#">click here</a>." at the end.</p> <p>Updated <a href="#">Switching Characteristics</a>:</p> <p>Added Note 13 and referred the same note in "Write Cycle".</p> <p>Updated <a href="#">Switching Waveforms</a>:</p> <p>Added Note 19 and referred the same note in <a href="#">Figure 7</a>.</p> <p>Updated <a href="#">Ordering Information</a> (Removed shade, no change in part numbers).</p> <p>Updated <a href="#">Package Diagrams</a>:</p> <p>spec 51-85082 – Changed revision from *D to *E.</p> <p>spec 51-85087 – Changed revision from *D to *E.</p> <p>spec 51-85150 – Changed revision from *G to *H.</p> <p>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a>.</p> <p>Updated to new template.</p> <p>Completing Sunset Review.</p>

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