THE DATASHEET OF

STV0684

STV0684

DIGITAL CAMERA PROCESSOR

PRODUCT PREVIEW

Features

- **Supports the UXGA (1600 x 1200 pixels) and SXGA (1280 x 1024 pixels) CMOS sensors from STMicroelectronics.**
- **High quality video processor**
  - RAM based firmware
  - Flexible defect pixel correction
  - NORA (Noise Reduction Algorithms)
  - Anti-vignetting algorithms
  - Advanced statistics processors
  - Two general purpose scalers
- **ST20 32-bit core**
  - Instruction, data cache and embedded memory for fast code execution
  - Embedded ROM bootloader for code storage in cost effective NAND flash memory
  - Code executed in SDRAM, no code-size limitation
- **On-chip 16-bit Sigma-Delta analog to digital converter for audio record**
- **Audio digital to analog converter for audio playback**
- **AVI (Audio Video Interleaved) clips directly recorded into the mass storage media**
  - Long clip length
  - Low power consumption
- **Flexible TFT - TFD digital interface with preview capability while recording**
  - Direct support for Casio, Epson and AU optronics display
  - Flexible digital interface designed to support future digital panels
- **PAL and NTSC encoder with on-chip digital to analog converter**
  - TV display of pictures and clips
- **Versatile mass storage interface**
  - support Compact-flash, Nand-on-board, Smartmedia, Secure Digital, Multi-media and Extreme Digital
- **USB 1.1 interface**
  - USB mass storage class compliant, Bulk only transfer protocol
  - USB audio and video class compliant
- **JPEG and MJPEG CODEC**

The STV0684 is a one-chip camera processor for SXGA and UXGA CMOS digital still cameras. ST supplies complete reference designs including the sensor and co-processor chipset, firmware and software drivers. The STV0684 uses a small BGA package (12 mm x 12 mm) ideal for the design of very small digital cameras. The STV0684 relies on ST unique and highly performing video processor algorithms including newly improved and patented algorithms (NORA, Anti-vignetting,...)

The sensor from the chipset relies on a high-performance process that uses pinned photodiode with improved low light performances, reducing the gap with CCD sensors.

Applications

- Digital still cameras
- Solid state video camera recorders
- Embedded cameras

Technical Specifications

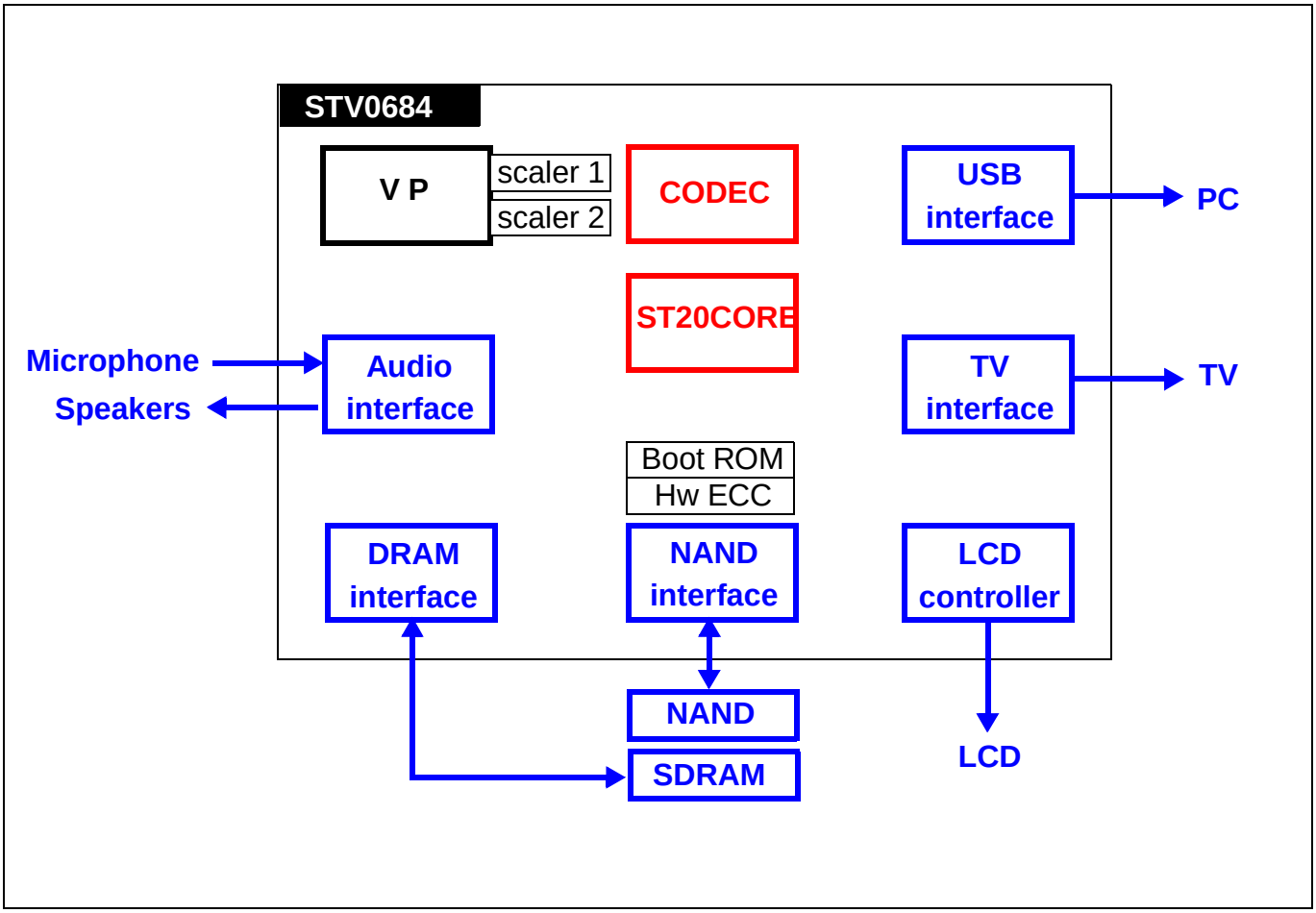
Resolution	UXGA - VV6700V001 SXGA - VV6601V001
Sample rate	up to 48 M sample/s (MSPS)
Power supply	3.3V and 1.8V
Power requirements	60 mA typical
Package	BGA196, 12x12 mm

Ordering Information

Sale type	Temperature	Package
STV0684	[0; +70] °C	BGA196

System Overview

Figure 1: STV0684 system overview



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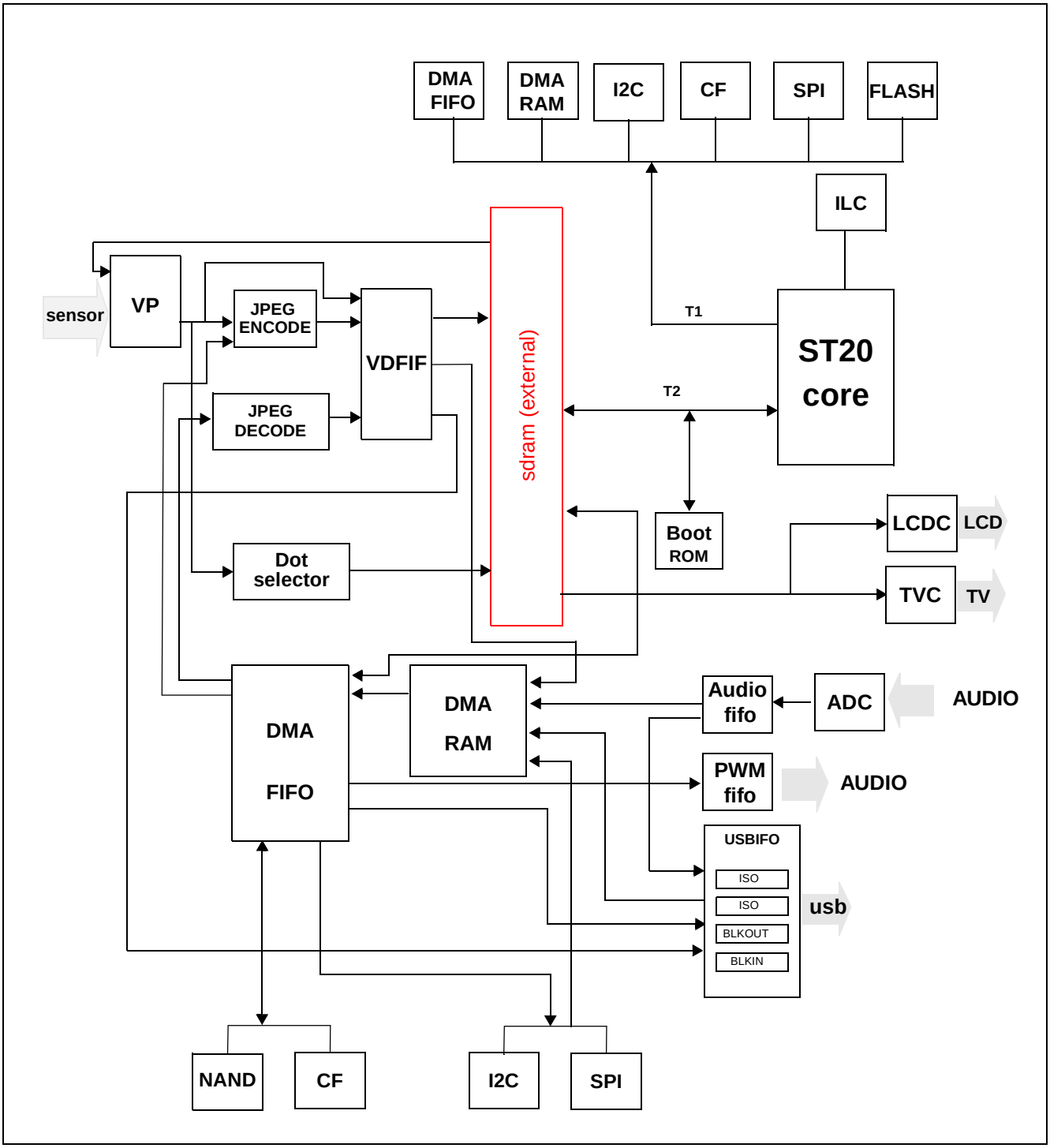
Document Revision History

Revision	Draft	Date	Comments
A		29.09.03	First draft
B			
C			

1 Functional Block Diagram

Figure 2: STV0684 functional block diagram



2 Signal Description

Table 1: STV0684 signal description[1] (196 pins)

Pin name	Location	Type	Description
BGA 196 TOTAL 196 PINS			
Power supplies: total 32 pins			
VDDI1	K11		VDD IO Supply 3.3V
VDDI2	G10		VDD IO Supply 3.3V
VDDI3	D9		VDD IO Supply 3.3V
VDDI4	E6		VDD IO Supply 3.3V
VDDI5	D2		VDD IO Supply 3.3V
VDDI6	J2		VDD IO Supply 3.3V
VDDI7	P2		VDD IO Supply 3.3V
VDDI8	N6		VDD IO Supply 3.3V
VDDI9	N8		VDD IO Supply 3.3V
VDDC1	H11		VDD CORE supply 1.8V
VDDC2	C8		VDD CORE supply 1.8V
VDDC3	D5		VDD CORE supply 1.8V
VDDC4	G1		VDD CORE supply 1.8V
VDDC5	N5		VDD CORE supply 1.8V
VDDC6	P10		VDD CORE supply 1.8V
VSS	J9		GROUND
VSS	G9		GROUND
VSS	F9		GROUND
VSS	E9		GROUND
VSS	G8		GROUND
VSS	G7		GROUND
VSS	E5		GROUND
VSS	E4		GROUND
VSS	H1		GROUND
VSS	H7		GROUND
VSS	M4		GROUND
VSS	J6		GROUND
VSS	J7		GROUND
VSS	H8		GROUND
VSS	K9		GROUND

Table 1: STV0684 signal description[1] (196 pins)

Pin name	Location	Type	Description
VDDP	C10		PLL core supply 3.3V
VSSP	D10		PLL core GND
Sensor interface: total 16 pins			
SDATA0	J8	I	Sensor interface Bit0 (Less Significant bit)
SDATA1	P9	I	Sensor interface Bit1
SDATA2	M9	I	Sensor interface Bit2
SDATA3	N9	I	Sensor interface Bit3
SDATA4	L9	I	Sensor interface Bit4
SDATA5	L10	I	Sensor interface Bit5
SDATA6	N10	I	Sensor interface Bit6
SDATA7	M10	I	Sensor interface Bit7
SDATA8	P11	I	Sensor interface Bit8
SDATA9	P12	I	Sensor interface Bit9 (Most Significant bit)
HSYNC	N11	I	Horizontal synchronization
VSYNC	L11	I	Vertical Synchronization
SENSOR CLOCK	N12	O	Clock supplied to the sensor
PIXEL CLOCK	M12	I	Clock supplied by the sensor
I2C SDA	M11		I2C Data line
I2C SCL	P13		I2C clock line
SDRAM interface: total 38 pins			
DQ0	K12		SDRAM
DQ1	N13		SDRAM
DQ2	K13		SDRAM
DQ3	P14		SDRAM
DQ4	K14		SDRAM
DQ5	N14		SDRAM
DQ6	J10		SDRAM
DQ7	M13		SDRAM
DQ8	M14		SDRAM
DQ9	J11		SDRAM
DQ10	L12		SDRAM
DQ11	J12		SDRAM
DQ12	L13		SDRAM
SQ13	J13		SDRAM
DQ14	K10		SDRAM

Table 1: STV0684 signal description[1] (196 pins)

Pin name	Location	Type	Description
DQ15	J14		SDRAM
DQML	L14		SDRAM
A0	H9		SDRAM
A1	H12		SDRAM
A2	H10		SDRAM
A3	H13		SDRAM
A4	H14		SDRAM
A5	G12		SDRAM
A6	G14		SDRAM
A7	G13		SDRAM
A8	G11		SDRAM
A9	F14		SDRAM
A10	F10		SDRAM
A11	F12		SDRAM
A12	F13		SDRAM
BA0	E14		SDRAM
BA1	F11		SDRAM
CLK	E13		SDRAM
CKE	E12		SDRAM
DQMH	E11		SDRAM
$\overline{RAS}$	D14		SDRAM
$\overline{CAS}$	D13		SDRAM
$\overline{WE}$	E10		SDRAM
Graphics LCD interface: total 18 pins			
TFT0 LP	P4		LCD interface
TFT1RES	M5		LCD interface
TFT2 XINH	L5		LCD interface
TFT3 XSCL	P5		LCD interface
TFT4 FRYP	K6		LCD interface
TFT5 FRYS	L6		LCD interface
TFT6 DY-PNL_CLK	M6		LCD interface
TFT7 YSCL-HSYNC	P6		LCD interface
TFT8 YSCLD-VSYNC	K7		LCD interface
TFT9 DOUT0	L7		LCD interface
TFT10 DOUT1	M7		LCD interface

Table 1: STV0684 signal description[1] (196 pins)

Pin name	Location	Type	Description
TFT11 DOUT2	N7		LCD interface
TFT12 DOUT3	P7		LCD interface
TFT13 DOUT4	K8		LCD interface
TFT14 DOUT5	M8		LCD interface
TFT15 FRX	P8		LCD interface
TFT16 GCP	L8		LCD interface
TFT18 BACKLIGHT	B6		LCD interface
TV interface: total 5 pins			
UOUT	D12		CVBS out
REXT	B14		TV Reference voltage
GNDA REXT	B13		TV Reference voltage
TV VDDA	C14		TV core supply 1.8V
TV VSSA	C13		TV core GND
SPI (used for MMC, SD and serial flash access): total 5 pins			
SPI MISO	A9		Master In Slave Out
SPI MOSI	B8		Master Out Slave In
SPI CLK	A8		SPI clock
SPI SS	D8		SPI slave/host selection
$\overline{\text{SPI CS}}$	E8		SPI Chip select
Audio interface: total 10 pins			
AUDIO CBS	C12		Audio Vbias
AUDIO ADC IN P	D11		Audio ADC Differential input
AUDIO ADC IN N	C11		Audio ADC differential input
AUDIO VC	B10		Audio PLL filter
AUDIO PWM OUT	A10		DAC: Pulse Width Modulator output
AUDIO $\overline{\text{ENABLE}}$	A5		ENABLE external audio amplifier
VDDA	A14		Audio analog power supply 3.3V
VSSA	B12		Audio analog ground
VDDAP	A12		Audio PLL supply 1.8V
VSSAP	A11		Audio PLL ground
NAND (Smartmedia) & Compact-flash interface (PC card Memory mode): total 29 pins			
IO0	E3		SMC D0 (PIN 6)- CF D00 (PIN 21)
IO1	F4		SMC D1 (PIN 7) - CF D01 (PIN 22)
IO2	F6		SMC D2 (PIN 8)- CF D02 (PIN 23)
IO3	F2		SMC D3 (PIN 9)- CF D03 (PIN2)

Table 1: STV0684 signal description[1] (196 pins)

Pin name	Location	Type	Description
IO4	F3		SMC D4 (PIN 13)- CF D04 (PIN 3)
IO5	F1		SMC D5 (PIN 14)- CF DO5 (PIN 4)
IO6	G4		SMC D6 (PIN 15)- CF DO6 (PIN 5)
IO7	G5		SMC D7 (PIN 16)- CF DO7 (PIN 6)
$\overline{WE}$	G6		SMC $\overline{WE}$ (PIN 4) - CF $\overline{WE}$ (PIN 36)
$\overline{NAND\ CS}$	G3		Nand Chip select
ALE $\overline{OE}$	H5		SMC ALE (PIN 3) - CF $\overline{OE}$ (PIN 9)
RST	H3		CF RESET (PIN 41)
CLE RDY	K3		SMC CLE (PIN 2) - CF READY(PIN 37)
RB $\overline{WAIT}$	J5		SMC R/-B (PIN 19) - CF $\overline{WAIT}$ (PIN 42)
$\overline{RE}$ $\overline{REG}$	K4		SMC $\overline{RE}$ (PIN 20) - CF $\overline{REG}$ (PIN 44)
$\overline{CS}$ $\overline{CARD\ EN}$	L1		SMC $\overline{CS}$ (PIN 21) - CF $\overline{CE1}$ (PIN 7)
WRIT_PROT $\overline{CARD\ DET1}$	L2		SMC $\overline{WP}$ (PIN 5) - CF WP (PIN 24)
CARD_DET $\overline{CARD\ DET1}$	L3		SMC CD (PIN 11) - CF CD1 (PIN 26)
CFA0	M1		SFP - CF A00 (PIN 20)
CFA1	M2		SFP - CF A01 (PIN 19)
CFA2	N1		SFP - CF A02 (PIN 18)
CFA3	P1		SFP - CF A03 (PIN 17)
CFA4	M3		SFP - CF AO4 (PIN 16)
CFA5	N2		SFP - CF A05 (PIN 15)
CFA6	N3		SFP - CF A06 (PIN 14)
CFA7	P3		SFP - CF A07 (PIN 12)
CFA8	L4		SFP - CF A08 (PIN 11)
CFA9	N4		SFP - CF AO9 (PIN 10)
CFA10	K5		SFP - PIN A10 (PIN8)
User Interface - system pins (firmware dedicated SFP): total 15 pins			
$\overline{MODE\ UP}$	F8		See firmware manual (UI section)
$\overline{MODE\ DOWN}$	A7		See firmware manual
$\overline{SELECT}$	B7		See firmware manual
$\overline{CANCEL}$	D7		See firmware manual
$\overline{SHUTTER}$	A6		See firmware manual
$\overline{LED0}$	B5		See firmware manual
$\overline{LED1}$	A4		See firmware manual

Table 1: STV0684 signal description[1] (196 pins)

Pin name	Location	Type	Description
WAKE UP	E1		See firmware manual
FLASH ENABLE	C7		See firmware manual
FLASH TRIGGER	B4		See firmware manual
POWER OFF	E7		See firmware manual
POWER DOWN	C6		See firmware manual
VP CNTL0	C5		Mechanical shutter interface
VP CNTL1	D4		Mechanical shutter interface
VP CNTL2	A3		Mechanical shutter interface
SUSPEND	D6		Sensor suspend pin
General Purpose Input/Output: total 8 pins			
GPIO0	B2		General purpose IO, to be allocated by firmware
GPIO1	A1		General purpose IO, to be allocated by firmware
GPIO2	C2		General purpose IO, to be allocated by firmware
GPIO3	B1		General purpose IO, to be allocated by firmware
GPIO4	D3		General purpose IO, to be allocated by firmware
GPIO5	C1		General purpose IO, to be allocated by firmware
GPIO6	D1		General purpose IO, to be allocated by firmware
GPIO7	F5		General purpose IO, to be allocated by firmware
USB interface: total 5 pins			
USB DP	H2		USB DATAP
USB DN	G2		USB DATAN
USB DETECT	H4		High when USB VCC present
USB TX_EN	F7		For debug
Battery level detector: total 2 pins			
LOW BATT	A13		Sense the battery level
BATT VREF	B11		Reference for the battery voltage
CLOCK, Reset signals: total 3 pins			
Xtal in	C9		27 Mhz Crystal input
Xtal out	B9		27 MHz Crystal Output
Reset	E2		ST20 RESET
JTAG, debug and test interface: total 10 pins			
VP TDI	C4		JTAG TDI EWARP
VP TDO	B3		JTAG TDO EWARP
VP TMS	C3		JTAG TMS EWARP
VP TCK	A2		JTAG TCK EWARP

Table 1: STV0684 signal description[1] (196 pins)

Pin name	Location	Type	Description
ST20 TRIGIN	J3		ST20 microconnect debug interface
ST20 TRIGOUT	J1		ST20 microconnect debug interface
ST20 TDI	J4		ST20 microconnect debug interface
ST20 TDO	H6		ST20 microconnect debug interface
ST20 TMS	K1		ST20 microconnect debug interface
ST20 TCK	K2		ST20 microconnect debug interface
ST20 TRST	H3		ST20 microconnect debug interface

1. As this is preliminary information on a device still undergoing development, the pinout might change.

3 Functional Description

3.1 Video processor (VP)

The video porcessor (VP) results from STMicroelectronics extensive knowledge and experience around the colour science for CMOS sensor. The block fulfills a set of functions related to colour reconstruction from a bayer filter, colour matrixing and sharpening, real-time and programmable defect pixel correction, AGC, AWB, anti flicker and gamma correction, scaling from the sensor matrix size to the required video size (either VGA or QVGA) and to any LCD matrix size. This new video processor benefits from STMicroelectronics latest algorithm developments such as the patented Noise Reduction Algorithm and anti-vignetting to perform the highest quality standard.

The VP combines hardware and firmware. The main block controller is powered by the E WARP (8051) microcontroller with RAM based firmware for the highest level of flexibility.

3.1.1 Feature list

System features

- RAM based firmware
- Dual video interface for ViewFinder and movie capture
- Bayer or YCbCr input from supported memory
- 48 Mpixel/s capable processing pipe
- Flashgun and shutter support
- Bayer/RGB/YUV 4:2:2 output formats

Image reconstruction functions

- x2, x2.5 horizontal downscaling
- Colour channel gains and offsets
- Anti-vignetting
- Defect correction
- NoRA - Active Noise Reduction
- Demosaic (bayer->rgb conv) and YUV matrix (rgb -> YUV)
- Image crop
- General purpose RGB downscaler
- RGB matrix
- Peaking
- Gamma correction

Statistics processor

- 4 programmable accumulators (real time programming)
- Programmable zones

Image control functions (tasks handled by the EWARP processor)

- Sensor detection, initialisation and configuration
- VP mode management: stills, streaming, etc.
- Automatic exposure control, automatic white balance
- Flicker correction

- Dampening/promotion tasks
- Scaler management
- Dark calibration
- Flashgun control
- Shutter control

3.2 ST20-C103 core

The ST20 is the core of the STV0684 system-on-chip. The processor executes its code either from the 64 kbyte of private SRAM or directly from the external SDRAM. Instruction/data cache ensure a fast code execution.

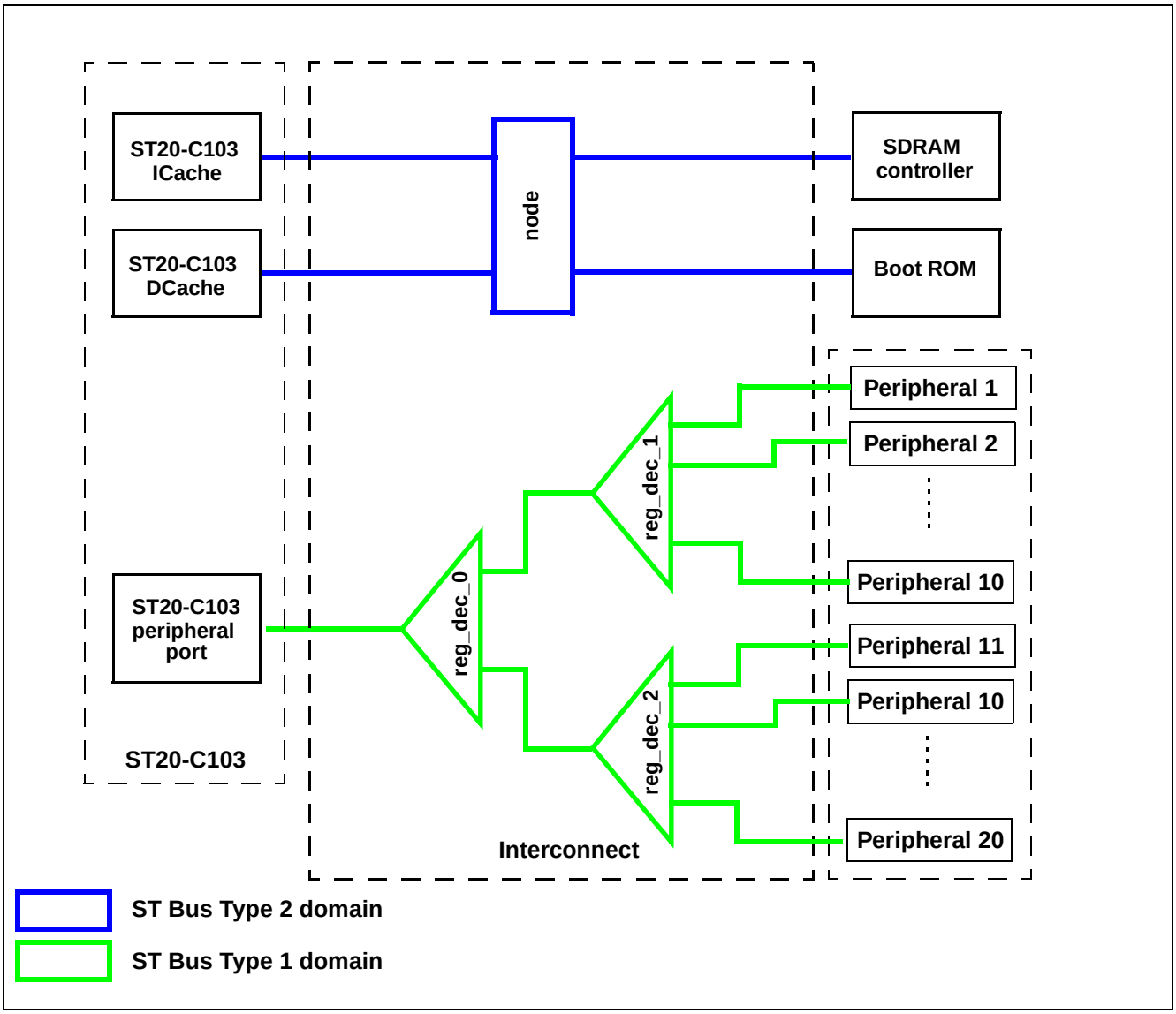
A boot loader or ROM provides the capability to boot the system by copying the application firmware image from the Non Volatile Memory (SPI flash or standard NAND flash) to the program SRAM or SDRAM memory. This mechanism ensures the lowest system cost by storing the application firmware on a low-cost mass storage memory and thus avoiding the extra cost of a NOR type memory. The boot loader also provides the useful possibility to upgrade the application firmware and therefore program cameras on the factory line.

The ST20-C103 core includes the following:

- ST20C1 processor running at 48 MHz frequency
- Diagnostic control unit DCU3 (4 compare, 4 capture, trace) for debug and code development
- PWM4 timer
- INTC2 interrupt controller (16 inputs)
- 64 K local RAM (SRAM)
- 4 K D-cache & 4 K I-cache instruction and data caches memory arbiter

3.2.1 Core architecture and block diagram

Figure 3: ST20DC3 architecture and block diagram



3.2.2 Memory map

Table 2 shows the STV0684 memory map organization.

Table 2: STV0684 memory map organization

DMA_RAM	FFFF_FFFF
	FFFF_F000
Video Processor	FFFF_EFFF
	F801_0000
Reserved	F800_FFFF
	F800_1400
ST20 External Peripheral Registers	F800_13FF
	F800_0000

Table 2: STV0684 memory map organization

ST20 Internal Peripheral Registers	F7FF_FFFF
	F000_0000
Reserved	EFFF_FFFF
	C000_4000
ROM	C000_3FFF
	C000_0000
SRAM	BFFF_FFFF
	8000_0000
Reserved	7FFF_FFFF
	5400_0000
SDRAM	53FF_FFFF
	5000_0000
Reserved	4FFF_FFFF
	4000_0100
SDRAM Registers	4000_00FF
	4000_0000

3.2.2.1 Configuration registers

Table 3: STV0684 configuration registers

Module Name	Periph_Base_Addr +
Compression engine	0000 - 01FF
DMA RAM (reg)	0200 - 02FF
Special Function Port	1200 - 13FF
USB I/F	0500 - 05FF
LCD	0600 - 06FF
Compact-flash control	0700 - 07FF
Audio Block	0800 - 08FF
NAND control	0900 - 09FF
Video FIFO	0A00 - 0AFF
Audio FIFO	0B00 - 0BFF
Power Management	0C00 - 0CFF
I2C	0D00 - 0DFF
SPI	0E00 - 0EFF
DMA FIFO	0F00 - 0FFF
TV encoder	1000 - 11FF
Video Processor	10000 - 1FFFF

Table 3: STV0684 configuration registers

TV FIFO	1400 - 14FF
ILC3	2000 - 2FFF
JPEG Decoder	1D00 - 1DFF
LCD Dot Select	1E00 - 1EFF

3.3 USB interface

The USB interface is used for the three following functions:

- PC download from the camera of all the various objects stored on the mass storage media. The STV0684 uses mass storage class, Bulk-only-transfer to ensure seamless connection with most of the current operating system from the market, including PC and Macintosh platforms.
- Stream concurrent audio and video through isochronous endpoints. The STV0684 uses established and newly developed standards to ensure the lowest burden of driver development. The STV0684 is compliant with both USB audio and video classes.
- Download the system program code necessary to run the application either in a serial flash or in a NAND flash soldered on the main camera PCB. This convenient function permits the programming of cameras on the manufacturing lines, it is not open to final users.

3.3.1 Features

- Compliant with USB protocol revision 1.1
- Support for full speed (12 Mbps) signalling bit rate
- Compliant with USB audio class
- Compliant with USB mass storage, Bulk-only transfer protocol
- Compliant with USB video class
- Simultaneously accessible endpoints:
  - Isochronous endpoint (IN) for video
  - Isochronous endpoint (IN) for audio
  - Bulk endpoint (IN) for download
  - Bulk endpoint (OUT) for download
  - Interrupt endpoint (IN) for shutter button with remote wake-up capability
  - Control pipe

3.4 Memory Interface

3.4.1 Description

The memory control block provides dedicated support for embedded SRAM, external SDRAM, NAND, Smartmedia and Compact Flash (via SFP pins).

Embedded SRAM

- Full-speed random read/write access from the ST20 to embedded SRAM
- Full-speed embedded SRAM address generation for real-time data writes from the compression engine, the video processor block, SPI, the audio block and USB module.
- Full-speed embedded SRAM address generation for data reads to the DMA out FIFO.

The source/destination module selection is managed by firmware.

External SDRAM

- ST20 memory mapped accesses to external SDRAM
- Full-speed embedded SDRAM address generation for real-time data writes from VDFIF
- Full-speed external SDRAM address generation/control to DMA out FIFO, TV FIFO, LCD FIFO or VP FIFO.

Mass storage media support

- Compact-flash support in memory mode
- Smartmedia card support
- NAND flash memory with a 512B+16 page organization, ECC done by hardware
- Support for multi-media card and secure digital with the SPI interface

3.5 Audio interface

The STV0684 is a single chip audio-video processor used for every single step of the processing chain to record, compress, record and playback audio.The STV0684 features a high quality 16-bit Sigma Delta analog to digital converter including automatic level control and noise gating, as well as volume control. It also features an ADPCM CODEC to maximize the length of video clips on a given mass storage media. Finally, the product features a digital to analog converter (PWM followed by RC filters) to directly address a speaker or buzzer for audio playback.

3.5.1 Description

The audio interface is used for the following functions:

- Audio record
- Audio playback
- Audio compression (ADPCM 4 to 1)

Audio record is performed through a 16 bit Sigma Delta interface while audio playback is done by a PWM that needs external RC filtering.

A simple audio compression ADPCM with a four to one compression ratio is used to maximize the length of audio-video clips.

3.5.1.1 Audio ADC description

The ADC block contains an analogue Sigma-Delta converter and associated digital filtering. The ADC block converts an analogue input to a 16-bit value which is then available for the ADPCM module. This ADC block contains two main blocks, the audio analogue front end and the ADC engine for digital filtering and control registers.

The purpose of the audio cell is to provide:

- 16 bits delta-sigma ADC
- Automatic level control and noise gate
- Volume control on ADC

3.5.1.2 Audio playback description

The pulse width modulator (PWM) block is split into four main blocks:

- Control registers
- FIFO
- Pulse width modulator
- Piezo buzzer control

The PWM module produces a pulse train with variable width according to the audio sample to be played. The rate at which individual pulses are produced is controlled by the sample rate control register. This module can playback audio at different rates within the range [8; 48] kHz. All values are generated from a counter clocked at 48MHz.

3.6 TV interface

The TV interface includes a digital encoder that supports both PAL and NTSC signaling and a video digital to analog converter (DAC). This interface supports both still and video display on a TV set.

3.6.1 Features

- Support PAL/NTSC analog TV standards
- Interlaced input data, YCrCb 4:2:2 format
- 16-bit x 16 words FIFO for buffering of incoming display data
- Interrupt generation
- PAL-NTSC CVBS encoder

3.7 LCD controller - Display interface

The STV0684 LCD controller has been specifically designed to include the following features:

- Support for low cost modules with direct interface without the need of an external timing controller IC.
- Flexibility with a high-level of programmability on all signals shapes, polarities and frequencies.

A dot selector converts 3 dot/pixel input RGB frame data into 1 dot/pixel RGB data. Thus, the display interface fully supports LCD panel dot selection modes like Delta, Delta Transverse, Delta Longitudinal and Mosaic as well as many other combinations presently available on the market.

Basic system functionality includes still picture review, ViewFinder mode as well as ViewFinder mode while recording a video clip.

3.7.1 Features

- Support Thin Film Transistor (TFT) color displays
- 64 or 256 grey level, 256 K (18 bit) or 16.7 Million (24 bit) color TFT support
- Support 6 bit or 8 bit display interfaces
- 16-deep, 16 bit deep FIFO for buffering of incoming display data
- Programmable resolution up to 1024 x 1024 pixels
- Programmable timing for different display panels
- Support CASIO, EPSON and AU Optronics panels
- Horizontal, vertical sync and pixel clock signals
- Support little-endian data formats
- Interrupt generation

3.8 JPEG CODEC

3.8.1 Description

The STV0684 features a compression and a decompression engine for both still pictures and video clips. This hardware CODEC ensures a fast system reaction time. The shutter to shutter timing is minimized. Images are rapidly displayed on the local display or the TV set.

3.8.1.1 Compression engine

The compression engine uses baseline sequential JPEG techniques of data compression. For example the ITU-656 digital video stream (at up to 12 Mpixel/s) is compressed down to a bandwidth that can be transmitted over the USB interface to the host, typically 500-900 Kbytes/s or to a mass storage media.

3.8.1.2 Decompression engine

The JPEG decoder block reads the compressed data from the DMA fifo, writes back decompressed data to DMA fifo. Data is organized in 8x8 blocks for respective color components.

3.9 Other Interfaces

3.9.1 SPI

The SPI interface is a generic serial interface with the following functions:

- Support for multi-media and secure digital cards
- Support for serial flash where the ST20-EWARP code can be located

The SPI supports:

- Full duplex, three-wire synchronous transfers
- Single master/slave operation selectable via firmware or hardware
- Programmable clock polarity
- End of transfer interrupt flag
- Write collision flag
- Busy flag indication

3.9.2 I2C

The STV0684 features a hardware I2C master interface and supports the following features:

- I2C protocol
- Standard I2C mode (100 kHz) / fast I^2C mode (400 kHz)
- Single master mode
- Transmitter/receiver performance
- 7/10 bit addressing
- DMA mode data transfer
- Clock stretching

3.9.3 Comparator for low battery detection

The comparator circuit compares the battery voltage with an external reference voltage and generates a low_batt signal for the CPU core.

4 Electrical Characteristics

4.1 Absolute maximum ratings

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DDC}	Supply voltage (core)	1.95	V
V_{DDI}	Supply voltage (IO)	3.6	V
V_{DDP}	Supply voltage (PLL)	3.6	V
V_{DDA}	Supply voltage (Audio)	3.6	V
V_{DDAP}	Supply voltage (Audio_PLL)	1.95	V
V_{TV_VDDA}	Supply voltage (TV)	1.95	V
I_{DD}	Supply current	TBC	mA
	Current on any signal pin	2	mA
T_{STO}	Storage temperature (10s)	-50 to 150	°C
T_{LEAD}	Lead temperature (soldering, 10 s)	TBC	°C

Caution:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Operating conditions

Table 5: Operating conditions

Symbol	Parameter	Value	Unit
V_{DDC}	Supply voltage (core)	1.8	V
V_{DDI}	Supply voltage (IO)	3.3	V
V_{DDP}	Supply voltage (PLL)	3.3	V
V_{DDA}	Supply voltage (Audio)	3.3	V
V_{DDAP}	Supply voltage (Audio_PLL)	1.8	V
V_{TV_VDDA}	Supply voltage (TV)	1.8	V
T_A	Ambient temperature	25	°C

4.3 Thermal data

Table 6: Thermal data

Symbol	Parameter	Value	Unit
Rth(j-a)	Junction-ambient thermal resistance - TFBGA56 (*Note 1*)	TBC	°C/W

Note: 1 Typical, measured with the component mounted on an evaluation PC board in free air.

5 STV0684 Package Details

5.1 STV0684 package mechanical data

Reference	Dimensions (mm)		
	Min.	Typ.	Max.
A	1.210		1.700
A1	0.270		
A2		1.120	
b	0.450	0.500	0.550
D	11.850	12.000	12.150
D1		10.400	
E	11.850	12.000	12.150
E1		10.400	
e	0.720	0.800	0.880
f	0.650	0.800	0.950
ddd			0.120

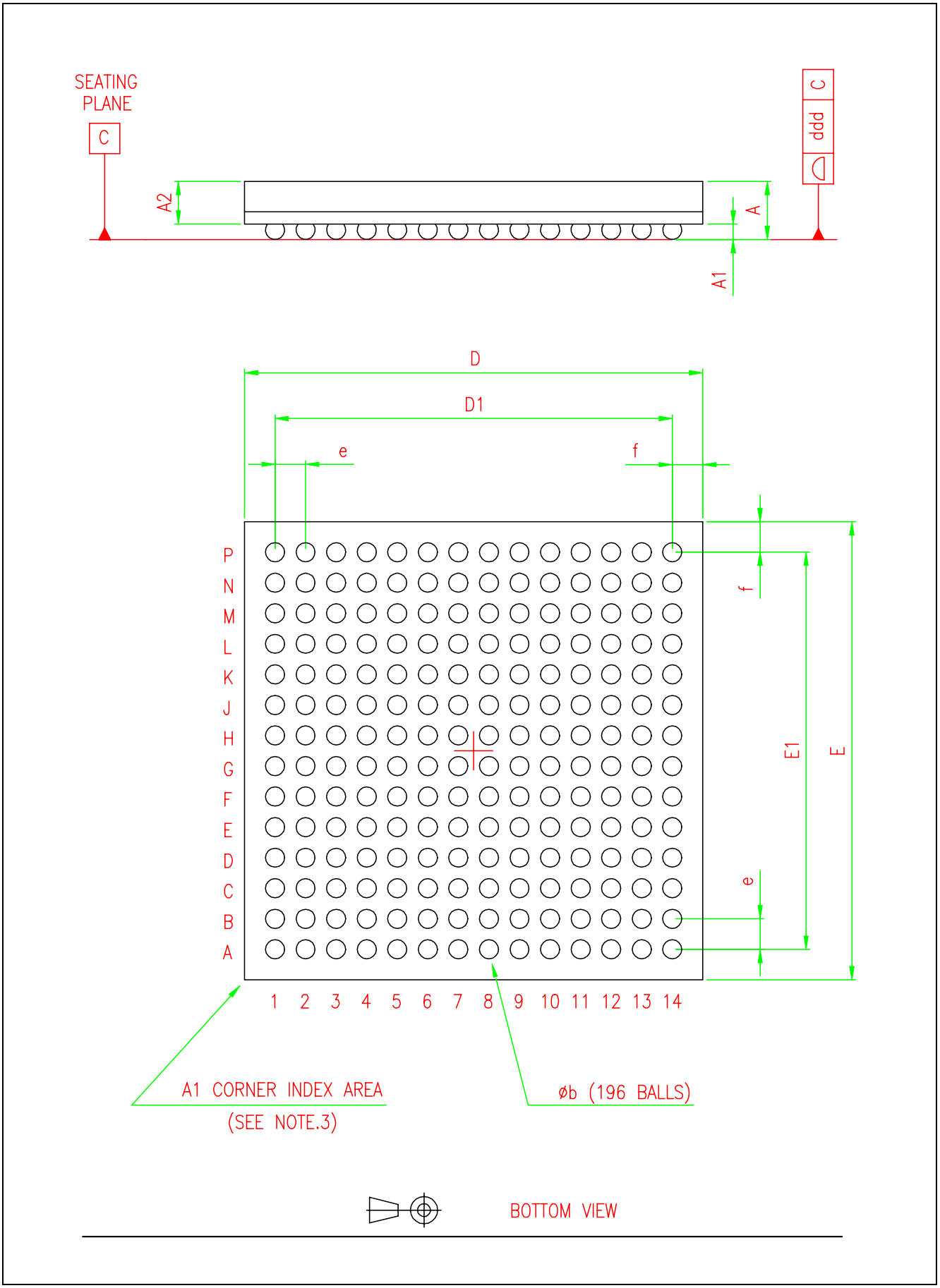
Note: 1 The maximum mounted height is 1.57 mm based on a 0.37 mm ball pad diameter. Solder paste is 0.15 mm thick with 0.37 mm ball pad diameter.

*2 LFBGA stands for **L**ow Profile **F**ine Pitch **B**all **G**rid **A**rray.*
Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component. A = [1.21 to 1.70] mm
FIne pitch: e<1.00 mm pitch.

3 The terminal A1 corner must be identitied on the top surface by using a cormer chamfer, ink or metalized markings or other features of package body or integral heatslug.
A distinguishing feature can be added on the bottom surface of the package to identify the terminal A1 corner.

Exact shape of each corner is optional.

Figure 4: LFBGA 12x12x1.70 196 (80% scale versus original drawing)



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