



**THE DATASHEET OF  
CY74FCT157CTQCT**

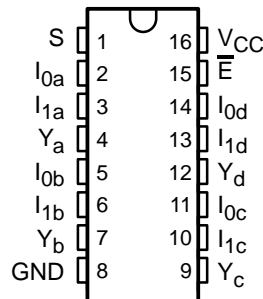


# CY54FCT157T, CY74FCT157T QUAD 2-INPUT MULTIPLEXERS WITH 3-STATE OUTPUTS

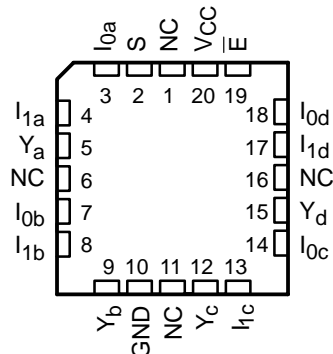
SCCS014B – MAY 1994 – REVISED NOVEMBER 2001

- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- CY54FCT157T
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT157T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current
- 3-State Outputs

CY74FCT157T . . . Q OR SO PACKAGE  
(TOP VIEW)



CY54FCT157T . . . L PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The 'FCT157T devices are quad two-input multiplexers that select four bits of data from two sources under the control of a common data-select (S) input. The output-enable ( $\bar{E}$ ) input is active low. When  $\bar{E}$  is high, all of the outputs (Y) are forced low, regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the 'FCT157T devices. The state of S determines the particular register from which the data comes. It also can be used as a function generator. These devices are useful for implementing highly irregular logic by generating any 4 of the 16 different functions of 2 variables, with 1 variable common.

The 'FCT157T devices are logic implementations of a four-pole, two-position switch, where the position of the switch is determined by the logic levels at S.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**CY54FCT157T, CY74FCT157T**  
**QUAD 2-INPUT MULTIPLEXERS**  
**WITH 3-STATE OUTPUTS**

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**PIN DESCRIPTION**

NAME	DESCRIPTION
S	Common select input
$\bar{E}$	Enable inputs (active low)
I <sub>0</sub>	Data inputs from source 0
I <sub>1</sub>	Data inputs from source 1
Y	Noninverted outputs

**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	QSOP – Q	Tape and reel	4.3	CY74FCT157CTQCT	FT157-3	
	SOIC – SO	Tube	4.3	CY74FCT157CTSOC	FCT157C	
		Tape and reel	4.3	CY74FCT157CTSOCT		
	-40°C to 85°C	QSOP – Q	Tape and reel	5	CY74FCT157ATQCT	FT157-1
		SOIC – SO	Tube	5	CY74FCT157ATSOC	FCT157A
			Tape and reel	5	CY74FCT157ATSOCT	
-55°C to 125°C	LCC – L	Tube	5.8	CY54FCT157ATLMB		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

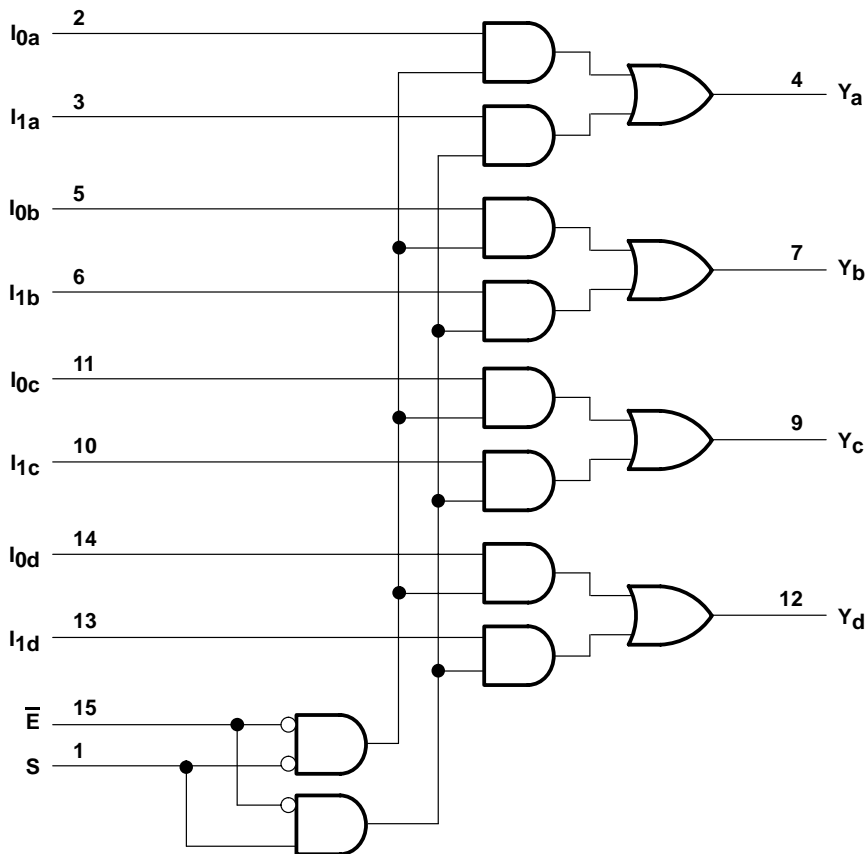
**FUNCTION TABLE**

INPUTS				OUTPUT
$\bar{E}$	S	I <sub>0</sub>	I <sub>1</sub>	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High logic level, L = Low logic level,  
X = Don't care



**logic diagram (positive logic)**



Pin numbers shown are for the Q and SO packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package .....	90°C/W
SO package .....	57°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to 135°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

# CY54FCT157T, CY74FCT157T QUAD 2-INPUT MULTIPLEXERS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 2)

		CY54FCT157T			CY74FCT157T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-12			-32	mA
I <sub>OL</sub>	Low-level output current			32			64	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT157T			CY74FCT157T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		-0.7	-1.2				V
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA				-0.7	-1.2		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA	2.4	3.3					V
	V <sub>CC</sub> = 4.75 V				2			
		I <sub>OH</sub> = -15 mA				2.4	3.3	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 32 mA		0.3	0.55				V
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA				0.3	0.55		
V <sub>hys</sub>	All inputs		0.2		0.2			V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>			5				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>					5		
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V			±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V					±1		
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V			±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V					±1		
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.7 V			10				μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 2.7 V					10		
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V			-10				μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0.5 V					-10		
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V	-60	-120	-225				mA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V				-60	-120	-225	
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V			±1			±1	μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V		0.1	0.2				mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.1	0.2		
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V <sup>§</sup> , f <sub>1</sub> = 0, Outputs open		0.5	2				mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V <sup>§</sup> , f <sub>1</sub> = 0, Outputs open				0.5	2		

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND



**CY54FCT157T, CY74FCT157T**  
**QUAD 2-INPUT MULTIPLEXERS**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS		CY54FCT157T		CY74FCT157T		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$I_{CCD}$ †	$V_{CC} = 5.5\text{ V}$ , One input switching at 50% duty cycle, Outputs open, $\bar{E} = \text{GND}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.06	0.12			mA/ MHz	
	$V_{CC} = 5.25\text{ V}$ , One input switching at 50% duty cycle, Outputs open, $\bar{E} = \text{GND}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$				0.06	0.12		
$I_C$ #	$V_{CC} = 5.5\text{ V}$ , Outputs open, $\bar{E} = \text{GND}$	One input switching at $f_1 = 10\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.7	1.4		mA	
			$V_{IN} = 3.4\text{ V}$ or GND	1	2.4			
		Four bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.7	1.4			
			$V_{IN} = 3.4\text{ V}$ or GND	1.7	5.4			
	$V_{CC} = 5.25\text{ V}$ , Outputs open, $\bar{E} = \text{GND}$	One input switching at $f_1 = 10\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.7		1.4
			$V_{IN} = 3.4\text{ V}$ or GND			1		2.4
		Four bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.7		1.4
			$V_{IN} = 3.4\text{ V}$ or GND			1.7		5.4
$C_i$			5	10	5	10	pF	
$C_o$			9	12	9	12	pF	

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

†† This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.

**switching characteristics over operating free-air temperature range (see Figure 1)**

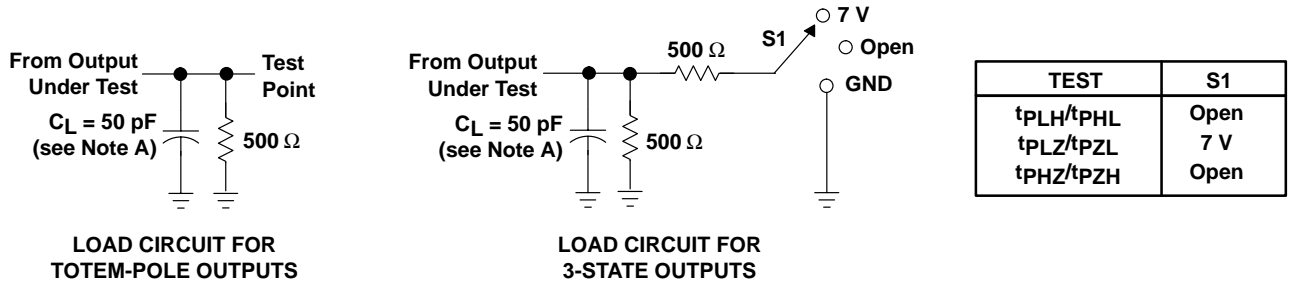
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT157AT		CY74FCT157AT		CY74FCT157CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	I	Y	1.5	5.8	1.5	5	1.5	4.3	ns
$t_{PHL}$			1.5	5.8	1.5	5	1.5	4.3	
$t_{PLH}$	$\bar{E}$	Y	1.5	7.4	1.5	6	1.5	4.8	ns
$t_{PHL}$			1.5	7.4	1.5	6	1.5	4.8	
$t_{PLH}$	S	Y	1.5	8.1	1.5	7	1.5	5.2	ns
$t_{PHL}$			1.5	8.1	1.5	7	1.5	5.2	



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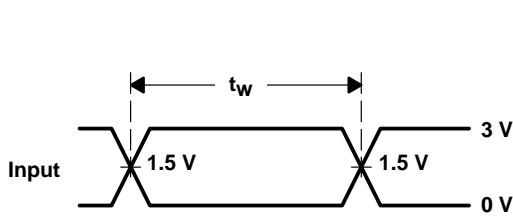
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## PARAMETER MEASUREMENT INFORMATION

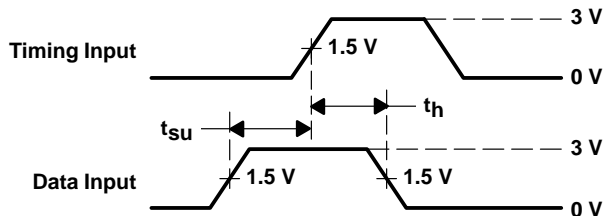


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

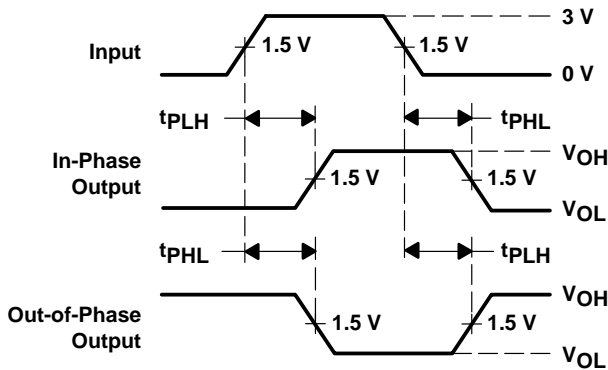
LOAD CIRCUIT FOR  
3-STATE OUTPUTS



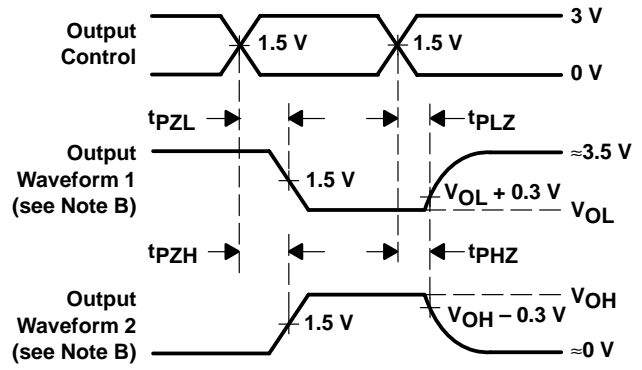
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9220803M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
CY74FCT157ATD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157ATDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157ATDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157ATDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157ATDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157ATDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157ATQCT	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT157ATQCTE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT157ATQCTG4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT157ATSOC	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157ATSOCE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157ATSOCG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTQCT	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT157CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT157CTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT157CTSOC	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTSOCE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTSOCG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CY74FCT157CTSOCT	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTSOCTE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT157CTSOCTG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT157ATDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CY74FCT157CTDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CY74FCT157CTSOCT	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT157ATDR	SOIC	D	16	2500	333.2	345.9	28.6
CY74FCT157CTDR	SOIC	D	16	2500	333.2	345.9	28.6
CY74FCT157CTSOCT	SOIC	DW	16	2000	346.0	346.0	33.0

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