# THE DATASHEET OF

# SI88620ED-ISR

www.win-source.net 0086-755-83957316

DATA SHEET

# Si88x2x: Dual Digital Isolators with DC-DC Converter

The Si88xx integrates Skyworks' proven digital isolator technology with an on-chip isolated dc-dc converter that provides regulated output voltages of 3.3 or 5.0 V (or >5 V with external components) at peak output power levels of up to 5 W. These devices provide up to two digital channels. The dc-dc converter has user-adjustable frequency for minimizing emissions, a soft-start function for safety, a shutdown option and loop compensation. The device requires only minimal passive components and a miniature transformer.

The ultra-low-power digital isolation channels offer substantial data rate, propagation delay, size and reliability advantages over legacy isolation technologies. Data rates up to 100 Mbps max are supported, and all devices achieve propagation delays of only 23 ns max. Ordering options include a choice of dc-dc converter features, isolation channel configurations and a fail-safe mode. All products are certified by UL, CSA, VDE, and CQC.

Automotive Grade is available. These products are built using automotive specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

## Applications

- Industrial automation systems
- Hybrid electric and electric vehicles
- Isolated power supplies
- Inverters
- Data acquisition
- Motor control
- PLCs, distributed control systems

## Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 5000 $V_{RMS}$ for one minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
- VDE certification conformity
  - 60747-17 (basic insulation, pending)
  - 62368-1 (conformity)
- CQC certification approval
  - GB4943.1

## Key Features

- High-speed isolators with integrated dc-dc converter
- Fully-integrated secondary sensing feedback controlled converter with dithering for low EMI
- DC-DC converter peak efficiency of 83% with external power switch
- Up to 5 W isolated power with external power switch
- Options include dc-dc shutdown, frequency control, and soft start
- Standard voltage conversion:
  - 3/5 V to isolated 3/5 V
  - 24 V to isolated 3/5 V
  - 3/5 V to isolated 24 V
  - 24 V to isolated 24 V
- Precise timing on digital isolators:
  - 0 to 100 Mbps
  - 18 ns typical prop delay
- High electromagnetic immunity and ultra-low emissions
- RoHS compliant packages:
  - SOIC-16 wide-body
  - SOIC-20 wide-body
- Isolation of up to 5000 $V_{RMS}$
- High transient immunity of 100 kV/µs (typical)
- AEC-Q100 qualified
- Wide temp range: –40 to +125 °C
- Automotive-grade OPNs available:
  - AIAG compliant PPAP documentation support
  - IMDS and CAMDS listing support

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

## 1. Pin Descriptions

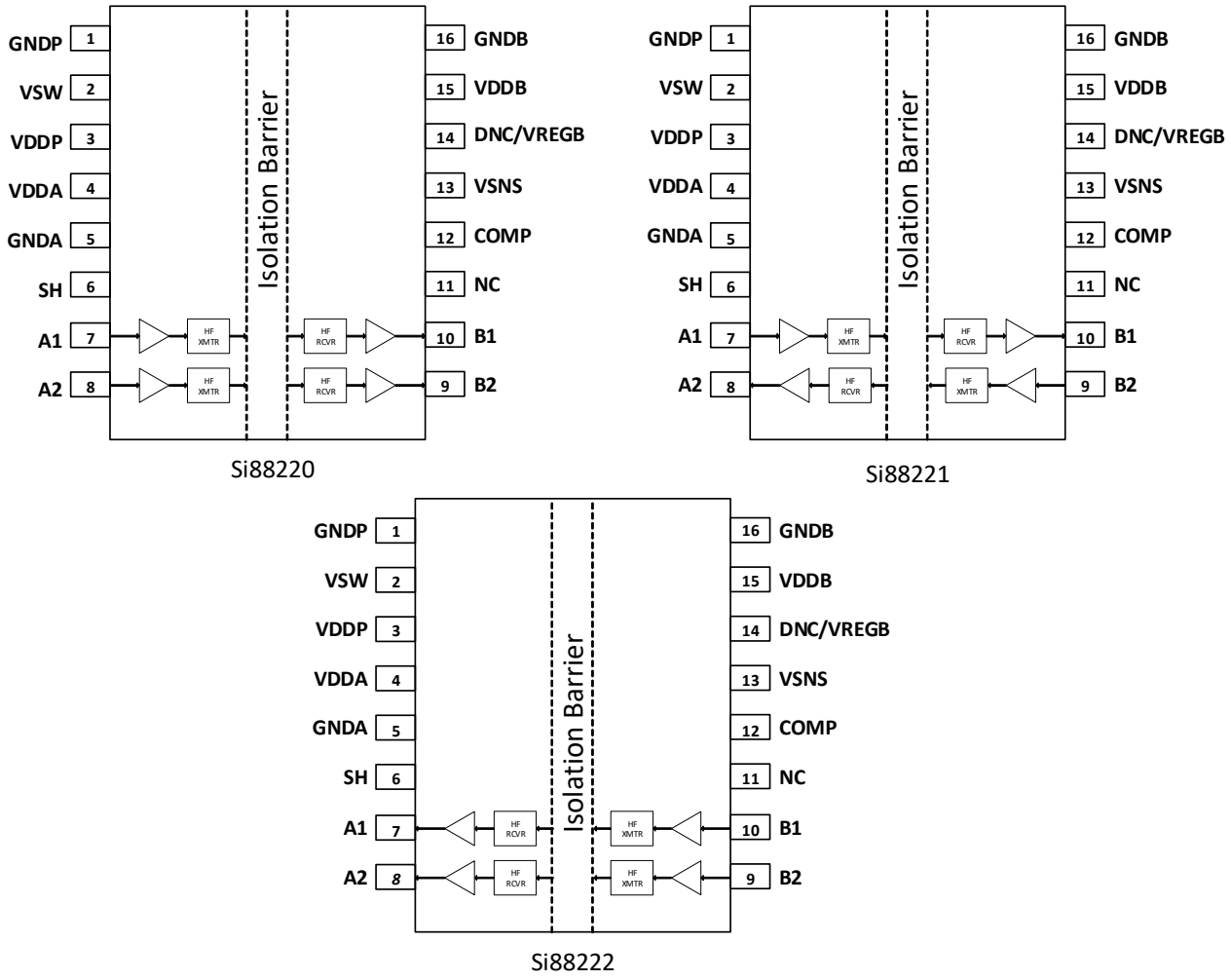


**Figure 1. Si8822x Pin Configurations**

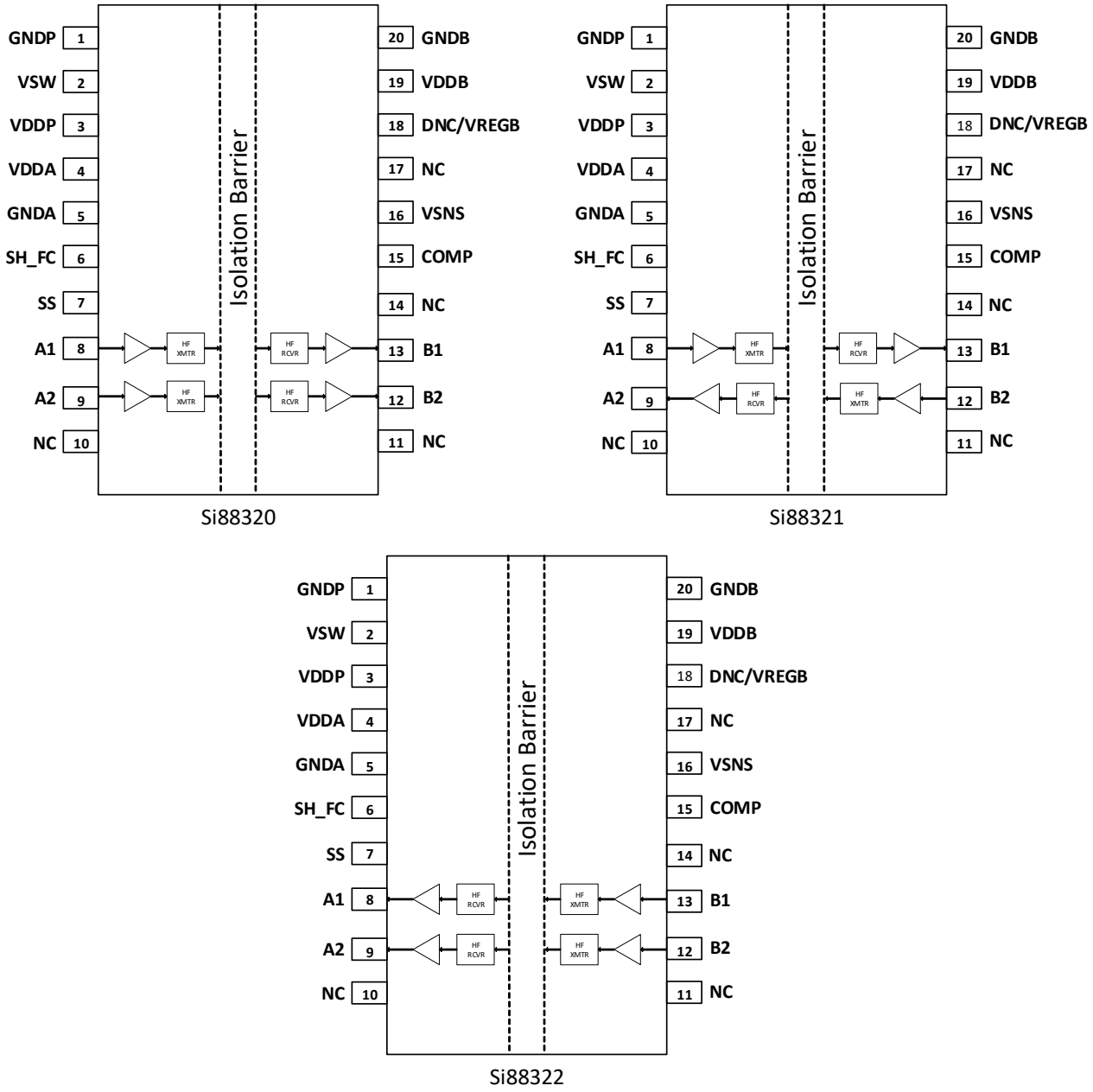


**Figure 2. Si8832x Pin Configurations**

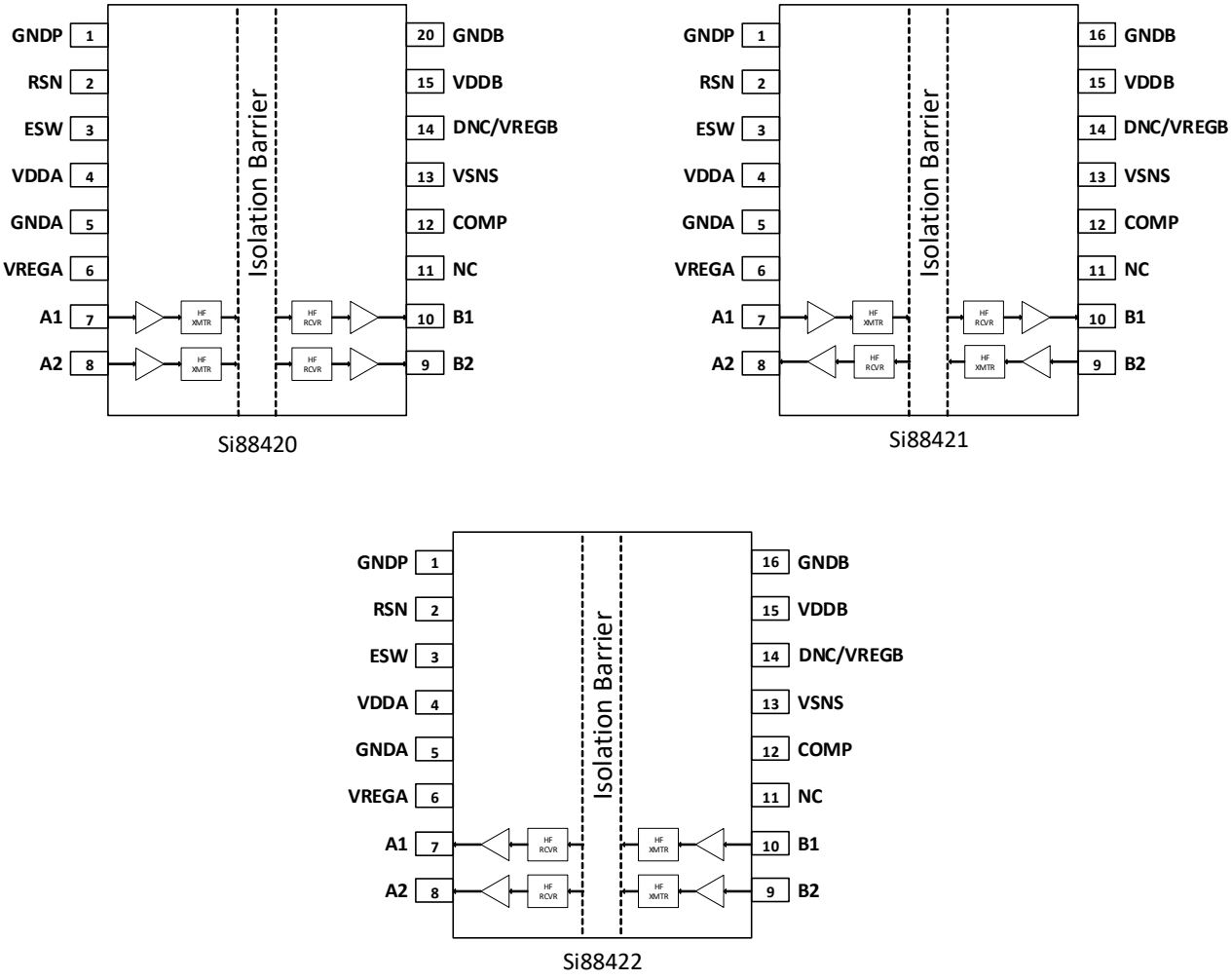


**Figure 3. Si8842x Pin Configurations**

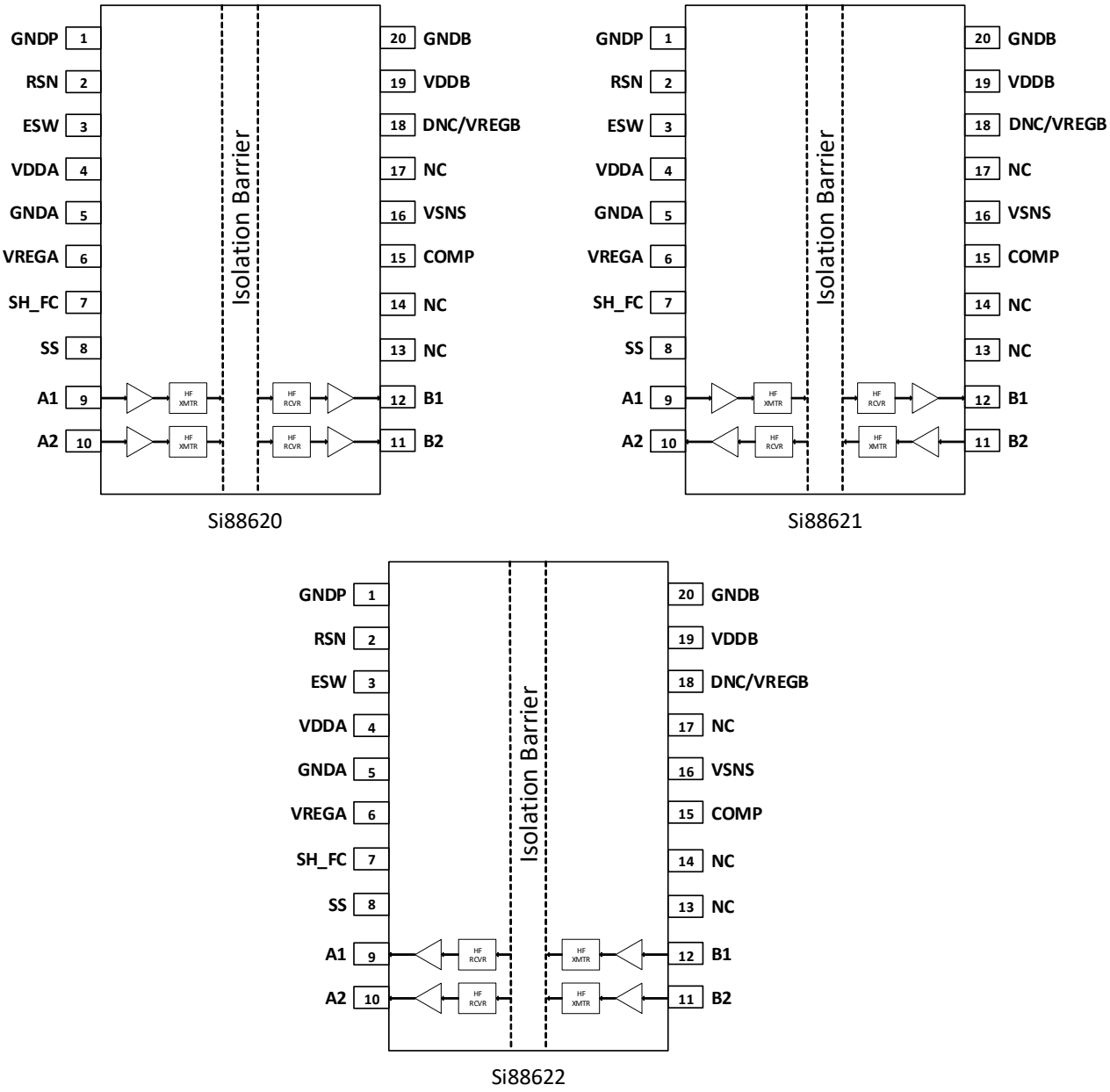


**Figure 4. Si8862x Pin Configurations**

**Table 1. Si88x2x Pin Descriptions**

| Pin Name | Description |
|---|---|
| **DC-DC Input Side** | |
| VDDP | Power stage primary power supply. |
| $V_{REGA}$ | Voltage reference output for external voltage regulator pin. |
| GNDP | Power stage ground. |
| ESW | Power stage external switch driver output. |
| VSW | Power stage internal switch output. |
| SS | Soft startup control. |
| SH, SH_FC | Shutdown and Switch frequency control. |
| RSN | Power stage current sense input. |
| **DC-DC Output Side** | |
| VSNS | Power stage feedback input. |
| COMP | Power stage compensation. |
| DNC/$V_{REGB}$ | Voltage reference output for external voltage regulator pin.<br>This pin has a Zener connected internally. Use this pin as reference only when output voltage from dc-dc is > 5.5 V.<br>If output voltage is ≤ 5.5 V, this pin should be read as DNC or Do Not Connect. |
| NC | No connect; this pin is not connected to the silicon. |
| **Digital Isolator VDDA Side** | |
| VDDA | Primary side signal power supply. |
| A1–A2 | I/O signal channel 1–4. |
| GNDA | Primary side signal ground. |
| **Digital Isolator VDDB Side** | |
| VDDB | Secondary side signal power supply. |
| B1–B2 | I/O signal channel 1–4. |
| GNDB | Secondary side signal ground. |

# 2. Functional Description

## 2.1. Theory of Operation

The Si88xx family of products is capable of transmitting and receiving digital data signals from an isolated power domain to a local system power domain with up to 5 kV of isolation. Each part has two unidirectional digital isolation channels. In addition, Si88xx products include an integrated controller and switches for a dc-dc converter which regulates output voltage by sensing it on the isolated side.

## 2.2. Digital Isolation

The operation of an Si88xx digital channel is analogous to that of a digital buffer, except an RF carrier transmits data across the isolation barrier. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si88xx channel is shown in Figure 5.

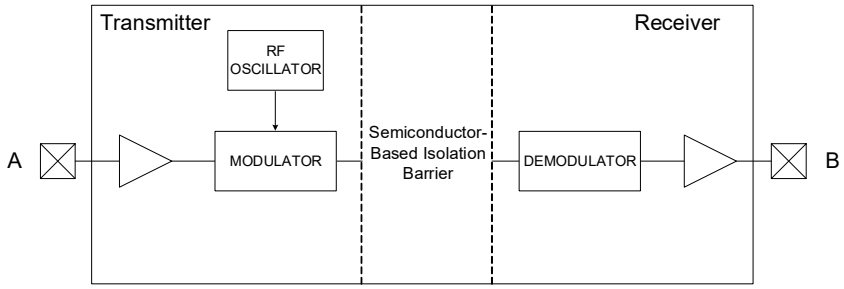


**Figure 5. Simplified Si88xx Channel Diagram**

A channel consists of an RF Transmitter and RF Receiver separated by a silicon dioxide capacitive isolation barrier. In the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 6 for more details.

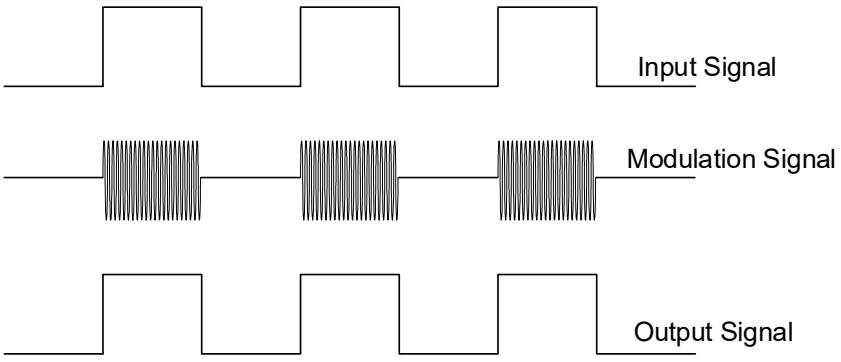


**Figure 6. Modulation Scheme**

## 2.3. DC-DC Converter Application Information

The Si88xx isolated dc-dc converter is based on a modified fly-back topology and uses an external transformer and Schottky rectifying diode for low cost and high operating efficiency. The PWM controller operates in closed-loop, peak current mode control and generates isolated output voltages with 2 W average output power at 5.0 V. Options are available for up to 24 Vdc input or output operation and externally configured switching frequency.

The dc-dc controller modulates a pair of internal primary-side power switches (see Figure 7, “Si883xx Block Diagram: 3 V to 5 V Input to 3 V to 5 V Output,” on page 10) to generate an isolated voltage at external diode D1 cathode. Closed-loop feedback is provided by a compensated error amplifier, which compares the voltage at the VSNS pin to an internal voltage reference. The resulting error voltage is fed back through the isolation barrier via an internal feedback path to the controller, thus completing the control loop.

For higher input supply voltages than 5 V, an external FET Q2 is modulated by a driver pin ESW as shown in Figure 9. A shunt resistor based voltage sense pin RSN provides current sensing capability to the controller.

Additional features include an externally-triggered shutdown of the converter functionality using the SH pin and a programmable soft start configured by a capacitor connected to the SS pin. The Si88xx can be used in low- or high-voltage configurations. These features and configurations are explained in more detail below.

### 2.3.1. Shutdown

This feature allows the operation of the dc-dc converter to be shut down when asserted high. This function is provided by pin 6 (labeled “SH” on the Si882xx) and Pin 7 (labeled “SH_FC” on the Si883xx and Si886xx). This feature is not available on the Si884xx. Pin 6 or Pin 7 provide the exact same functionality and shut down the dc-dc converter when asserted high. For normal operation, Pins 6 and 7 should be connected to ground.

### 2.3.2. Soft-Start

The dc-dc controller has an internal timer that controls the power conversion start-up to limit inrush current. There is also the Soft Start option where users can program the soft start up by an external capacitor connected to the SS pin. This feature is available on the Si883xx and the Si886xx.

### 2.3.3. Programmable Frequency

The frequency of the PWM modulator is set to a default of 250 kHz for Si882xx/4xx. Users can program their desired frequency within a given band of 200 kHz to 800 kHz by controlling the time constant of an external RC connected to the SH_FC and SS pins for Si883xx/6xx.

### 2.3.4. External Transformer Driver

The dc-dc controller has internal switches (VSW) for driving the transformer with up-to a 5.5 V voltage supply. For higher voltages on the primary side, a driver output (ESW) is provided that can drive an external NMOS power transistor for driving the transformer. When this configuration is used, a shunt resistor based voltage sense pin (RSN) provides current sensing to the controller.

### 2.3.5. $V_{REGA}$, $V_{REGB}$

For supporting voltages greater than 5.5 V, an internal voltage regulator ($V_{REGA}$, $V_{REGB}$) needs to be used in conjunction with an external NPN transistor, a resistor and a capacitor to provide regulated voltage to the IC.

### 2.3.6. Output Voltage Control

The isolated output voltage ($V_{OUT}$) is sensed by a resistor divider that provides feedback to the controller through the VSNS pin. The voltage error is encoded and transmitted back to the primary side controller across the isolation barrier, which in turn changes the duty cycle of the transformer driver. The equation for $V_{OUT}$ is as follows:

$$V_{OUT} = V_{SNS} \times \left(1 + \frac{R1}{R2}\right) + R1 \times I_{OFFSET}$$

### 2.3.7. Compensation

The dc-dc converter uses peak current mode control. The loop is compensated by connecting an external resistor in series with a capacitor from the COMP pin to GNDB. The compensation resistance, RCOMP is fixed at 49.9 kΩ for Si882xx/3xx and 100 kΩ for Si884xx/6xx to match internal resistance. Capacitance value is given by the following equation, where $f_C$ is crossover frequency:

$$CCOMP = \left(\frac{6}{2 \times \pi \times f_C \times RCOMP}\right)$$

For more details on the calculations involved, see "AN892: Design Guide for Isolated DC/DC Using the Si882xx/883xx".

### 2.3.8. Thermal Protection

A thermal shutdown circuit is included to protect the system from over-temperature events. The thermal shutdown is activated at a junction temperature that prevents permanent damage from occurring.

### 2.3.9. Cycle Skipping

Cycle skipping is included to reduce switching power losses at light loads. This feature is transparent to the user and is activated automatically at light loads. The product options with integrated power switches (Si882xx/3xx) may never experience cycle skipping during operation even at light loads while the external power switch options (Si884xx/6xx) are likely to have cycle skipping start at light loads.

### 2.3.10. Low-Voltage Configuration

The low-voltage configuration is used for converting 3.0 V to 5.5 V. All product options of the Si882xx and Si883xx are intended for this configuration.

An advantage of Si88xx devices over other converters that use this same topology is that the output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the dc-dc to operate with superior line and load regulation while reducing external components and increasing lifetime reliability.

In a typical digital signal isolation application, the dc-dc powers the Si882xx and Si883xx VDDB as shown in Figure 7, "Si883xx Block Diagram: 3 V to 5 V Input to 3 V to 5 V Output," on page 10. In addition to powering the isolated side of the dc-dc, it can deliver up to 2 W of power to external loads. The dc-dc requires an input capacitor, C2, blocking capacitor, C1, transformer, T1, rectifying diode, D1, and an output capacitor, C3. Resistors R1 and R2 divide the output voltage to match the internal reference of the error amplifier and set the Vout voltage level.

Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. Though it is not necessary for normal operation, we recommend that a snubber be used to reduce any voltage spikes at the VSW pin and minimize radiated emissions.

To ensure reliable dc-dc operation the following layout guidelines are recommended:

1. VDDA and VDDP should be connected by the shortest possible trace. A minimum trace width of 15 mils is recommended.
2. GNDA and GNDP should be directly connected by the shortest possible trace. A minimum trace width of 15 mils is recommended.
3. Bypass capacitor C2 should be directly connected to both VDDP and GNDP. A minimum trace width of 15 mils is recommended.
4. GNDA should be directly connected to a ground plane.

More details can be found in "AN892: Design Guide for Isolated DC/DC Using the Si882xx/883xx".

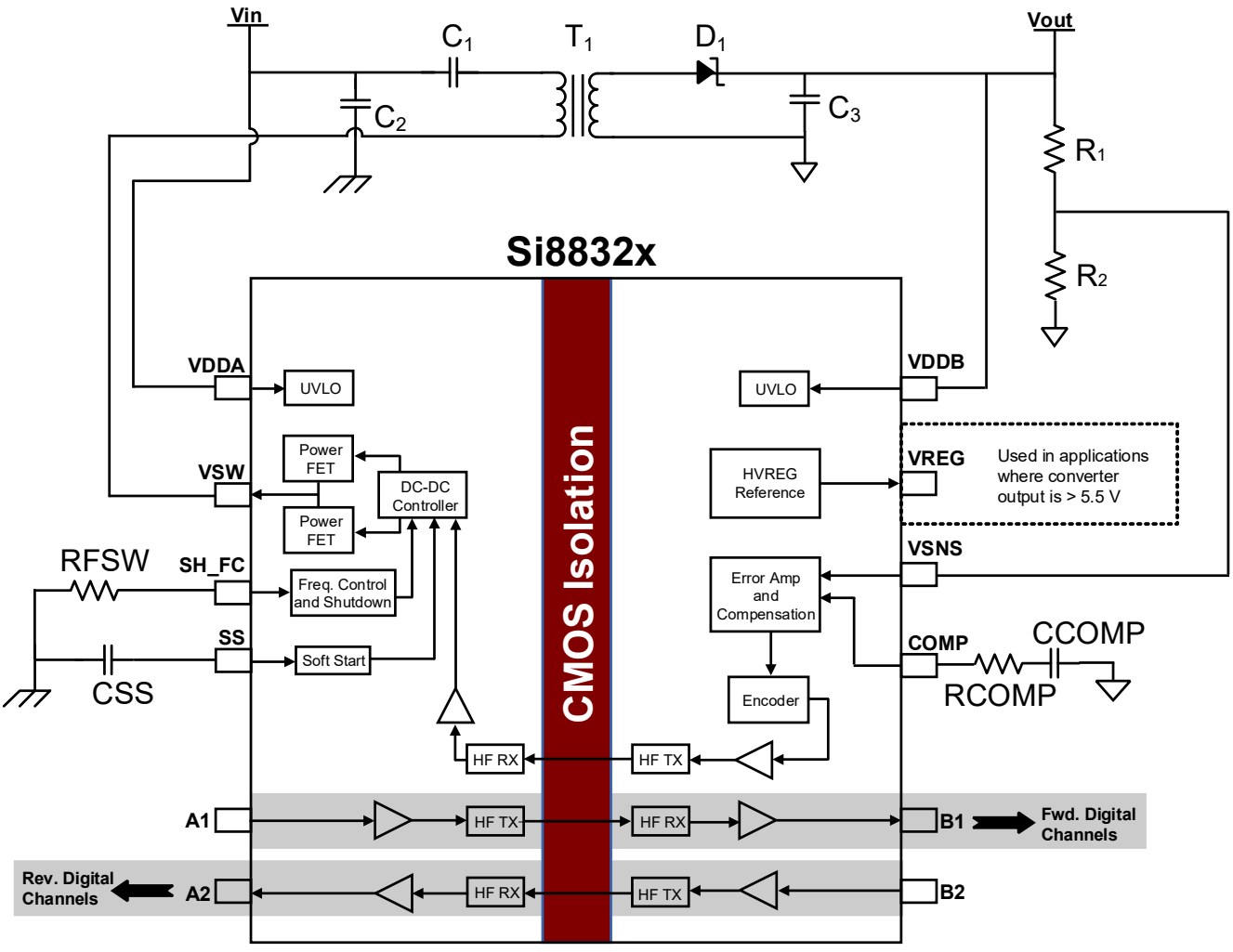


**Figure 7. Si883xx Block Diagram: 3 V to 5 V Input to 3 V to 5 V Output**

### 2.3.11. Low-Voltage to High-Voltage Configuration

The low-voltage to high-voltage configuration is used for converting 3.0 V to 5.5 V, up to 24 V.

In a typical digital signal isolation application, the dc-dc powers the Si882xx and Si883xx VOUT as shown in the figure below. In addition to powering the isolated side of the dc-dc, it can deliver up to 2 W of power to external loads. The dc-dc requires an input capacitor, C2, blocking capacitor, C1, transformer, T1, rectifying diode, D1, and an output capacitor, C3. Resistors R1 and R2 divide the output voltage to match the internal reference of the error amplifier. To supply VDDB, Q3 transistor is biased and filtered by R5 and C4. Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. Though it is not necessary for normal operation, we recommend that a snubber be used to minimize radiated emissions. More details can be found in "AN892: Design Guide for Isolated DC/DC Using the Si882xx/883xx".

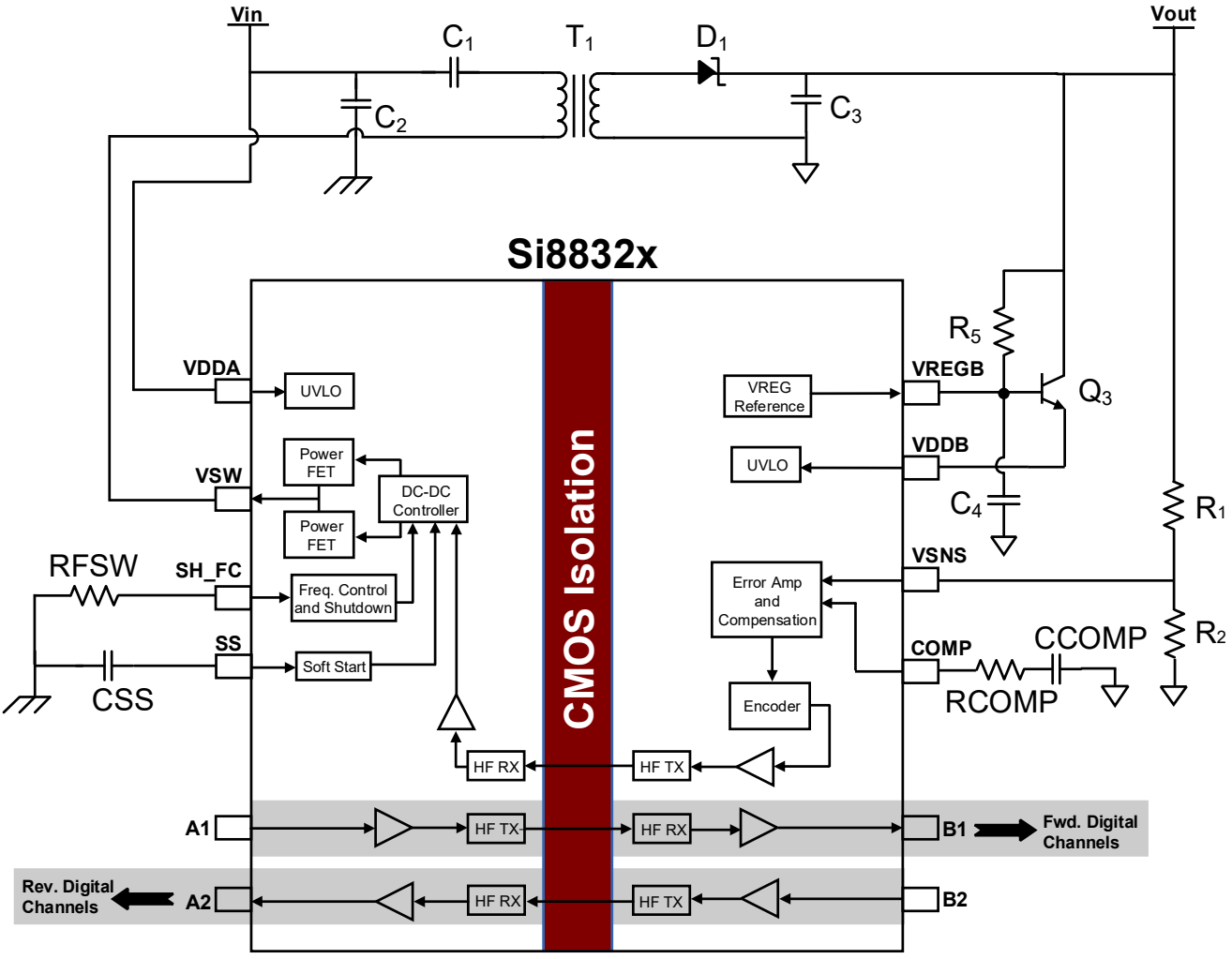


**Figure 8. Si883xx Block Diagram: 3 V to 5 V Input to up to 24 V Output**

### 2.3.12. High-Voltage to Low-Voltage Configuration

The high-voltage configuration is used for converting up to 24 V to 3.3 V or 5.0 V. All product options of the Si884xx and Si886xx are intended for this configuration.

Si884xx and Si886xx can be used for dc-dc applications that have primary side voltage greater than 5.5 V. The dc-dc converter uses the isolated flyback topology. With this topology, the switch and sense resistor are external, allowing higher switching voltages. Digital isolator supply VDDA of the Si884xx and Si886xx require a supply less than or equal to 5.5 V. If a suitable supply is not available on the primary side, the $V_{REGA}$ voltage reference with external NPN transistor can supply VDDA. This eliminates the need to design an additional linear regulator circuit. Like the Si882xx and Si883xx, the output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the dc-dc to operate with superior line and load regulation.

The figure below shows the block diagram of an Si886xx with external components. Si886xx is different from the Si882xx/883xx as it has externally-controlled switching frequency and soft start. The dc-dc requires input capacitor C2, transformer T1, switch Q1, sense resistor R4, rectifying diode D1 and an output capacitor C3. To supply VDDA, Q2 transistor is biased and filtered by R3 and C1. External frequency and soft start behavior is set by CSS and RFSW. Resistors R1 and R2 divide the output voltage to match the internal reference of the error amplifier. Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. Though it is not necessary for normal operation, we recommend to use a snubber, to minimize high-frequency emissions. For further details, see “AN901: Design Guide for Isolated DC/DC Using the Si884xx, Si886xx, or Si8282/84”.

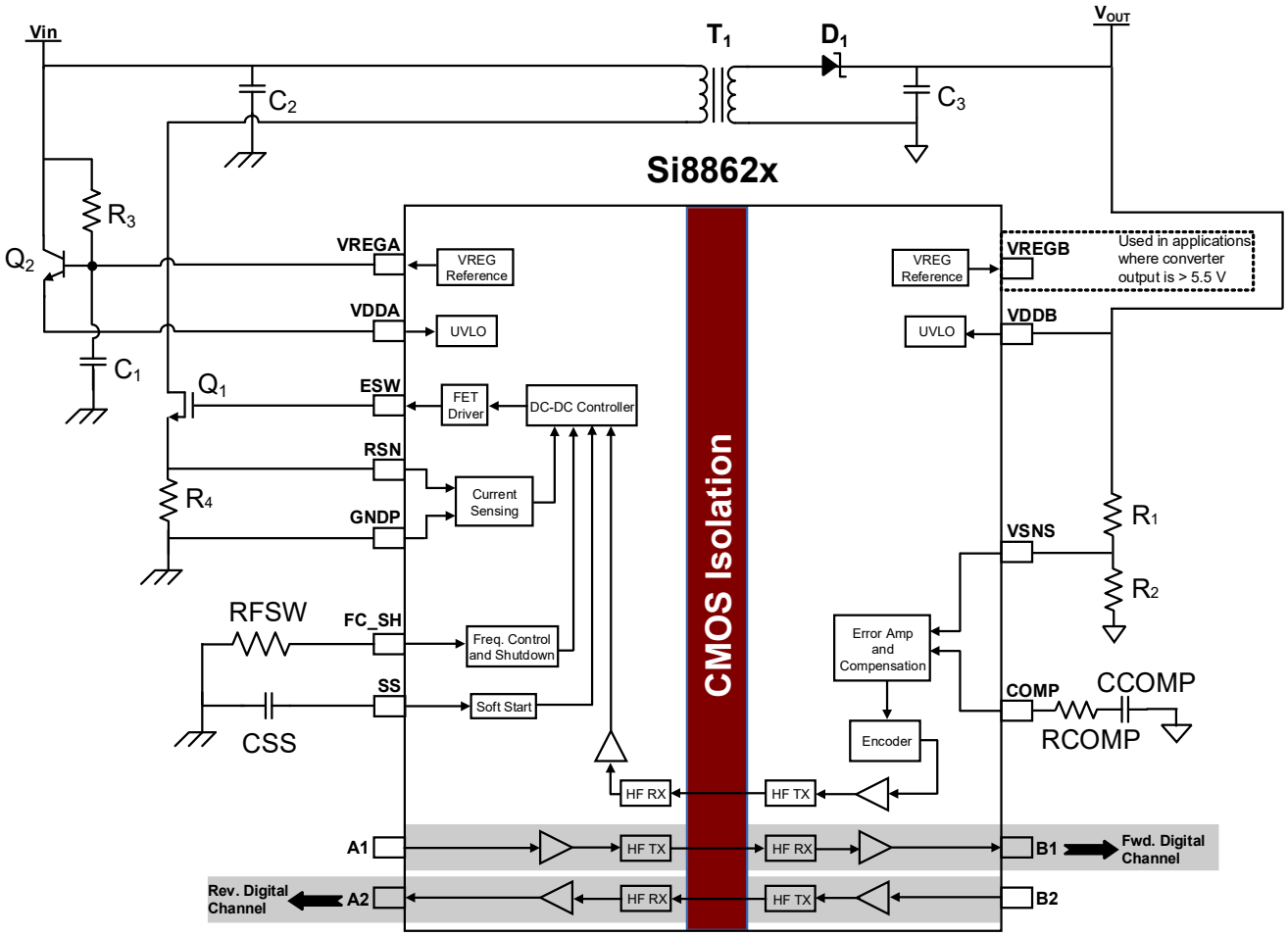


**Figure 9. Si886xx Block Diagram: 24 V Input to 5 V Output**

### 2.3.13. High-Voltage to High-Voltage Configuration

The high-voltage configuration is used for converting up to 24 V to up to 24 V.

Si884xx and Si886xx can be used for dc-dc applications that have primary side voltage greater than 5.5 V. The dcdc converter uses the isolated flyback topology. With this topology, the switch and sense resistor are external, allowing higher switching voltages. Digital isolator supply VDDA of the Si884xx and Si886xx require a supply less than or equal to 5.5 V. If a suitable supply is not available on the primary side, the $V_{REGA}$ voltage reference with external NPN transistor can supply VDDA. This eliminates the need to design an additional linear regulator circuit. Like the Si882xx and Si883xx, the output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the dc-dc to operate with superior line and load regulation.

The figure below shows the block diagram of an Si886xx with external components. Si886xx is different from the Si882xx/883xx as it has externally-controlled switching frequency and soft start. The dc-dc requires input capacitor C2, transformer T1, switch Q1, sense resistor R4, rectifying diode D1 and an output capacitor C3. To supply VDDA, Q2 transistor is biased and filtered by R3 and C1. External frequency and soft start behavior is set by CSS and RFSW. Resistors R1 and R2 divide the output voltage to match the internal reference of the error amplifier. To supply VDDB, Q3 transistor is biased and filtered by R5 and C4. Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. Though it is not necessary for normal operation, we recommend to use a

snubber, to minimize high-frequency emissions. For more details, see "AN901: Design Guide for Isolated DC/DC Using the Si884xx, Si886xx, or Si8282/84".

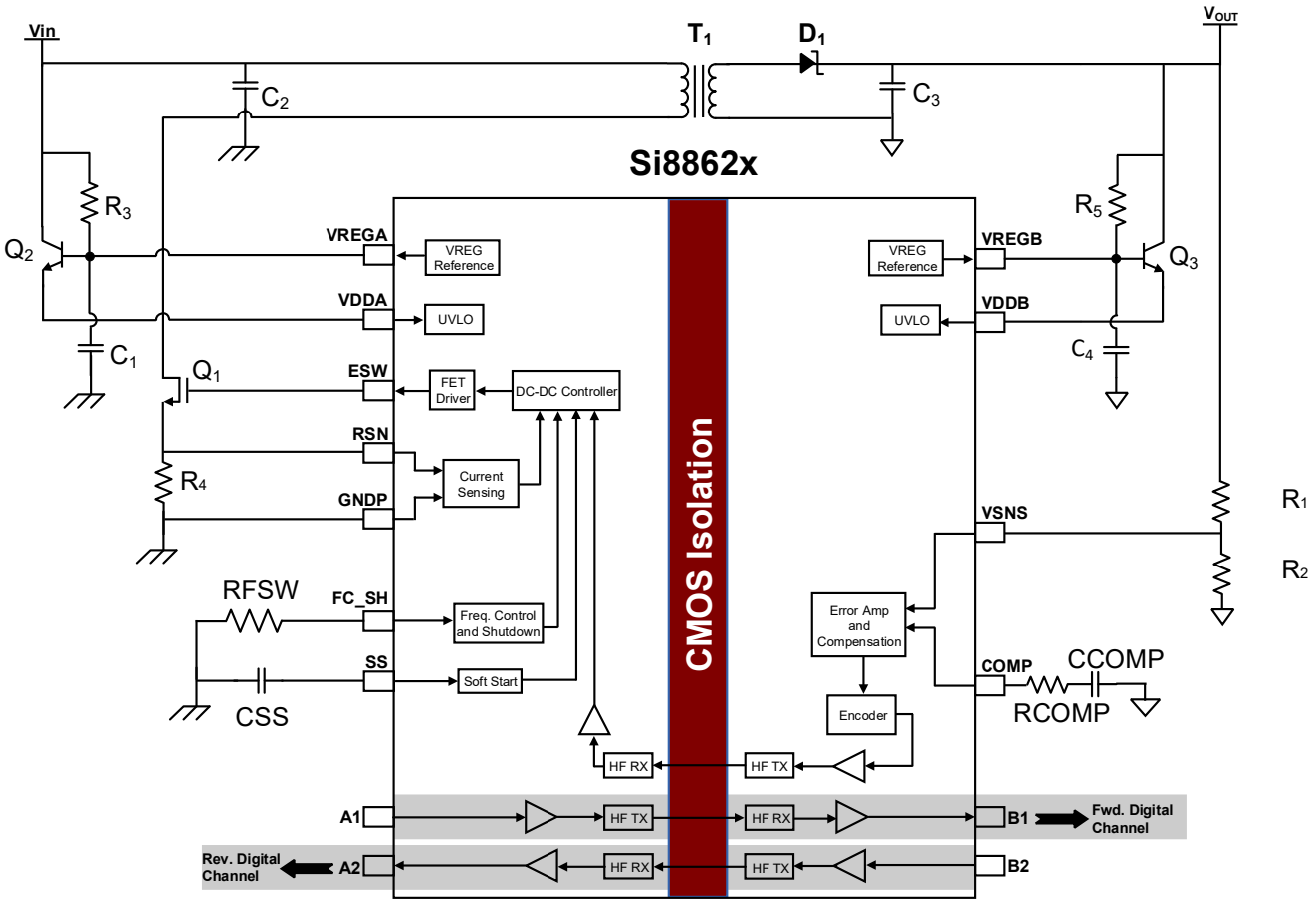


**Figure 10. Si886xx Block Diagram: Up to 24 V Input to up to 24 V Output**

## 2.4. Transformer Design

The table below provides a list of transformers and their parametric characteristics that have been validated to work with Si882xx/3xx products (input voltage of 3 to 5 V) and Si884xx/Si886xx products (input voltage of 24 V). It is recommended that users order the transformers from the vendors per the part numbers given below. Refer to "AN892: Design Guide for Isolated DC/DC using the Si882xx/883xx" and "AN901: Design Guide for Isolated DC/DC Using the Si884xx, Si886xx, or Si8282/84" for voltage translation applications not listed below.

To manufacture transformers from your preferred suppliers that may not be listed below, please specify to supplier the parametric characteristics as specified in the table below for a given input voltage and isolation rating.

**Table 2. Transformer Specifications[1]**

| Transformer Supplier | Ordering Part # | Input Voltage | Output Voltage | Turns Ratio P:S | Leakage Inductance | Primary Inductance | Primary Resistance | Isolation Rating |
|---|---|---|---|---|---|---|---|---|
| UMEC (http://www.umec-usa.com) | UTB02185s | 4.5 to 5.5 V | 3.0 to 5.5 V | 1.0:4.0 | 100 nH max | 2 µH ± 5% | 0.05 Ω max | 2.5 $kV_{RMS}$ |

**Table 2. Transformer Specifications[1] (Continued)**

| Transformer Supplier | Ordering Part # | Input Voltage | Output Voltage | Turns Ratio P:S | Leakage Inductance | Primary Inductance | Primary Resistance | Isolation Rating |
|---|---|---|---|---|---|---|---|---|
| UMEC (http://www.umec-usa.com) | UTB02205s | 12 V, 24 V | 3.3 to 5.0 V, 15 V | 3.0:1.0 | 800 nH max | 25 µH ± 5% | 0.135 Ω max | 2.5 $kV_{RMS}$ |
| UMEC (http://www.umec-usa.com) | UTB02240s | 4.5 to 5.5V | 3.0 to 5.5 V | 1.0:4.0 | 100 nH max | 2 µH ±5% | 0.05 Ω max | 5 $kV_{RMS}$ |
| UMEC (http://www.umec-usa.com) | UTB02250s | 7 to 24 V | 3.3 to 5.5 V | 3.0:1.0 | 600 nH max | 25 µH ± 5% | 0.135 Ω max | 5 $kV_{RMS}$ |
| Coilcraft[2] (http://www.coilcraft.com) | TA7608-AL | 4.5 to 5.5 V | 3.0 to 5.5 V | 1.0:4.0 | 60 nH max | 2 µH ± 5% | 0.033 Ω max | 2.5 $kV_{RMS}$ |
| Coilcraft[2] (http://www.coilcraft.com) | TA7618-AL | 4.5 to 5.5V | 3.0 to 5.5 V | 1.0:4.0 | 64 nH max | 2.0 µH ±5% | 0.031 Ω max | 5 $kV_{RMS}$ |
| Coilcraft[2] (http://www.coilcraft.com) | TA7788-AL | 12V | 5 V, 15 V | 1.00 : 1.25 : 0.75 | 554 nH max | 25 µH ±5% | 0.49 Ω max | 5 $kV_{RMS}$ |
| Coilcraft[2] (http://www.coilcraft.com) | UA7902 | 12V | 5 V, 15 V | 3.0:1.0 | 971 nH max | 25 µH ±5% | 0.075 Ω max | 5 $kV_{RMS}$ |
| TDK (http://www.tdk.com) | P100940_A1 | 4.5 to 5.5V | 3.0 to 5.5 V | 1.0:4.0 | 40 nH max | 2.0 µH ±10% | 0.1 Ω max | 2.4 $kV_{RMS}$ |
| Mentech[2] (http://www.mnc-tek.com) | TTER09-0457S1 | 8 to 24 V | 15 V, 24 V | 1.0:1.0 | 550 nH max | 25 µH ±10% | 0.4 Ω max | 2.5 $kV_{RMS}$ |
| Mentech[2] (http://www.mnc-tek.com) | TTER09-0458S1 | 8 to 24 V | 8 to 24 V | 1.0:1.0 | 550 nH max | 25 µH ±10% | 0.4 Ω max | 5 $kV_{RMS}$ |
| Mentech[2] (http://www.mnc-tek.com) | TTER09-0568S1 TTAER09-2091SG | 3.3 to 5.5 V | 3.3 to 5.5 V | 1.0:4.0 | 100 nH max | 1.5 µH ±8% | 0.05 Ω max | 5 $kV_{RMS}$ |
| Pulse (http://www.pulseelectronics.com/) | PA4896NL | 8 to 24 V | 7 to 24 V | 1.0:1.0 | 650 nH max | 25 µH ±10% | 0.25 Ω max | 2.5 $kV_{RMS}$ |
| Pulse (http://www.pulseelectronics.com/) | PA4897NL | 8 to 24 V | 7 to 24 V | 1.0:1.0 | 650 nH max | 25 µH ±10% | 0.25 Ω max | 5 $kV_{RMS}$ |

1. For reference design details, see "AN892: Design Guide for Isolated DC/DC Using the Si882xx/883xx" or "AN901: Design Guide for Isolated DC/DC Using the Si884xx, Si886xx, or Si8282/84".
2. AEC-Q200 qualified.

# 3. Digital Isolator Device Operation

**Table 3. Si88xx Logic Operation**

| VI Input | VDDI [1,2,3,4] | VDDO [1,2,3,4] | VO Output | Comments |
|---|---|---|---|---|
| H | P | P | H | Normal operation. |
| L | P | P | L | |
| X | UP | P | L[4]<br>H[4] | Upon transition of VDDI from unpowered to powered, $V_O$ returns to the same state as $V_I$. |
| X | P | UP | Undetermined | Upon transition of VDDO from unpowered to powered, $V_O$ returns to the same state as $V_I$. |

1. VDDI and VDDO are the input and output power supplies. VI and VO are the respective input and output terminals.
2. P = powered; UP = unpowered.
3. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current. This situation should be avoided. We recommend that I/Os not be driven high when primary side supply is turned off or when in dc-dc shutdown mode.
4. See 8. Ordering Guide for details. This is the selectable fail-safe operating mode (ordering option). When VDDB is powered via the primary side and the integrated dc-dc, the default outputs are undetermined as secondary side power is not available when primary side power shuts off.

## 3.1. Device Startup

Outputs are held low during power up until VDDx is above the UVLO threshold for time period $t_{SU}$. Following this, the outputs follow the states of inputs.

## 3.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDDx is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when VDDA falls below $V_{DDUV-}$ and exits UVLO when VDDA rises above $V_{DDUV+}$. Side B operates the same as Side A with respect to its VDD supply.

## 3.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 $V_{AC}$) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 $V_{AC}$) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 8, “Insulation and Safety-Related Specifications,” on page 30 and Table 10, “IEC60747-17 Insulation Characteristics,” on page 31 detail the working voltage and creepage/clearance capabilities of the Si88xx. These tables also detail the component standards (UL1577 and IEC 60747-17), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification requirements (e.g., 61010-1, 62368-1, 60601-1, etc.) before starting any design that uses a digital isolator.

### 3.3.1. Supply Bypass

The Si88xx family requires a 0.1 µF bypass capacitor between all VDDx and their associated GNDx. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

### 3.3.2. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving high-impedance terminated PCB traces, output pins should be source-terminated to minimize reflections.

## 3.4. Fail-Safe Operating Mode

Si88xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered.
See Table 3, “Si88xx Logic Operation,” on page 16 and Table 20, “Si88x2x Ordering Guide” on page 40 for more information.

## 3.5. Typical Performance Characteristics

The typical performance characteristics are for information only. Refer to Table 6, “Electrical Characteristics” on page 23 for specification limits. The data below is for all channels switching.

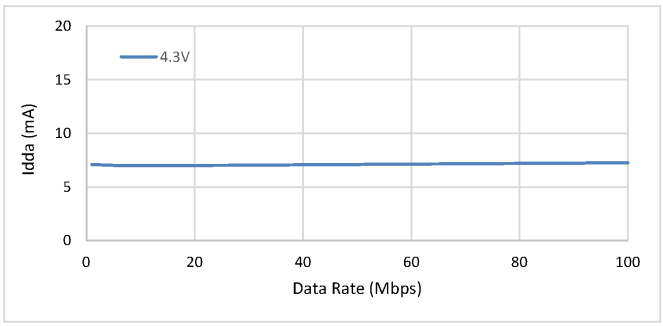


**Figure 11. Si88620 Typical $V_{DDA}$ Supply Current vs. Data Rate Using $V_{REGA}$ (4.3 V)**

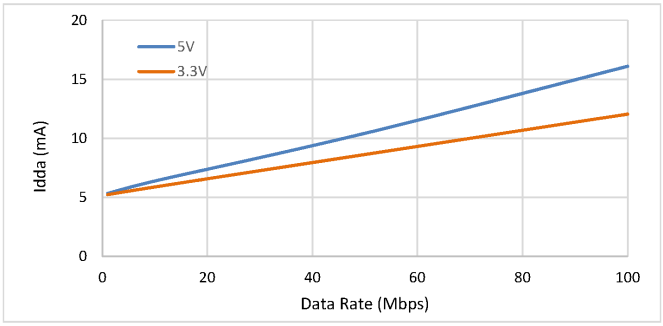


**Figure 12. Si88620 Typical $V_{DDB}$ Supply Current vs. Data Rate (5 V and 3.3 V Operation)**

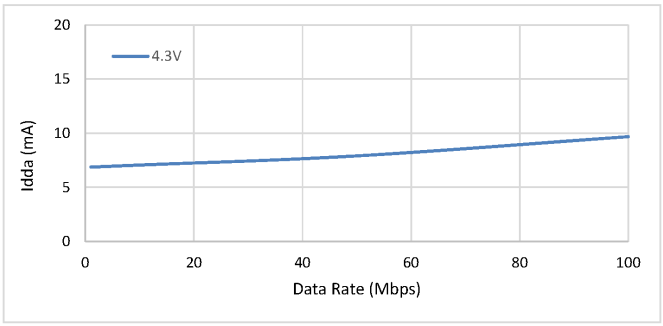


**Figure 13. Si88621 Typical $V_{DDA}$ Supply Current vs. Data Rate Using $V_{REGA}$ (4.3 V)**

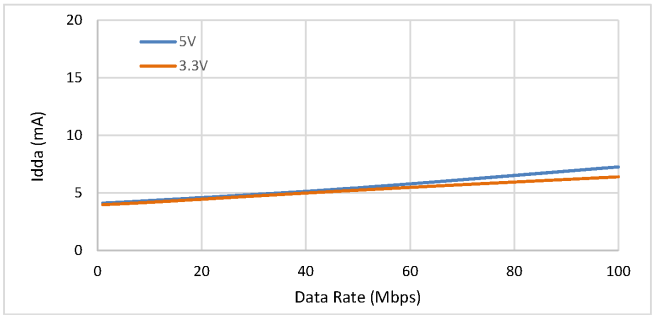


**Figure 14. Si88621 Typical $V_{DDB}$ Supply Current vs. Data Rate (5 V and 3.3 V Operation)**

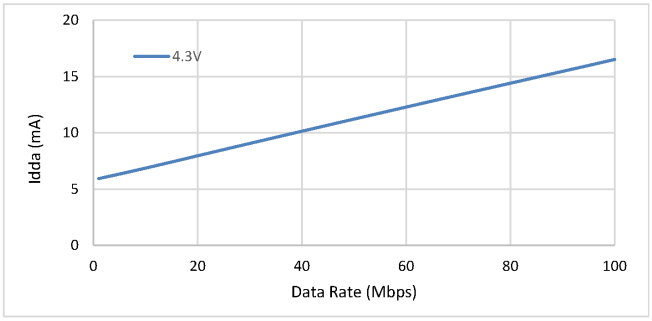


**Figure 15. Si88622 Typical $V_{DDA}$ Supply Current vs. Data Rate Using $V_{REGA}$ (4.3 V)**

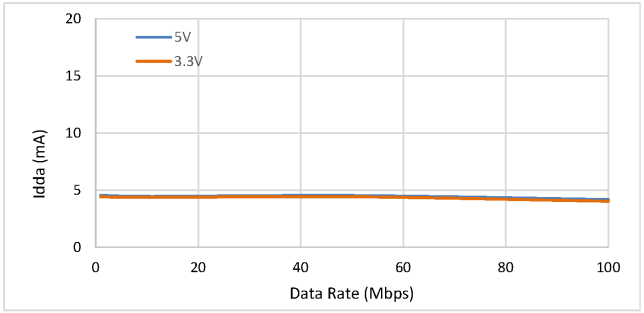


**Figure 16. Si88622 Typical $V_{DDB}$ Supply Current vs. Data Rate (5 V and 3.3 V Operation)**

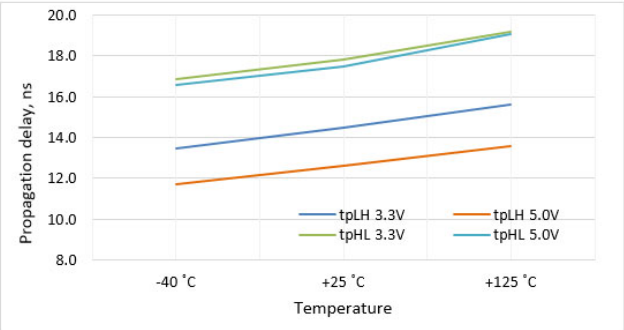


**Figure 17. Propagation Delay vs. Temperature**

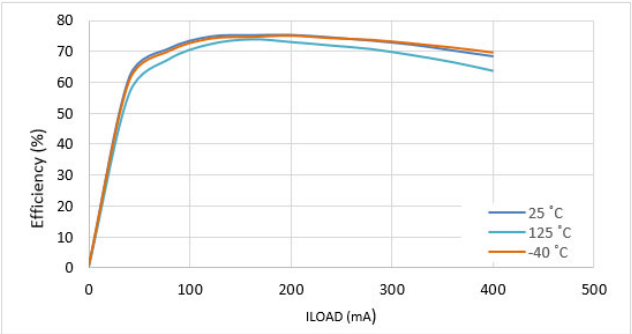


**Figure 18. DC-DC Efficiency vs. Load Current over Temperature (3.3 V to 3.3 V)**

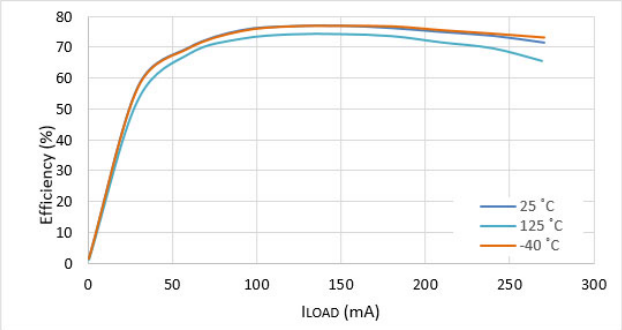


**Figure 19. DC-DC Efficiency vs. Load Current over Temperature (3.3 V to 5.0 V)**

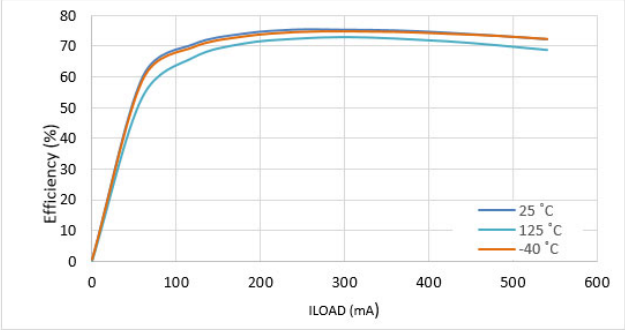


**Figure 20. DC-DC Efficiency vs. Load Current over Temperature (5.0 V to 3.3 V)**

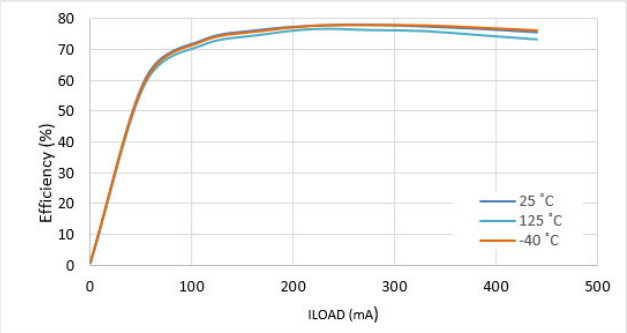


**Figure 21. DC-DC Efficiency vs. Load Current over Temperature (5.0 V to 5.0 V)**

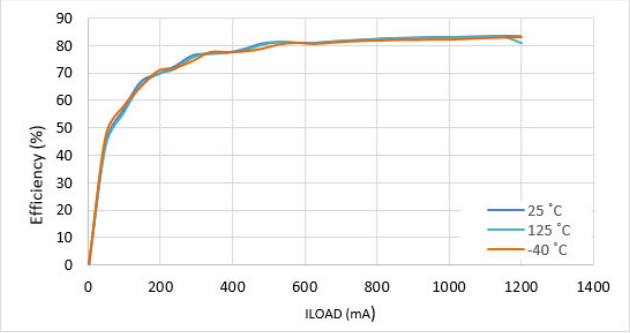


**Figure 22. DC-DC Efficiency vs. Load Current over Temperature (24 V to 5 V)**

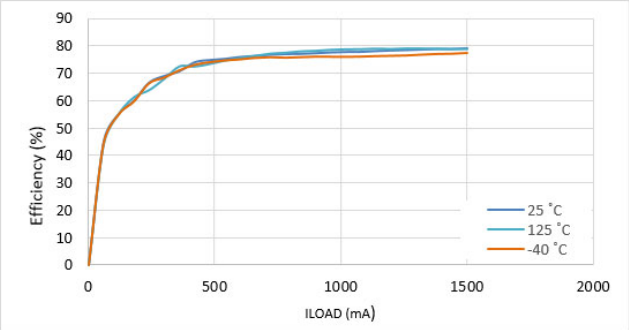


**Figure 23. DC-DC Efficiency vs. Load Current over Temperature (24 V to 3.3 V)**

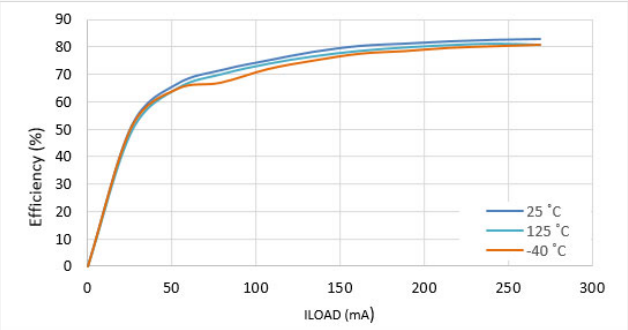


**Figure 24. DC-DC Efficiency vs. Load Current over Temperature (12 V to 5 V)**

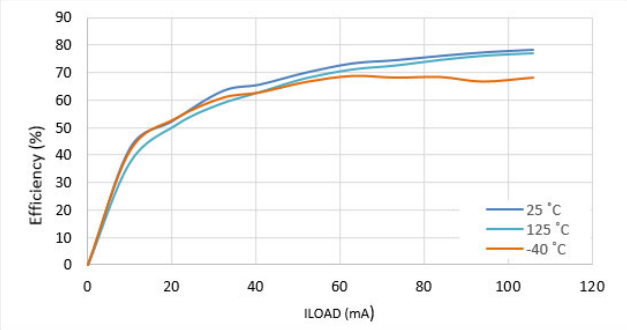


**Figure 25. DC-DC Efficiency vs. Load Current over Temperature (7 V to 24 V)**

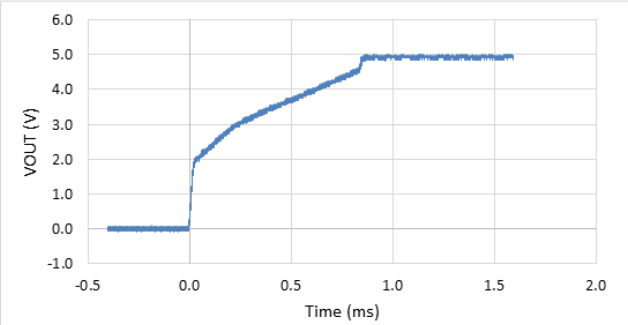


**Figure 26. DC-DC 24 V to 5 V VOUT Startup vs.Time, No Load Current**

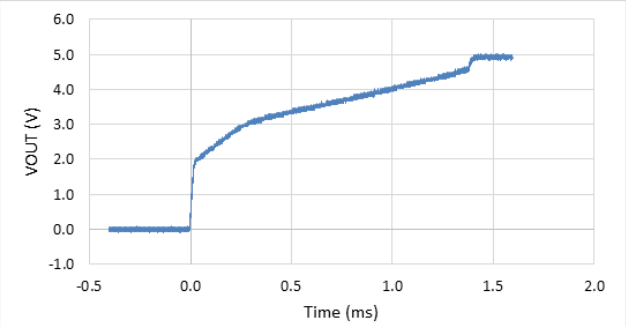


**Figure 27. DC-DC 24 V to 5 V VOUT Startup vs.Time, 50 mA Load Current**

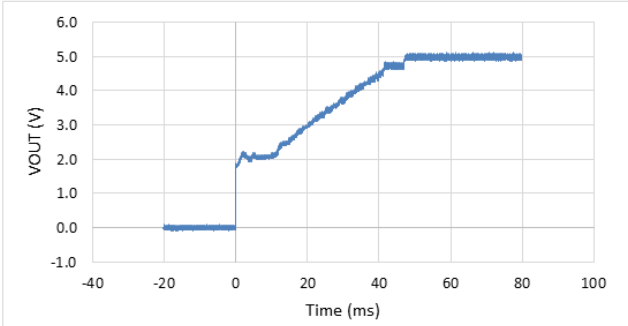


**Figure 28. DC-DC 24 V to 5 V VOUT Startup vs.Time, 400 mA Load Current**

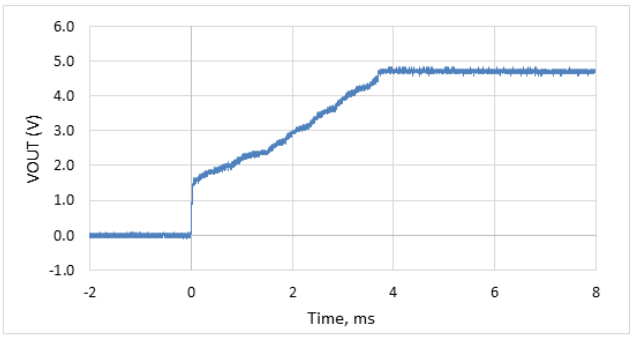


Figure 29. DC-DC 5 V to 5 V VOUT Startup vs.Time (No Load)

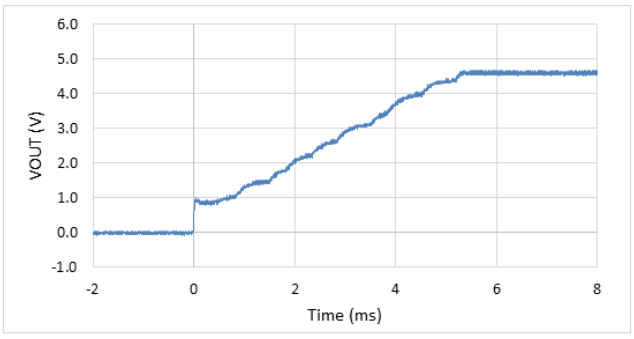


Figure 30. DC-DC 5 V to 5 V VOUT Startup vs.Time (50 mA Load Current)

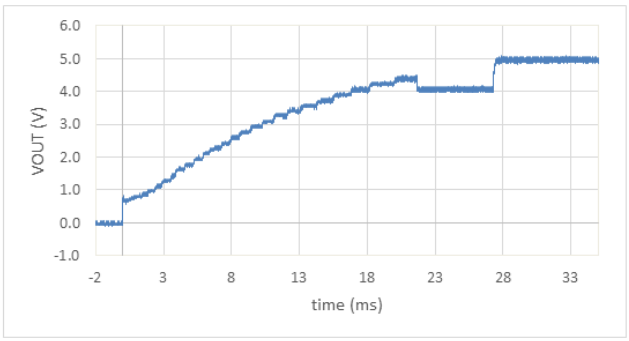


Figure 31. DC-DC 5 V to 5 V VOUT Startup vs.Time (400 mA Load Current)

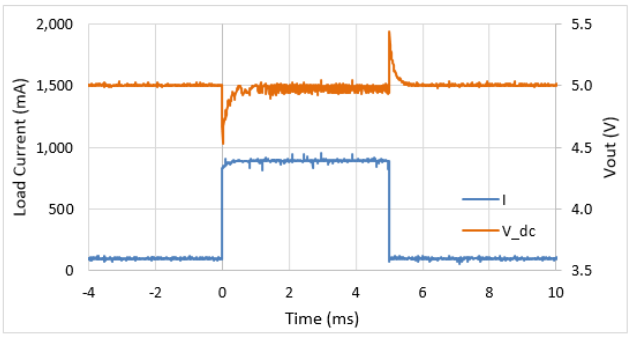


Figure 32. DC-DC 24 V to 5 V VOUT Load Transient Response (10% to 90% Load)

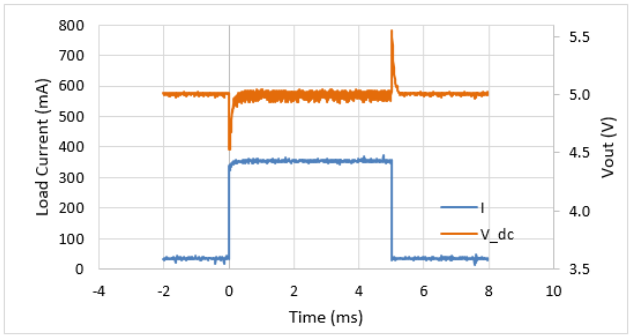


Figure 33. DC-DC 5 V to 5 V VOUT Load Transient Response (10% to 90% Load)

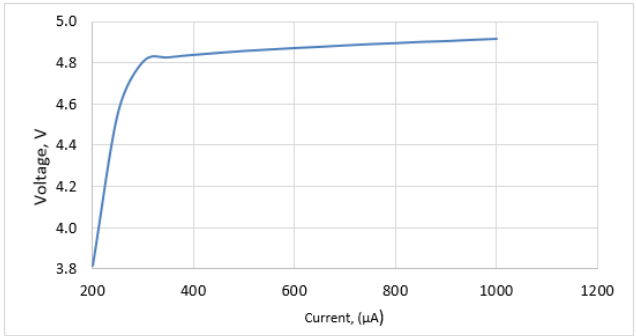


Figure 34. Typical I-V Curve for $V_{REGA}/V_{REGB}$

# 4. Electrical Specifications

**Table 4. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Storage temperature | $T_{STG}$ | –65 | +150 | °C |
| Junction temperature | $T_J$ | — | +150 | °C |
| Input-side Supply Voltage | VDDA<br>VDDP | –0.6 | 6.0 | V |
| Output supply | VDDB | –0.6 | 6.0 | V |
| Voltage on any pin with respect to ground | $V_{IN}$ | –0.5 | VDD + 0.5 | V |
| Output drive current per channel | $I_O$ | | 10 | mA |
| Input current for $V_{REGA}$, $V_{REGB}$ | $I_{REG}$ | — | 1 | mA |
| Lead solder temperature (10 s) | | — | 260 | °C |
| ESD per AEC-Q100 | HBM | — | 4 | kV |
| | CDM | — | 2 | kV |

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.

**Table 5. Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | –40 | 25 | 125 | °C |
| Power Input Voltage | VDDP | 3.0 | — | 5.5 | V |
| Supply Voltage | VDDA | 3.0 | — | 5.5 | V |
| | VDDB | 3.0 | — | 5.5 | V |

**Table 6. Electrical Characteristics[1]**

**$V_{IN}$ = 24 V; VDDA = VDDP = 3.0 to 5.5 V (see Figure 36) for all Si8822x/32x; VDDA = 4.3 V (see Figure 37) for all Si8842x/62x; $T_A$ = –40 to 125 °C unless otherwise noted**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DC/DC Converter** | | | | | | |
| Switching Frequency Si8822x, Si8842x | FSW | — | 225 | 250 | 275 | kHz |
| Switching Frequency Si8832x, Si8862x | FSW | $R_{FSW}$ = 23.3 kΩ<br>FSW = 1025.5/(RFSW x CSS)<br><br>CSS = 220 nF<br>(see Figure 9, "Si886xx Block Diagram: 24 V Input to 5 V Output," on page 13)<br>(1% tolerance on BOM) | 180 | 200 | 220 | kHz |
| | | $R_{FSW}$ = 9.3 kΩ<br>FSW = 1025.5/(RFSW x CSS)<br><br>CSS = 220 nF<br>(see Figure 9, "Si886xx Block Diagram: 24 V Input to 5 V Output," on page 13)<br>(1% tolerance on BOM) | 450 | 500 | 550 | kHz |
| | | $R_{FSW}$ = 5.18 kΩ,<br><br>CSS = 220 nF<br>(see Figure 9, "Si886xx Block Diagram: 24 V Input to 5 V Output," on page 13) | 810 | 900 | 990 | kHz |
| VSNS voltage | VSNS | $I_{LOAD}$ = 0 A | 1.002 | 1.05 | 1.097 | V |
| VSNS current offset | $I_{offset}$ | | –500 | — | 500 | nA |
| Output Voltage Accuracy[2] | — | See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28<br>$I_{LOAD}$ = 0 mA | –5 | — | +5 | % |
| Line Regulation | ΔVOUT(line)/ ΔVDDP | See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28<br>$I_{LOAD}$ = 50 mA<br>VDDP varies from 4.5 to 5.5 V | — | 1 | — | mV/V |
| Load Regulation | ΔVOUT(load)/ VOUT | See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28<br>$I_{LOAD}$ = 50 to 400 mA | — | 0.1 | — | % |
| Output Voltage Ripple Si8822x, Si8832x Si8842x, Si8862x | — | $I_{LOAD}$ = 100 mA<br>See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28<br>See Figure 37, "Measurement Circuit for Converter Efficiency and Regulation for Si884xx, Si886xx," on page 28 | — | 100 | — | mV p-p |
| Turn-on overshoot | ΔVOUT(start) | See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28<br>$C_{IN}$ = $C_{OUT}$ = 0.1 µF in parallel with 10 µF, $I_{LOAD}$ = 0 A | — | 2 | — | % |

**Table 6. Electrical Characteristics[1] (Continued)**
**$V_{IN}$ = 24 V; VDDA = VDDP = 3.0 to 5.5 V (see Figure 36) for all Si8822x/32x; VDDA = 4.3 V (see Figure 37) for all Si8842x/62x; $T_A$ = –40 to 125 °C unless otherwise noted**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Continuous Output Current | | | | | | |
| Si8822x, Si8832x | | | | | | |
| 5.0 V to 5.0 V | | | — | 400 | — | |
| 3.3 V to 3.3 V | | See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28 | — | 400 | — | |
| 3.3 V to 5.0 V | $I_{LOAD}$ (max) | | — | 250 | — | mA |
| 5.0 V to 3.3 V | | | — | 550 | — | |
| Si8842x, Si8862x | | | | | | |
| 24.0 to 5.0 V | | | — | 1000 | — | |
| 24.0 to 3.3 V | | | — | 1500 | — | |
| Cycle-by-cycle average current limit Si8822x, Si8832x | $I_{LIM}$ | See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28 Output short circuited | — | 3 | — | A |
| No Load Supply Current IDDP Si8822x, Si8832x | $I_{DDPQ_DCDC}$[3] | See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28 VDDP = VDDA = 5 V | — | 30 | — | mA |
| No Load Supply Current IDDA Si8822x, Si8832x | $I_{DDAQ_DCDC}$[4] | See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28 VDDP = VDDA = 5 V | — | 5.7 | — | mA |
| No Load Supply Current IDDP Si8842x, Si8862x | $I_{DDPQ_DCDC}$[3] | See Figure 37, "Measurement Circuit for Converter Efficiency and Regulation for Si884xx, Si886xx," on page 28 $V_{IN}$ = 24 V | — | 0.8 | — | mA |
| No Load Supply Current IDDA Si8842x, Si8862x | $I_{DDAQ_DCDC}$[4] | See Figure 37, "Measurement Circuit for Converter Efficiency and Regulation for Si884xx, Si886xx," on page 28 $V_{IN}$ = 24 V | — | 5.8 | — | mA |
| Peak Efficiency | | | | | | |
| Si8822x, Si8832x | η | See Figure 36, "Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx," on page 28 | — | 78 | — | % |
| Si8842x, Si8862x | | See Figure 37, "Measurement Circuit for Converter Efficiency and Regulation for Si884xx, Si886xx," on page 28 | — | 83 | — | |
| Voltage Regulator Reference Voltage Si8842x, Si8862x | $V_{REGA}$, $V_{REGB}$ | $I_{REG}$ = 600 µA See Figure 21, "DC-DC Efficiency vs. Load Current over Temperature (5.0 V to 5.0 V)," on page 19 for typical I–V curve | — | 4.8 | — | V |
| VREG tempco | $K_{TVREG}$ | — | — | –0.43 | — | mV/°C |
| VREG input current | $I_{REG}$ | — | 350 | — | 950 | µA |
| Soft start time, full load | | | | | | |
| Si8822x, Si8842x | $t_{SST}$ | See Figure 26, "DC-DC 24 V to 5 V VOUT Startup vs.Time, No Load Current," on page 20 through Figure 31, "DC-DC 5 V to 5 V VOUT Startup vs.Time (400 mA Load Current)," on page 21 for typical soft start times over load conditions. | — | 25 | — | ms |
| Si8832x, Si8862x | | | — | 50 | — | |
| Restart Delay from Over-Temperature Event | $t_{OTP}$ | — | — | 21 | — | s |

**Table 6. Electrical Characteristics[1] (Continued)**
**$V_{IN}$ = 24 V; VDDA = VDDP = 3.0 to 5.5 V (see Figure 36) for all Si8822x/32x; VDDA = 4.3 V (see Figure 37) for all Si8842x/62x; $T_A$ = –40 to 125 °C unless otherwise noted**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Digital Isolator** | | | | | | |
| VDD Undervoltage Threshold | $VDD_{UV+}$ | VDDA, VDDB rising | — | 2.7 | — | V |
| VDD Undervoltage Threshold | $VDD_{UV–}$ | VDDA, VDDB falling | — | 2.6 | — | V |
| VDD Undervoltage Hysteresis | $VDD_{HYS}$ | — | — | 100 | — | mV |
| Positive-Going Input Threshold | $V_{T+}$ | All inputs rising | — | 1.67 | — | V |
| Negative-Going Input Threshold | $V_{T–}$ | All inputs falling | — | 1.23 | — | V |
| Input Hysteresis | $V_{HYS}$ | — | — | 0.44 | — | V |
| High Level Input Voltage | $V_{IH}$ | — | 2.0 | — | — | V |
| Low Level Input Voltage | $V_{IL}$ | — | — | — | 0.8 | V |
| High Level Output Voltage | $V_{OH}$ | $I_{OH}$ = –4 mA | $V_{DDA}$,?$V_{DDB}$ – 0.4 | — | — | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 4 mA | — | — | 0.4 | V |
| Input Leakage Current | $I_L$ | — | — | — | ±10 | µA |
| Output Impedance[5] | $Z_O$ | — | — | 50 | — | Ω |
| **Supply Current, $C_{LOAD}$ = 15 pF** | | | | | | |
| **DC, VDDx = 3.3 V ±10%** | | | | | | |
| **Si88x20ED** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 4.2 | 7.2 | 10.2 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 2.5 | 4.5 | 6.5 | |
| $I_{DDA}$ | — | All inputs = 1 | 1.8 | 4.8 | 7.8 | |
| $I_{DDB}$ | — | All inputs = 1 | 2.0 | 4.0 | 6.0 | |
| **Si88x21ED** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 2.7 | 5.7 | 8.7 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 3.9 | 5.9 | 7.9 | |
| $I_{DDA}$ | — | All inputs = 1 | 1.8 | 4.8 | 7.8 | |
| $I_{DDB}$ | — | All inputs = 1 | 2.0 | 4.0 | 6.0 | |
| **Si88x22ED** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 0.8 | 3.8 | 6.8 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 5.3 | 7.3 | 9.3 | |
| $I_{DDA}$ | — | All inputs = 1 | 1.8 | 4.8 | 7.8 | |
| $I_{DDB}$ | — | All inputs = 1 | 2.0 | 4.0 | 6.0 | |
| **Si88x20BD** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 1.8 | 4.8 | 7.8 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 2.0 | 4.0 | 6.0 | |
| $I_{DDA}$ | — | All inputs = 1 | 4.2 | 7.2 | 10.2 | |
| $I_{DDB}$ | — | All inputs = 1 | 2.5 | 4.5 | 6.5 | |
| **Si88x21BD** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 1.8 | 4.8 | 7.8 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 2.0 | 4.0 | 6.0 | |
| $I_{DDA}$ | — | All inputs = 1 | 2.7 | 5.7 | 8.7 | |
| $I_{DDB}$ | — | All inputs = 1 | 3.9 | 5.9 | 7.9 | |
| **Si88x22BD** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 1.8 | 4.8 | 7.8 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 2.0 | 4.0 | 6.0 | |
| $I_{DDA}$ | — | All inputs = 1 | 0.8 | 3.8 | 6.8 | |
| $I_{DDB}$ | — | All inputs = 1 | 5.3 | 7.3 | 9.3 | |

**Table 6. Electrical Characteristics[1] (Continued)**
**$V_{IN}$ = 24 V; VDDA = VDDP = 3.0 to 5.5 V (see Figure 36) for all Si8822x/32x; VDDA = 4.3 V (see Figure 37) for all Si8842x/62x; $T_A$ = –40 to 125 °C unless otherwise noted**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DC, VDDx = 5 V ± 10%** | | | | | | |
| **Si88x20ED** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 6.5 | 9.5 | 12.5 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 2.5 | 4.5 | 6.5 | |
| $I_{DDA}$ | — | All inputs = 1 | 3.0 | 6.0 | 9.0 | |
| $I_{DDB}$ | — | All inputs = 1 | 2.0 | 4.0 | 6.0 | |
| **Si88x21ED** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 5.0 | 8.0 | 11.0 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 4.0 | 6.0 | 8.0 | |
| $I_{DDA}$ | — | All inputs = 1 | 3.0 | 6.0 | 9.0 | |
| $I_{DDB}$ | — | All inputs = 1 | 2.0 | 4.0 | 6.0 | |
| **Si88x22ED** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 3.5 | 6.5 | 9.5 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 5.5 | 7.5 | 9.5 | |
| $I_{DDA}$ | — | All inputs = 1 | 3.0 | 6.0 | 9.0 | |
| $I_{DDB}$ | — | All inputs = 1 | 2.0 | 4.0 | 6.0 | |
| **Si88x20BD** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 3.0 | 6.0 | 9.0 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 2.0 | 4.0 | 6.0 | |
| $I_{DDA}$ | — | All inputs = 1 | 6.5 | 9.5 | 12.5 | |
| $I_{DDB}$ | — | All inputs = 1 | 2.5 | 4.5 | 6.5 | |
| **Si88x21BD** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 3.0 | 6.0 | 9.0 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 2.0 | 4.0 | 6.0 | |
| $I_{DDA}$ | — | All inputs = 1 | 5.0 | 8.0 | 11.0 | |
| $I_{DDB}$ | — | All inputs = 1 | 4.0 | 6.0 | 8.0 | |
| **Si88x22BD** | | | | | | |
| $I_{DDA}$ | — | All inputs = 0 | 3.0 | 6.0 | 9.0 | mA |
| $I_{DDB}$ | — | All inputs = 0 | 2.0 | 4.0 | 6.0 | |
| $I_{DDA}$ | — | All inputs = 1 | 3.5 | 6.5 | 9.5 | |
| $I_{DDB}$ | — | All inputs = 1 | 5.5 | 7.5 | 9.5 | |
| **NOTE:** For calculating total current, including the dynamic component, see “4.2. Calculating Total Current Consumption” on page 33. | | | | | | |
| **Timing Characteristics** | | | | | | |
| Data Rate | — | — | 0 | — | 100 | Mbps |
| Minimum Pulse Width | — | — | 10 | — | — | ns |
| Propagation Delay | $t_{PHL}$ | See Figure 35, “Propagation Delay Timing for Digital Channels,” on page 27 VDDx = 3.3 V | 12.0 | 17.0 | 22.0 | ns |
| Propagation Delay | $t_{PLH}$ | See Figure 35, “Propagation Delay Timing for Digital Channels,” on page 27 VDDx = 3.3 V | 11.0 | 15.0 | 20.0 | ns |
| Propagation Delay | $t_{PHL}$ | See Figure 35, “Propagation Delay Timing for Digital Channels,” on page 27 VDDx = 5.0 V | 13.0 | 18.0 | 23.0 | ns |
| Propagation Delay | $t_{PLH}$ | See Figure 35, “Propagation Delay Timing for Digital Channels,” on page 27 VDDx = 5.0 V | 10.0 | 13.0 | 18.0 | ns |

**Table 6. Electrical Characteristics[1] (Continued)**
**$V_{IN}$ = 24 V; VDDA = VDDP = 3.0 to 5.5 V (see Figure 36) for all Si8822x/32x; VDDA = 4.3 V (see Figure 37) for all Si8842x/62x; $T_A$ = –40 to 125 °C unless otherwise noted**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$ | PWD | See Figure 35, "Propagation Delay Timing for Digital Channels," on page 27 VDDx = 3.3 V | — | 2.5 | 5.0 | ns |
| Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$ | PWD | See Figure 35, "Propagation Delay Timing for Digital Channels," on page 27 VDDx = 5.0 V | — | 4.5 | 7.0 | ns |
| Propagation Delay Skew[6] | $t_{PSK(P-P)}$ | — | — | 3.0 | 10.0 | ns |
| Channel-Channel Skew | $t_{PSK}$ | — | — | 2.0 | 4.0 | ns |
| Output Rise Time | $t_r$ | $C_L$ = 15 pF | — | 2.5 | — | ns |
| Output Fall Time | $t_f$ | $C_L$ = 15 pF | — | 2.5 | — | ns |
| Common Mode? Transient Immunity | CMTI | $V_I$ = VDDx or 0 V $V_{CM}$ = 1500 V See Figure 38, "Common-Mode Transient Immunity Test Circuit," on page 29 | 40 | 100 | — | kV/µs |
| Startup Time[7] | $t_{SU}$ | — | — | 55 | — | µs |

1. Over recommended operating conditions as noted in Table 5, "Recommended Operating Conditions," on page 22.
2. $V_{OUT} = V_{SNS}$ x (1 + R1/R2) + R1 x $I_{offset}$
3. $V_{DDP}$ current needed for dc-dc circuits.
4. $V_{DDA}$ current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from when the UVLO threshold is exceeded to valid data at the output.

***ESD Handling:*** *Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

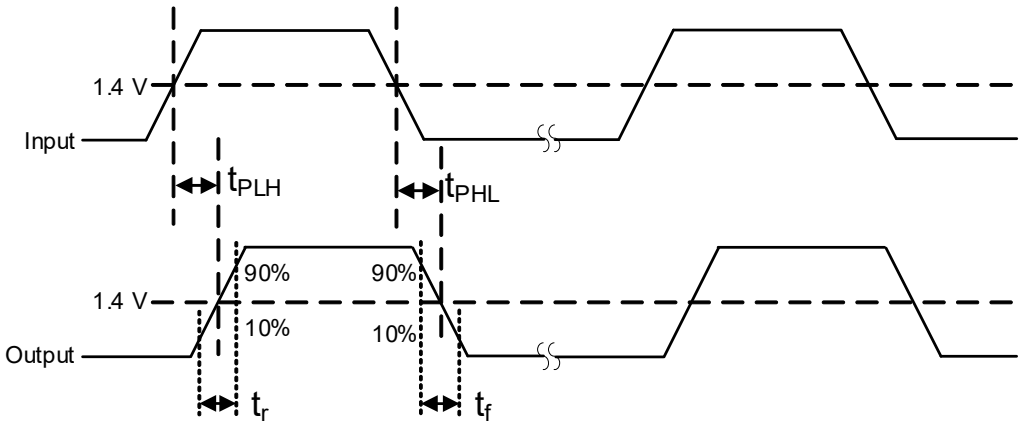


**Figure 35. Propagation Delay Timing for Digital Channels**

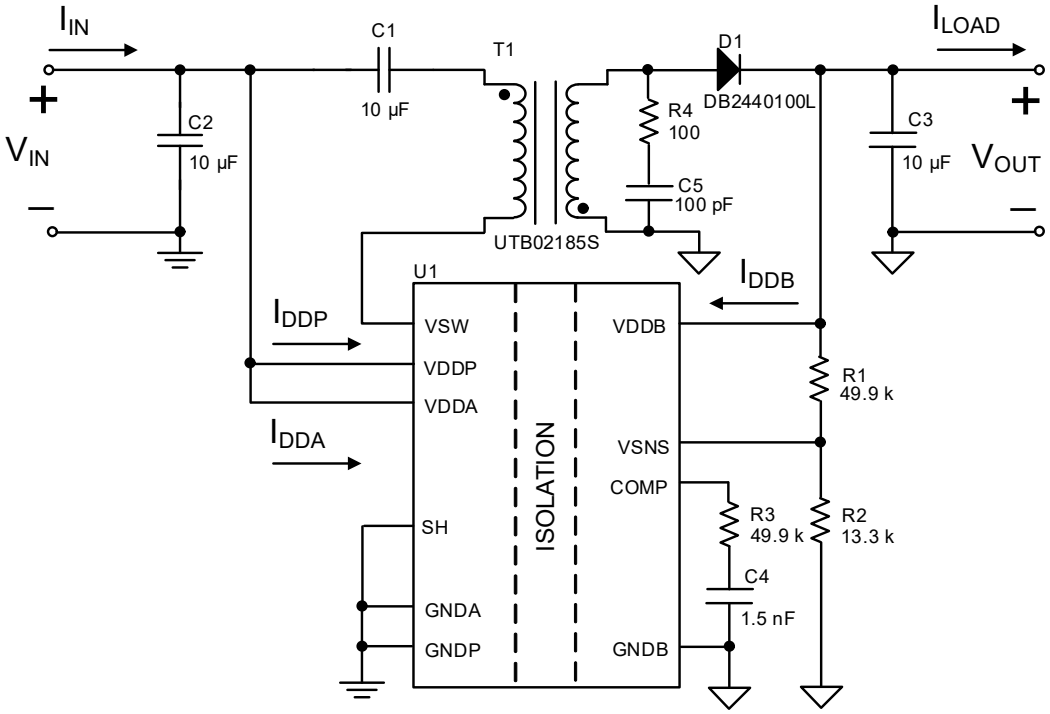


**Figure 36. Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx**

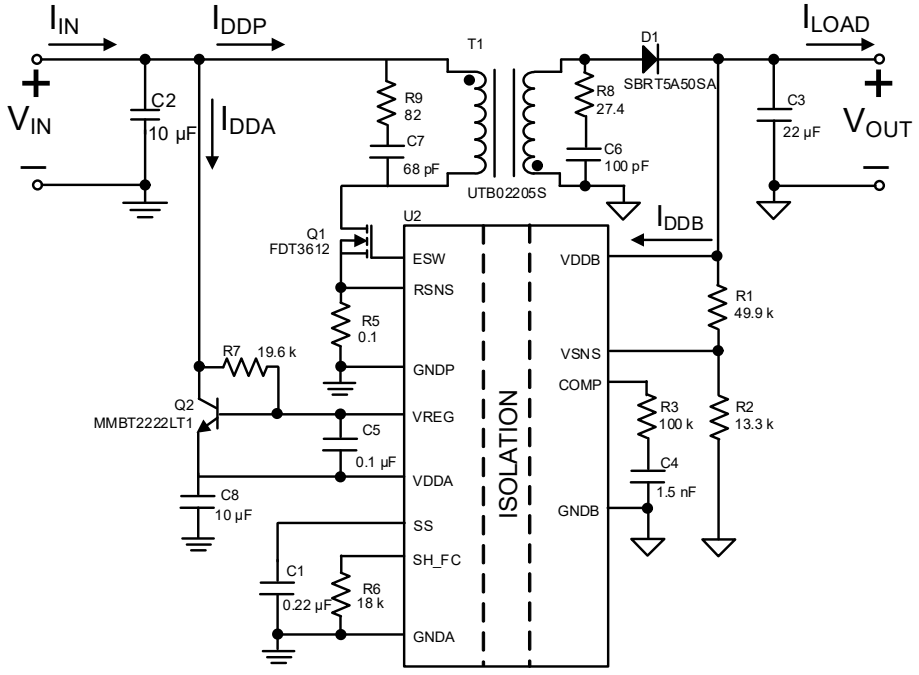


**Figure 37. Measurement Circuit for Converter Efficiency and Regulation for Si884xx, Si886xx**

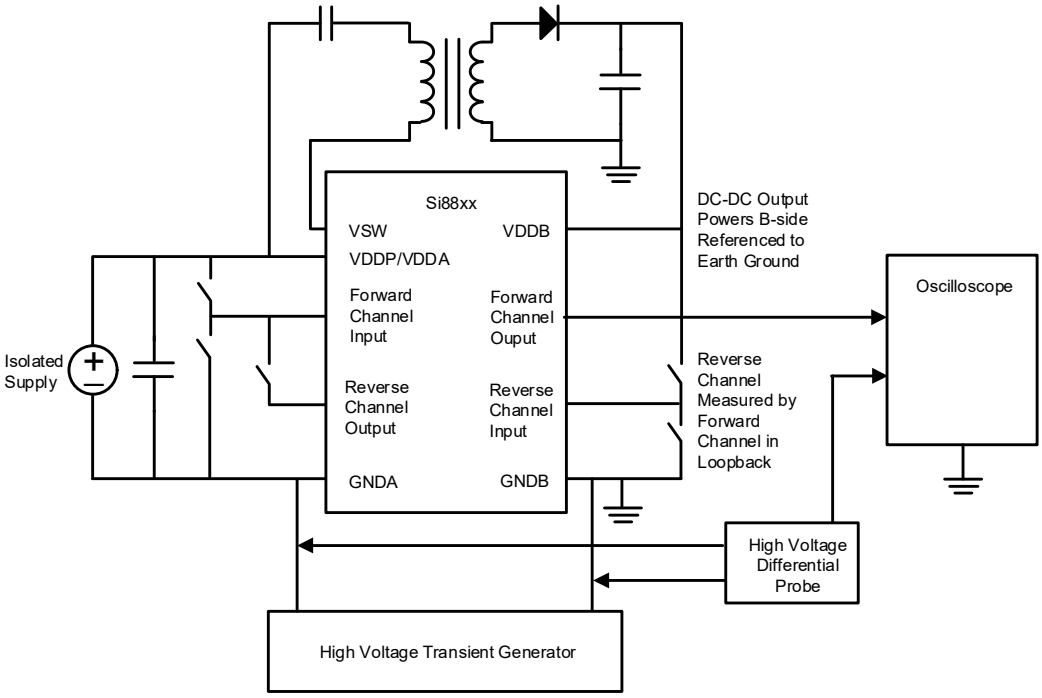


**Figure 38. Common-Mode Transient Immunity Test Circuit**

## 4.1. Safety Certifications and Specifications

**Table 7. Regulatory Information (Pending)[1]**

| |
|---|
| **CSA** |
| The Si88xx is certified under CSA. For more details, see Master Contract Number 232873. |
| 62368-1: Up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| **VDE** |
| The Si88xx is certified under VDE. For more details, see File 5028467. |
| 60747-17: Up to 1414 Vpeak for basic insulation working voltage. |
| 62368-1: Conforms to standard. See statement of conformity. |
| **UL** |
| The Si88xx is certified under UL1577 component recognition program. For more details, see File E257455. |
| Rated up to 5000 $V_{RMS}$ $V_{ISO}$ isolation voltage for basic protection. |
| **CQC** |
| The Si88xx is certified under GB4943.1. |
| Rated up to 250 $V_{RMS}$ reinforced insulation working voltage at 5000 meters tropical climate. |

1. For more information, see "8. Ordering Guide" on page 40

**Table 8. Insulation and Safety-Related Specifications**

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| | | | WB SOIC-16, WB SOIC-20 | |
| Nominal External Air Gap (Clearance) | CLR | | 7.6 | mm |
| Nominal External Tracking (Creepage) | CRP | | 7.6 | mm |
| Minimum Internal Gap (Internal Clearance) | DTI | | 0.016 | mm |
| Tracking Resistance | PTI or CTI | IEC60112 | 600 | $V_{RMS}$ |
| Erosion Depth | ED | | 0.019 | mm |
| Resistance (Input-Output)[1] | $R_{IO}$ | Test voltage = 500 V, 25°C | $10^{12}$ | Ω |
| Capacitance (Input-Output)[1] | $C_{IO}$ | f = 1 MHz | 1.4 | pF |
| Input Capacitance[2] | $C_I$ | | 4.0 | pF |

1. To determine resistance and capacitance, the Si88xx is converted into a 2-terminal device. All pins on input side are shorted together to form the first terminal, and similarly, all pins on the output side are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input to ground.

**Table 9. IEC 60664-1 Ratings**

| Parameter | Test Condition | Specification |
|---|---|---|
| | | WB SOIC-16, WB SOIC-20 |
| Material Group | | I |
| Overvoltage Category | Rated Mains Voltage ≤ 150 $V_{RMS}$ | I-IV |
| | Rated Mains Voltage ≤ 300 $V_{RMS}$ | I-IV |
| | Rated Mains Voltage ≤ 600 $V_{RMS}$ | I-III |
| | Rated Mains Voltage ≤ 1000 $V_{RMS}$ | I-II |

**Table 10. IEC60747-17 Insulation Characteristics[1]**

| Parameter | Symbol | Test Condition | Characteristic | Unit |
|---|---|---|---|---|
| | | | WB SOIC-16, WB SOIC-20 | |
| Maximum Working Isolation Voltage | $V_{IOWM}$ | According to Time-Dependent Dielectric Breakdown (TDDB) Test | 1000 | $V_{RMS}$ |
| Maximum Repetitive Isolation Voltage | $V_{IORM}$ | According to Time-Dependent Dielectric Breakdown (TDDB) Test | 1414 | $V_{peak}$ |
| Apparent charge | $q_{pd}$ | Method b: At routine test (100% production) and preconditioning (type test); $V_{ini}$ = 1.2 x $V_{IOTM}$, tini = 1 s; $V_{pd(m)}$ = 1.875 x $V_{IORM}$, tm = 1 s (method b1) or $V_{pd(m)}$ = $V_{ini}$, tm = tini (method b2) | ≤ 5 | pC |
| Maximum Transient Isolation Voltage | $V_{IOTM}$ | $V_{TEST}$ = $V_{IOTM}$, t = 60 s (qualification); $V_{TEST}$ = 1.2 x $V_{IOTM}$, t = 1 s (100% production) | C = 5302<br>D = 7070 | $V_{peak}$ |
| Maximum Surge Isolation Voltage | $V_{IOSM}$ | Tested in oil with 1.3 x $V_{IMP}$ and 1.2 µs/50 µs profile | 8000 | $V_{peak}$ |
| Maximum Impulse Voltage | $V_{IMP}$ | Tested in air with 1.2 µs/50 µs profile | 6150 | $V_{peak}$ |
| Isolation Resistance | $R_{IO_S}$ | $T_{AMB}$ = $T_S$, $V_{IO}$ = 500 V | $>10^9$ | Ω |
| Pollution Degree | | | 2 | |
| Climatic category | | | 40/125/21 | |

1. This coupler is suitable for “basic electrical insulation” only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

**Table 11. UL 1577 Insulation Characteristics**

| Parameter | Symbol | Test Condition | Characteristic | Unit |
|---|---|---|---|---|
| Maximum withstanding isolation voltage | $V_{ISO}$ | $V_{TEST}$ = $V_{ISO}$, t = 60 s (qualification); $V_{TEST}$ = 1.2 x $V_{ISO}$, t = 1 s (100% production) | C = 3750<br>D = 5000 | $V_{RMS}$ |

**Table 12. IEC60747-17 Safety Limiting Values[1]**

| Parameter | Symbol | Test Condition | Max | Unit |
|---|---|---|---|---|
| | | | WB SOIC-16, WB SOIC-20 | |
| Safety temperature | $T_S$ | | 150 | °C |
| Safety input, output, or supply current | $I_S$ | $\theta_{JA}$ = 55 °C/W (WB SOIC-16 or SOIC-20), VDD = 5.5 V, $T_J$ = 150 °C, $T_A$ = 25 °C | 413 | mA |
| Safety input, output, or total power | $P_S$ | | 2.27 | W |

1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 39 on page 32.

**Table 13. Thermal Characteristics**

| Parameter | Symbol | WB SOIC-16, WB SOIC-20 | Unit |
|---|---|---|---|
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ | 55 | °C/W |

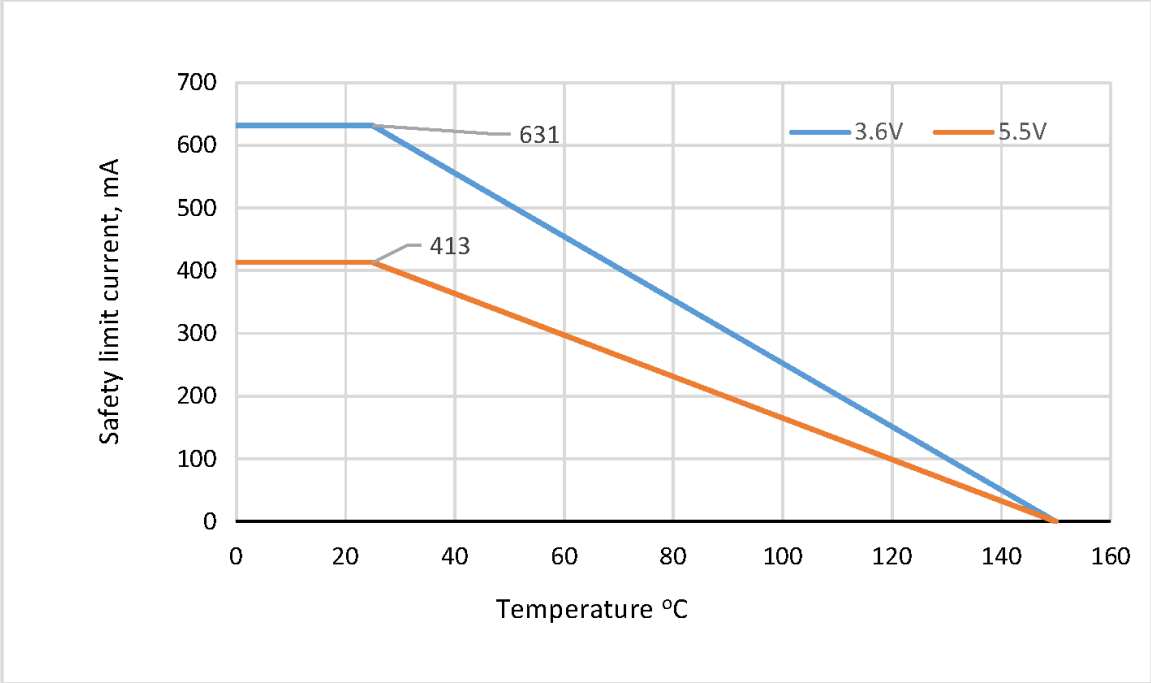


**Figure 39. WB SOIC-16/20 Thermal Derating Curve (Dependence of Safety Limiting Values)**

## 4.2. Calculating Total Current Consumption

Use the following guidelines to calculate dynamic supply current:

$$IDD(ac) = (C_L) \times (V) \times \left(\frac{D}{2}\right) \times 1E^{-3}$$

Where:
IDD(ac) is the dynamic component of current, per output channel, in mA.
D is the data-rate of that channel, in Mbps.
$C_L$ is the load capacitance connected to the output, in pF.
V is the VDD on the output side, in V.

**Equation 1.**

For example, for the Si88x21ED-IS, the total current can be calculated as follows:

The average dc IDDA/B is the average of the dc current values at input 0 and input 1, for VDDA and VDDB, respectively, as stated in the table below for Si88x21ED.

| CL (pF) | VDD (V) | Data-rate (MBps) | IDD(ac) per Output Channel (mA) | Total IDDA (ac) (mA) | Total IDDB (ac) (mA) | Average DC IDDA (mA) | Average DC IDDB (mA) | Total IDDA (mA) | Total IDDB (mA) |
|---|---|---|---|---|---|---|---|---|---|
| 20.00 | 5.00 | 10.00 | 0.50 | 0.50 | 0.50 | 8.25 | 6.95 | 8.75 | 7.45 |
| 20 | 3.3 | 100 | 3.30 | 3.30 | 3.30 | 8.25 | 6.95 | 11.55 | 10.25 |

# 5. Package Outlines

## 5.1. Package Outline: 16-Pin Wide-Body SOIC

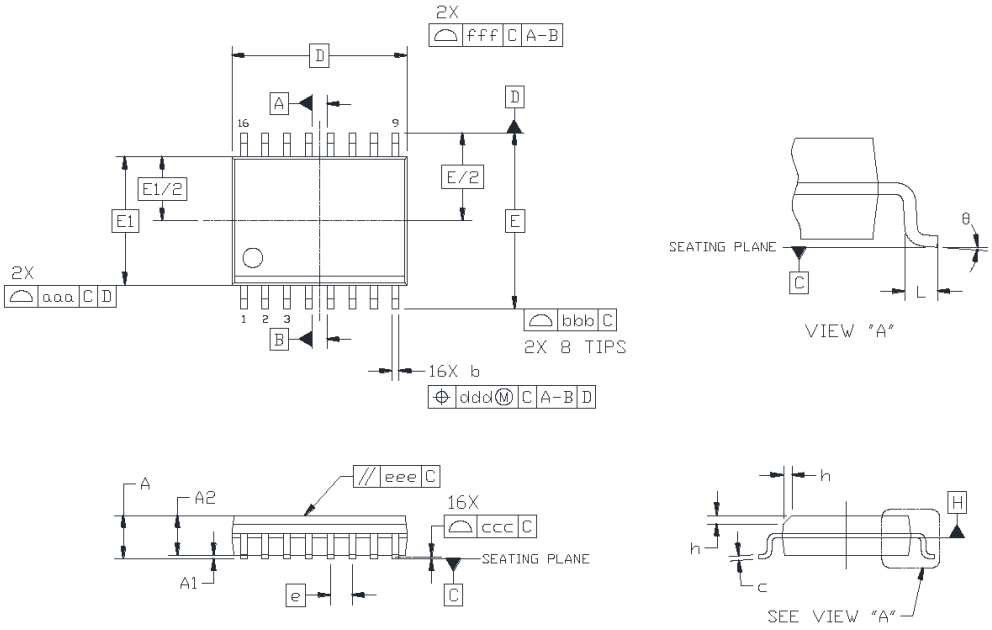


**Figure 40. 16-Pin Wide-Body SOIC Package Diagram**

**Table 14. 16-Pin Wide-Body SOIC Package Diagram Dimensions[1,2,3,4]**

| Dimension | Min | Max |
|---|---|---|
| A | — | 2.65 |
| A1 | 0.10 | 0.30 |
| A2 | 2.05 | — |
| b | 0.31 | 0.51 |
| c | 0.20 | 0.33 |
| D | 10.30 BSC | |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| h | 0.25 | 0.75 |
| θ | 0° | 8° |
| aaa | — | 0.10 |
| bbb | — | 0.33 |
| ccc | — | 0.10 |
| ddd | — | 0.25 |
| eee | — | 0.10 |
| fff | — | 0.20 |

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

## 5.2. Package Outline: 20-Pin Wide-Body SOIC

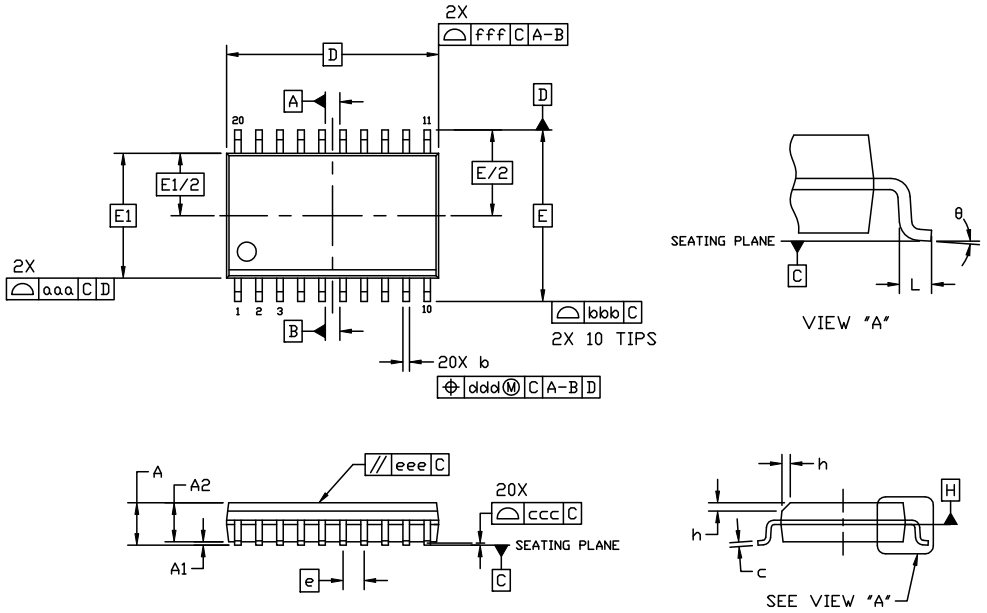


**Figure 41. 20-Pin Wide-Body SOIC Package Diagram**

**Table 15. 20-Pin Wide-Body SOIC Package Diagram Dimensions[1,2,3,4]**

| Dimension | Min | Max |
|---|---|---|
| A | — | 2.65 |
| A1 | 0.10 | 0.30 |
| A2 | 2.05 | — |
| b | 0.31 | 0.51 |
| c | 0.20 | 0.33 |
| D | 12.80 BSC | |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| h | 0.25 | 0.75 |
| θ | 0° | 8° |
| aaa | — | 0.10 |
| bbb | — | 0.33 |
| ccc | — | 0.10 |
| ddd | — | 0.25 |
| eee | — | 0.10 |
| fff | — | 0.20 |

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Drawing conforms to JEDEC Outline MS-013, Variation AC.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

# 6. Land Patterns

## 6.1. Land Pattern: 16-Pin Wide-Body SOIC

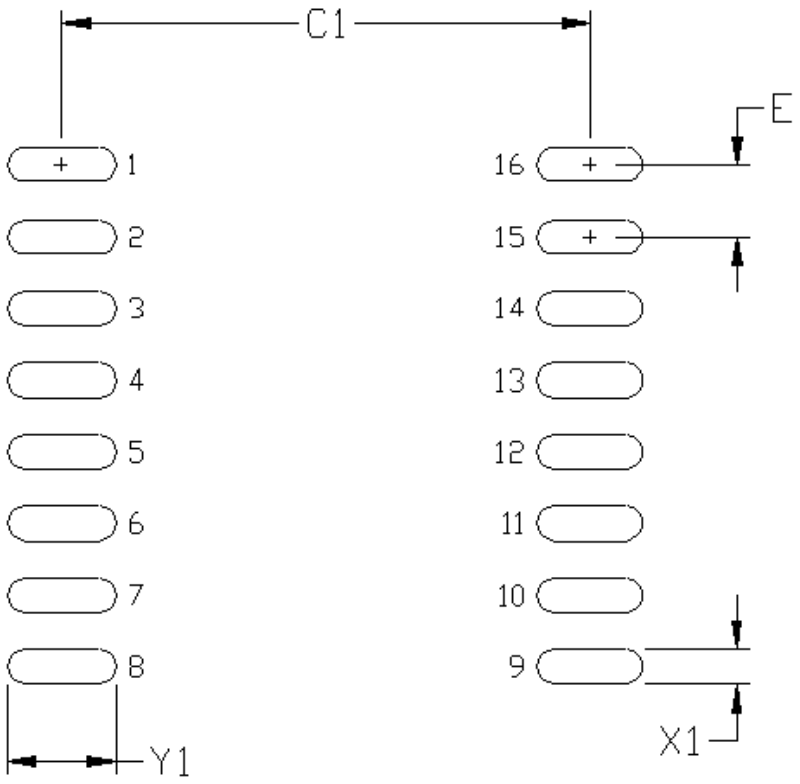


**Figure 42. 16-Pin Wide-Body SOIC Land Pattern Drawing**

**Table 16. 16-Pin Wide-Body SOIC Land Pattern Drawing Dimensions[1,2]**

| Dimension | Feature | (mm) |
|---|---|---|
| C1 | Pad Column Spacing | 9.40 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.90 |

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 6.2. Land Pattern: 20-Pin SOIC

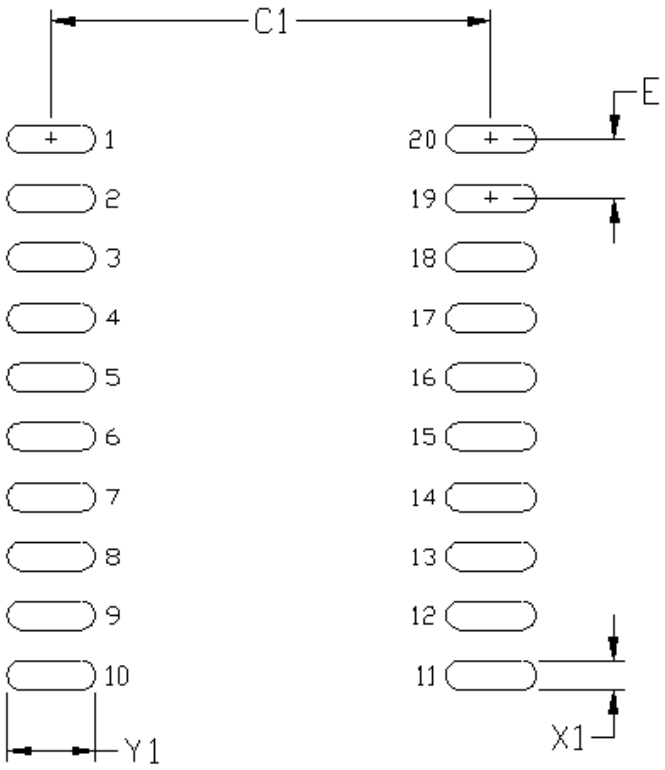


**Figure 43. 20-Pin SOIC PCB Land Pattern Drawing**

**Table 17. 20-Pin SOIC PCB Land Pattern Drawing Dimensions[1,2]**

| Dimension | mm |
|---|---|
| C1 | 9.40 |
| E | 1.27 |
| X1 | 0.60 |
| Y1 | 1.90 |

1. This Land Pattern Design is based on IPC-7351 design guidelines for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

# 7. Top Markings

## 7.1. Si88x2x Top Marking: 16-Pin Wide-Body SOIC

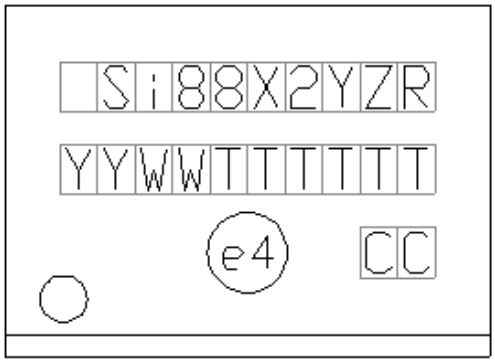


**Figure 44. 16-Pin Wide-Body SOIC Top Marking**

**Table 18. 16-Pin Wide-Body SOIC Top Marking Explanation**

| | | |
|---|---|---|
| **Line 1 Marking:** | Base Part Number<br>Ordering Options<br>See 8. Ordering Guide for more information. | Si88x2 = 5 kV rated 2 channel digital isolator with dc-dc converter<br>X = 2, 4<br>2 = dc-dc shutdown<br>4 = external FET<br>Y = Number of reverse channels<br>Z = E, B<br>E = default high<br>B = default low<br>R = C, D<br>C = 3.75 $kV_{RMS}$ isolation rating<br>D = 5 $kV_{RMS}$ isolation rating |
| **Line 2 Marking:** | YY = Year<br>WW = Workweek | Assigned by the Assembly House. Corresponds to the year and workweek of the mold date. |
| | TTTTTT = Mfg Code | Manufacturing Code from Assembly Purchase Order form. |
| **Line 3 Marking:** | Circle = 1.5 mm Diameter<br>(Center Justified) | “e4” Pb-Free Symbol |
| | Country of Origin<br>ISO Code Abbreviation | CC = Country Code |

## 7.2. Si88x2x Top Marking: 20-Pin Wide-Body SOIC

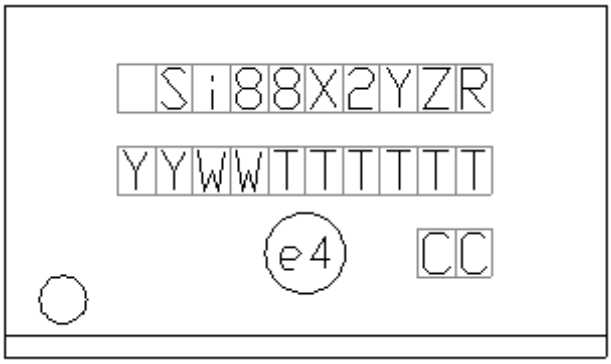


**Figure 45. 20-Pin Wide-Body SOIC Top Marking**

**Table 19. 20-Pin Wide-Body SOIC Top Marking Explanation**

| | | |
|---|---|---|
| **Line 1 Marking:** | Base Part Number<br>Ordering Options<br>See 8. Ordering Guide for more information. | Si88x2 = 5 kV rated 2-channel digital isolator with dc-dc converter<br>X = 3, 6<br>3 = Full-featured dc-dc with integrated FET<br>6 = full featured dc-dc with external FET<br>Y = Number of reverse channels<br>Z = E, B<br>E = default high<br>B = default low<br>R = C, D<br>C = 3.75 $kV_{RMS}$ isolation rating<br>D = 5 $kV_{RMS}$ isolation rating |
| **Line 2 Marking:** | YY = Year<br>WW = Workweek | Assigned by the Assembly House. Corresponds to the year and work-week of the mold date. |
| | TTTTTT = Mfg Code | Manufacturing Code from Assembly Purchase Order form. |
| **Line 3 Marking:** | Circle = 1.5 mm Diameter<br>(Center Justified) | “e4” Pb-Free Symbol |
| | Country of Origin<br>ISO Code Abbreviation | CC = Country Code |

# 8. Ordering Guide

## 8.1. Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an "-I" in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with AEC-Q100, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an "-A" in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

**Table 20. Si88x2x Ordering Guide[1,2,3,4]**

| Ordering Part Number (OPN) | Automotive Grade OPN[5,6] | Default Output[7] | DC-DC Shutdown | Soft Start | Frequency Control | External Switch | Forward Digital | Reverse Digital | Package |
|---|---|---|---|---|---|---|---|---|---|
| **3.75 $kV_{RMS}$ Insulation Rating** | | | | | | | | | |
| Si88220BC-IS | Si88220BC-AS | Low | Y | N | N | N | 2 | 0 | WB SOIC-16 |
| Si88221BC-IS | Si88221BC-AS | Low | Y | N | N | N | 1 | 1 | WB SOIC-16 |
| Si88222BC-IS | Si88222BC-AS | Low | Y | N | N | N | 0 | 2 | WB SOIC-16 |
| Si88320BC-IS | Si88320BC-AS | Low | Y | Y | Y | N | 2 | 0 | WB SOIC-20 |
| Si88321BC-IS | Si88321BC-AS | Low | Y | Y | Y | N | 1 | 1 | WB SOIC-20 |
| Si88322BC-IS | Si88322BC-AS | Low | Y | Y | Y | N | 0 | 2 | WB SOIC-20 |
| Si88420BC-IS | Si88420BC-AS | Low | N | N | N | Y | 2 | 0 | WB SOIC-16 |
| Si88421BC-IS | Si88421BC-AS | Low | N | N | N | Y | 1 | 1 | WB SOIC-16 |
| Si88422BC-IS | Si88422BC-AS | Low | N | N | N | Y | 0 | 2 | WB SOIC-16 |
| Si88620BC-IS | Si88620BC-AS | Low | Y | Y | Y | Y | 2 | 0 | WB SOIC-20 |
| Si88621BC-IS | Si88621BC-AS | Low | Y | Y | Y | Y | 1 | 1 | WB SOIC-20 |
| Si88622BC-IS | Si88622BC-AS | Low | Y | Y | Y | Y | 0 | 2 | WB SOIC-20 |
| Si88220EC-IS | Si88220EC-AS | High | Y | N | N | N | 2 | 0 | WB SOIC-16 |
| Si88221EC-IS | Si88221EC-AS | High | Y | N | N | N | 1 | 1 | WB SOIC-16 |
| Si88222EC-IS | Si88222EC-AS | High | Y | N | N | N | 0 | 2 | WB SOIC-16 |
| Si88320EC-IS | Si88320EC-AS | High | Y | Y | Y | N | 2 | 0 | WB SOIC-20 |
| Si88321EC-IS | Si88321EC-AS | High | Y | Y | Y | N | 1 | 1 | WB SOIC-20 |
| Si88322EC-IS | Si88322EC-AS | High | Y | Y | Y | N | 0 | 2 | WB SOIC-20 |
| Si88420EC-IS | Si88420EC-AS | High | N | N | N | Y | 2 | 0 | WB SOIC-16 |
| Si88421EC-IS | Si88421EC-AS | High | N | N | N | Y | 1 | 1 | WB SOIC-16 |
| Si88422EC-IS | Si88422EC-AS | High | N | N | N | Y | 0 | 2 | WB SOIC-16 |
| Si88620EC-IS | Si88620EC-AS | High | Y | Y | Y | Y | 2 | 0 | WB SOIC-20 |
| Si88621EC-IS | Si88621EC-AS | High | Y | Y | Y | Y | 1 | 1 | WB SOIC-20 |
| Si88622EC-IS | Si88622EC-AS | High | Y | Y | Y | Y | 0 | 2 | WB SOIC-20 |

**Table 20. Si88x2x Ordering Guide[1,2,3,4] (Continued)**

| Ordering Part Number (OPN) | Automotive Grade OPN[5,6] | Default Output[7] | DC-DC Shutdown | Soft Start | Frequency Control | External Switch | Forward Digital | Reverse Digital | Package |
|---|---|---|---|---|---|---|---|---|---|
| **5.0 $kV_{RMS}$ Insulation Rating** | | | | | | | | | |
| Si88220BD-IS | Si88220BD-AS | Low | Y | N | N | N | 2 | 0 | WB SOIC-16 |
| Si88221BD-IS | Si88221BD-AS | Low | Y | N | N | N | 1 | 1 | WB SOIC-16 |
| Si88222BD-IS | Si88222BD-AS | Low | Y | N | N | N | 0 | 2 | WB SOIC-16 |
| Si88320BD-IS | Si88320BD-AS | Low | Y | Y | Y | N | 2 | 0 | WB SOIC-20 |
| Si88321BD-IS | Si88321BD-AS | Low | Y | Y | Y | N | 1 | 1 | WB SOIC-20 |
| Si88322BD-IS | Si88322BD-AS | Low | Y | Y | Y | N | 0 | 2 | WB SOIC-20 |
| Si88420BD-IS | Si88420BD-AS | Low | N | N | N | Y | 2 | 0 | WB SOIC-16 |
| Si88421BD-IS | Si88421BD-AS | Low | N | N | N | Y | 1 | 1 | WB SOIC-16 |
| Si88422BD-IS | Si88422BD-AS | Low | N | N | N | Y | 0 | 2 | WB SOIC-16 |
| Si88620BD-IS | Si88620BD-AS | Low | Y | Y | Y | Y | 2 | 0 | WB SOIC-20 |
| Si88621BD-IS | Si88621BD-AS | Low | Y | Y | Y | Y | 1 | 1 | WB SOIC-20 |
| Si88622BD-IS | Si88622BD-AS | Low | Y | Y | Y | Y | 0 | 2 | WB SOIC-20 |
| Si88220ED-IS | Si88220ED-AS | High | Y | N | N | N | 2 | 0 | WB SOIC-16 |
| Si88221ED-IS | Si88221ED-AS | High | Y | N | N | N | 1 | 1 | WB SOIC-16 |
| Si88222ED-IS | Si88222ED-AS | High | Y | N | N | N | 0 | 2 | WB SOIC-16 |
| Si88320ED-IS | Si88320ED-AS | High | Y | Y | Y | N | 2 | 0 | WB SOIC-20 |
| Si88321ED-IS | Si88321ED-AS | High | Y | Y | Y | N | 1 | 1 | WB SOIC-20 |
| Si88322ED-IS | Si88322ED-AS | High | Y | Y | Y | N | 0 | 2 | WB SOIC-20 |
| Si88420ED-IS | Si88420ED-AS | High | N | N | N | Y | 2 | 0 | WB SOIC-16 |
| Si88421ED-IS | Si88421ED-AS | High | N | N | N | Y | 1 | 1 | WB SOIC-16 |
| Si88422ED-IS | Si88422ED-AS | High | N | N | N | Y | 0 | 2 | WB SOIC-16 |
| Si88620ED-IS | Si88620ED-AS | High | Y | Y | Y | Y | 2 | 0 | WB SOIC-20 |
| Si88621ED-IS | Si88621ED-AS | High | Y | Y | Y | Y | 1 | 1 | WB SOIC-20 |
| Si88622ED-IS | Si88622ED-AS | High | Y | Y | Y | Y | 0 | 2 | WB SOIC-20 |

1. All packages are RoHS-compliant with peak solder reflow temperatures of 260°C according to the JEDEC industry standard classifications.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 qualified.
4. An “R” at the end of the part number denotes tape and reel packaging option.
5. Automotive-Grade devices (with an “–A” suffix) are identical in construction materials, topside marking format, and electrical parameters to their Industrial-Grade (with an “–I” suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In 7. Top Markings, the manufacturing code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.
7. On input power loss.

# 9. Revision History

| Revision | Date | Description |
|---|---|---|
| B | September, 2023 | Corrected input/output voltage configuration block diagrams:<br>Figure 7, "Si883xx Block Diagram: 3 V to 5 V Input to 3 V to 5 V Output," on page 10.<br>Figure 8, "Si883xx Block Diagram: 3 V to 5 V Input to up to 24 V Output," on page 11.<br>Figure 9, "Si886xx Block Diagram: 24 V Input to 5 V Output," on page 13.<br>Figure 10, "Si886xx Block Diagram: Up to 24 V Input to up to 24 V Output," on page 14. |
| A | August, 2023 | Updated decimal-based revision number to alphanumeric code.<br>Updated Safety Regulatory Approvals on front page and in tables in:<br>4.1. Safety Certifications and Specifications.<br>Reordered sections to conform to Skyworks conventions. |
| 1.04 | October, 2020 | Corresponding -A OPNs are added for all existing -I OPNs to 8. Ordering Guide.<br>62368 regulatory information added to Table 7, "Regulatory Information (Pending)," on page 30.<br>Provided additional layout guidelines.<br>Minor edits and text corrections. |
| 1.03 | May, 2020 | Added an Automotive Grade OPNs subsection to 8. Ordering Guide. |
| 1.02 | March, 2019 | Corrected Transformer Specification table. |
| 1.01 | November, 2018 | Updated Transformer Specification table. |
| 1.0 | February, 2018 | Updated Ordering Guide Table 2.1.<br>Updated Transformer Table 3.1.<br>Updated Spec Table 4.2.<br>Added section 4.1 (Calculating total current).<br>Corrected pin-outs Fig 6.1, 6.3. |
| 0.6 | May, 2017 | Updated format to current style guide.<br>Added WB-SOIC-16 to Table 12. IEC60747-17 Safety Limiting Values.<br>Updated Table 2, "Transformer Specifications".<br>Updated 3.5. Typical Performance Characteristics.<br>Updated pinouts and pin description table in "1. Pin Descriptions" on page 2. |
| 0.5 | July, 2015 | Initial release. |

Copyright © 2023, Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks' Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks' published specifications or parameters.

Skyworks, the Skyworks symbol, Sky5®, SkyOne®, SkyBlue™, Skyworks Green™, ClockBuilder®, DSPLL®, ISOmodem®, ProSLIC®, SiPHY®, and RFeIC® are trademarks or registered trademarks of Skyworks Solutions, Inc. or its subsidiaries in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at www.skyworksinc.com, are incorporated by reference.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View SI88620ED-ISR on WIN SOURCE
- Skyworks Solutions Inc. Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management