

ISO6760L Six-Channel Reinforced Digital Isolators with Integrated Interlock and Robust EMC

1 Features

- ISO6760 with integrated Interlock function
 - Designed to support opposite polarity of adjacent channels
 - Three sets of paired interlock channels
- Robust isolation barrier:
 - High lifetime at 1500 V_{RMS} working voltage
 - Up to 5000 V_{RMS} isolation rating
 - Up to 10 kV surge capability
 - ±130 kV/μs typical CMTI
- Wide supply range: 1.71 V to 1.89 V and 2.25 V to 5.5 V
- Channel output *non-inverting* (ISO6760L) and *inverting* (ISO6760LN) options
- 50 Mbps data rate
- 1.71 V to 5.5 V level translation
- Wide temperature range: –40°C to 125°C
- 1.4 mA per channel typical at 1 Mbps
- Robust electromagnetic compatibility (EMC)
 - System-level ESD, EFT, and surge immunity
 - Low emissions
- Wide-SOIC (DW-16) Package
- [Safety-Related Certifications](#):
 - DIN EN IEC 60747-17 (VDE 0884-17)
 - UL 1577 component recognition program
 - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1 certifications

2 Applications

- [Motor drives](#)
- [Appliances](#)
- [Grid](#)
- [Building Automation](#)

3 Description

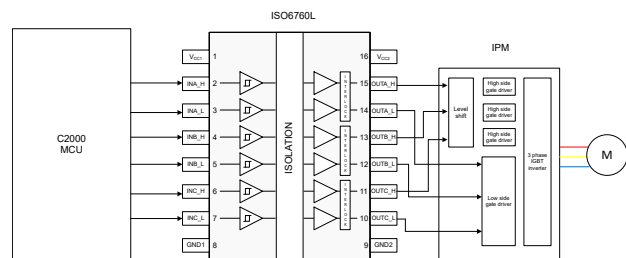
The ISO6760L and ISO6760LN devices are high-performance, six-channel digital isolators with integrated interlock function for applications requiring up to 5000 V_{RMS} isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO6760L family of devices integrate a series of logic gates to provide hardware interlock functionality for adjacent channels. The interlock feature ensures that each channel, in a channel pairing, will not be enabled at the same time. If both channels in the pairing share the same input logic, the output logic will always be low. The ISO6760L family of devices have all six channels in the same direction and provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO₂) insulation barrier.

Used in conjunction with intelligent power modules (IPMs), the interlock feature in these devices help prevent shoot through current between the high side and low side gate driver during turn on and turn off events. Six channels, including three pairings of interlock circuitry, are integrated in a 16-pin SOIC wide-body (DW) package with space savings greater than 50% compared to optocoupler solutions. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO6760L devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

Device Description

Part Number	Package	Body Size
ISO6760L, ISO6760LN	SOIC (DW)	10.30 mm × 7.50 mm



Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (February 2023)	Page
• Changed standard name From: "DIN V VDE V 0884-11:2017-01" To: "DIN EN IEC 60747-17 (VDE 0884-17)" throughout the document.....	1
• Removed references to standard IEC/EN/CSA 60950-1 throughout the document.....	1
• Updated standards marked as "planned" to include certificate numbers throughout the document.....	1
• Removed standard revision and year references from all standard names throughout the document.....	1
• Added Maximum impulse voltage (V_{IMP}) specification per DIN EN IEC 60747-17 (VDE 0884-17).....	7
• Changed test conditions and values of Maximum surge isolation voltage (V_{IOSM}) specification per DIN EN IEC 60747-17 (VDE 0884-17).....	7
• Clarified method b test conditions of Apparent charge (q_{PD}).....	7
• Changed Maximum surge isolation voltage (V_{IOSM}) from 6250 V_{PK} to 10000 V_{PK}	9
• Changed working voltage lifetime margin From: 87.5% To: 50%, minimum required insulation lifetime From: 37.5 years To: 30 years and insulation lifetime per TDDb From: 220 years To: 36 years per DIN EN IEC 60747-17 (VDE 0884-17).....	29
• Changed Figure 10-2 as per DIN EN IEC 60747-17 (VDE 0884-17).....	29
• Updated to DW0016B mechanical drawing.....	33

5 Pin Configuration and Functions

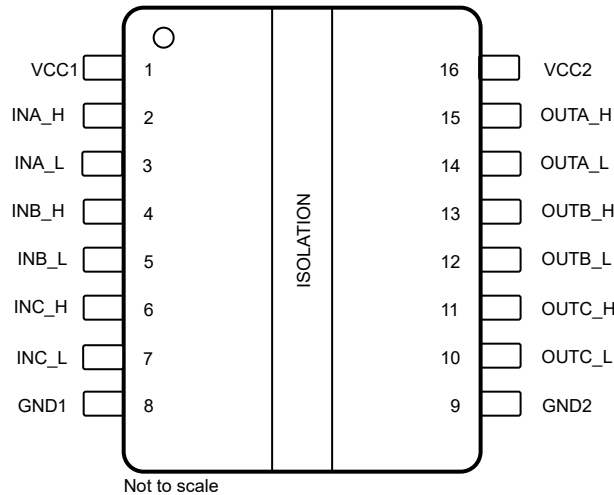


Figure 5-1. ISO6760L DW Package 16-Pin SOIC-WB Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	ISO6760L		
GND1	8	—	Ground connection for V_{CC1}
GND2	9	—	Ground connection for V_{CC2}
INA_H	2	I	Input, channel A_H (Interlock paired with channel A_L)
INA_L	3	I	Input, channel A_L (Interlock paired with channel A_H)
INB_H	4	I	Input, channel B_H (Interlock paired with channel B_L)
INB_L	5	I	Input, channel B_L (Interlock paired with channel B_H)
INC_H	6	I	Input, channel C_H (Interlock paired with channel C_L)
INC_L	7	I	Input, channel C_L (Interlock paired with channel C_H)
OUTA_H	15	O	Output, channel A_H (Interlock paired with channel A_L)
OUTA_L	14	O	Output, channel A_L (Interlock paired with channel A_H)
OUTB_H	13	O	Output, channel B_H (Interlock paired with channel B_L)
OUTB_L	12	O	Output, channel B_L (Interlock paired with channel B_H)
OUTC_H	11	O	Output, channel C_H (Interlock paired with channel C_L)
OUTC_L	10	O	Output, channel C_L (Interlock paired with channel C_H)
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	16	—	Power supply, side 2

6 Specifications

6.1 Absolute Maximum Ratings

See⁽¹⁾

		MIN	MAX	UNIT
Supply Voltage ⁽²⁾	V _{CC1} to GND1	-0.5	6	V
	V _{CC2} to GND2	-0.5	6	
Input/Output Voltage	IN _x to GND _x	-0.5	V _{CCX} + 0.5 ⁽³⁾	V
	OUT _x to GND _x	-0.5	V _{CCX} + 0.5 ⁽³⁾	
Output Current	I _o	-15	15	mA
Temperature	Operating junction temperature, T _J		150	°C
	Storage temperature, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
- (3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

(1) (2)

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT	
V_{CC1} ⁽¹⁾	Supply Voltage Side 1 ⁽³⁾	1.71		1.89	V	
V_{CC1} ⁽¹⁾	Supply Voltage Side 1 ⁽³⁾	2.25		5.5	V	
V_{CC2} ⁽¹⁾	Supply Voltage Side 2 ⁽³⁾	1.71		1.89	V	
V_{CC2} ⁽¹⁾	Supply Voltage Side 2 ⁽³⁾	2.25		5.5	V	
V_{CC} (UVLO+)	UVLO threshold when supply voltage is rising		1.53	1.71	V	
V_{CC} (UVLO-)	UVLO threshold when supply voltage is falling	1.1	1.41		V	
V_{hys} (UVLO)	Supply voltage UVLO hysteresis	0.08	0.13		V	
V_{IH}	High level Input voltage	$0.7 \times V_{CCI}$ ⁽²⁾		V_{CCI}	V	
V_{IL}	Low level Input voltage	0	$0.3 \times V_{CCI}$		V	
I_{OH}	High level output current	V_{CCO} ⁽²⁾ = 5 V			-4	mA
		V_{CCO} = 3.3 V			-2	mA
		V_{CCO} = 2.5 V			-1	mA
		V_{CCO} = 1.8 V			-1	mA
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	mA
		V_{CCO} = 2.5 V			1	mA
		V_{CCO} = 1.8 V			1	mA
DR	Data Rate	V_{CC} = 2.25 V to 5.5 V	0		50	Mbps
		V_{CC} = 1.71 V to 1.89 V	0		25	Mbps
T_A	Ambient temperature	-40	25	125	°C	

(1) V_{CC1} and V_{CC2} can be set independent of one another

(2) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

(3) The channel outputs are in undetermined state when $1.89 \text{ V} < V_{CC1}$, $V_{CC2} < 2.25 \text{ V}$ and $1.05 \text{ V} < V_{CC1}$, $V_{CC2} < 1.71 \text{ V}$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO6760L	UNIT
		DW (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6760L						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, Input a 25-MHz 50% duty cycle square wave			200	mW
P_{D1}	Maximum power dissipation (side-1)				45	mW
P_{D2}	Maximum power dissipation (side-2)				155	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (2)				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDDB) Test; See Insulation Lifetime Projection Data	1500	V _{RMS}
		DC voltage	2121	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 x V _{IOTM} , t = 1 s (100% production)	7071	V _{PK}
V _{IMP}	Maximum impulse voltage ⁽³⁾	Tested in air, 1.2/50-us waveform per IEC 62368-1	7692	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽⁴⁾	V _{IOSM} ≥ 1.3 x V _{IMP} ; Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	10000	V _{PK}
q _{pd}	Apparent charge ⁽⁵⁾	Method a, After Input-output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 x V _{IORM} , t _m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 x V _{IORM} , t _m = 10 s	≤5	
		Method b: At routine test (100% production) and preconditioning (type test); V _{ini} = 1.2 x V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 x V _{IORM} , t _m = 1 s (method b1) or V _{pd(m)} = V _{ini} , t _m = t _{ini} (method b2)	≤5	
C _{IO}	Barrier capacitance, input to output ⁽⁶⁾	V _{IO} = 0.4 x sin(2πft), f = 1 MHz	~1	pF
R _{IO}	Isolation resistance ⁽⁶⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 x V _{ISO} , t = 1 s (100% production)	5000	V _{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).

- (6) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1, IEC 61010-1 and IEC 60601	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 7071 V _{PK} ; Maximum repetitive peak isolation voltage, 2121 V _{PK} ; Maximum surge isolation voltage, 10000 V _{PK}	600 V _{RMS} reinforced insulation per CSA 62368-1 and IEC 62368-1; 600 V _{RMS} reinforced insulation per CSA 61010-1 and IEC 61010-1 (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V _{RMS} max working voltage	Single protection, 5000 V _{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V _{RMS} maximum working voltage	5000 V _{RMS} reinforced insulation per EN 61010-1 and EN 62368-1 up to working voltage of 600 V _{RMS}
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC21001304083	Client ID number: 077311

6.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I _S	Safety input, output, or supply current ⁽¹⁾	R _{θJA} = 68.8°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C			330	mA
		R _{θJA} = 68.8°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C			504	mA
		R _{θJA} = 68.8°C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C			660	mA
		R _{θJA} = 68.8°C/W, V _I = 1.89 V, T _J = 150°C, T _A = 25°C			956	mA
P _S	Safety input, output, or total power ⁽¹⁾	R _{θJA} = 68.8°C/W, T _J = 150°C, T _A = 25°C			1820	mW
T _S	Maximum safety temperature ⁽¹⁾				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, R_{θJA}, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.
T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum allowed junction temperature.
P_S = I_S × V_I, where V_I is the maximum input voltage.

6.9 Electrical Characteristics—5-V Supply

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA; See Switching Characteristics Test Circuit and Voltage Waveforms	$V_{CCO} - 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA; See Switching Characteristics Test Circuit and Voltage Waveforms			0.4	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}$ ⁽¹⁾		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at INx			10	μ A
I_{IL}	Low-level input current	$V_{IL} = 0$ V at INx	-10			μ A
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V, $V_{CM} = 1200$ V; see Common-Mode Transient Immunity Test Circuit	50	130		kV/us
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2$ MHz, $V_{CC} = 5$ V		2.8		pF

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

(2) Measured from input pin to same side ground.

6.10 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5$ V $\pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO6760L							
Supply current - DC signal	Output A: GND for ISO6760L and V_{CC} for ISO6760LN Output B: V_{CC} for ISO6760L and GND for ISO6760LN	I_{CC1}		5.11	6.97	mA	
		I_{CC2}		3.3	5.38		
Supply current - AC signal	All channels switching with square wave clock input; $CL = 15$ pF	1 Mbps	I_{CC1}		5.13		6.99
			I_{CC2}		3.7		5.83
		10 Mbps	I_{CC1}		5.29		7.19
			I_{CC2}		7.27		9.9
		50 Mbps	I_{CC1}		6.12		8.16
			I_{CC2}		23.62		27.74

6.11 Electrical Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$; See Switching Characteristics Test Circuit and Voltage Waveforms	$V_{CCO} - 0.2$			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$; See Switching Characteristics Test Circuit and Voltage Waveforms			0.2	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}^{(1)}$		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Common-Mode Transient Immunity Test Circuit	50	130		kV/us
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2\text{ MHz}$, $V_{CC} = 3.3\text{ V}$		2.8		pF

- (1) $V_{CCI} =$ Input-side V_{CC} ; $V_{CCO} =$ Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.12 Supply Current Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO6760L							
Supply current - DC signal	Output A: GND for ISO6760L and Vcc for ISO6760LN Output B: Vcc for ISO6760L and GND for ISO6760LN	I_{CC1}		5.08	6.89	mA	
		I_{CC2}		3.28	5.36		
Supply current - AC signal	All channels switching with square wave clock input; CL = 15 pF	1 Mbps	I_{CC1}		5.1		6.9
			I_{CC2}		3.57		5.68
		10 Mbps	I_{CC1}		5.18		7.04
			I_{CC2}		6.07		8.62
		50 Mbps	I_{CC1}		5.74		7.68
			I_{CC2}		17.54		21.5

6.13 Electrical Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1\text{ mA}$; See Switching Characteristics Test Circuit and Voltage Waveforms	$V_{CCO} - 0.1$			V
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{ mA}$; See Switching Characteristics Test Circuit and Voltage Waveforms			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}^{(1)}$		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Common-Mode Transient Immunity Test Circuit	50	130		kV/us
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2\text{ MHz}$, $V_{CC} = 2.5\text{ V}$		2.8		pF

(1) $V_{CCI} =$ Input-side V_{CC} ; $V_{CCO} =$ Output-side V_{CC}

(2) Measured from input pin to same side ground.

6.14 Supply Current Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO6760L							
Supply current - DC signal	Output A: GND for ISO6760L and Vcc for ISO6760LN Output B: Vcc for ISO6760L and GND for ISO6760LN	I_{CC1}		5.07	6.85	mA	
		I_{CC2}		3.28	5.35		
Supply current - AC signal	All channels switching with square wave clock input; CL = 15 pF	1 Mbps	I_{CC1}		5.08		6.87
			I_{CC2}		3.49		5.59
		10 Mbps	I_{CC1}		5.14		6.97
			I_{CC2}		5.34		7.8
		25 Mbps	I_{CC1}		5.59		7.49
			I_{CC2}		13.83		17.47

6.15 Electrical Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1\text{ mA}$; See Switching Characteristics Test Circuit and Voltage Waveforms	$V_{CCO} - 0.1$			V
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{ mA}$; See Switching Characteristics Test Circuit and Voltage Waveforms			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}^{(1)}$		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Common-Mode Transient Immunity Test Circuit	50	75		kV/us
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 2\text{ MHz}$, $V_{CC} = 1.8\text{ V}$		2.8		pF

(1) $V_{CCI} =$ Input-side V_{CC} ; $V_{CCO} =$ Output-side V_{CC}

(2) Measured from input pin to same side ground.

6.16 Supply Current Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO6760L							
Supply current - DC signal	Output A: GND for ISO6760L and V_{CC} for ISO6760LN Output B: V_{CC} for ISO6760L and GND for ISO6760LN	I_{CC1}		4.27	6.24	mA	
		I_{CC2}		3.15	5.39		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		4.28		6.25
			I_{CC2}		3.3		5.55
		10 Mbps	I_{CC1}		4.37		6.37
			I_{CC2}		4.6		7.04
		50 Mbps (25Mbps)	I_{CC1}		4.5		6.5
			I_{CC2}		6.84		9.47

6.17 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6760L						
t_{PLH}, t_{PHL}	Propagation delay time	One input in static state and other input is toggled at 100kbps. See Switching Characteristics Test Circuit and Voltage Waveforms		13	20.5	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			1	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				6	ns
t_r	Output signal rise time	See Switching Characteristics Test Circuit and Voltage Waveforms		2.6	4.5	ns
t_f	Output signal fall time			2.6	4.5	ns
t_{PU}	Time from UVLO to valid output data	Time from UVLO to valid output data			300	us
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Default Output Delay Time Test Circuit and Voltage Waveforms		0.1	0.3	us
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Switching Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6760L						
t_{PLH} , t_{PHL}	Propagation delay time	One input in static state and other input is toggled at 100kbps. See Switching Characteristics Test Circuit and Voltage Waveforms		13	21	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			1	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				7	ns
t_r	Output signal rise time	See Switching Characteristics Test Circuit and Voltage Waveforms		1.6	2.8	ns
t_f	Output signal fall time			1.6	2.8	ns
t_{PU}	Time from UVLO to valid output data	Time from UVLO to valid output data			300	us
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Default Output Delay Time Test Circuit and Voltage Waveforms		0.1	0.3	us
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.19 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6760L						
t_{PLH}, t_{PHL}	Propagation delay time	One input in static state and other input is toggled at 100kbps. See Switching Characteristics Test Circuit and Voltage Waveforms		14.5	23.5	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			1	7.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				7.9	ns
t_r	Output signal rise time	See Switching Characteristics Test Circuit and Voltage Waveforms		2	4	ns
t_f	Output signal fall time			2	4	ns
t_{PU}	Time from UVLO to valid output data	Time from UVLO to valid output data			300	us
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Default Output Delay Time Test Circuit and Voltage Waveforms		0.1	0.3	us
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.20 Switching Characteristics—1.8-V Supply

 $V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 5\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6760L						
t_{PLH}, t_{PHL}	Propagation delay time	One input in static state and other input is toggled at 100kbps. See Switching Characteristics Test Circuit and Voltage Waveforms		18	31	ns
PWD	Pulse width distortion $ t_{PHL} - t_{PLH} $			1	8.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽¹⁾	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽²⁾				11.7	ns
t_r	Output signal rise time	See Switching Characteristics Test Circuit and Voltage Waveforms		2.7	5.3	ns
t_f	Output signal fall time			2.7	5.3	ns
t_{PU}	Time from UVLO to valid output data	Time from UVLO to valid output data			300	us
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Default Output Delay Time Test Circuit and Voltage Waveforms		0.1	0.3	us
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

- (1) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.21 Insulation Characteristics Curves

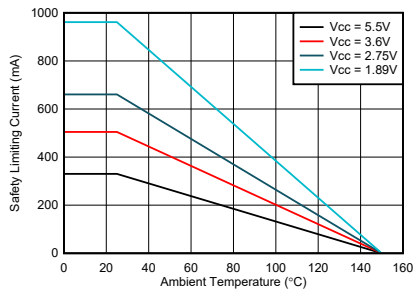


Figure 6-1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package

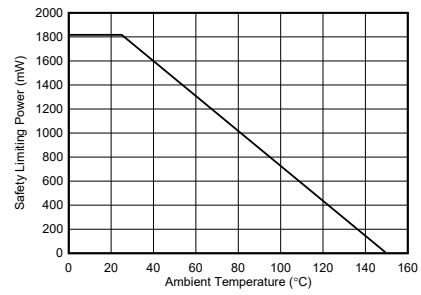


Figure 6-2. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

6.22 Typical Characteristics

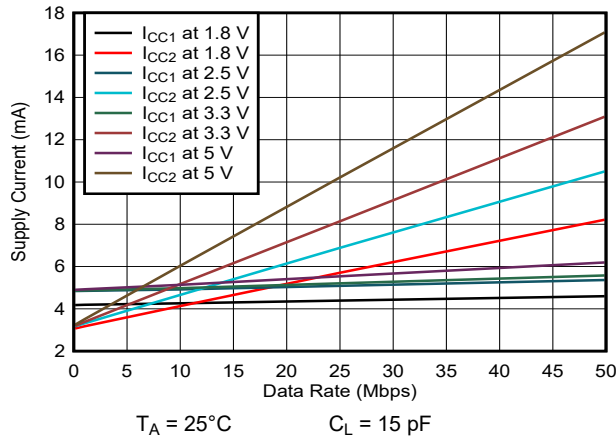


Figure 6-3. ISO6760L Supply Current vs Data Rate (With 15-pF Load)

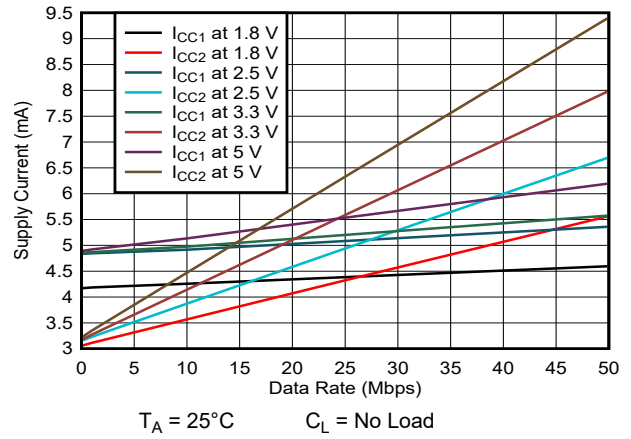


Figure 6-4. ISO6763 Supply Current vs Data Rate (With No Load)

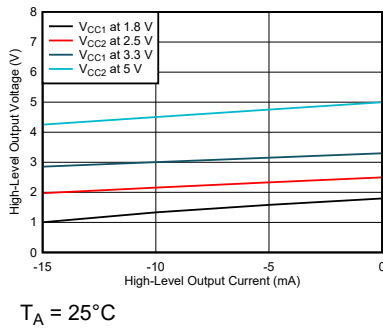


Figure 6-5. High-Level Output Voltage vs High-level Output Current

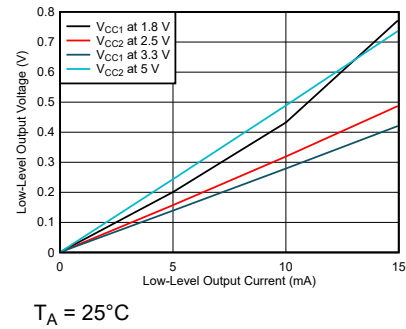


Figure 6-6. Low-Level Output Voltage vs Low-Level Output Current

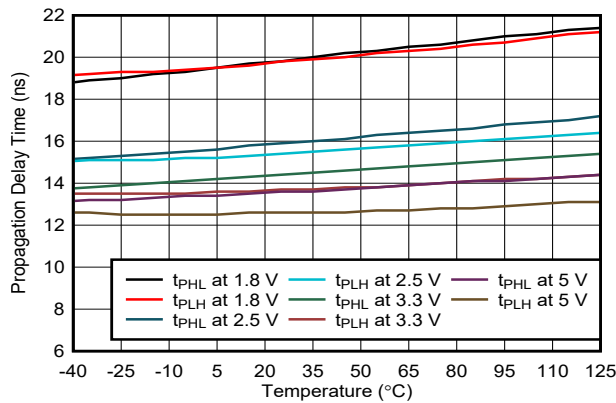


Figure 6-7. Propagation Delay Time vs Free-Air Temperature

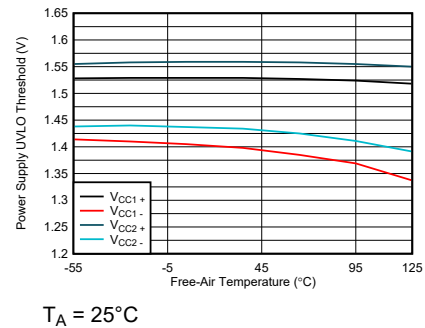
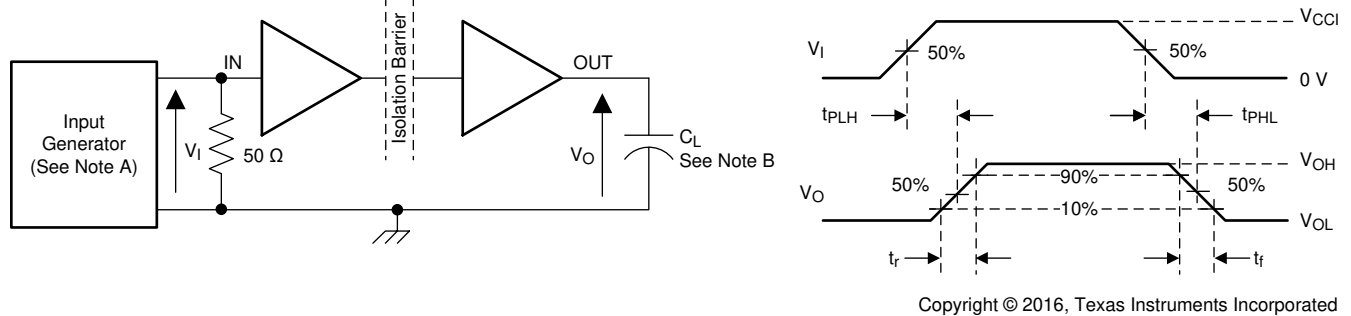


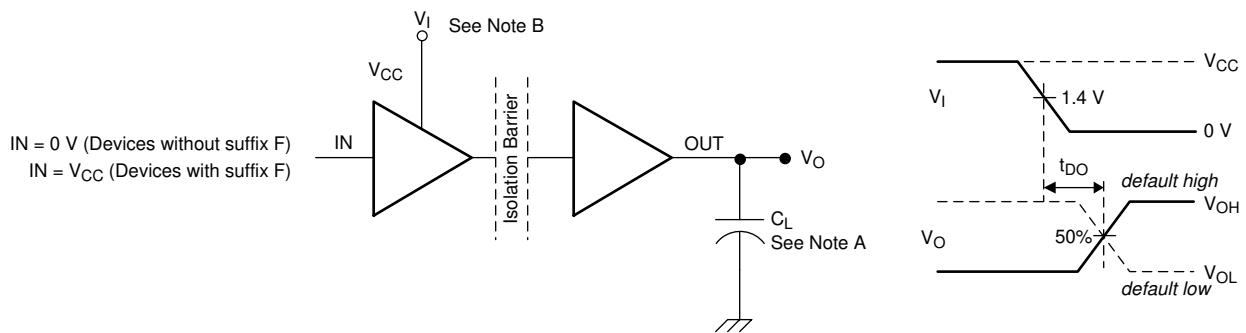
Figure 6-8. Power Supply Undervoltage Threshold vs Free-Air Temperature

7 Parameter Measurement Information



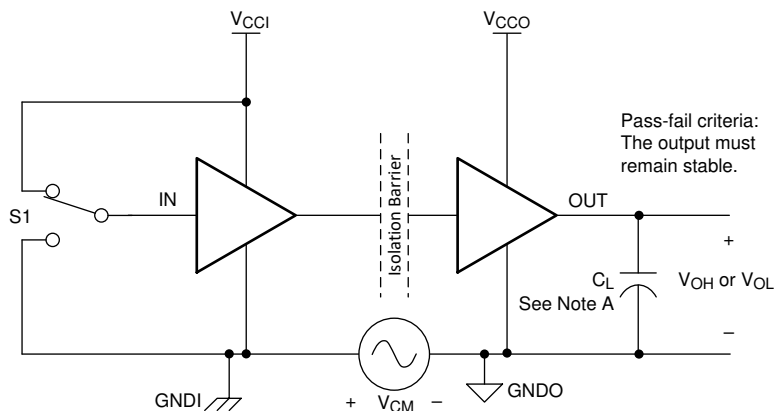
- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$. At the input, 50Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. Power Supply Ramp Rate = 10 mV/ns

Figure 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. For optimized CMTI performance, a $0.1 \mu\text{F} + 1 \mu\text{F}$ decoupling capacitor should be placed close to V_{CC1} and V_{CC2} . Please see [Section 12.2](#) for capacitor placement details. A recommended $0.1 \mu\text{F}$ capacitor is LLL185R71A104MA11L (CAP CER 0.1UF 10V X7R 0306 - LW Reversed Low ESL Chip Ceramic Capacitors) or equivalent.

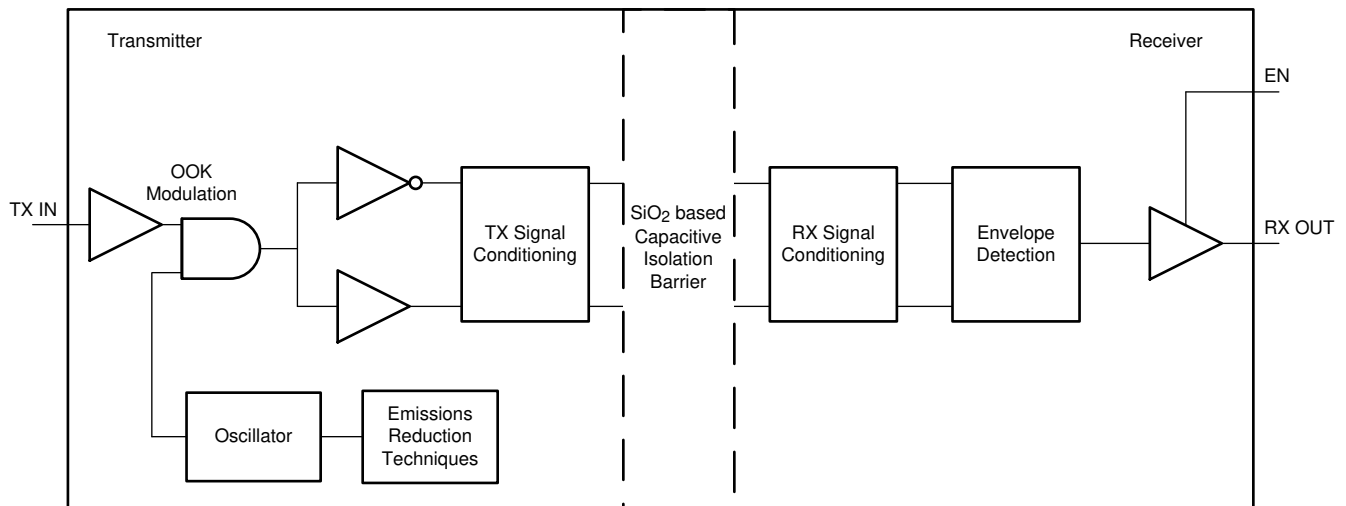
Figure 7-3. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO6760L family of devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output which goes through an interlock stage before an output buffer. The ISO6760L family offers two options, a standard non-inverting channel, ISO6760L, and a channel inverting ISO6760LN. The two offerings make the ISO6760L family compatible with historical optocoupler based solutions. The ISO6760L devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 8-1](#), shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram



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Figure 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator

[Figure 8-2](#) shows a conceptual detail of how the ON-OFF keying scheme works.

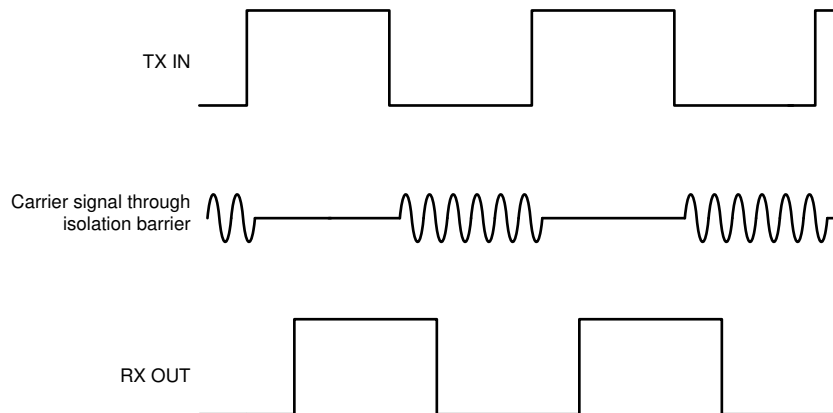


Figure 8-2. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

Table 8-1 provides an overview of the device features.

Table 8-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	OUTPUT	PACKAGE	RATED ISOLATION ⁽¹⁾
ISO6760L	6 Forward, 3 Interlock Pairs	50 Mbps	Non-Inverted	DW-16	5000 V _{RMS} / 7000 V _{PK}
ISO6760LN	6 Forward, 3 Interlock Pairs	50 Mbps	Inverted	DW-16	5000 V _{RMS} / 7000 V _{PK}

(1) See for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 32. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO676x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.3.2 Interlock Capability

The ISO6760L family incorporates a series of logic gates to protect adjacent channel pairings from both registering high simultaneously. When paired with an IPM, this interlock circuitry provides protection preventing shoot through current to both the high-side and low-side switch of the module. This design, shown in [ISO6760L Channel Pairing Block Diagram of Interlock](#), is used to make sure that when one of the channel pairings is logic high, the other channel will output logic low. [ISO6760L Device Truth Table](#) provides the logic output state to the corresponding input state for ISO6760L and [ISO6760LN \(Inverted\) Device Truth Table](#) provides the logic output state to the corresponding input state for ISO6760LN (inverted output version).

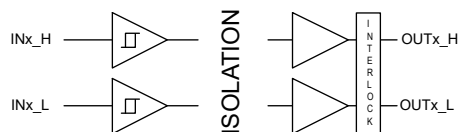


Figure 8-3. ISO6760L Channel Pairing Block Diagram of Interlock

ISO6760L Device Truth Table

INx_H	INx_L	OUTx_H	OUTx_L
High	Low	High	Low
Low	High	Low	High
High	High	Low	Low
Low	Low	Low	Low
Floating	Floating	Low	Low

Table 8-2. ISO6760LN (Inverted) Device Truth Table

INx_H	INx_L	OUTx_H	OUTx_L
High	Low	Low	High
Low	High	High	Low
High	High	Low	Low
Low	Low	Low	Low
Floating	Floating	Low	Low

8.4 Device Functional Modes

Function Table lists the functional modes for the ISO6760L devices.

Function Table

V _{CCI} ⁽¹⁾	V _{CCO}	INPUT (IN _{x_H} and IN _{x_L}) ⁽³⁾	OUTPUT (OUT _{x_H} and OUT _{x_L})	COMMENTS
PU	PU	H	Normal	Normal Operation: A channel output assumes the logic state of its input noted in ISO6760L Device Truth Table and ISO6760LN (Inverted) Device Truth Table .
		L		
		Open		
PD	PU	X	Low	Output Low: When V _{CCI} is unpowered and V _{CCO} is powered up, the output interlock circuit will set the output to logic low. When V _{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state in ISO6760L Device Truth Table and ISO6760LN (Inverted) Device Truth Table . When V _{CCI} transitions from powered-up to unpowered, channel output will be the output low state.
X	PD	X	Undetermined	When V _{CCO} is unpowered, a channel output is undetermined ⁽²⁾ . When V _{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of its input noted in ISO6760L Device Truth Table and ISO6760LN (Inverted) Device Truth Table .

- (1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 1.71 V); PD = Powered down (V_{CC} ≤ 1.05 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
- (2) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V and 1.05 V < V_{CCI}, V_{CCO} < 1.71 V
- (3) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output

8.4.1 Device I/O Schematics

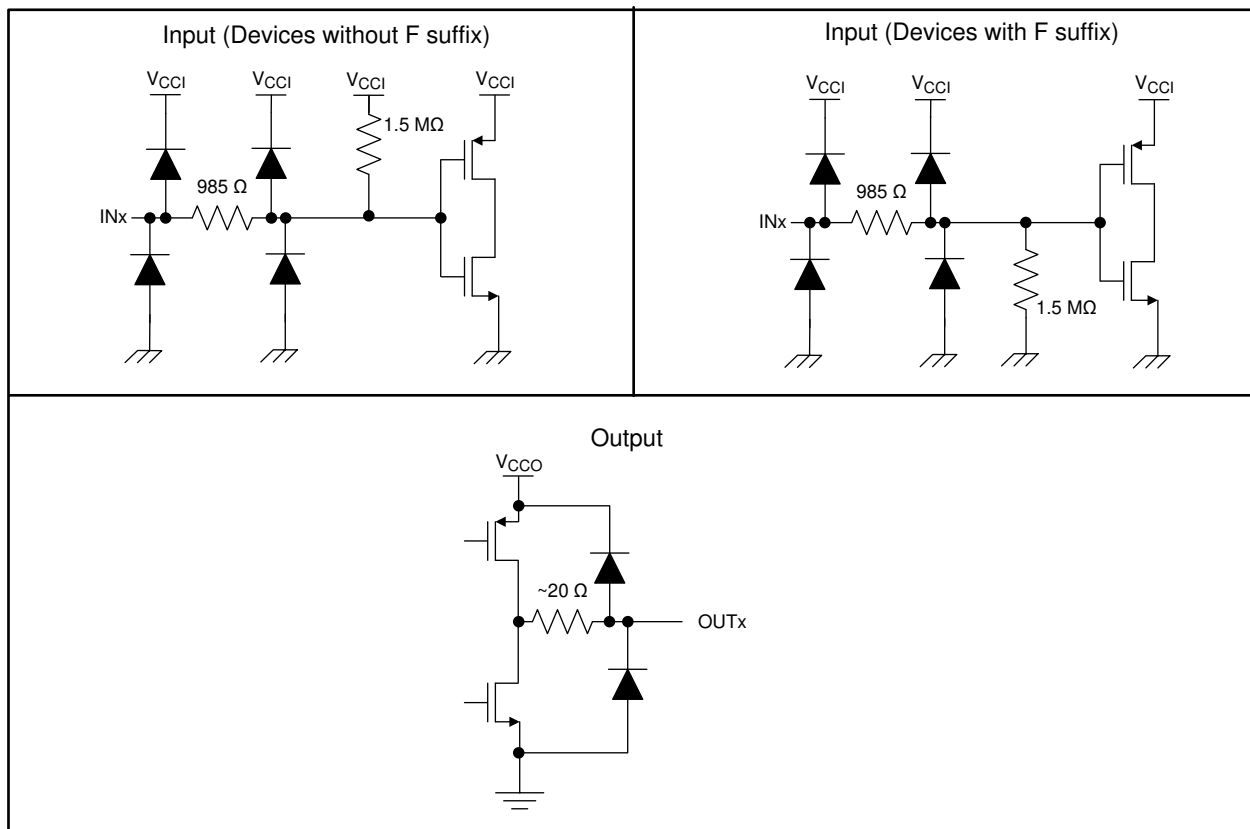


Figure 8-4. Device I/O Schematics

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO6760L devices are high-performance, six-channel digital isolators. The ISO6760L devices use single-ended CMOS-logic switching technology with built in hardware interlock logic. The supply voltage range is from 1.71 V to 5.5 V for both supplies, V_{CC1} and V_{CC2} . Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. As an example, it is possible to supply ISO6760L V_{CC1} with 3.3 V (which is within 1.71 V to 5.5 V) and V_{CC2} with 5V (which is also within 1.71 V to 5.5 V). You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

Figure 9-1 shows the isolated connections between a processor and Intelligent Power Module (IPM) interface implementation.

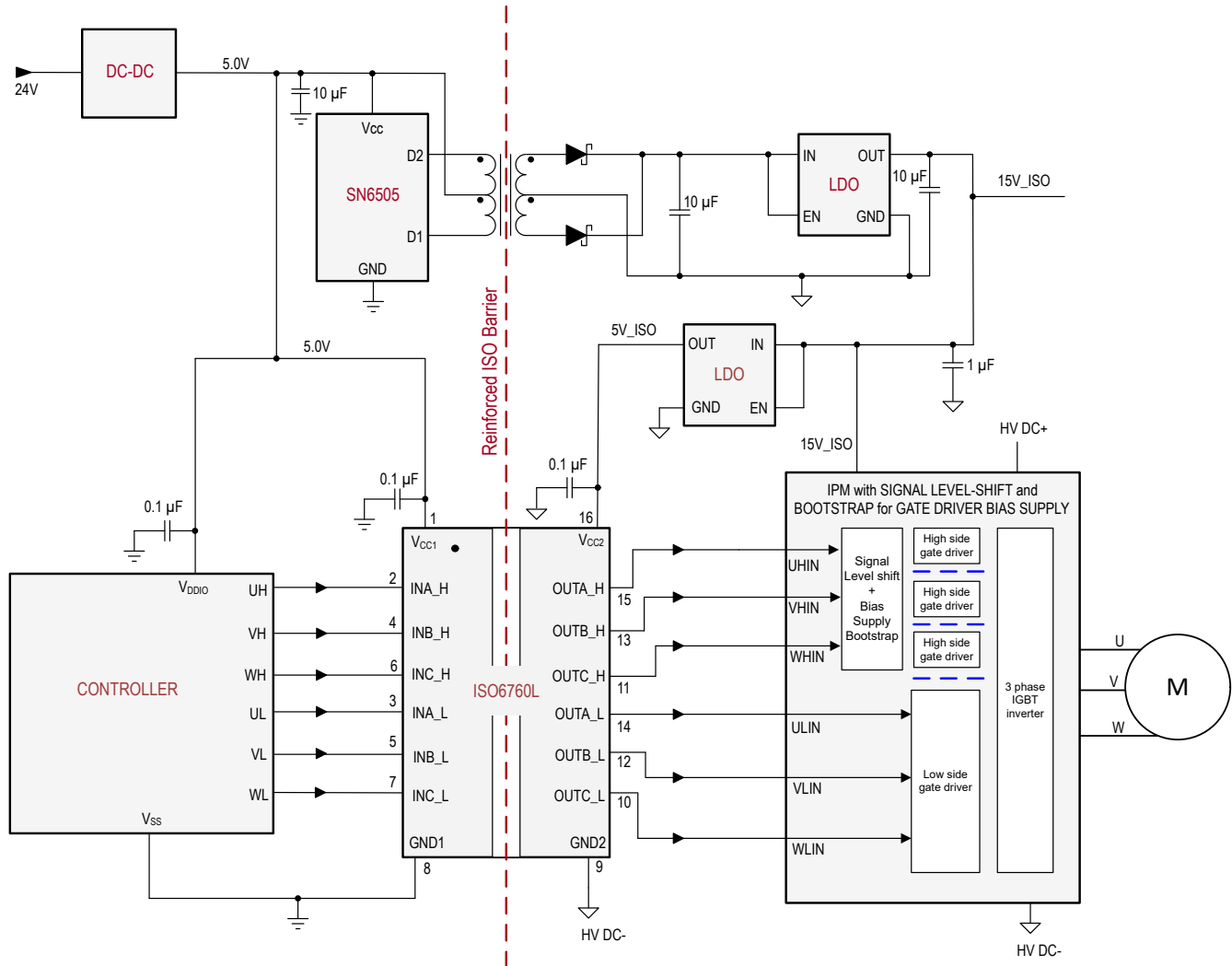


Figure 9-1. Isolation for Intelligent Power Module (IPM) Interface

9.2.1 Design Requirements

To design with these devices, use the parameters listed in [Table 9-1](#).

Table 9-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	1.71 V to 1.89 V and 2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 μ F
Decoupling capacitor from V_{CC2} and GND2	0.1 μ F

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO6760L family of devices only require two external bypass capacitors to operate.

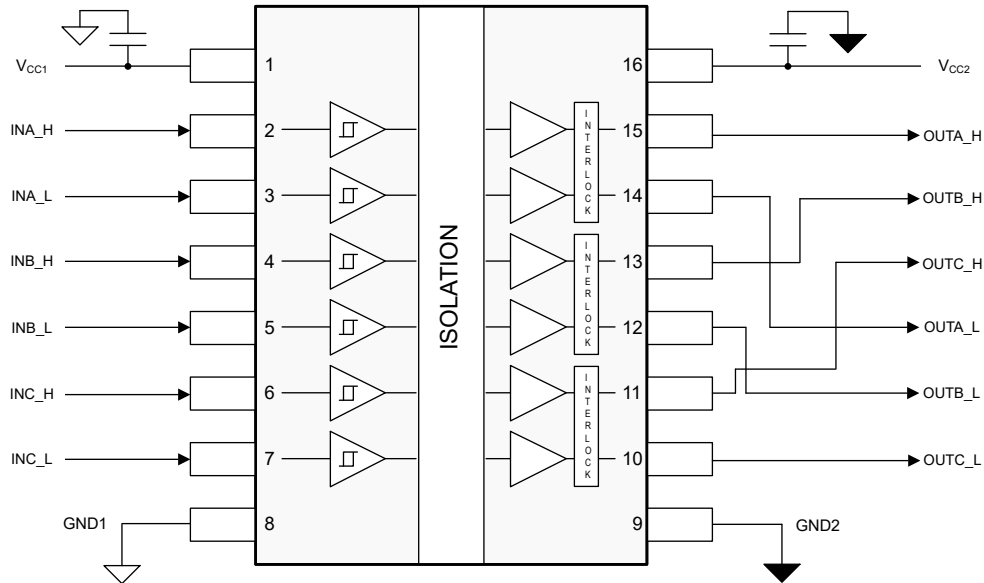


Figure 9-2. Typical ISO6760L Circuit Hook-up

9.2.3 Application Curve

The following diagrams of the ISO6760L family of devices show how the hardware interlock circuitry protects against shoot through current. Within a channel pairing, both outputs cannot be high simultaneously. [ISO6760L Interlock Diagram](#) shows the ISO6760L demonstrating the hardware interlock on a 200 Hz input signal out of phase between two adjacent channels. [ISO6760L Interlock Diagram](#) shows the the normal ISO6760 (device offered without interlock circuitry) with a 200 Hz input signal out of phase between two adjacent channels for comparison.

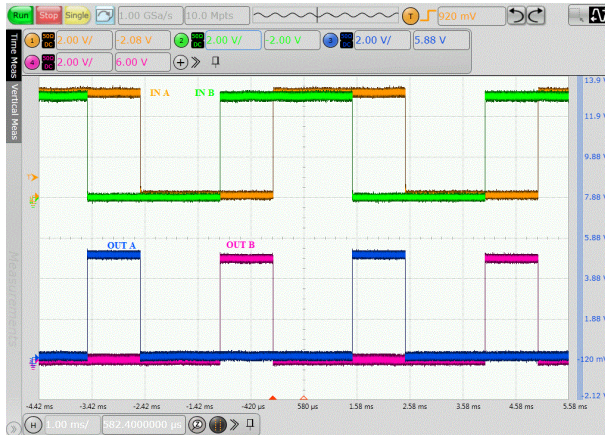


Figure 9-3. ISO6760L Interlock Diagram

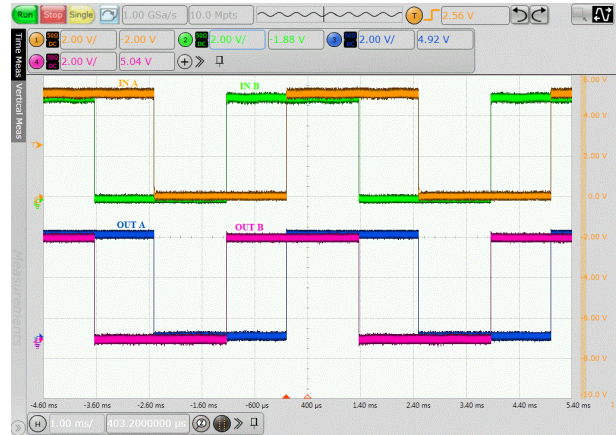


Figure 9-4. ISO6760 (Device without Interlock) Diagram

10 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See [Figure 10-1](#) for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

[Figure 10-2](#) shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.

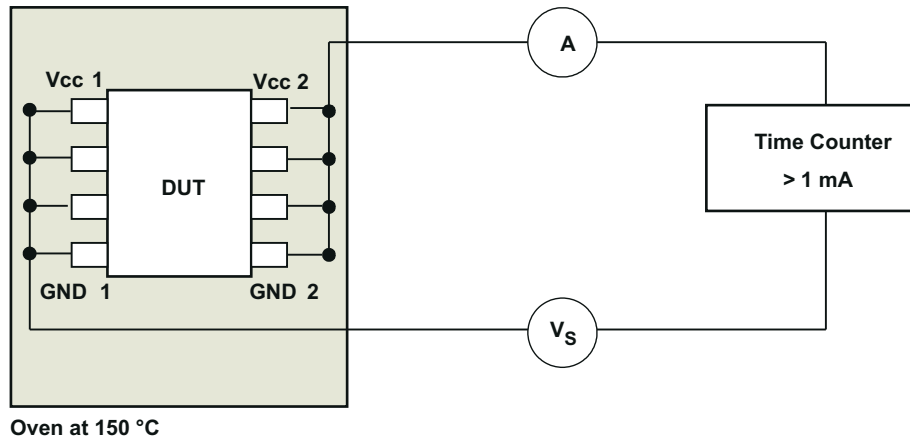


Figure 10-1. Test Setup for Insulation Lifetime Measurement

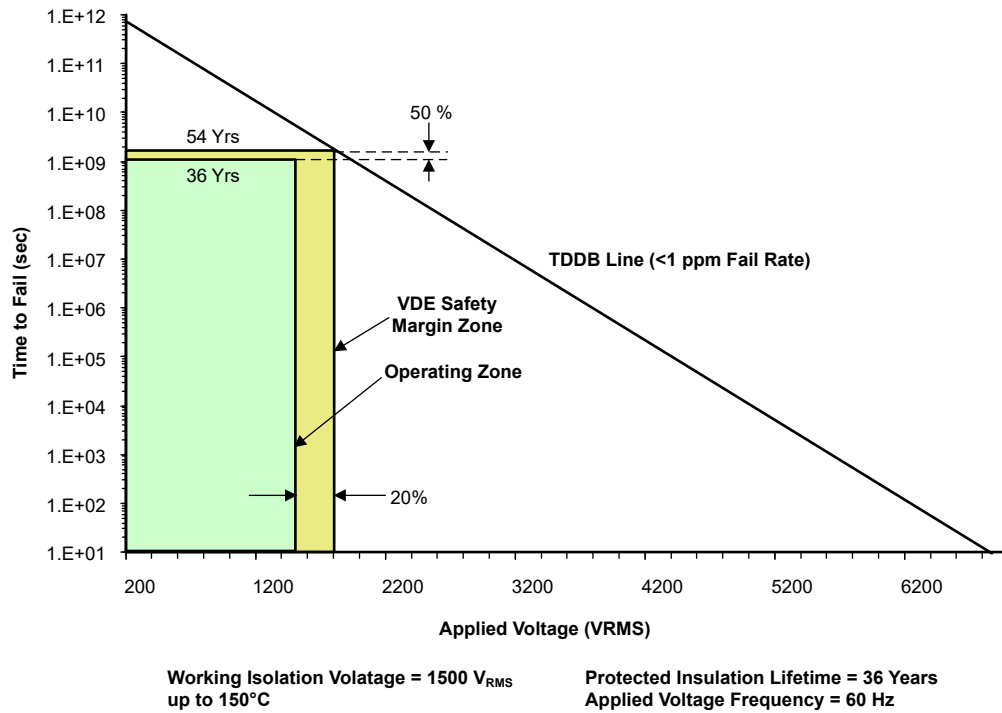


Figure 10-2. Insulation Lifetime Projection Data

11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- μ F bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For industrial applications, please use Texas Instruments' [SN6501](#) or [SN6505B](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies](#) or [SN6505B-Q1 Low-noise, 1-A Transformer Drivers for Isolated Power Supplies](#).

12 Layout

12.1 Layout Guidelines

A minimum of two layers is required to accomplish a low EMI PCB design. To further improve EMI, a four layer board can be used (see [Figure 12-2](#)). Layer stacking for a four layer board should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

12.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

12.2 Layout Example

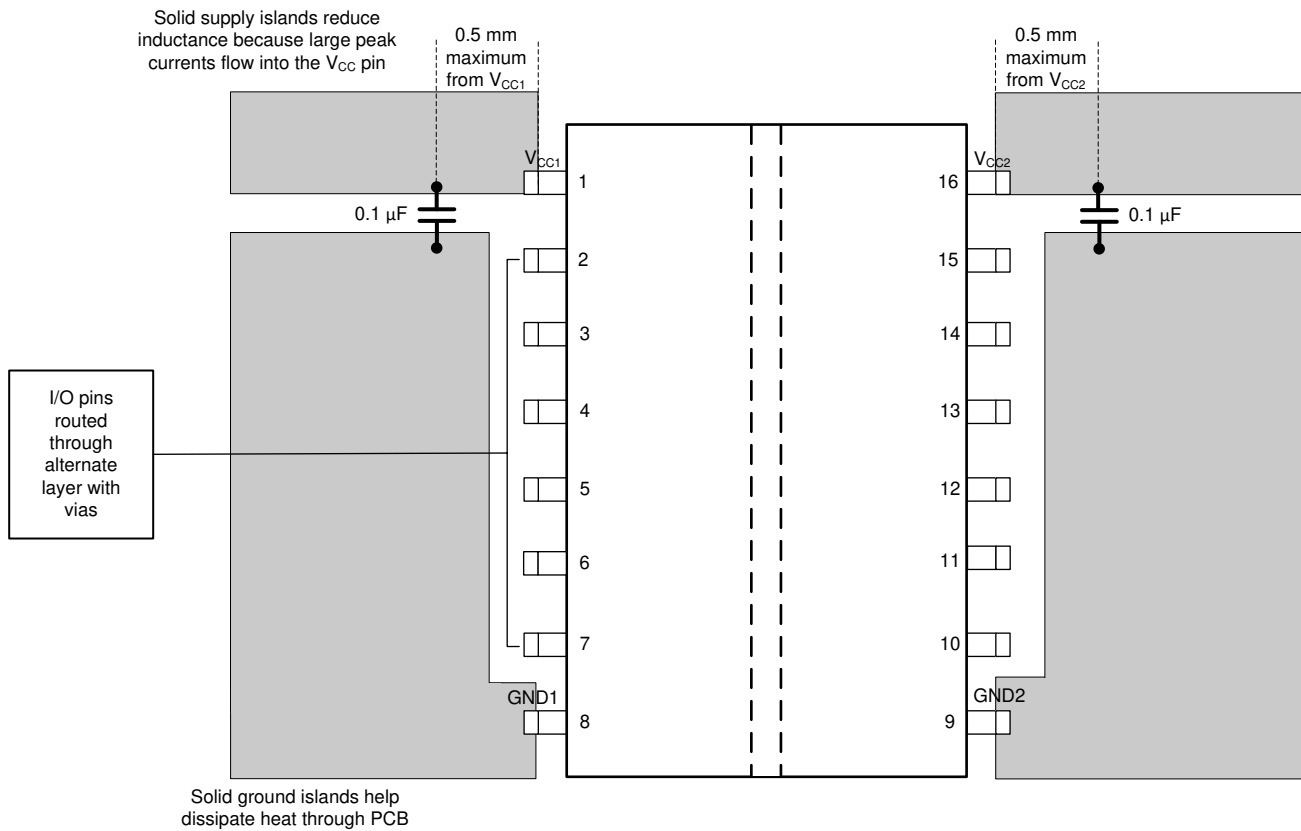


Figure 12-1. Layout Example

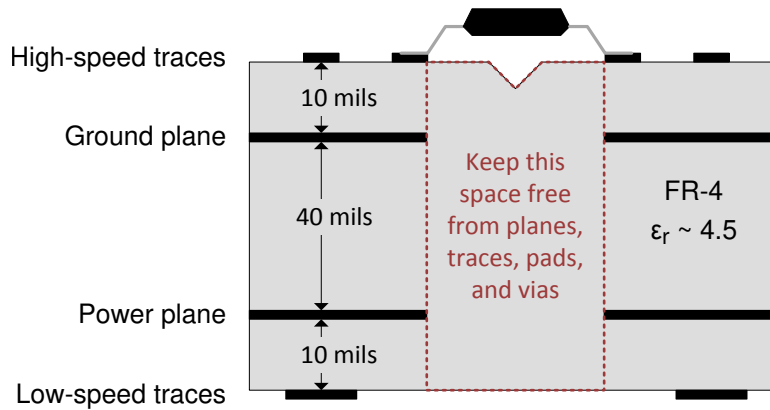


Figure 12-2. Four Layer Board Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)
- Texas Instruments, [How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems application report](#)
- Texas Instruments, [ADS79xx 12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs data sheet](#)
- Texas Instruments, [DAC161P997 Single-Wire 16-bit DAC for 4- to 20-mA Loops data sheet](#)
- Texas Instruments, [MSP430G2132 Mixed Signal Microcontroller data sheet](#)
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#)
- Texas Instruments, [TPS76333 Low-Power 150-mA Low-Dropout Linear Regulators data sheet](#)

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

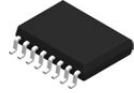
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

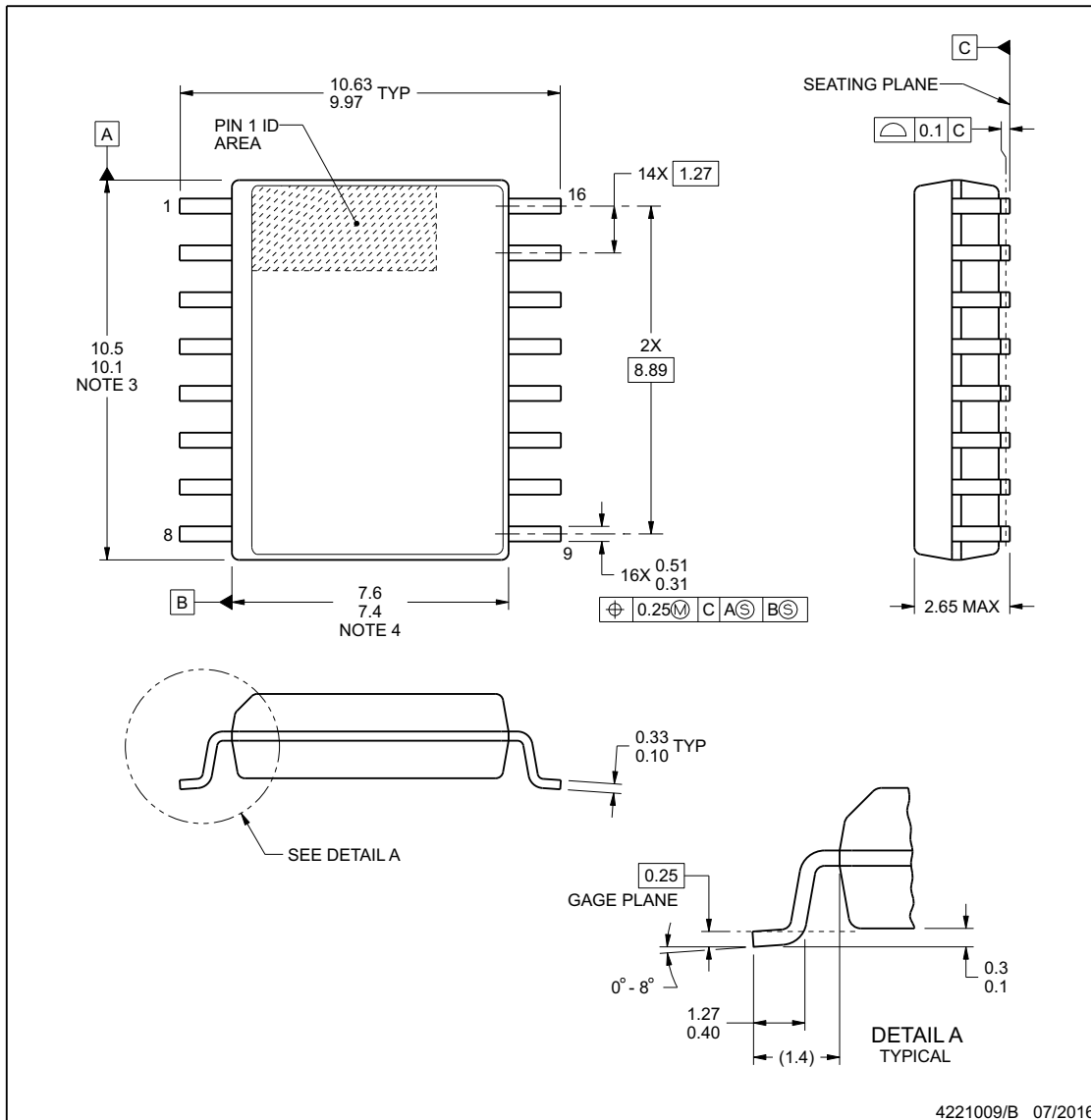
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



DW0016B

PACKAGE OUTLINE
SOIC - 2.65 mm max height

SOIC



NOTES:

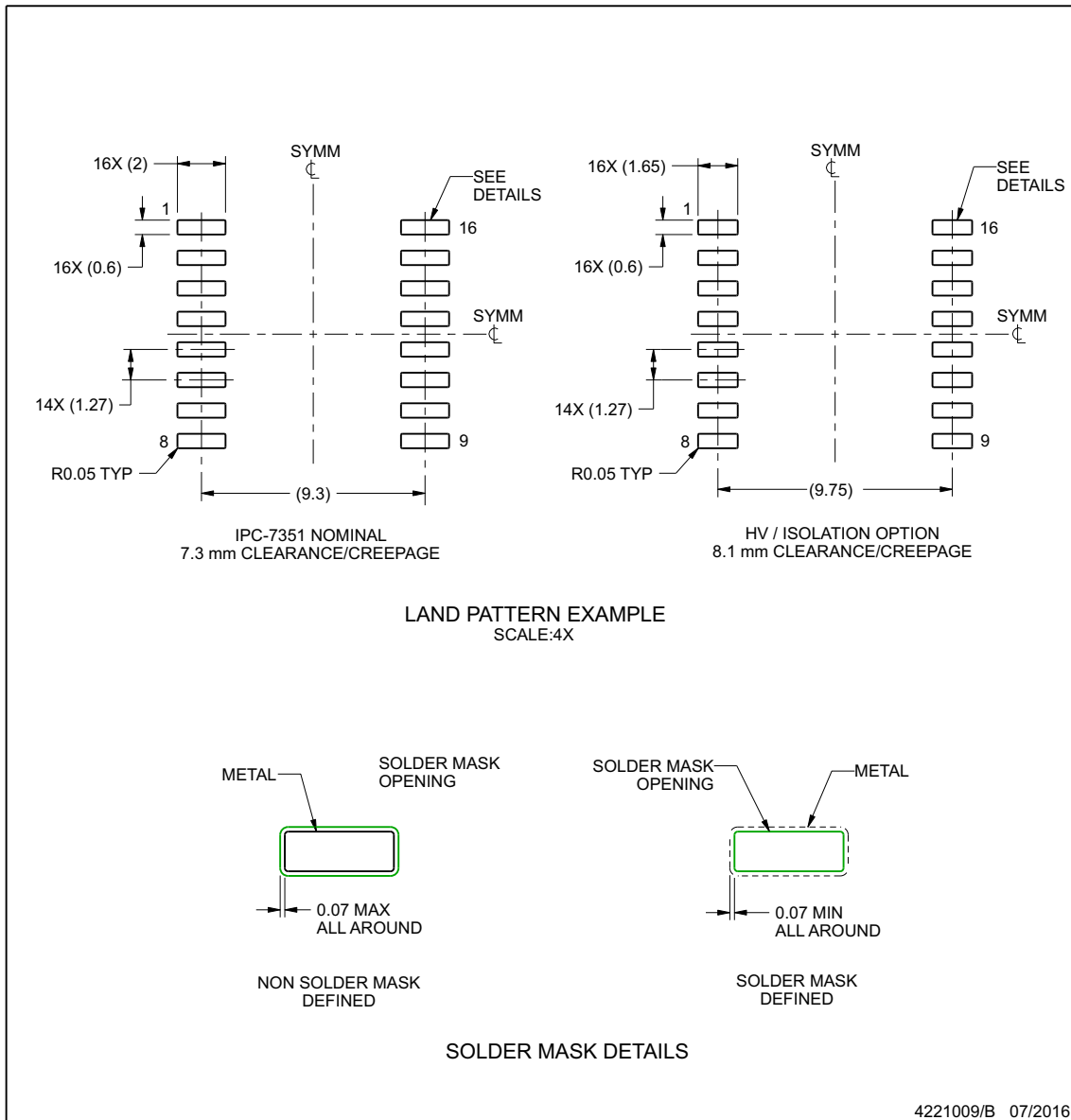
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

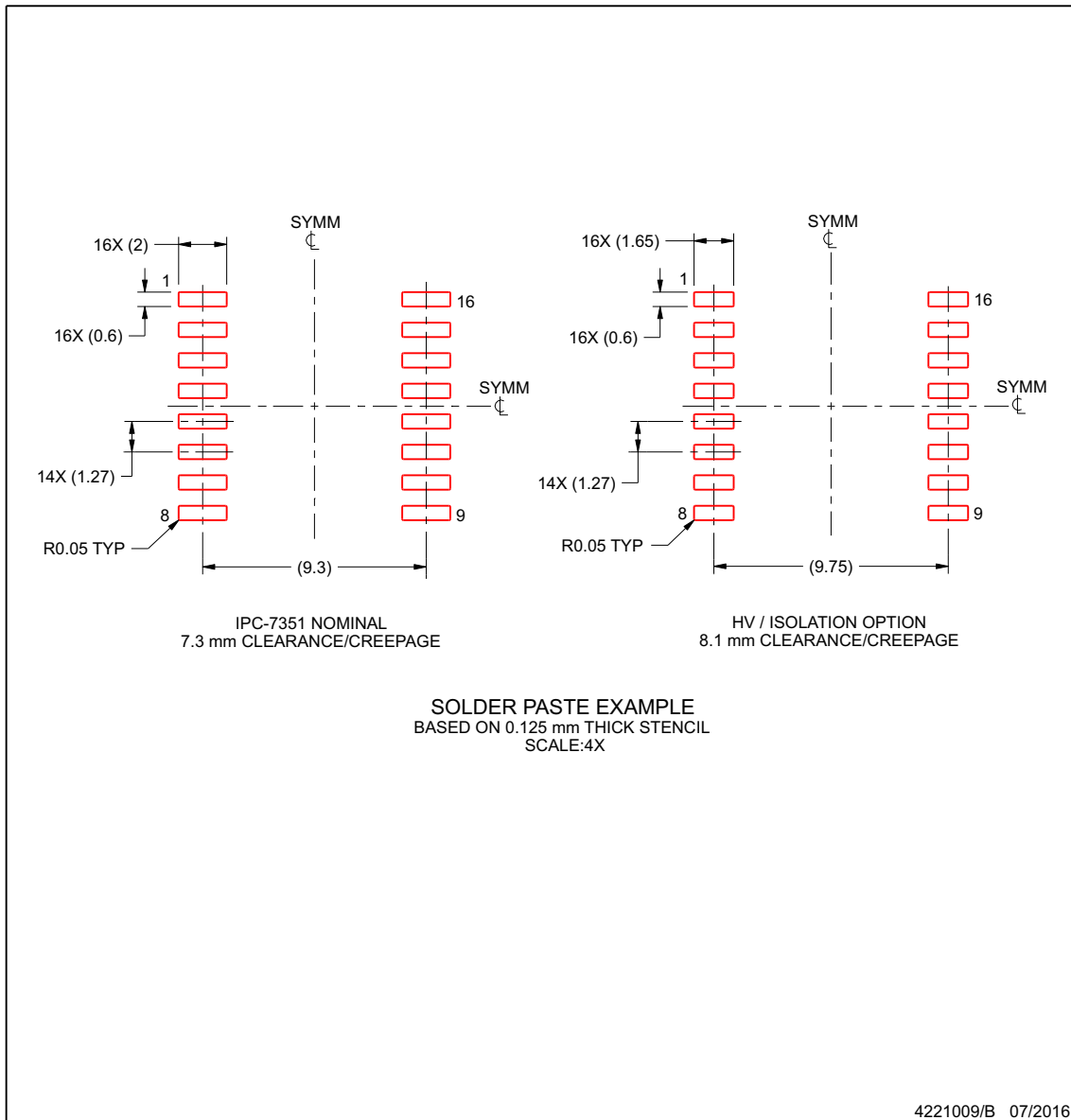
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EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO6760LDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760L	Samples
ISO6760LNDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760LN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

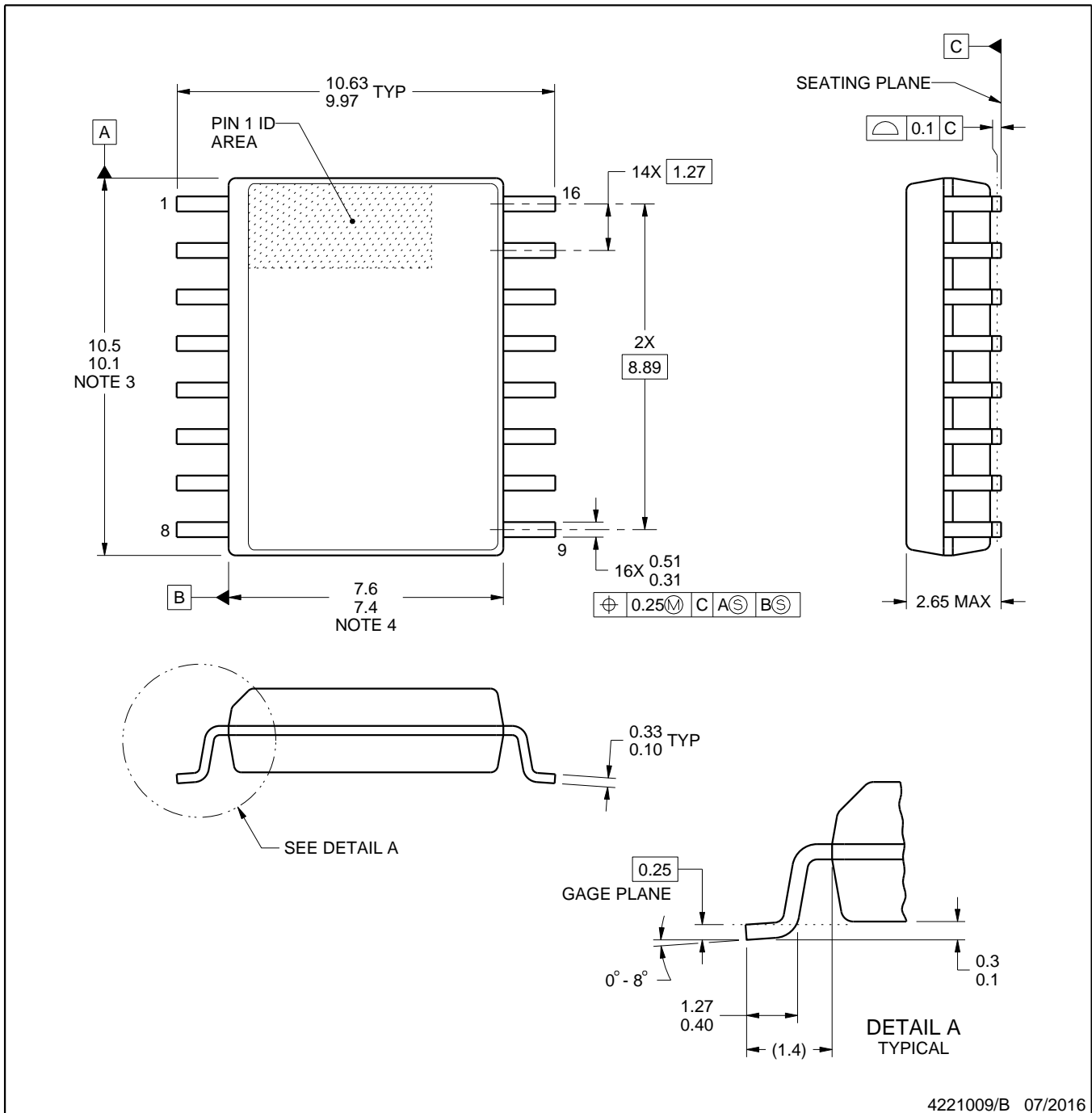


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

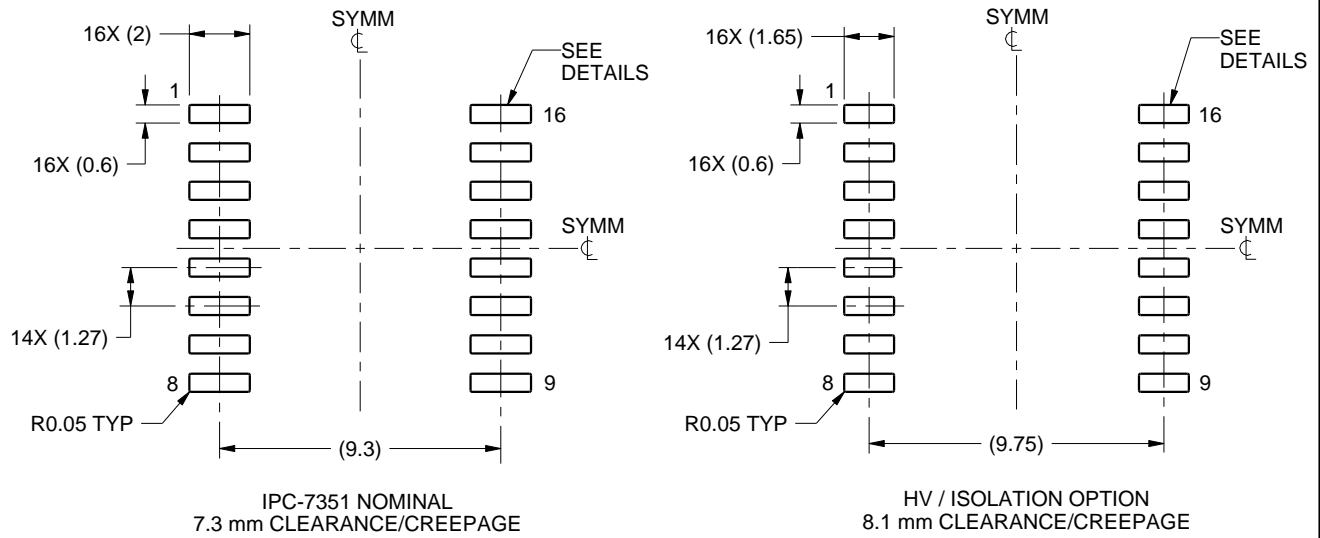
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

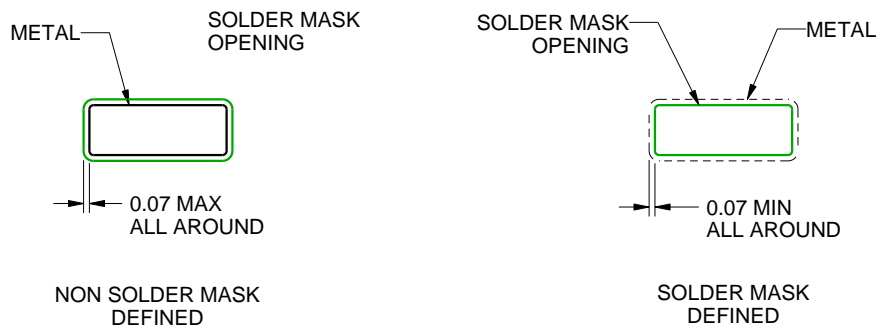
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

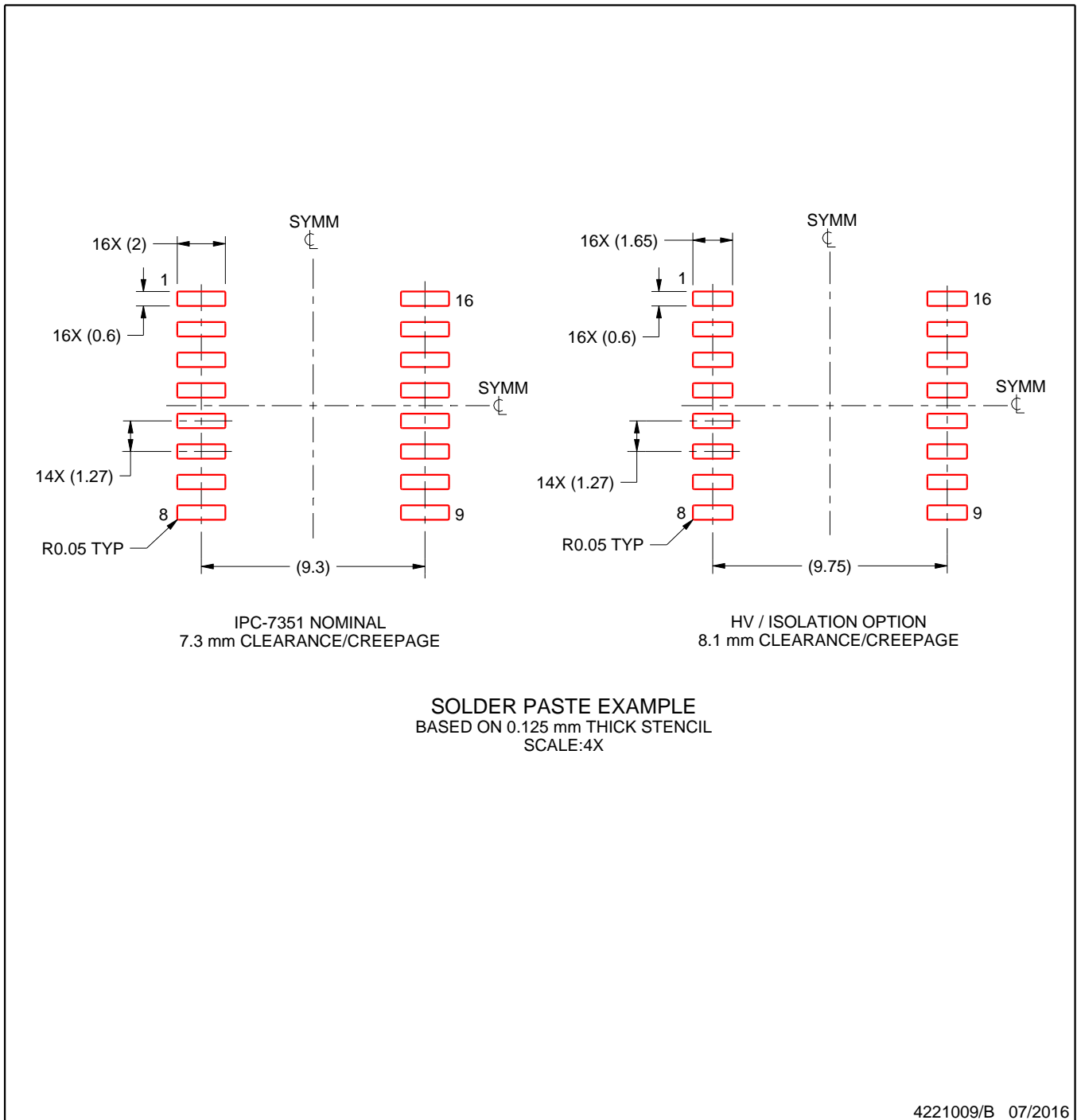
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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