WINSOURCE ELECTRONICS

THE DATASHEET OF

ISO7730QDWRQ1

MP2174C

2.7V-5.5V,4A, High-Efficiency, Synchronous Step-Down Converter with Forced CCM in 2×2mm QFN

DESCRIPTION

The MP2174C is a monolithic, step-down, switch mode converter with built-in, internal power MOSFETs. It achieves 4A of continuous output current from a 2.7V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

The constant-on-time (COT) control scheme provides fast transient response and easy loop stabilization.

Fault condition protections include cycle-by-cycle current limit and thermal shutdown.

The MP2174C requires a minimal number of readily available, standard external components, and is available in an ultra-small QFN-12 (2mmx2mm) package.

The MP2174C is ideal for a wide range of applications, including PDAs, portable instruments, DVD drives, and small handheld devices.

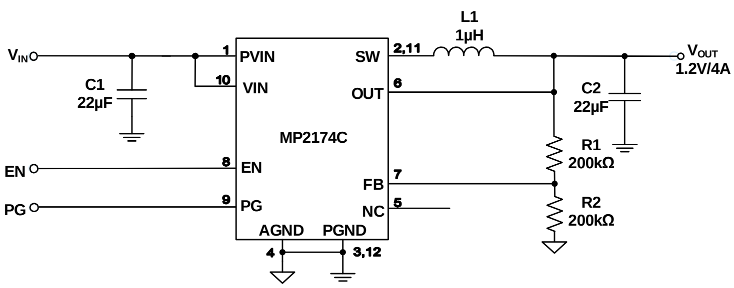
FEATURES

- Forced PWM Mode Operation
- Wide 2.7V to 5.5V Operating Input Range
- Output Voltage as Low as 0.6V
- 4A Output Current
- 35mΩ and 18mΩ Internal Power MOSFET
- Peak Efficiency Above 96%
- 1.1MHz Frequency
- 100% Duty Cycle in Dropout
- 0.5ms Internal Soft-Start Time
- EN and Power Good for Power Sequencing
- Auto-Discharge at Power-Off
- Short-Circuit Protection with Hiccup Mode
- Available in a QFN-12 (2mmx2mm) Package

APPLICATIONS

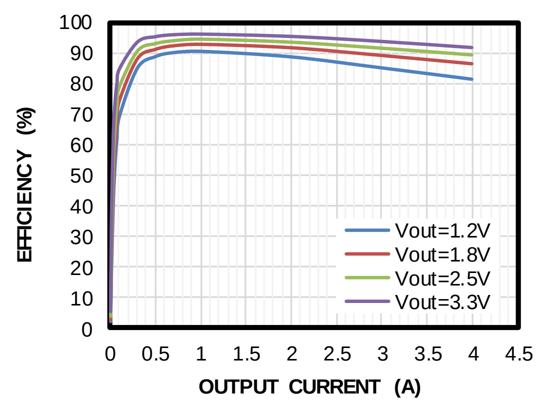
- Storage Drives
- Portable/Handheld Devices
- Low-Voltage I/O System Power

TYPICAL APPLICATION



Efficiency vs. Output Current

V_{IN} = 5V, DCR = 27mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2174CGG	QFN12 (2mm x 2mm)	*See Below*

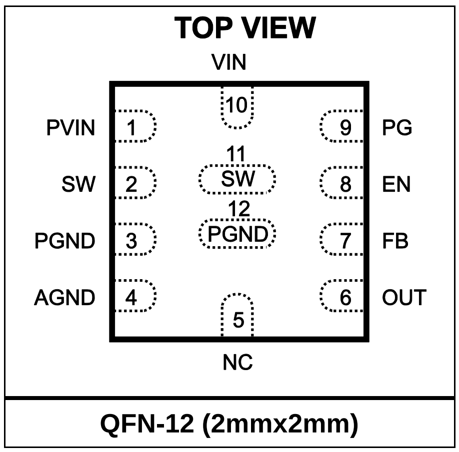
* For Tape & Reel, add suffix –Z (e.g. MP2174CGG–Z).

TOP MARKING

KCY
LLL

KC: Product code of MP2174CGG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	PVIN	**Supply voltage to power FETs.** PVIN is connected to VIN internally.
2, 11	SW	**Switch output.** Pin 2 and 11 can be connected together.
3, 12	PGND	**Power ground.** Pin 3 and 12 can be connected together.
4	AGND	**Quiet ground for controller circuits.**
5	NC	**No connection.** Leave this pin open. Do not connect it to ground.
6	OUT	**Input sense pin for output voltage.**
7	FB	**Feedback.** An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
8	EN	**On/off control.**
9	PG	**Power good indicator.** The output of this pin is an open drain pin.
10	VIN	**Supply voltage to internal control circuitry.** VIN is connected to PVIN internally.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} ....
-0.3V (-3V for <10ns) to +6.5V (8V for <10ns)
All other pins............................... -0.3V to +6.5V
Junction temperature .... 150°C
Lead temperature .... 260°C
Continuous power dissipation (T_A = 25°C) (2)
…………….. ....1.6W
Storage temperature................ -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .... 2.7V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-12 (2mmx2mm)
EV2174C-G-00A (4)..................45........ 8....°C/W
JESD51-7 (5)………...........…....80.......16...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV2174C-G-00A, 2-layer PCB, 63mmx63mm.
5) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_A = -40°C to +125°C [(6)], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage	V_{FB}	2.7V ≤ V_{IN} ≤ 5.5V T_J = 25°C	594	600	606	mV
Feedback voltage	V_{FB}	2.7V ≤ V_{IN} ≤ 5.5V	588	600	612	mV
Feedback current	I_{FB}	V_{FB} = 0.63V		10	50	nA
PFET switch on resistance	R_{DSON_P}	V_{IN} = 5V		35		mΩ
NFET switch on resistance	R_{DSON_N}	V_{IN} = 5V		18		mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 5.5V, V_{SW} = 0V and 5.5V, T_J = 25°C		0	5	μA
PFET peak current limit [(7)]		T_J = 25°C	5	6.5		A
NFET valley current limit [(7)]				4.5		A
On time	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V		220		ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V		300		
Switching frequency	f_{SW}	V_{OUT} = 1.2V		1100		kHz
Minimum off time	$t_{MIN-OFF}$			100		ns
Minimum on time [(7)]	t_{MIN-On}			80		ns
Soft-start time	t_{SS-ON}	From 10% V_{OUT} to 90% V_{OUT}		0.5	1	ms
Soft-stop time	t_{SS-OFF}	From 90% V_{OUT} to 10% V_{OUT}			0.3	ms
EN off delay		V_{EN} off to 90% V_{OUT} drop			0.4	ms
Power good upper trip threshold		FB with respect to the regulation		+10		%
Power good lower trip threshold				-10		%
Power good delay		Rising		90		μs
Power good sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
Power good logic high voltage	V_{PG_HI}	V_{IN} = 5V, V_{FB} = 0.63V	4.9			V
Under-voltage lockout threshold rising		-40°C ≤ T_J ≤ +85°C		2.48	2.68	V
Under-voltage lockout threshold hysteresis				450		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_A = -40°C to +125°C [6], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN turn-on delay [7]		EN on to SW active		255		μs
EN rising threshold			0.5	0.65	0.9	V
EN hysteresis				0.09		V
EN input current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		μA
Supply current (shutdown)		V_{EN} = 0V, T_J = 25°C		0	1	μA
Supply current (quiescent)		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V, T_J = 25°C		500		μA
Thermal shutdown [7]				155		°C
Thermal hysteresis [7]				25		°C

Notes:

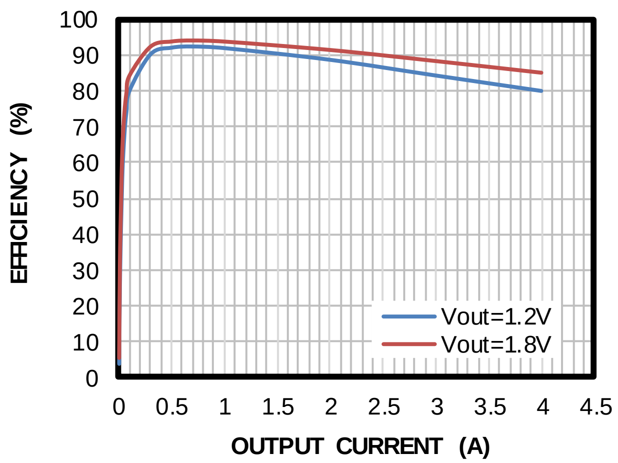
6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, T_A = 25°C, unless otherwise noted.

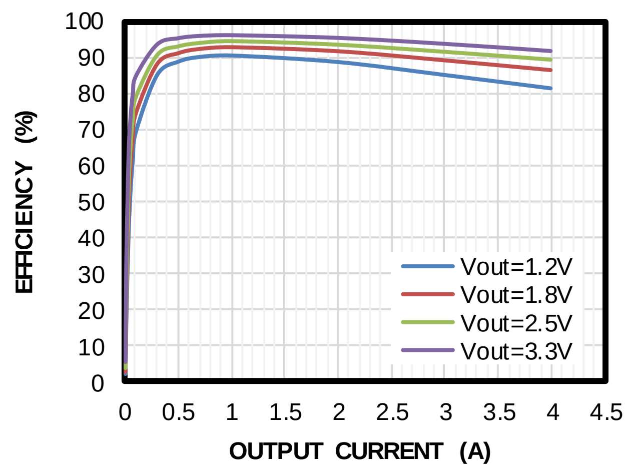
Efficiency vs. Output Current

V_{IN} = 3.3V



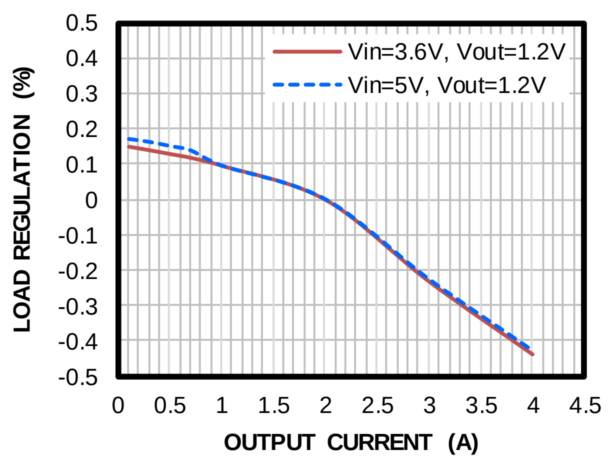
Efficiency vs. Output Current

V_{IN} = 5V



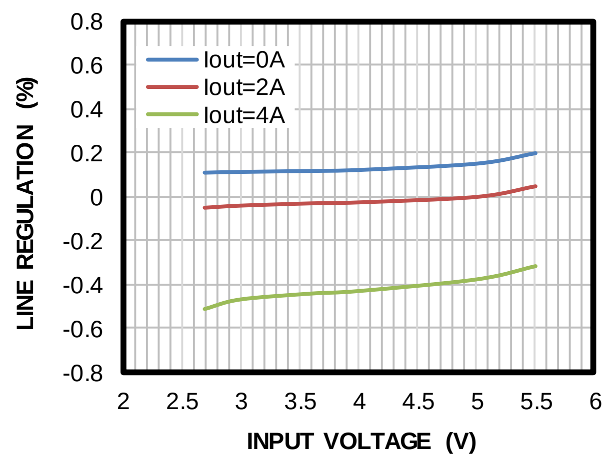
Load Regulation vs. Output Current

V_{IN} = 3.6V/5V, I_{OUT} = 0.1A to 4A

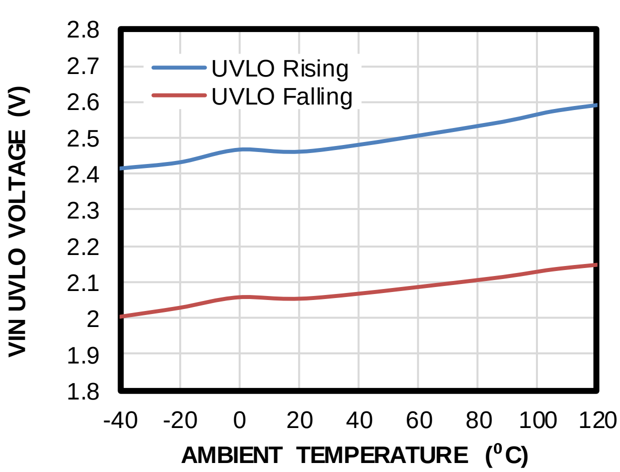


Line Regulation vs. Output Current

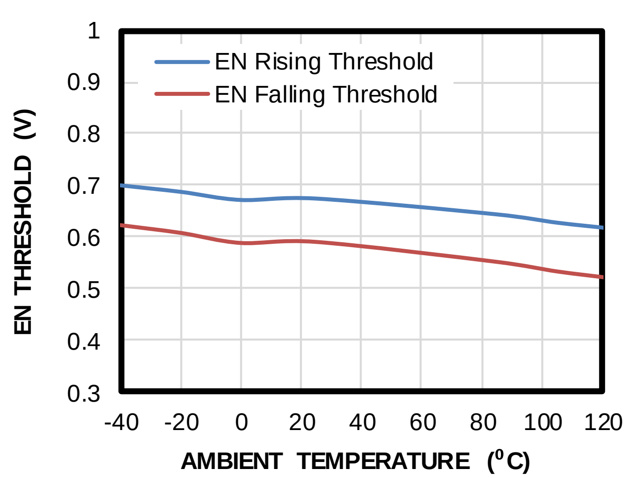
V_{IN} = 2.7V to 5.5V



VIN UVLO vs. Temperature



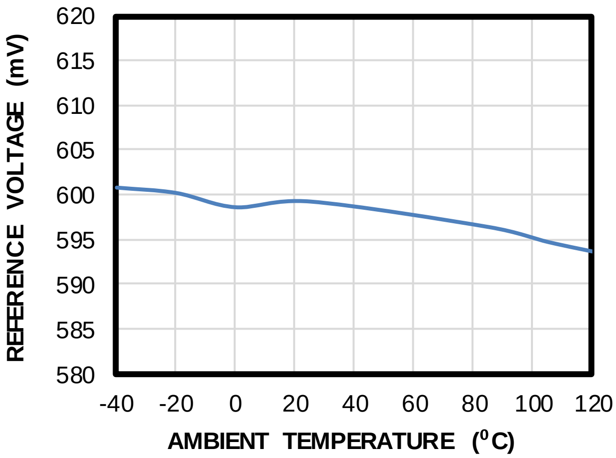
EN Threshold vs. Temperature



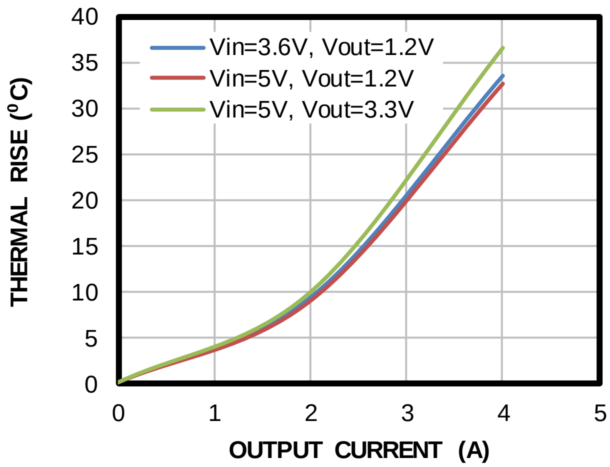
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, T_A = 25°C, unless otherwise noted.

Reference Voltage vs. Temperature



Thermal Rise vs. Output Current

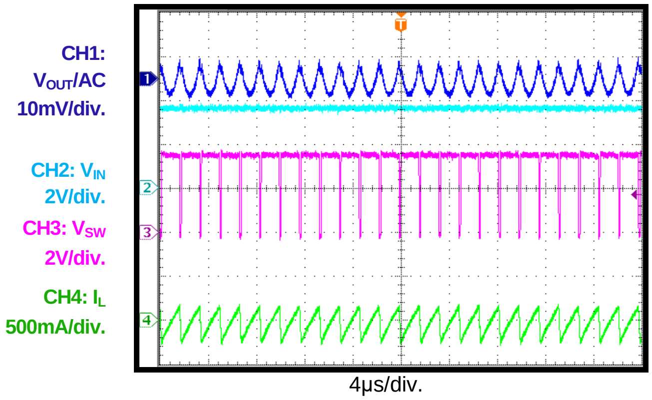


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, T_A = 25°C, unless otherwise noted.

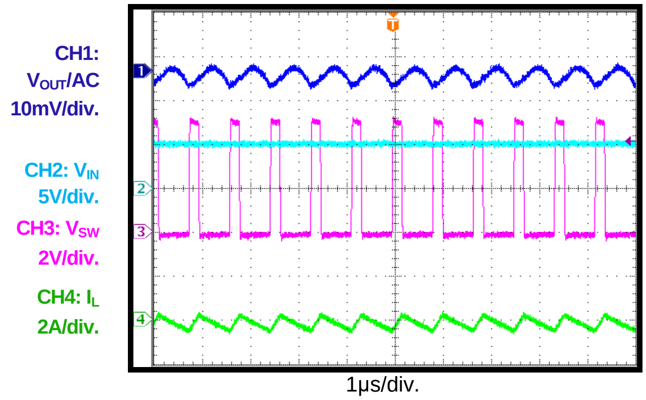
Output Ripple

V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 0A



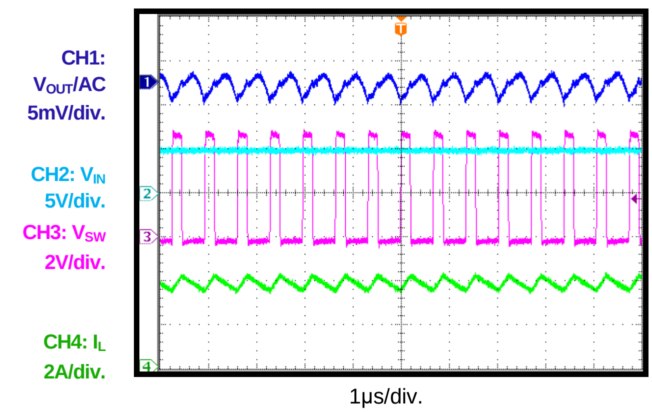
Output Ripple

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



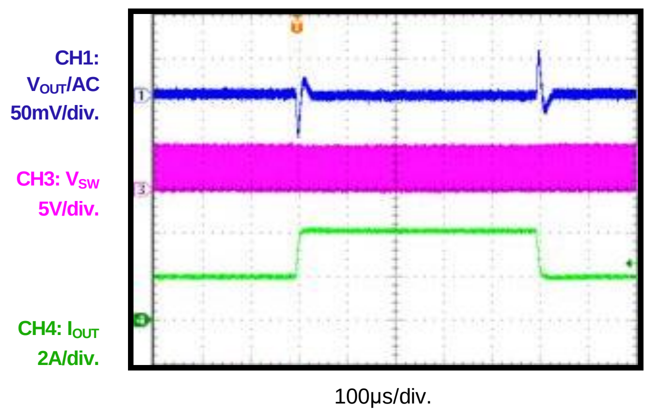
Output Ripple

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 4A



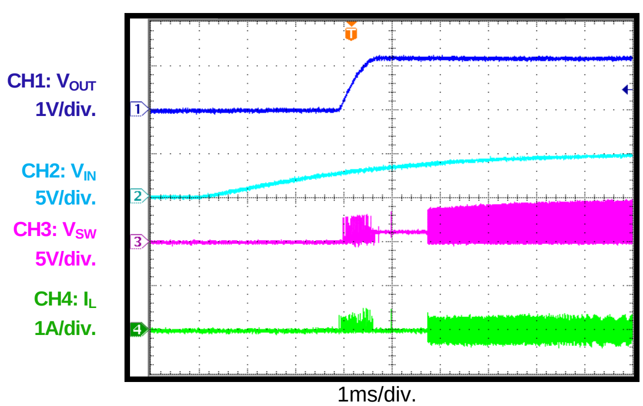
Transient

I_{OUT} = 2A to 4A, 2.5A/µs



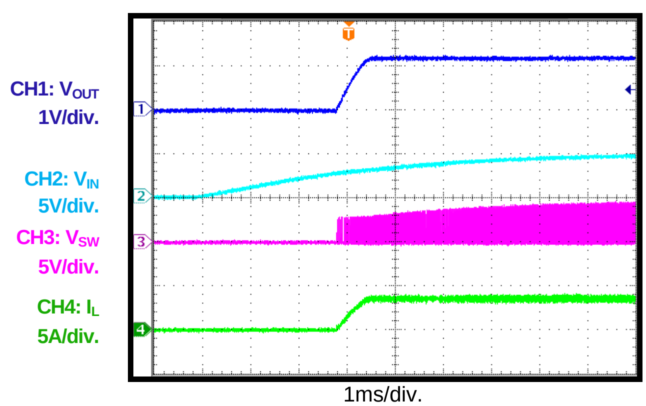
VIN Start-Up

I_{OUT} = 0A



VIN Start-Up

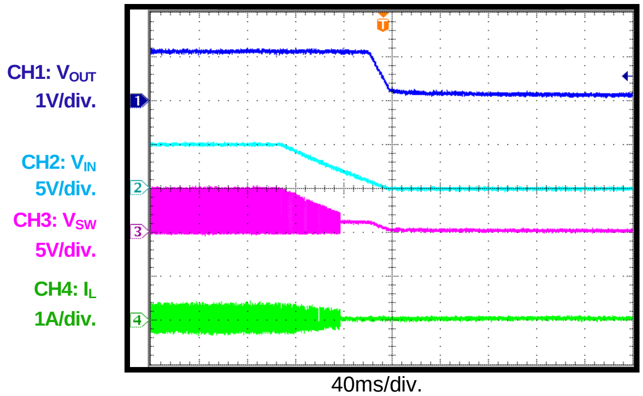
I_{OUT} = 4A



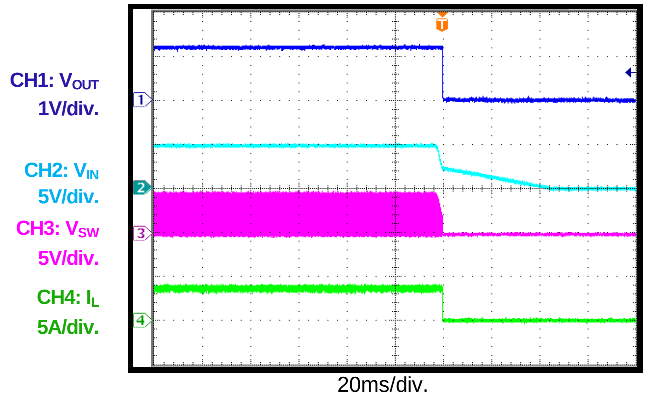
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, T_A = 25°C, unless otherwise noted.

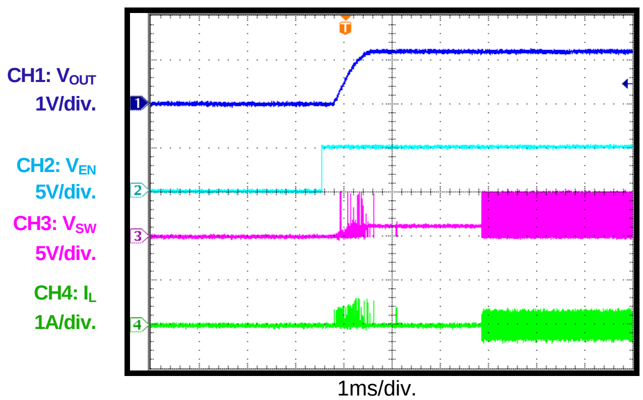
VIN Shutdown
I_{OUT} = 0A



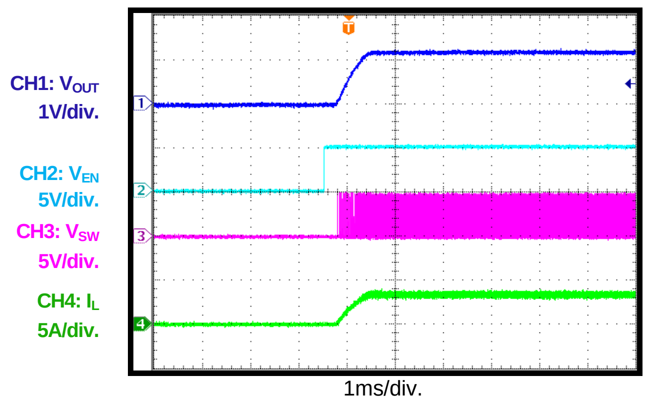
VIN Shutdown
I_{OUT} = 4A



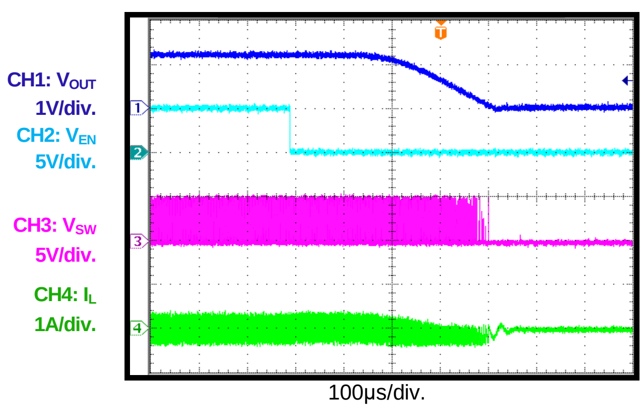
EN Start-Up
I_{OUT} = 0A



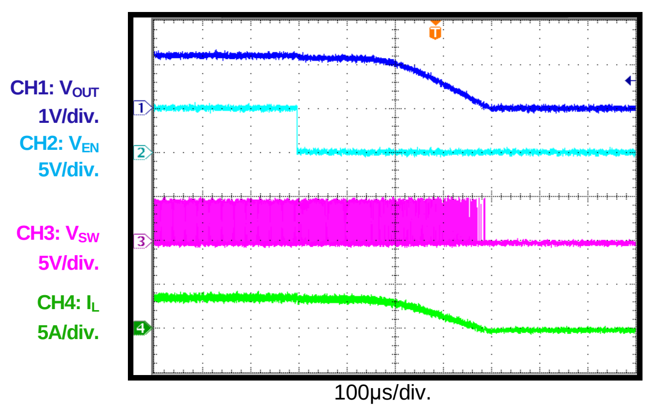
EN Start-Up
I_{OUT} = 4A



EN Shutdown
I_{OUT} = 0A



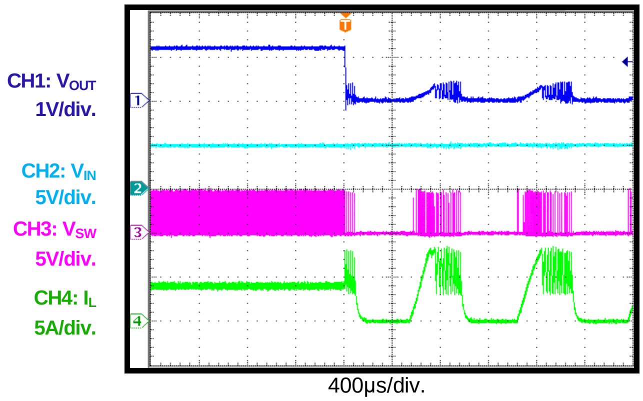
EN Shutdown
I_{OUT} = 4A



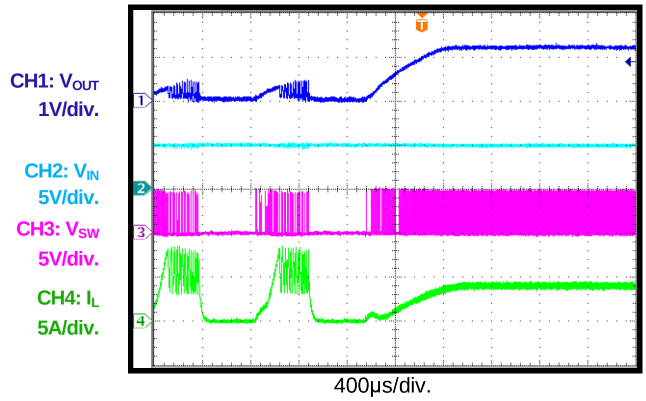
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, T_A = 25°C, unless otherwise noted.

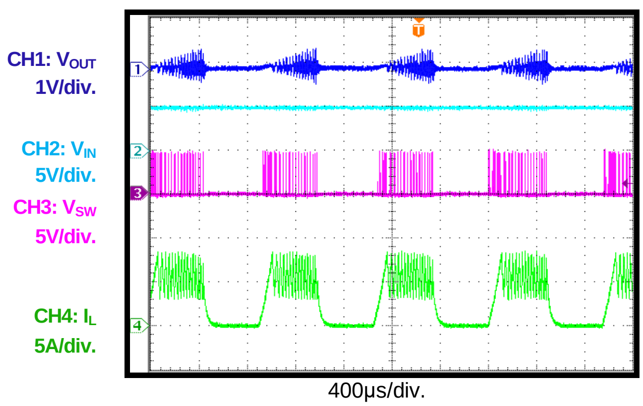
SCP Entry
I_{OUT} = 4A



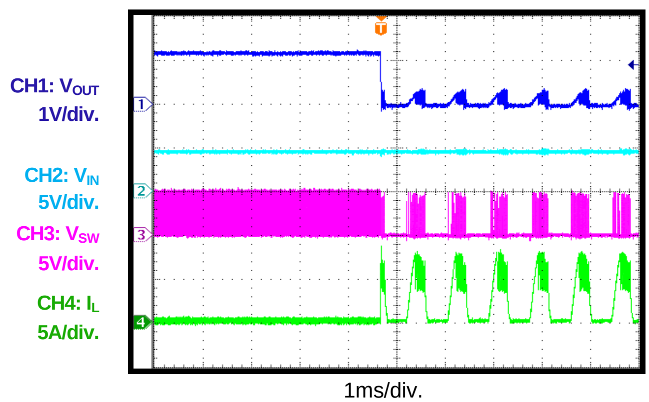
SCP Recovery
I_{OUT} = 4A



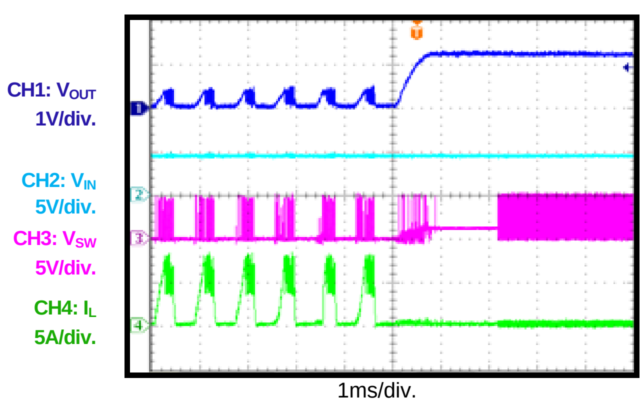
SCP State
I_{OUT} = 4A



SCP Entry
I_{OUT} = 0A



SCP Recovery
I_{OUT} = 0A



FUNCTIONAL BLOCK DIAGRAM

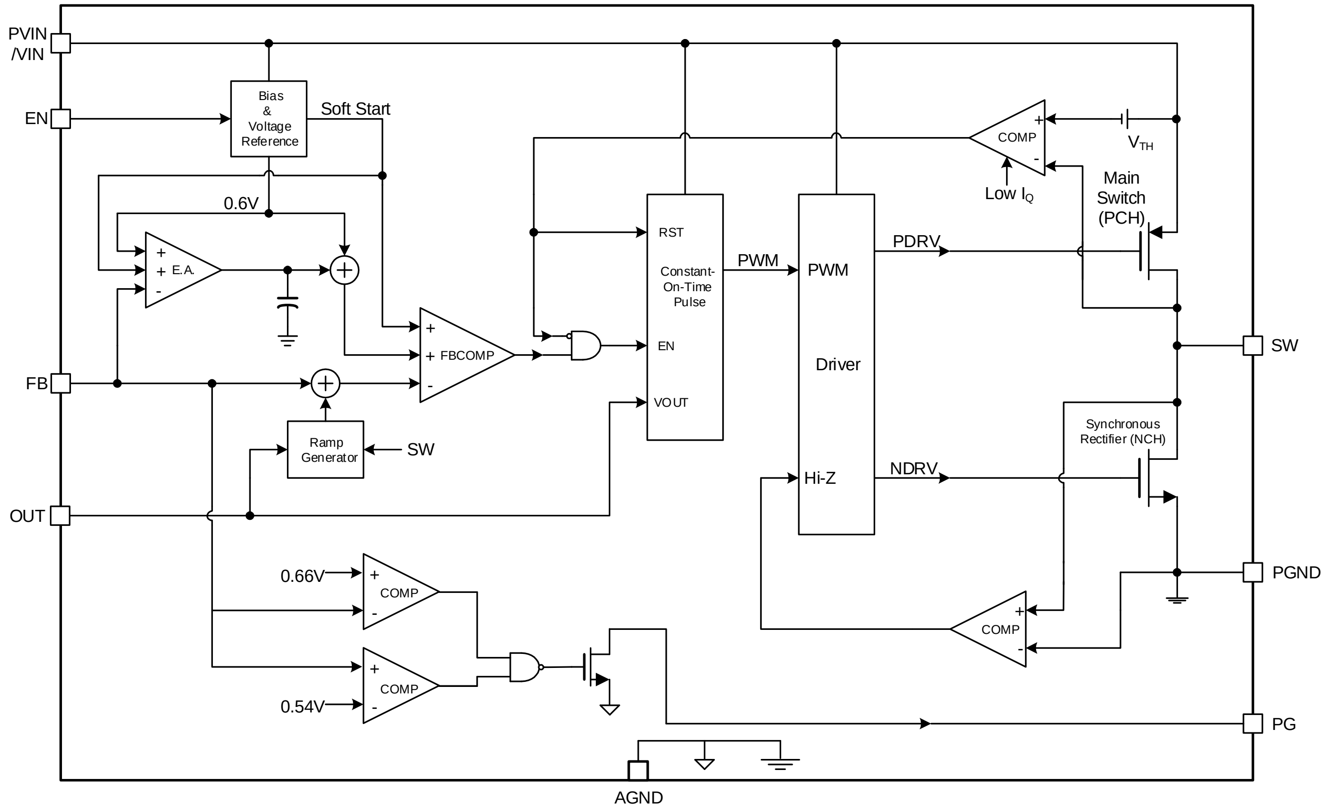


Figure 1: Functional Block Diagram

OPERATION

The MP2174C uses constant-on-time control with input voltage feed forward to stabilize the switching frequency over the full input range.

Constant-On-Time Control

Compare to fixed-frequency PWM control, constant-on-time control offers the advantage of a simpler control loop and faster transient response. By using input voltage feed forward, the MP2174C maintains a nearly constant switching frequency across the input and output voltage ranges. The on-time of the switching pulse can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.909\mu s \qquad (1)$$

To prevent inductor current runaway during load transient, the MP2174C limits the minimum off time to 100ns. This minimum off time limit does not affect the operation of the MP2174C in steady state in any way.

Forced PWM Operation

The MP2174C works in continuous conduction mode (CCM) to achieve a smaller V_O ripple, load regulation, and load transient across the full load range.

Enable

When the input voltage exceeds the under-voltage lockout (UVLO) threshold (typically 2.5V), the MP2174C can be enabled by pulling the EN pin above 0.65V (typical). Leaving EN below 0.55V (typical) or floating it disables the MP2174C. There is an internal 1MΩ resistor from the EN pin to ground.

When EN is pulled down, there is a discharge path for output. All processes, from EN turning off to the output dropping to 0V, take less than 0.8ms.

Soft Start/Stop

The MP2174C has a built-in soft start that ramps up the output voltage in a controlled slew rate, avoiding overshoot at start-up. The soft-start time is typically about 0.5ms.

When disabled, the MP2174C ramps down the internal reference and allows the load to linearly discharge the output. The soft-stop time is less than 0.3ms.

Power Good Indicator

The MP2174C has an open-drain output. The PG pin requires an external pull-up resistor (100kΩ to 500kΩ) for the power good indicator.

When the FB pin is within ±10% of the regulation voltage (i.e. 0.6V), the PG pin is pulled up. If the FB voltage is out of the ±10% window, PG is pulled down to ground by an internal MOSFET. The MOSFET has a maximum $R_{DS(ON)}$ of less than 100Ω.

Current Limit

The MP2174C has a typical 6.5A current limit for the HS-FET, and a 4.5A current limit for the LS-FET. Once the high-side switch hits current limit, the MP2174C turns off the HS-FET and turns on the LS-FET to reduce the inductor current. When the inductor current drops to the valley current limit, the LS-FET turns off and the HS-FET turns on. If the HS-FET reaches the peak current limit and the LS-FET reaches the valley current limit every cycle for 150µs, the MP2174C remains in hiccup mode until the current decreases. This prevents the inductor current from continuing to build up, which could result in damage to the components.

Short Circuit and Recovery

If the output voltage of the buck converter is shorted to GND, the current limit is triggered. If the current limit is triggered every cycle for 150µs, the MP2174C enters hiccup mode. It disables the output power stage, discharges the soft-start capacitor, and then automatically retries soft start. If the short-circuit condition still remains after soft start ends, the MP2174C repeats this operation cycle until the short condition is removed and the output rises back to the regulation level.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the Typical Application Circuit section on page 15). Choose a larger resistance for lower leakage or a smaller one to avoid noise. Choose R1 to be between 120kΩ and 200kΩ. R2 is then calculated using Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

Figure 2 shows the feedback circuit.

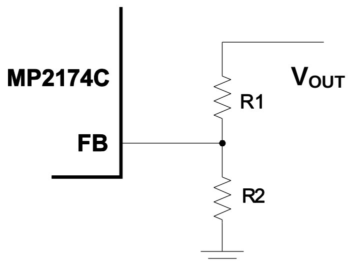


Figure 2: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Inductor

A 0.82µH to 4.7µH inductor is recommended for most applications. For highest efficiency, the inductor DC resistance should be small. For most designs, the inductance value can be determined with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. Calculated the maximum inductor peak current with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and a capacitor is required to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. For a higher output voltage, a 47µF capacitor may be needed to stabilize the system.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

An output capacitor (C2) is required to maintain the DC output voltage.

Low-ESR ceramic capacitors can be used with the MP2174C to keep the output ripple low. Generally, a 10μF output ceramic capacitor is sufficient. In higher output voltage conditions, a 22μF capacitor may be needed for system stability.

Using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and is the main cause of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{8}$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \tag{9}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 3 and follow the guidelines below:

1. Place the input decoupling capacitor as close as possible to the IC pins, pin 1 and pin 3 (an 0805 ceramic capacitor is used).
2. Ensure the two ends of the ceramic capacitor are connected directly to PVIN (pin 1) and PGND (pin 3).

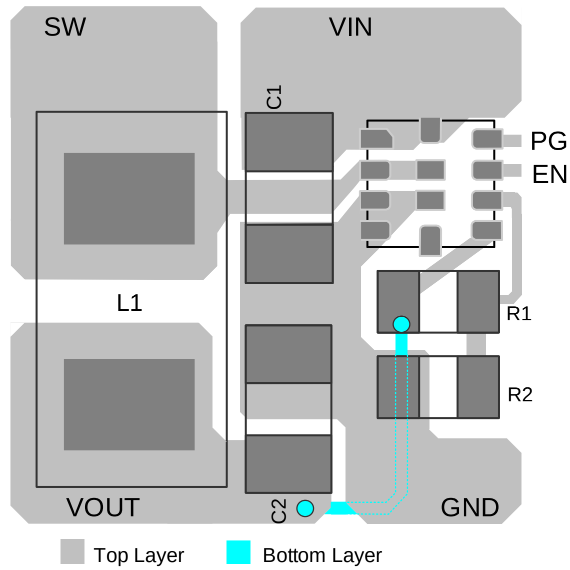


Figure 3: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

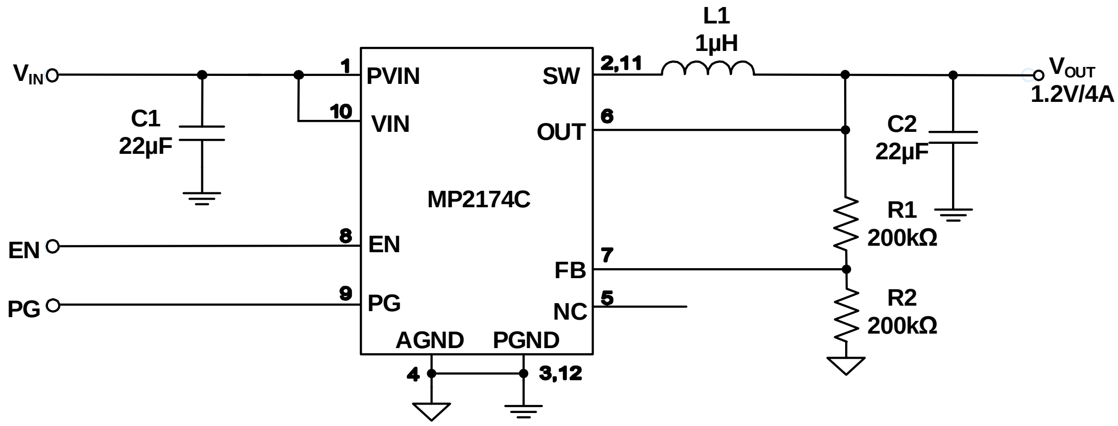
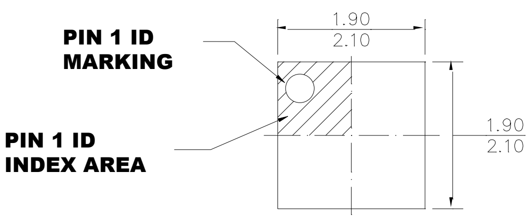


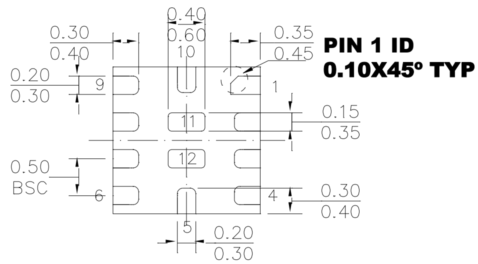
Figure 4: $5V_{IN}$, 1.2 V/4A

PACKAGE INFORMATION

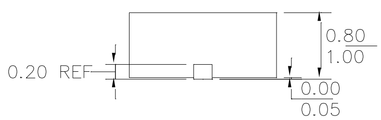
QFN-12 (2mmx2mm)



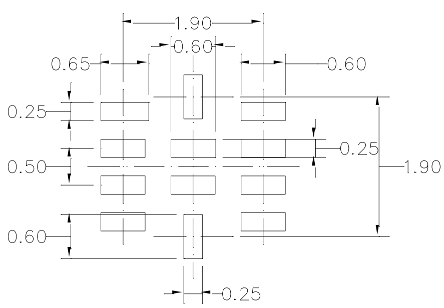
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.