WINSOURCE ELECTRONICS

# THE DATASHEET OF

# CY62128DV30LL-70ZI

# 1-Mb (128K x 8) Static RAM

## Features

- **Very high speed: 55 and 70 ns**
- **Wide voltage range: 2.2V to 3.6V**
- **Pin compatible with CY62128V**
- **Ultra-low active power**
  - **— Typical active current: 0.85 mA @ f = 1 MHz**
  - **— Typical active current: 5 mA @ f = $f_{MAX}$**
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{CE}_1$, $CE_2$, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **Available in Pb-free and non Pb-free 32-lead SOIC, 32-lead TSOP and 32-lead Small TSOP, non Pb-free 32-lead Reverse TSOP packages**

## Functional Description[1]

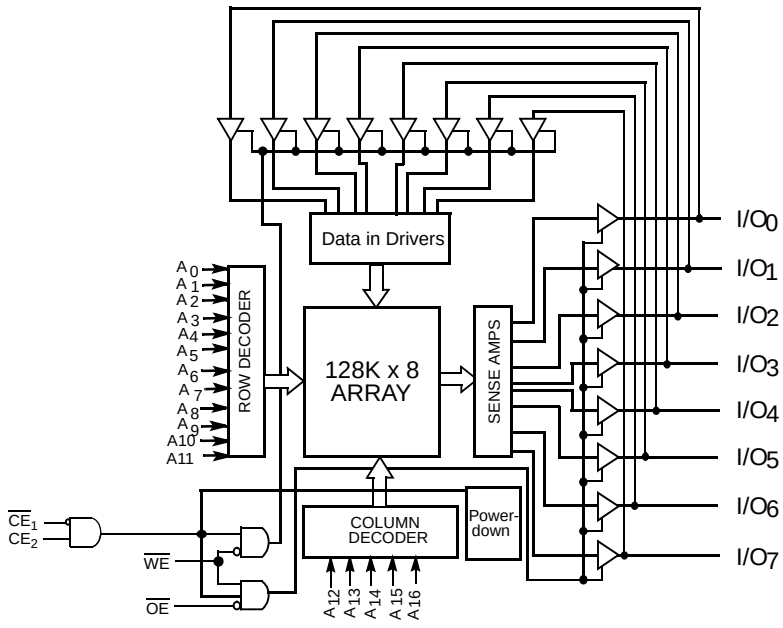
The CY62128DV30 is a high-performance CMOS static RAM organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 ($CE_2$) LOW. The input/output pins ($I/O_0$ through $I/O_7$) are placed in a high-impedance state when: deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 ($CE_2$) LOW, outputs are disabled ($\overline{OE}$ HIGH), or during a write operation (Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 ($CE_2$) HIGH and Write Enable ($\overline{WE}$) LOW).

Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) LOW with Chip Enable 2 ($CE_2$) HIGH and Write Enable ($\overline{WE}$) LOW. Data on the eight I/O pins is then written into the location specified on the Address pin ($A_0$ through $A_{16}$).

Reading from the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) LOW with Chip Enable 2 ($CE_2$) HIGH and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

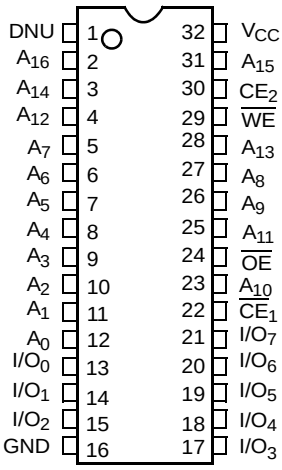
The eight input/output pins ($I/O_0$ through $I/O_7$) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW), the outputs are disabled ($\overline{OE}$ HIGH) or during a write operation ($\overline{CE}_1$ LOW, $CE_2$ HIGH), and $\overline{WE}$ LOW).

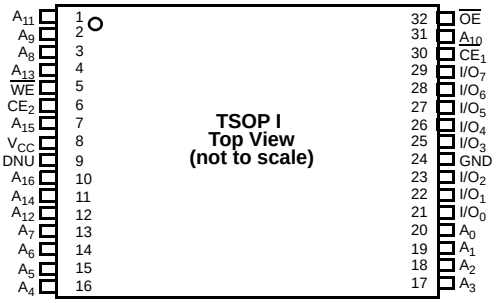
## Logic Block Diagram

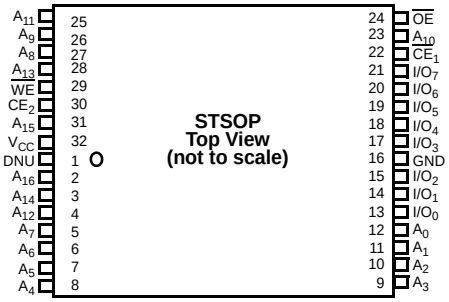


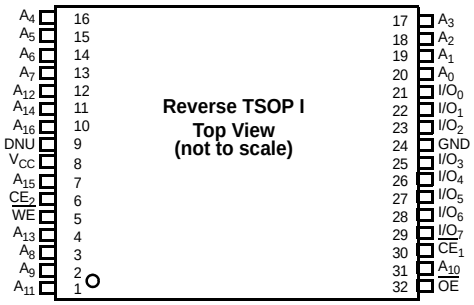

**Note:**
1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

## Pin Configurations[2]




## Product Portfolio

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Operating, $I_{CC}$ (mA) | | | | Standby, $I_{SB2}$ (µA) | |
| | | | | | f = 1 MHz | | f = $f_{MAX}$ | | | |
| | Min. | Typ. | Max. | | Typ.[4] | Max. | Typ.[4] | Max. | Typ.[4] | Max. |
| CY62128DV30L | 2.2 | 3.0 | 3.6 | 55/70 | 0.85 | 1.5 | 5 | 10 | 1.5 | 5 |
| CY62128DV30LL | | | | 55/70 | 0.85 | 1.5 | 5 | 10 | 1.5 | 4 |

**Notes:**
2. NC pins are not connected to the die.
3. DNU pins have to be left floating or tied to Vss to ensure proper application.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.3V to 3.9V

DC Voltage Applied to Outputs in High-Z State[5] ..... –0.3V to $V_{CC}$ + 0.3V

DC Input Voltage[5] ..... –0.3V to $V_{CC}$ + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

## Operating Range

| Range | Ambient Temperature ($T_A$) | $V_{CC}$[6] |
|---|---|---|
| Industrial | –40°C to +85°C | 2.2V to 3.6V |

## DC Electrical Characteristics (Over the Operating Range)

| Parameter | Description | Test Conditions | | | CY62128DV30-55/70 Min. | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OH}$ = –0.1 mA | | 2.0 | | | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OH}$ = –1.0 mA | | 2.4 | | | |
| $V_{OL}$ | Output LOW Voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OL}$ = 0.1 mA | | | | 0.4 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OL}$ = 2.1 mA | | | | 0.4 | |
| $V_{IH}$ | Input HIGH Voltage | $2.2 \le V_{CC} \le 2.7$ | | | 1.8 | | $V_{CC}$ + 0.3 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | | 2.2 | | $V_{CC}$ + 0.3 | |
| $V_{IL}$ | Input LOW Voltage | $2.2 \le V_{CC} \le 2.7$ | | | –0.3 | | 0.6 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | | –0.3 | | 0.8 | |
| $I_{IX}$ | Input Leakage Current | $GND \le V_I \le V_{CC}$ | | | –1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | $GND \le V_O \le V_{CC}$, Output Disabled | | | –1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $f = f_{MAX} = 1/t_{RC}$ | $V_{CC}$ = 3.6V, $I_{OUT}$ = 0mA, CMOS level | | | 5 | 10 | mA |
| | | f = 1 MHz | | | | 0.85 | 1.5 | |
| $I_{SB1}$ | Automatic CE Power-down Current – CMOS Inputs | $\overline{CE}_1 \ge V_{CC}$ – 0.2V, $CE_2 \le 0.2$V, $V_{IN} \ge V_{CC}$ – 0.2V, $V_{IN} \le 0.2$V, f = $f_{MAX}$ (Address and Data Only), f = 0 (OE, WE,) | | L | | 1.5 | 5 | µA |
| | | | | LL | | 1.5 | 4 | |
| $I_{SB2}$ | Automatic CE Power-down Current – CMOS Inputs | $\overline{CE}_1 \ge V_{CC}$ – 0.2V, $CE_2 \le 0.2$V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le 0.2$V, f = 0, $V_{CC}$=3.6V | | L | | 1.5 | 5 | µA |
| | | | | LL | | 1.5 | 4 | |

## Capacitance[7]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz $V_{CC}$ = $V_{CC(typ)}$ | 8 | pF |
| $C_{OUT}$ | Output Capacitance | | 8 | pF |

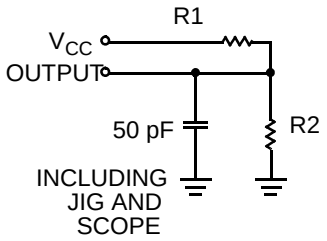
## Thermal Resistance[7]

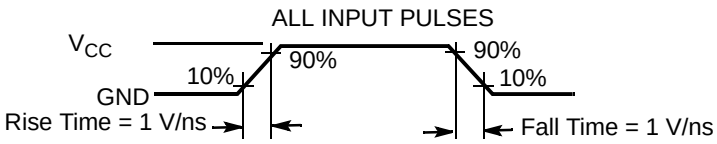
| Parameter | Description | Test Conditions | SOIC | TSOP I | RTSOP | STSOP | Unit |
|---|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board | 69 | 93 | 93 | 65 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction to Case) | | 34 | 17 | 17 | 15 | °C/W |

**Notes:**

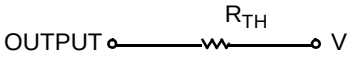
5. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns. $V_{IH(max.)}$ = $V_{CC}$+0.75V for pulse durations less than 20 ns.
6. Full device operation requires linear ramp of $V_{CC}$ from 0V to $V_{CC(min)}$ and $V_{CC}$ must be stable at $V_{CC(min)}$ for 500 µ s.
7. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms[8]




Equivalent to: THEVENIN EQUIVALENT

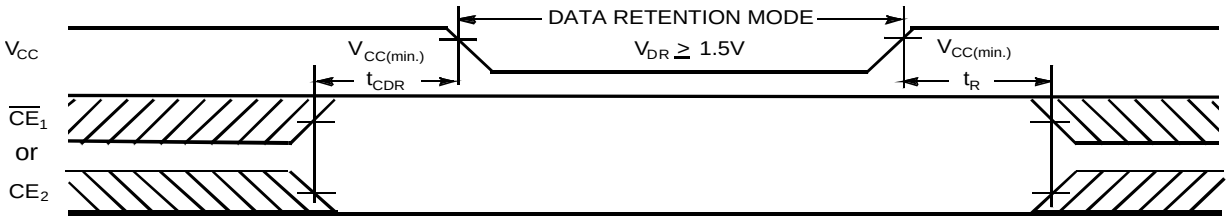



| Parameters | 2.5V (2.2V - 2.7V) | 3.0V (2.7V - 3.6V) | Unit |
|---|---|---|---|
| R1 | 16600 | 1103 | Ω |
| R2 | 15400 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

## Data Retention Characteristics

| Parameter | Description | Conditions | | Min. | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | | 1.5 | | | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}$ = 1.5V, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | L | | | 4 | µA |
| | | | LL | | | 3 | |
| $t_{CDR}$[4] | Chip Deselect to Data Retention Time | | | 0 | | | ns |
| $t_R$[8] | Operation Recovery Time | | | 100 | | | µs |

## Data Retention Waveform



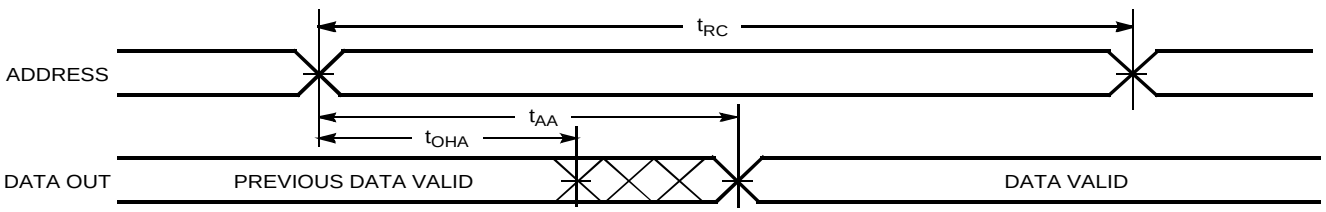

**Note:**
8. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)} > 100$ µs.

## Switching Characteristics (Over the Operating Range)[9]

| Parameter | Description | CY62128DV30-55 | | CY62128DV30-70 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 55 | | 70 | | ns |
| $t_{AA}$ | Address to Data Valid | | 55 | | 70 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}_1$ LOW or $CE_2$ HIGH to Data Valid | | 55 | | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 25 | | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z[10] | 5 | | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[10, 11] | | 20 | | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}_1$ LOW or $CE_2$ HIGH to Low Z[10] | 10 | | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH or $CE_2$ LOW to High Z[10, 11] | | 20 | | 25 | ns |
| $t_{PU}$ | $\overline{CE}_1$ LOW or $CE_2$ HIGH to Power-up | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}_1$ HIGH or $CE_2$ LOW to Power-down | | 55 | | 70 | ns |
| **Write Cycle**[12] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 55 | | 70 | | ns |
| $t_{SCE}$ | $\overline{CE}_1$ LOW or $CE_2$ HIGH to Write End | 40 | | 60 | | ns |
| $t_{AW}$ | Address Set-up to Write End | 40 | | 60 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-up to Write Start | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 40 | | 50 | | ns |
| $t_{SD}$ | Data Set-up to Write End | 25 | | 30 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[10, 11] | | 20 | | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z[10] | 10 | | 10 | | ns |

## Switching Waveforms

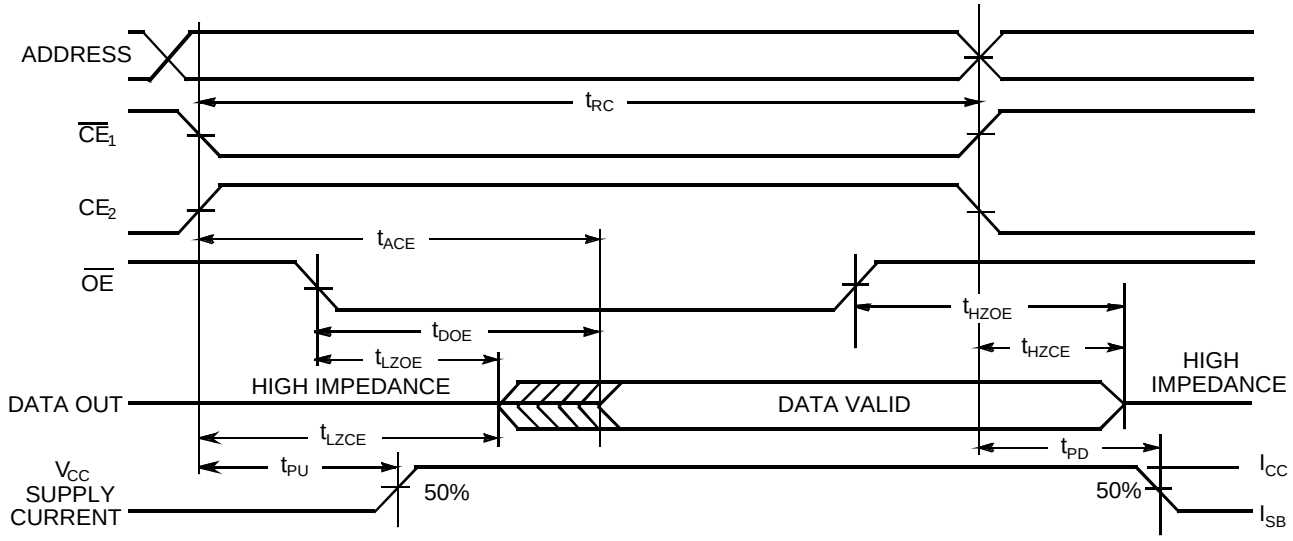
### Read Cycle No. 1 (Address Transition Controlled)[13, 14]



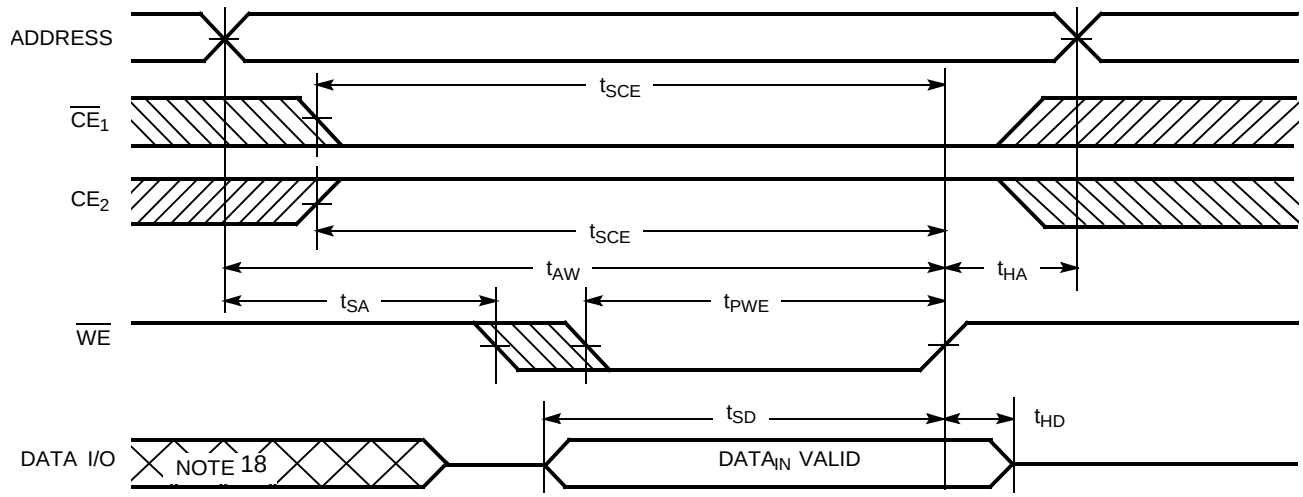

**Notes:**
9. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified $I_{OL}$.
10. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than t.
11. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high-impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals.
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
14. $\overline{WE}$ is HIGH for Read cycle.

## Switching Waveforms (continued)

### Read Cycle No. 2 ($\overline{OE}$ Controlled)[11, 14, 15]



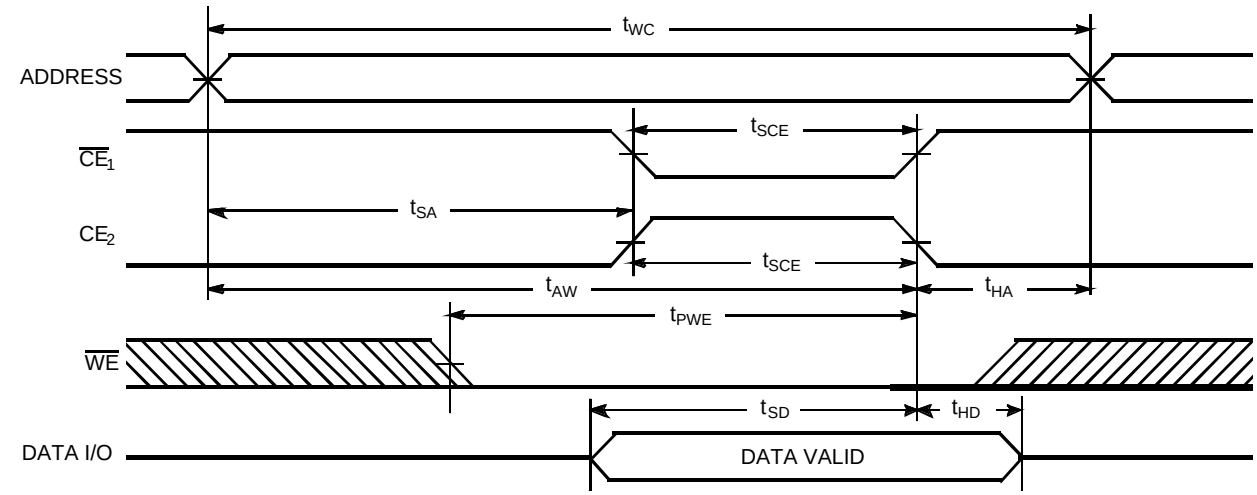

### Write Cycle No. 1 ($\overline{WE}$ Controlled)[12, 16, 17, 18]



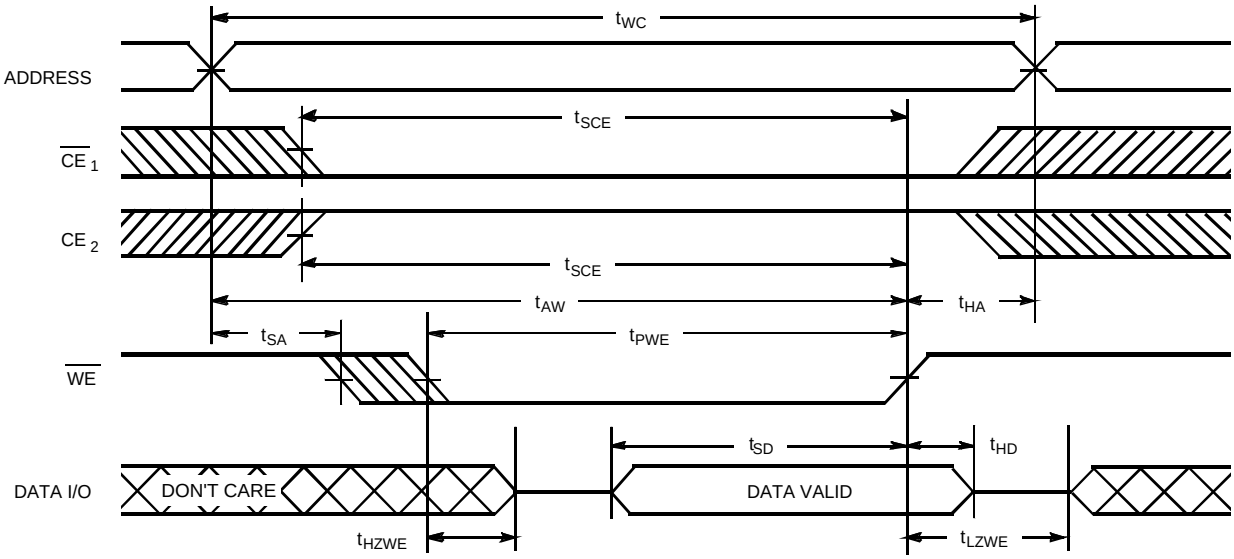

**Notes:**
15. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and $CE_2$ transition HIGH.
16. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
17. If $\overline{CE}_1$ goes HIGH or $CE_2$ goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

**Write Cycle No. 2 ($\overline{CE_1}$ or $CE_2$ Controlled)**[12, 16, 17, 18]




**Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)**[10, 16, 17]




## Truth Table

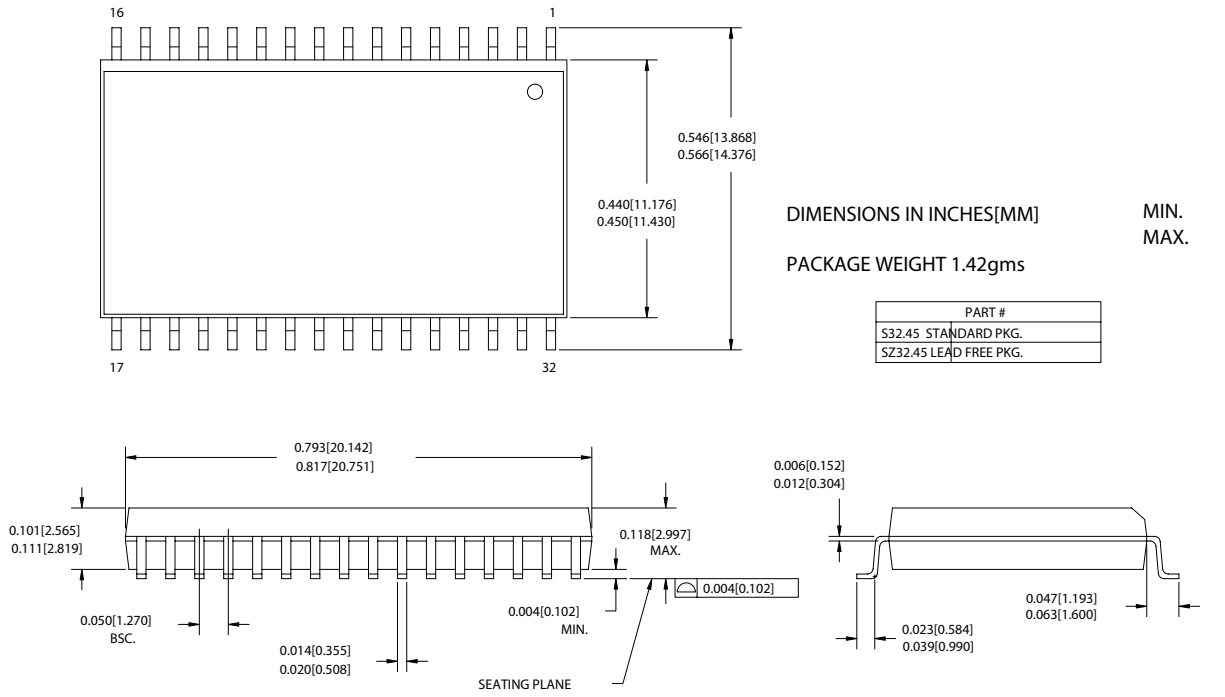
| $\overline{CE_1}$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | $I/O_0$-$I/O_7$ | MOde | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | High Z | Deselet/Power-down | Standby ($I_{SB}$) |
| X | L | X | X | High Z | Deselet/Power-down | Standby ($I_{SB}$) |
| L | H | H | L | Data out | Read | Active ($I_{CC}$) |
| L | H | H | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | L | X | Data In | Write | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 55 | CY62128DV30L-55SI | 51-85081 | 32-lead SOIC | Industrial |
| | CY62128DV30LL-55SI | 51-85081 | 32-lead SOIC | |
| | CY62128DV30LL-55SXI | 51-85081 | 32-lead SOIC (Pb-Free) | |
| | CY62128DV30L-55ZI | 51-85056 | 32-lead TSOP Type 1 | |
| | CY62128DV30LL-55ZI | 51-85056 | 32-lead TSOP Type 1 | |
| | CY62128DV30LL-55ZXI | 51-85056 | 32-lead TSOP Type 1 (Pb-Free) | |
| | CY62128DV30L-55ZAI | 51-85094 | 32-lead Small TSOP | |
| | CY62128DV30LL-55ZAI | 51-85094 | 32-lead Small TSOP | |
| | CY62128DV30LL-55ZAXI | 51-85094 | 32-lead Small TSOP (Pb-Free) | |
| | CY62128DV30L-55ZRI | 51-85089 | 32-lead Reverse TSOP | |
| | CY62128DV30LL-55ZRI | 51-85089 | 32-lead Reverse TSOP | |
| | CY62128DV30LL-55ZRXI | 51-85089 | 32-lead Reverse TSOP | |
| 70 | CY62128DV30L-70SI | 51-85081 | 32-lead SOIC | |
| | CY62128DV30LL-70SI | 51-85081 | 32-lead SOIC | |
| | CY62128DV30LL-70SXI | 51-85081 | 32-lead SOIC (Pb-Free) | |
| | CY62128DV30L-70ZI | 51-85056 | 32-lead TSOP Type 1 | |
| | CY62128DV30LL-70ZI | 51-85056 | 32-lead TSOP Type 1 | |
| | CY62128DV30LL-70ZXI | 51-85056 | 32-lead TSOP Type 1 (Pb-Free) | |
| | CY62128DV30L-70ZAI | 51-85094 | 32-lead Small TSOP | |
| | CY62128DV30LL-70ZAI | 51-85094 | 32-lead Small TSOP | |
| | CY62128DV30LL-70ZAXI | 51-85094 | 32-lead Small TSOP (Pb-Free) | |
| | CY62128DV30L-70ZRI | 51-85089 | 32-lead Reverse TSOP | |
| | CY62128DV30LL-70ZRI | 51-85089 | 32-lead Reverse TSOP | |

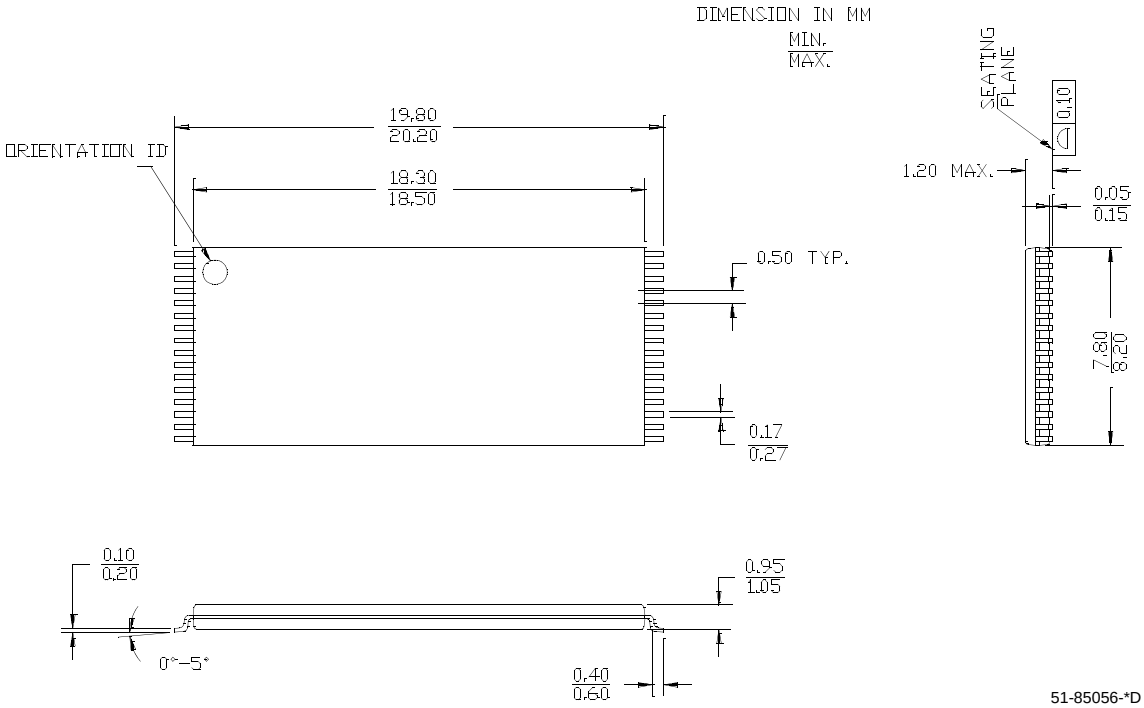
## Package Diagrams

### 32-Lead (450-Mil) SOIC (51-85081)




51-85081-*B

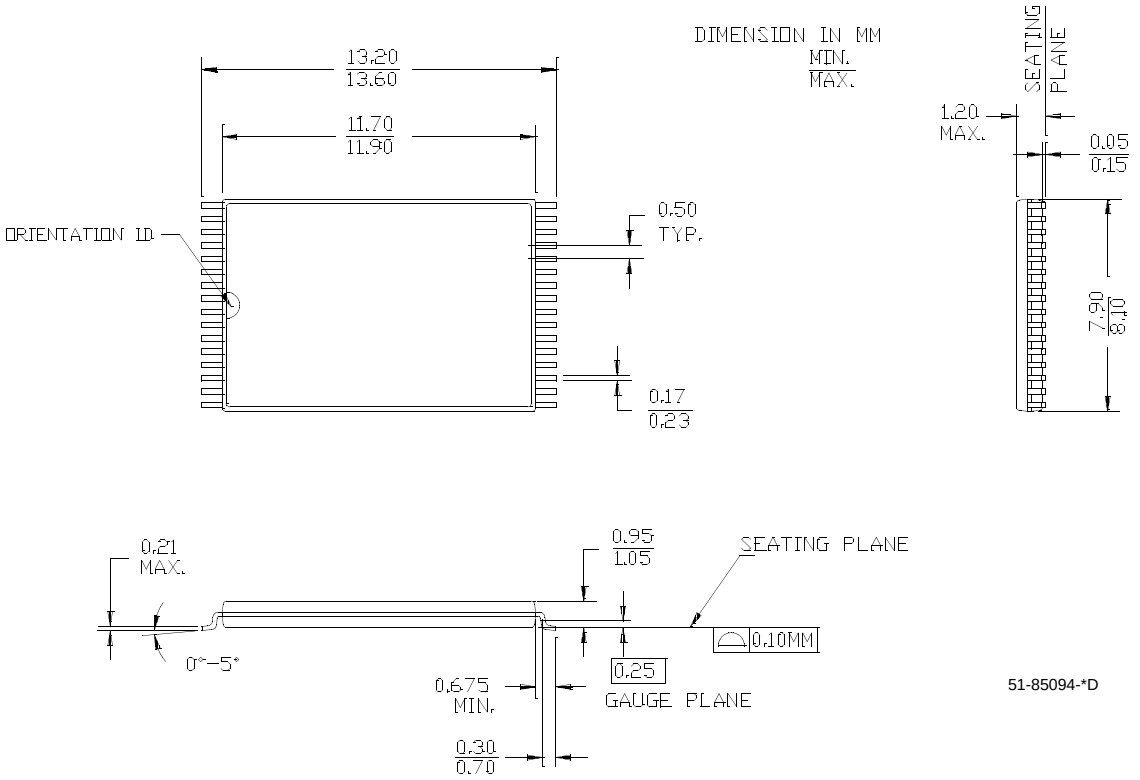
### 32-Lead TSOP Type I (8 x 20 mm) (51-85056)



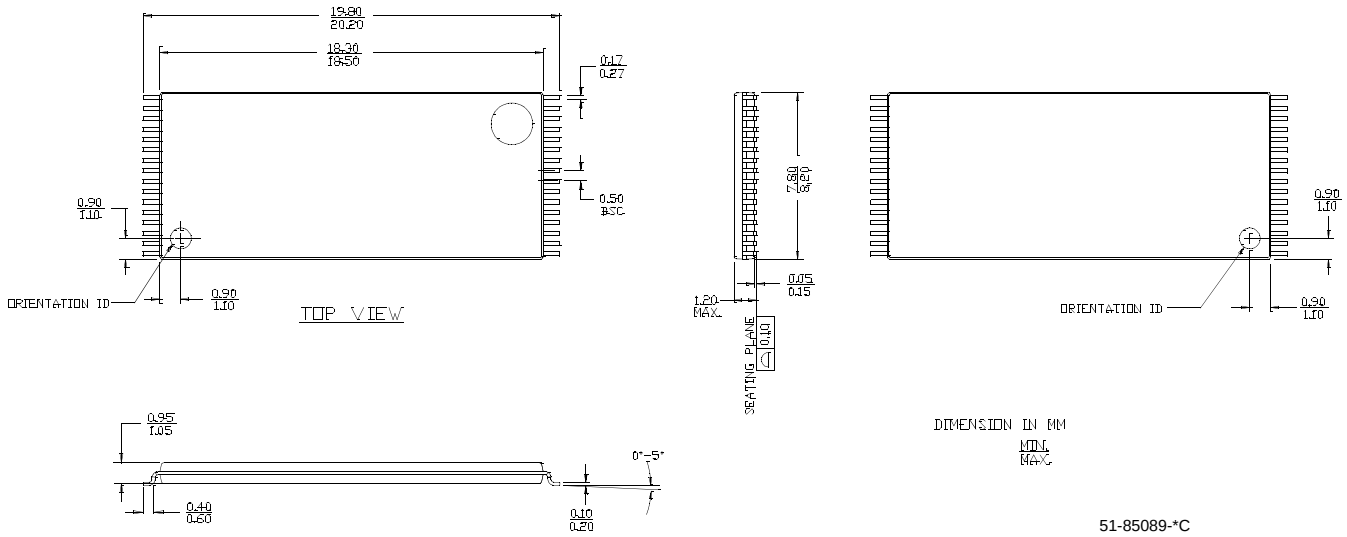

51-85056-*D

## Package Diagrams (continued)

**32-Lead STSOP (8 x 13.4 mm) (51-85094)**




**32-Lead RTSOP (51-85089)**



## Document History Page

| Document Title: CY62128DV30 1-Mb (128K x 8) Static RAM<br>Document Number: 38-05231 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 117691 | 08/27/02 | JUI | New Data Sheet |
| *A | 127314 | 5/27/03 | MPR | Changed from Advance Information to Preliminary<br>Changed Isb2 to 5 μA (L), 4 μA (LL)<br>Changed Iccdr to 4 μA (L), 3 μA (LL)<br>Changed Cin from 6 pF to 8 pF |
| *B | 128342 | 07/23/03 | JUI | Changed from Preliminary to Final<br>Add 70-ns speed, updated ordering information |
| *C | 129002 | 08/29/03 | CDY | Changed Icc 1 MHz typ from 0.5 mA to 0.85 mA |
| *D | 347394 | See ECN | PCI | Added Lead-Free Packages in Ordering Information Table |
| *E | 395936 | See ECN | SYT | Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court”<br>Corrected $\overline{CE}_1$ and $CE_2$ waveforms on Write Cycle No.1 on Page# 6.<br>Edited the Write Cycle No.1 switching waveform Data I/O to include Don’t Care Condition on Page# 6<br>Updated the ordering information on Page # 8 |
| *F | 428906 | See ECN | AJU | Added Thermal Resistance numbers for RTSOP package<br>Updated Ordering Information table by replacing Package Name column with Package Diagram |
| *G | 464721 | See ECN | NXR | Updated the Block Diagram on page # 1 |
| *H | 470383 | See ECN | NXR | Changed pin# 1 of SOIC and STSOP I, pin # 9 of TSOP I and RTSOP I from NC to DNU and added footnote# 3 |

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