



**THE DATASHEET OF
CY62126EV30LL-45ZSXIT**



1-Mbit (64K x 16) Static RAM

Features

- High speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to +85 °C
 - Automotive: -40 °C to +125 °C
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62126DV30
- Ultra low standby power
 - Typical standby current: 1 μ A
 - Maximum standby current: 4 μ A
- Ultra low active power
 - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 48-ball very fine pitch ball grid array (VFBGA) and 44-pin thin small outline package (TSOP) II packages

Functional Description

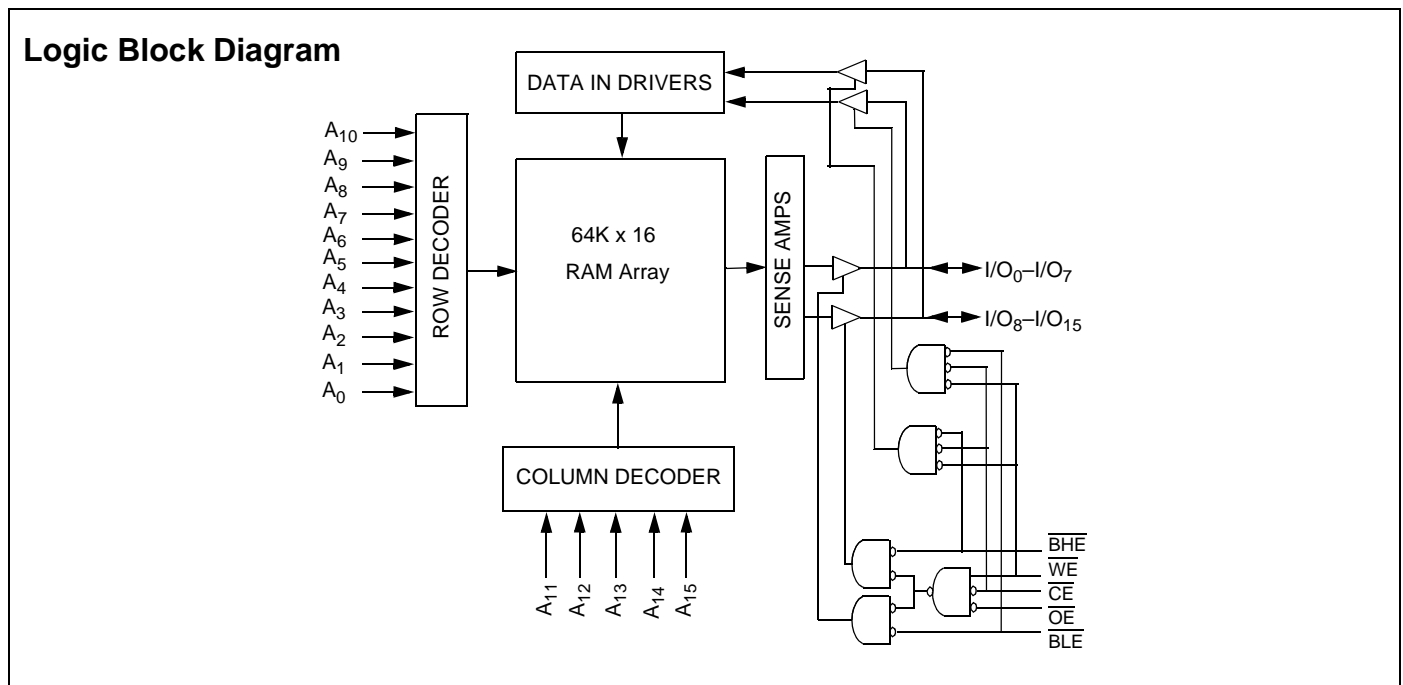
The CY62126EV30 is a high performance CMOS static RAM organized as 64K words by 16 bits. This device features

advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life[™] (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE} HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH) or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the "Truth Table" on page 11 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).



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Pin Configuration

Figure 1. 48-Ball VFBGA (Top View)

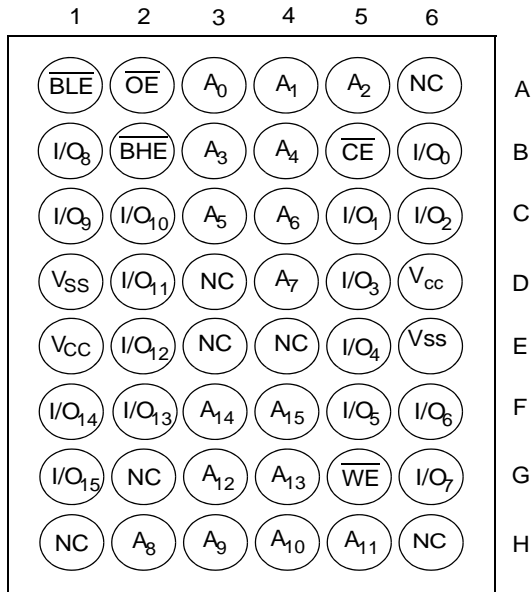


Figure 2. 44-Pin TSOP II (Top View) [1]

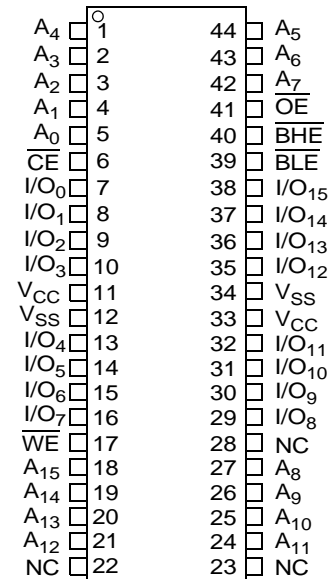


Table 1. Product Portfolio

| Product | Range | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---------------|------------|---------------------------|--------------------|----------------------|------------|---------------------------------|-----|--------------------|-----|--------------------------------|-----|
| | | | | | | Operating, I _{CC} (mA) | | | | Standby, I _{SB2} (μA) | |
| | | f = 1 MHz | | f = f _{max} | | | | | | | |
| | | Min | Typ ^[2] | Max | | Typ ^[2] | Max | Typ ^[2] | Max | Typ ^[2] | Max |
| CY62126EV30LL | Industrial | 2.2 | 3.0 | 3.6 | 45 | 1.3 | 2 | 11 | 16 | 1 | 4 |
| CY62126EV30LL | Automotive | 2.2 | 3.0 | 3.6 | 55 | 1.3 | 4 | 11 | 35 | 1 | 30 |

Notes

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the battery life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage to ground potential -0.3 V to 3.6 V ($V_{CCmax} + 0.3$ V)
 DC voltage applied to outputs in High Z state^[3, 4] -0.3 V to 3.6 V ($V_{CCmax} + 0.3$ V)

DC input voltage^[3, 4] -0.3 V to 3.6 V ($V_{CCmax} + 0.3$ V)
 Output current into outputs (LOW) 20 mA
 Static discharge voltage > 2001 V (MIL-STD-883, Method 3015)
 Latch up current > 200 mA

Operating Range

| Device | Range | Ambient Temperature | V_{CC} ^[5] |
|---------------|------------|---------------------|-------------------------|
| CY62126EV30LL | Industrial | -40 °C to +85 °C | 2.2 V to 3.6 V |
| | Automotive | -40 °C to +125 °C | |

Electrical Characteristics

(Over the Operating Range)

| Parameter | Description | Test Conditions | 45 ns (Industrial) | | | 55 ns (Automotive) | | | Unit |
|--------------------------|---|---|--------------------|--------------------|----------------|--------------------|--------------------|----------------|---------|
| | | | Min | Typ ^[6] | Max | Min | Typ ^[6] | Max | |
| V_{OH} | Output high voltage | $I_{OH} = -0.1$ mA | 2.0 | - | - | 2.0 | - | - | V |
| | | $I_{OH} = -1.0$ mA, $V_{CC} \geq 2.70$ V | 2.4 | - | - | 2.4 | - | - | V |
| V_{OL} | Output low voltage | $I_{OL} = 0.1$ mA | - | - | 0.4 | - | - | 0.4 | V |
| | | $I_{OL} = 2.1$ mA, $V_{CC} \geq 2.70$ V | - | - | 0.4 | - | - | 0.4 | V |
| V_{IH} | Input high voltage | $V_{CC} = 2.2$ V to 2.7 V | 1.8 | - | $V_{CC} + 0.3$ | 1.8 | - | $V_{CC} + 0.3$ | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2.2 | - | $V_{CC} + 0.3$ | 2.2 | - | $V_{CC} + 0.3$ | V |
| V_{IL} | Input low voltage | $V_{CC} = 2.2$ V to 2.7 V | -0.3 | - | 0.6 | -0.3 | - | 0.6 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | -0.3 | - | 0.8 | -0.3 | - | 0.8 | V |
| I_{IX} | Input leakage current | $GND \leq V_I \leq V_{CC}$ | -1 | - | +1 | -4 | - | +4 | μ A |
| I_{OZ} | Output leakage current | $GND \leq V_O \leq V_{CC}$, Output Disabled | -1 | - | +1 | -4 | - | +4 | μ A |
| I_{CC} | V_{CC} operating supply current | $f = f_{max} = 1/t_{RC}$ | | 11 | 16 | - | 11 | 35 | mA |
| | | $f = 1$ MHz | | 1.3 | 2.0 | - | 1.3 | 4.0 | |
| I_{SB1} | Automatic CE power down current—CMOS inputs | $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V) $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, BHE, BLE and WE), $V_{CC} = 3.60$ V | - | 1 | 4 | - | 1 | 35 | μ A |
| I_{SB2} ^[7] | Automatic CE power down current—CMOS inputs | $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$, $V_{CC} = 3.60$ V | - | 1 | 4 | - | 1 | 30 | μ A |

Notes

- $V_{IL(min)}$ = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.75$ V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μ s ramp time from 0 to $V_{CC(min)}$ and 200 μ s wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
- Chip enable (CE) needs to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

For all packages. Tested initially and after any design or process changes that may affect these parameters.

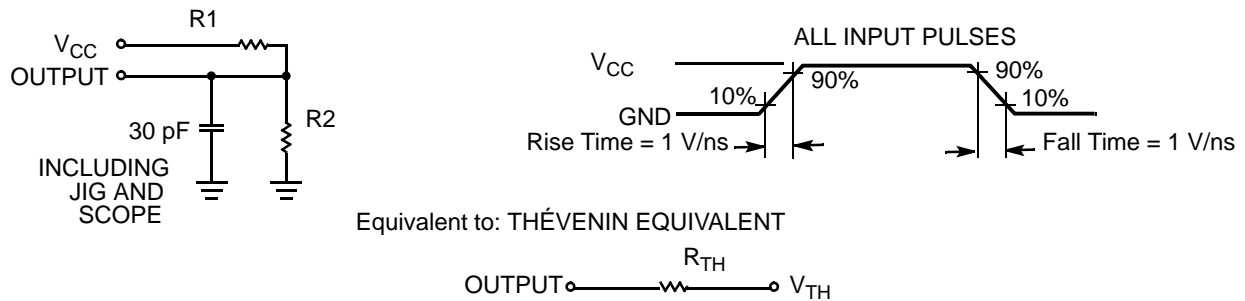
| Parameter | Description | Test Conditions | Max | Unit |
|------------------|--------------------|---|-----|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)} | 10 | pF |
| C _{OUT} | Output capacitance | | 10 | pF |

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | VFBGA Package | TSOP II Package | Unit |
|-----------------|--|---|---------------|-----------------|------|
| Θ _{JA} | Thermal resistance (Junction to ambient) | Still Air, soldered on a 4.25 × 1.125 inch, two-layer printed circuit board | 58.85 | 28.2 | °C/W |
| Θ _{JC} | Thermal resistance (Junction to case) | | 17.01 | 3.4 | °C/W |

Figure 3. AC Test Loads and Waveforms



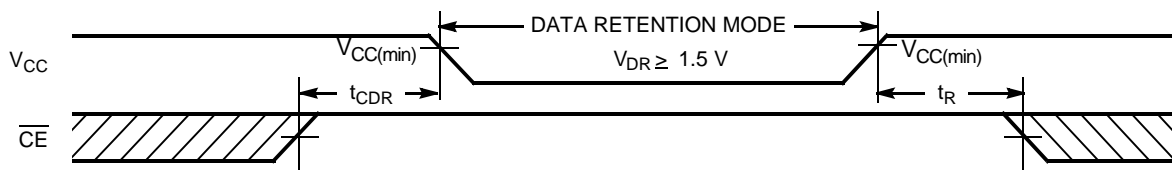
| Parameters | 2.2 V - 2.7 V | 2.7 V - 3.6 V | Unit |
|-----------------|---------------|---------------|------|
| R ₁ | 16600 | 1103 | Ω |
| R ₂ | 15400 | 1554 | Ω |
| R _{TH} | 8000 | 645 | Ω |
| V _{TH} | 1.2 | 1.75 | V |

Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[8] | Max | Unit | |
|----------------------------------|--------------------------------------|--|-----------------|--------------------|-----|------|----|
| V _{DR} | V _{CC} for data retention | | 1.5 | – | – | V | |
| I _{CCDR} ^[9] | Data retention current | V _{CC} = V _{DR} , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V | Industrial | – | – | 3 | μA |
| | | | Automotive | – | – | 30 | μA |
| t _{CDR} ^[10] | Chip deselect to data retention time | | 0 | – | – | ns | |
| t _R ^[10] | Operation recovery time | | t _{RC} | – | – | ns | |

Figure 4. Data Retention Waveform



Notes

- 8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- 9. Tested initially and after any design or process changes that may affect these parameters.
- 10. Full device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} > 100 μs.

Switching Characteristics

Over the Operating Range ^[11, 12]

| Parameter | Description | 45 ns (Industrial) | | 55 ns (Automotive) | | Unit |
|------------------------------------|--|--------------------|-----|--------------------|-----|------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t _{RC} | Read cycle time | 45 | – | 55 | – | ns |
| t _{AA} | Address to data valid | – | 45 | – | 55 | ns |
| t _{OHA} | Data hold from address change | 10 | – | 10 | – | ns |
| t _{ACE} | \overline{CE} LOW to data valid | – | 45 | – | 55 | ns |
| t _{DOE} | \overline{OE} LOW to data valid | – | 22 | – | 25 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z ^[13] | 5 | – | 5 | – | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[13, 14] | – | 18 | – | 20 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[13] | 10 | – | 10 | – | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[13, 14] | – | 18 | – | 20 | ns |
| t _{PU} | \overline{CE} LOW to power up | 0 | – | 0 | – | ns |
| t _{PD} | \overline{CE} HIGH to power down | – | 45 | – | 55 | ns |
| t _{DBE} | \overline{BHE} / \overline{BLE} LOW to data valid | – | 22 | – | 25 | ns |
| t _{LZBE} | \overline{BHE} / \overline{BLE} LOW to Low Z ^[13] | 5 | – | 5 | – | ns |
| t _{HZBE} | \overline{BHE} / \overline{BLE} HIGH to High Z ^[13, 14] | – | 18 | – | 20 | ns |
| Write Cycle ^[15] | | | | | | |
| t _{WC} | Write cycle time | 45 | – | 55 | – | ns |
| t _{SCE} | \overline{CE} LOW to write end | 35 | – | 40 | – | ns |
| t _{AW} | Address setup to write end | 35 | – | 40 | – | ns |
| t _{HA} | Address hold from write end | 0 | – | 0 | – | ns |
| t _{SA} | Address setup to write start | 0 | – | 0 | – | ns |
| t _{PWE} | \overline{WE} pulse width | 35 | – | 40 | – | ns |
| t _{BW} | \overline{BHE} / \overline{BLE} pulse width | 35 | – | 40 | – | ns |
| t _{SD} | Data setup to write end | 25 | – | 25 | – | ns |
| t _{HD} | Data hold from write end | 0 | – | 0 | – | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[13, 14] | – | 18 | – | 20 | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[13] | 10 | – | 10 | – | ns |

Notes

11. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
12. AC timing parameters are subject to byte enable signals (\overline{BHE} or \overline{BLE}) not switching when chip is disabled. See [application note AN13842](#) for further clarification.
13. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
15. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address transition controlled)^[16, 17]

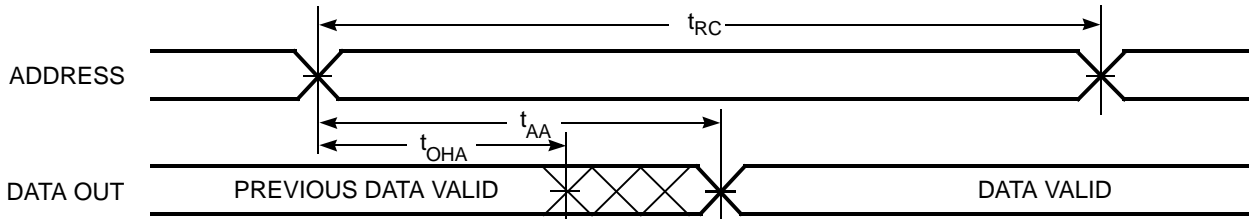
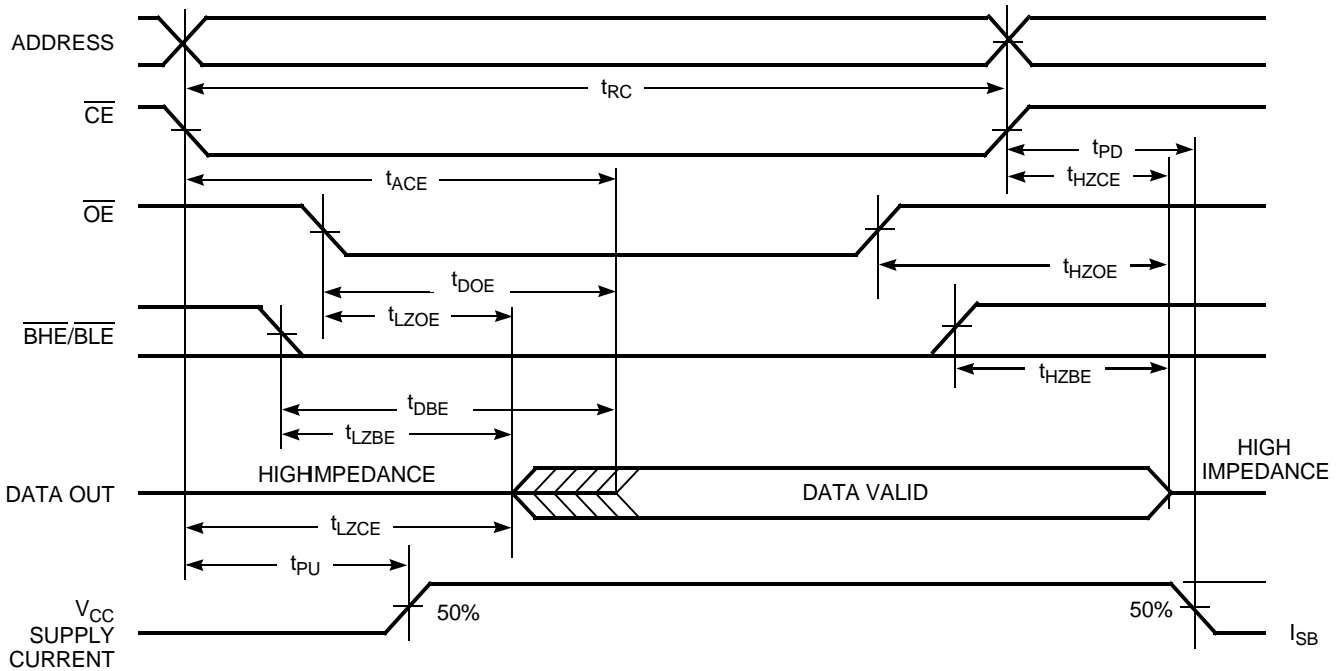


Figure 6. Read Cycle No. 2 (\overline{OE} controlled)^[17, 18]



Notes

- 16. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} .
- 17. \overline{WE} is high for read cycle.
- 18. Address valid before or similar to \overline{CE} and \overline{BHE} , \overline{BLE} transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (\overline{WE} controlled)^[19, 20, 21]

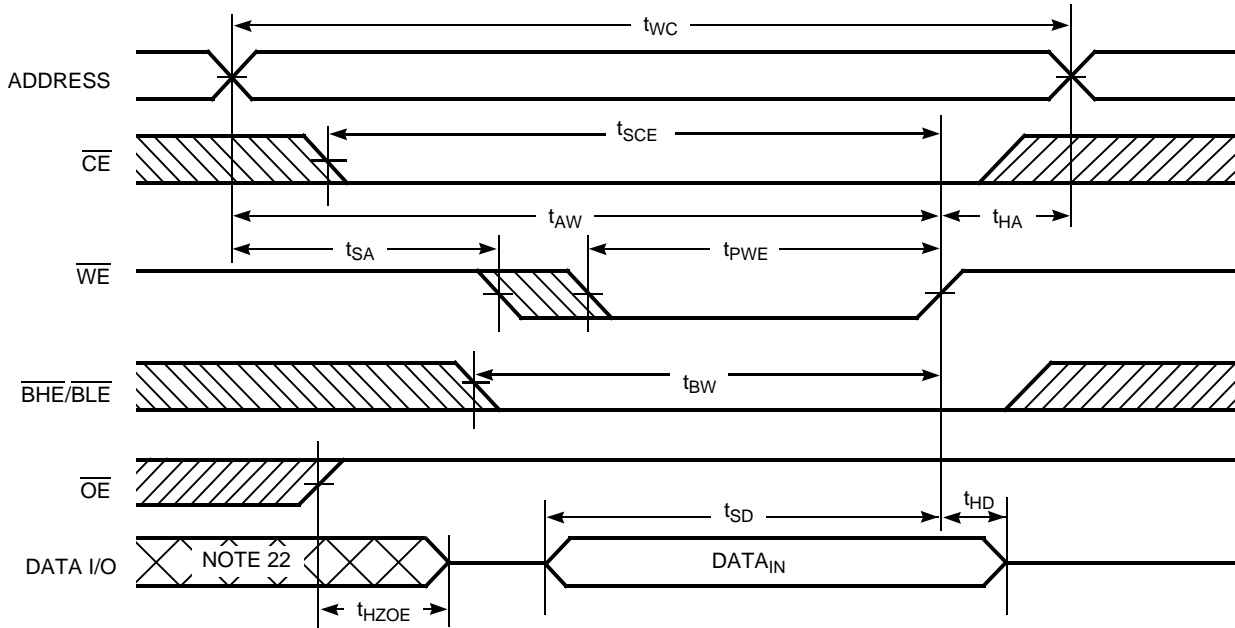
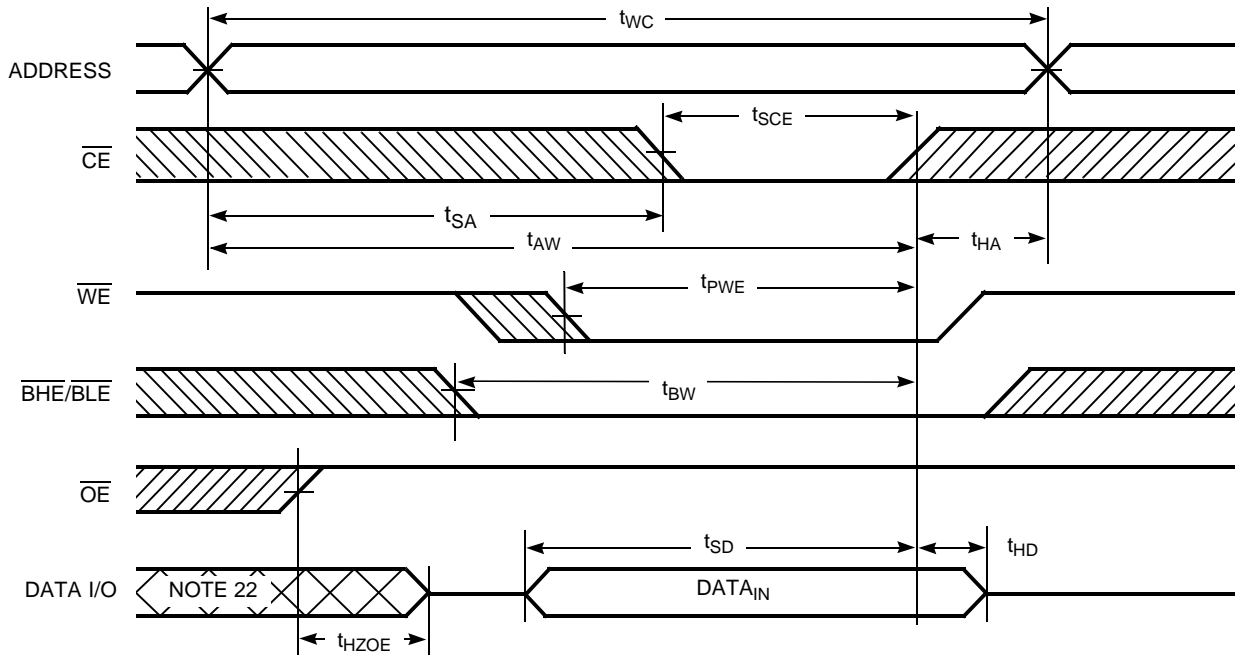


Figure 8. Write Cycle No. 2 (\overline{CE} controlled)^[19, 20, 21]



Notes

- 19. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.
- 20. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 21. If \overline{CE} goes high simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 22. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW)^[23]

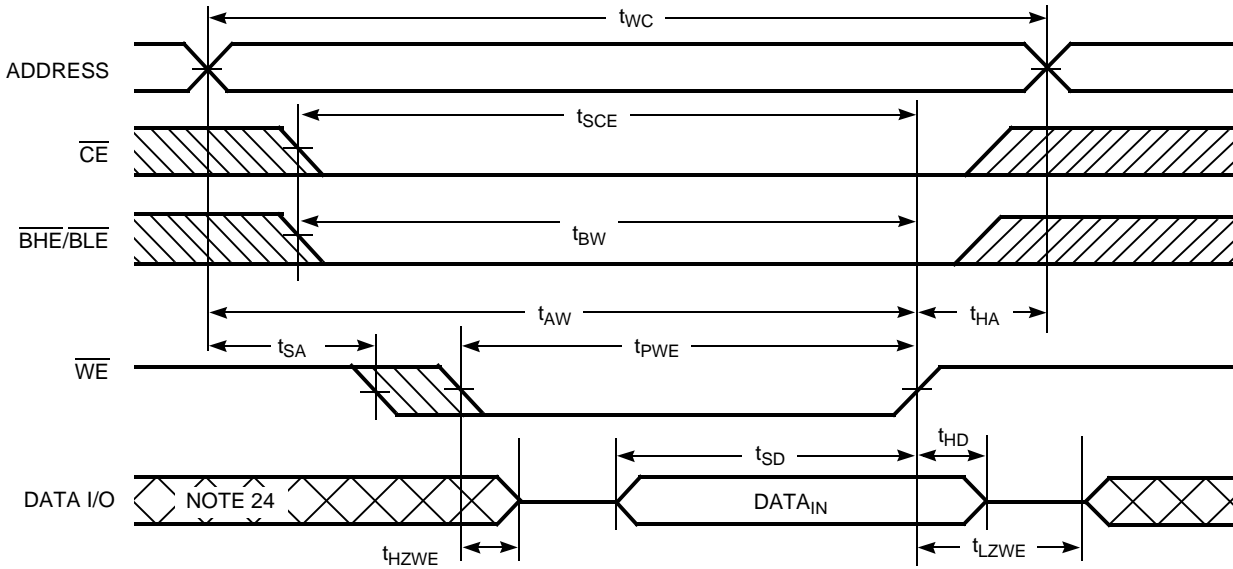
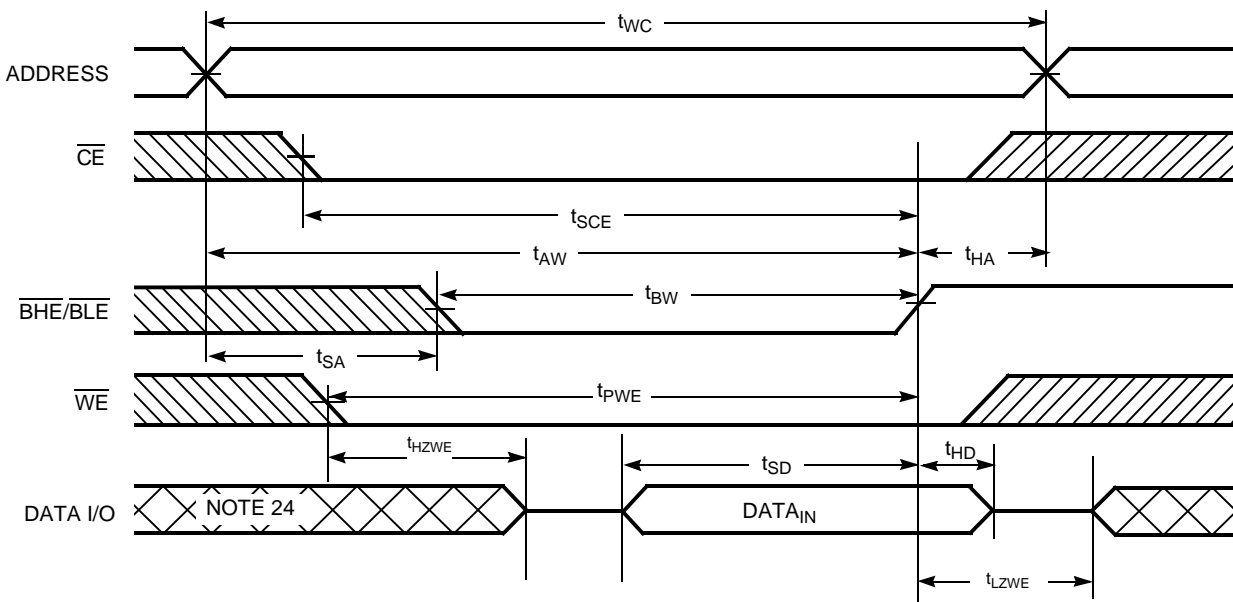


Figure 10. Write Cycle No. 4 ($\overline{BHE/BLE}$ controlled, \overline{OE} LOW)^[23]



Note

- 23. If \overline{CE} goes high simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 24. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

| $\overline{CE}^{[25]}$ | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs/Outputs | Mode | Power |
|------------------------|-----------------|-----------------|------------------|------------------|---|---------------------|----------------------|
| H | X | X | X | X | High Z | Deselect/power down | Standby (I_{SB}) |
| L | X | X | H | H | High Z | Output disabled | Active (I_{CC}) |
| L | H | L | L | L | Data out (I/O_0 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | L | H | L | Data out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z | Read | Active (I_{CC}) |
| L | H | L | L | H | Data out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z | Read | Active (I_{CC}) |
| L | H | H | L | L | High Z | Output disabled | Active (I_{CC}) |
| L | H | H | H | L | High Z | Output disabled | Active (I_{CC}) |
| L | H | H | L | H | High Z | Output disabled | Active (I_{CC}) |
| L | L | X | L | L | Data in (I/O_0 – I/O_{15}) | Write | Active (I_{CC}) |
| L | L | X | H | L | Data in (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z | Write | Active (I_{CC}) |
| L | L | X | L | H | Data in (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z | Write | Active (I_{CC}) |

Note

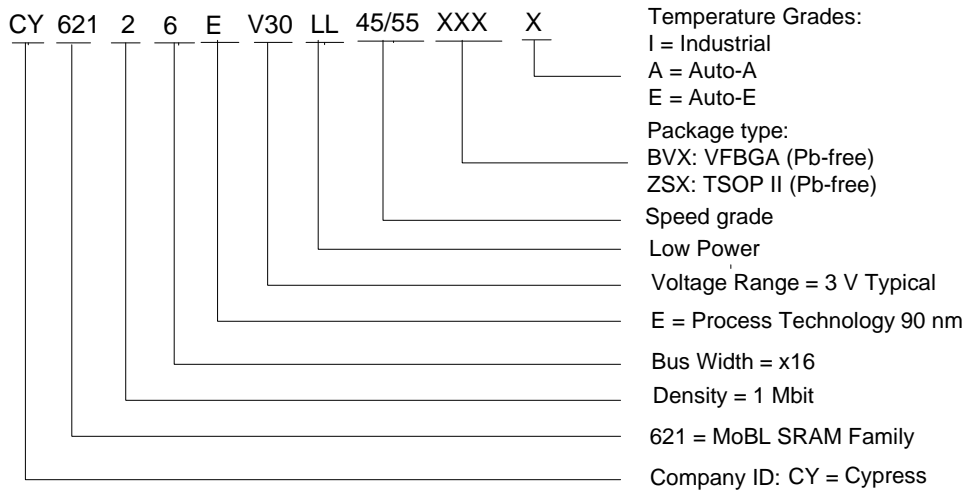
25. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|----------------------|-----------------|--------------------------|-----------------|
| 45 | CY62126EV30LL-45BVXI | 51-85150 | 48-ball VFBGA (Pb-free) | Industrial |
| | CY62126EV30LL-45ZSXI | 51-85087 | 44-pin TSOP II (Pb-free) | Industrial |
| | CY62126EV30LL-45ZSXA | 51-85087 | 44-pin TSOP II (Pb-free) | Automotive-A |
| 55 | CY62126EV30LL-55BVXE | 51-85150 | 48-ball VFBGA (Pb-free) | Automotive-E |
| | CY62126EV30LL-55ZSXE | 51-85087 | 44-pin TSOP II (Pb-free) | Automotive-E |

Contact your local Cypress sales representative for availability of other parts.

Ordering Code Definitions



Package Diagrams

Figure 11. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150

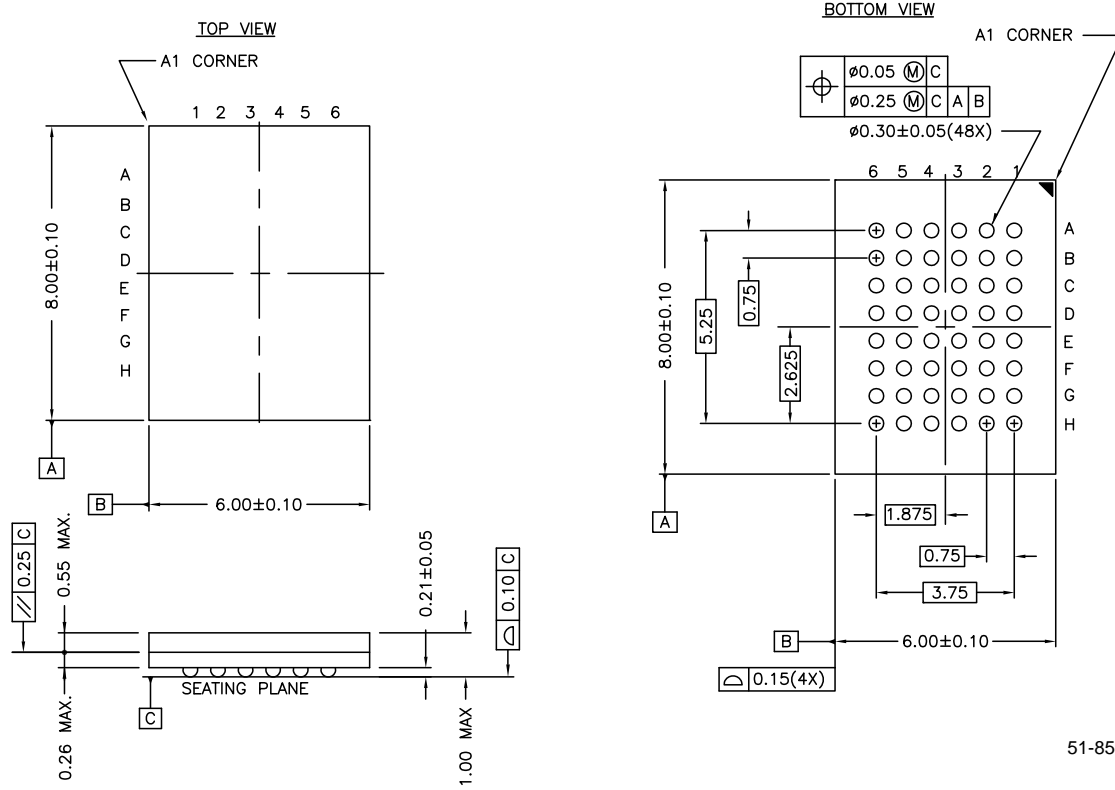
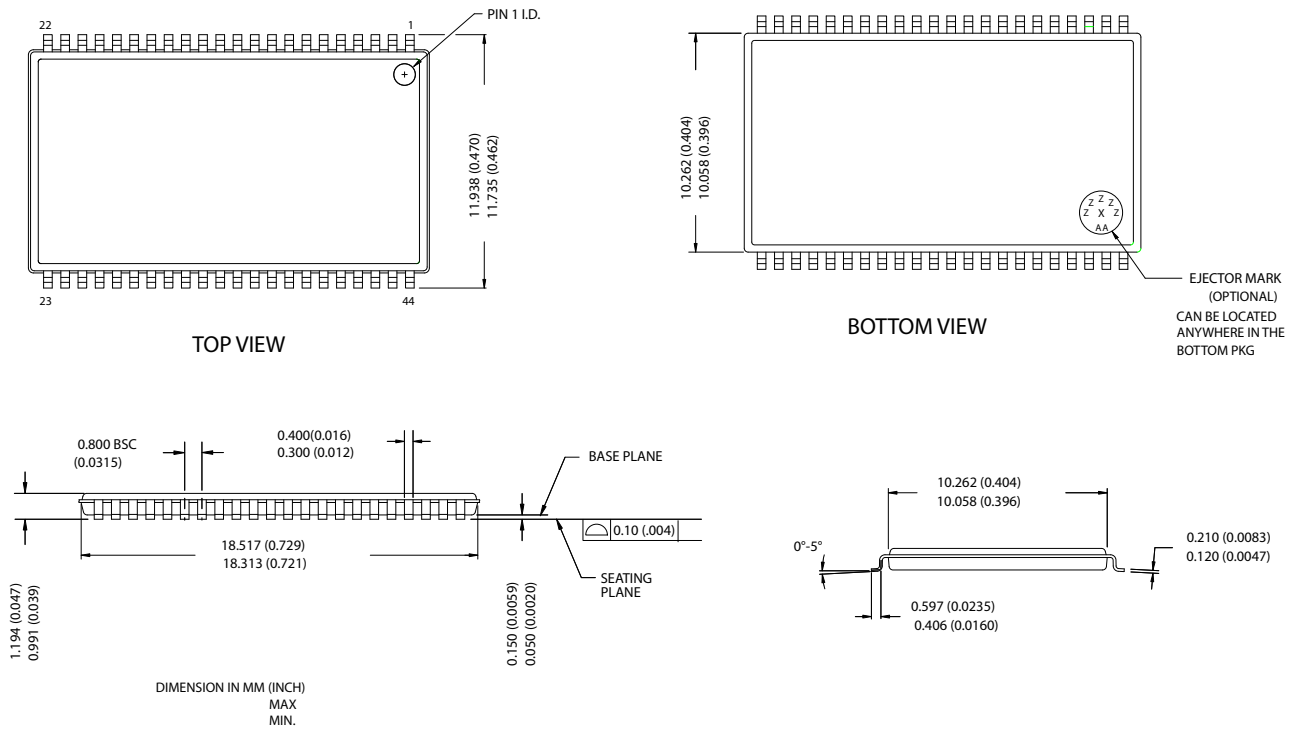


Figure 12. 44-Pin TSOP II, 51-85087



51-85087-°C

Acronyms

| Acronym | Description |
|-------------------------|---|
| $\overline{\text{BHE}}$ | byte high enable |
| $\overline{\text{BLE}}$ | byte low enable |
| CMOS | complementary metal oxide semiconductor |
| $\overline{\text{CE}}$ | chip enable |
| I/O | input/output |
| $\overline{\text{OE}}$ | output enable |
| SRAM | static random access memory |
| TSOP | thin small outline package |
| VFBGA | very fine ball gird array |
| $\overline{\text{WE}}$ | write enable |

Document History Page

| Document Title: CY62126EV30 MoBL®, 1-Mbit (64K x 16) Static RAM | | | | |
|---|---------|-----------------|-----------------|---|
| Document Number: 38-05486 | | | | |
| Rev. | ECN No. | Submission Date | Orig. of Change | Description of Change |
| ** | 202760 | See ECN | AJU | New data sheet |
| *A | 300835 | See ECN | SYT | <p>Converted from Advance Information to Preliminary</p> <p>Specified Typical standby power in the Features Section</p> <p>Changed E3 ball from DNU to NC in the Pin Configuration for the FBGA Package and removed the footnote associated with it on page #2</p> <p>Changed t_{OHA} from 6 ns to 10 ns for both 35- and 45-ns speed bins, respectively</p> <p>Changed t_{DOE}, t_{SD} from 15 to 18 ns for 35-ns speed bin</p> <p>Changed t_{HZOE}, t_{HZBE}, t_{HZWE} from 12 and 15 ns to 15 and 18 ns for the 35- and 45-ns speed bins, respectively</p> <p>Changed t_{HZCE} from 12 and 15 ns to 18 and 22 ns for the 35- and 45-ns speed bins, respectively</p> <p>Changed t_{SCE}, t_{BW} from 25 and 40 ns to 30 and 35 ns for the 35- and 45-ns speed bins, respectively</p> <p>Changed t_{AW} from 25 to 30 ns and 40 to 35 ns for 35 and 45-ns speed bins respectively</p> <p>Changed t_{DBE} from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins respectively</p> <p>Removed footnote that read “$\overline{BHE}.\overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE}. Chip can be deselected by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE}” on page # 4</p> <p>Removed footnote that read “If both \overline{BHE} and \overline{BLE} are toggled together, then t_{LZBE} is 10 ns” on page # 5</p> <p>Added Pb-free package information</p> |
| *B | 461631 | See ECN | NXR | <p>Converted from Preliminary to Final</p> <p>Removed 35 ns Speed Bin</p> <p>Removed “L” version of CY62126EV30</p> <p>Changed $I_{CC(Typ)}$ from 8 mA to 11 mA and $I_{CC(max)}$ from 12 mA to 16 mA for $f = f_{max}$</p> <p>Changed $I_{CC(max)}$ from 1.5 mA to 2.0 mA for $f = 1$ MHz, I_{SB1}, $I_{SB2(max)}$ from 1 μA to 4 μA, I_{SB1}, $I_{SB2(Typ)}$ from 0.5 μA to 1 μA, $I_{CCDR(max)}$ from 1.5 μA to 3 μA, AC Test load Capacitance value from 50 pF to 30 pF, t_{LZOE} from 3 to 5 ns, t_{LZCE} from 6 to 10 ns, t_{HZCE} from 22 to 18 ns, t_{LZBE} from 6 to 5 ns, t_{PWE} from 30 to 35 ns, t_{SD} from 22 to 25 ns, t_{LZWE} from 6 to 10 ns, and updated the Ordering Information table.</p> |
| *C | 925501 | See ECN | VKN | <p>Added footnote #7 related to I_{SB2} and I_{CCDR}</p> <p>Added footnote #11 related AC timing parameters</p> |
| *D | 1045260 | See ECN | VKN | <p>Added Automotive information</p> <p>Updated Ordering Information table</p> |
| *E | 2631771 | 01/07/09 | NXR/PYRS | <p>Changed CE condition from X to L in Truth table for Output Disable mode</p> <p>Updated template</p> |
| *F | 2944332 | 06/04/2010 | VKN | <p>Added Contents</p> <p>Removed byte enable from footnote #2 in Electrical Characteristics</p> <p>Added footnote related to chip enable in Truth Table</p> <p>Updated Package Diagrams</p> <p>Updated links in Sales, Solutions, and Legal Information</p> |
| *G | 2996166 | 07/29/2010 | AJU | <p>Added CY62126EV30LL-45ZSXA part in Ordering Information.</p> <p>Added Ordering Code Definitions.</p> <p>Modified table footnote format.</p> |
| *H | 3113864 | 12/17/2010 | PRAS | Updated Figure 1 and Package Diagram, and fixed Typo in Figure 3.. |

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