



**THE DATASHEET OF
CY29942AXCT**

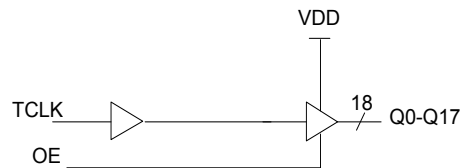


1:18 Clock Distribution Buffer

Features

- Operational range: Up to 200 MHz
- LVCMOS/LVTTL clock input
- LVCMOS-/LVTTL-compatible logic input
- 18 clock outputs: Drive up to 36 clock lines
- Output-to-output Skew: 110 ps (typical)
- Output enable control
- Supply voltage: 2.5 V or 3.3 V
- Temperature range: Commercial and Industrial
- 32-pin TQFP package
- Pin compatible with MPC942C

Logic Block Diagram



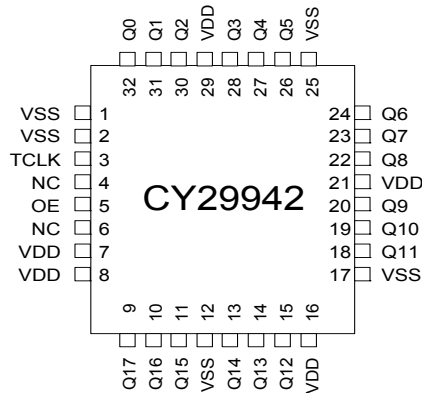
Functional Description

The CY29942 is a low voltage clock distribution buffer with an LVCMOS or LVTTL compatible clock input. The output enable control input is LVCMOS/LVTTL compatible. The eighteen outputs are 2.5 V or 3.3 V LVCMOS or LVTTL compatible, operate up to 200 MHz, and can drive 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces, giving the devices an effective fanout of 1:36. Low output-to-output skews make the CY29942 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

For a complete list of related documentation, [click here](#).

Pin Configuration

Figure 1. 32-pin TQFP pinout



Pin Descriptions

Pin	Name	I/O	Description
3	TCLK	Input	External reference/Test clock input. Weak internal pull-down resistor.
5	OE	Input	Output enable. When HIGH, all outputs are enabled. When set LOW, the outputs are at high impedance. Weak internal pull-up resistor.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	Output	Clock outputs
7, 8, 16, 21, 29	VDD		2.5 V or 3.3 V power supply
1, 2, 12, 17, 25	VSS		Ground
4, 6	NC		No connection

Absolute Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested. ^[1]

Maximum input voltage relative to V_{SS} : $V_{SS} - 0.3$ V

Maximum input voltage relative to V_{DD} : $V_{DD} + 0.3$ V

Storage temperature: -65 °C to 150 °C

Operating temperature: -40 °C to 85 °C

Maximum ESD protection 2 kV

Maximum power supply: 5.5 V

Maximum input current: ± 20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, I/O voltages should be constrained to the range:

$$V_{SS} < V_{I/O} < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications

$V_{DD} = 3.3$ V $\pm 5\%$ or 2.5 V $\pm 5\%$ over the specified temperature range.

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low voltage		V_{SS}	–	0.8	V
V_{IH}	Input high voltage		2.0	–	V_{DD}	V
I_{IL}	Input low current ^[2]		–	–	–200	μ A
I_{IH}	Input high current ^[2]		–	–	200	μ A
V_{OL}	Output low voltage ^[3]	$I_{OL} = 20$ mA	–	–	0.5	V
V_{OH}	Output high voltage ^[3]	$I_{OH} = -20$ mA, $V_{DD} = 3.3$ V	2.4	–	–	V
		$I_{OH} = -16$ mA, $V_{DD} = 2.5$ V	2.0	–	–	V
I_{DDQ}	Quiescent supply current	OE = V_{SS}	–	5	7	mA
I_{DD}	Dynamic supply current	$V_{DD} = 3.3$ V, Outputs at 150 MHz, CL = 15 pF	–	285	–	mA
		$V_{DD} = 3.3$ V, Outputs at 200 MHz, CL = 15 pF	–	335	–	mA
		$V_{DD} = 2.5$ V, Outputs at 150 MHz, CL = 15 pF	–	200	–	mA
		$V_{DD} = 2.5$ V, Outputs at 200 MHz, CL = 15 pF	–	240	–	mA
Z_{out}	Output impedance	$V_{DD} = 3.3$ V	8	12	16	Ω
		$V_{DD} = 2.5$ V	10	15	20	Ω
C_{in}	Input capacitance		–	4	–	pF

Thermal Resistance

Parameter ^[4]	Description	Test Conditions	32-pin TQFP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	67	°C/W
θ_{JC}	Thermal resistance (junction to case)		28	°C/W

Notes

1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Inputs have pull-up/pull-down resistors that effect input current.
3. Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.
4. These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

$V_{DD} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$ over the specified temperature range ^[5]

Parameter	Description	Conditions	Min	Typ	Max	Unit
Fmax	Input frequency		–	–	200	MHz
tpd	TTL_CLK to Q delay ^[6, 7]	$V_{DD} = 3.3\text{ V}$	1.8	3.3	3.8	ns
		$V_{DD} = 2.5\text{ V}$	2.3	3.8	4.4	ns
DC	Output duty cycle ^[6, 7, 8]	Measured at $V_{DD}/2$	45	–	55	%
tsk(0)	Output-to-output skew ^[6, 7]		–	110	200	ps
tskew(pp)	Part-to-part skew ^[9]	$V_{DD} = 3.3\text{ V}$	–	–	1.0	ns
		$V_{DD} = 2.5\text{ V}$	–	–	1.3	ns
tskew(pp)	Part-to-part skew ^[10]		–	–	600	ps
tr/tf	Output clocks rise/fall time ^[6, 7]	0.8 V to 2.0 V, $V_{DD} = 3.3\text{ V}$; 0.5 V to 1.8 V, $V_{DD} = 2.5\text{ V}$	0.2	–	1.1	ns

Notes

5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving $50\ \Omega$ transmission lines.
7. See [Figure 2](#).
8. 50% input duty cycle.
9. Across temperature and voltage ranges, includes output skew.
10. For a specific temperature and voltage, includes output skew.

Figure 2. LVCMOS_CLK CY29942 Test Reference for $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 2.5\text{ V}$

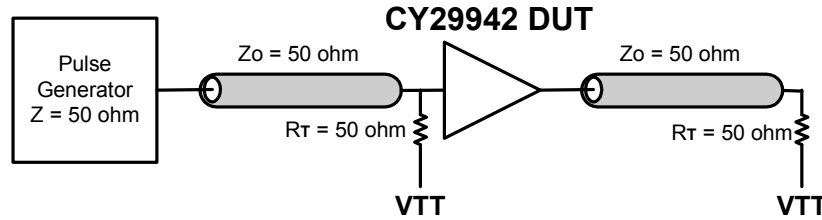


Figure 3. LVCMOS Propagation Delay (t_{pd}) Test Reference

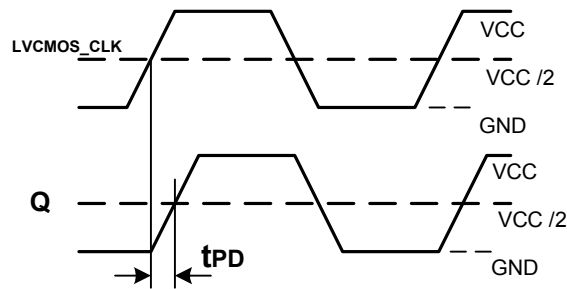


Figure 4. Output Duty Cycle (DC)

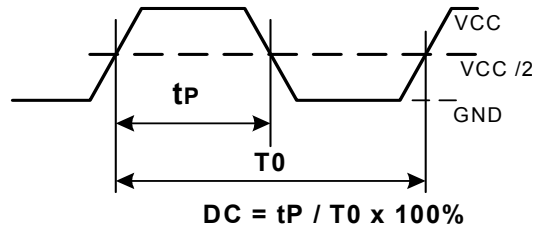
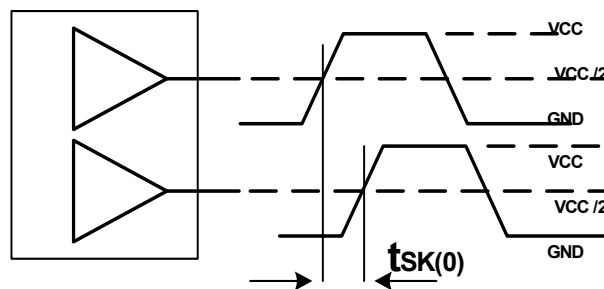


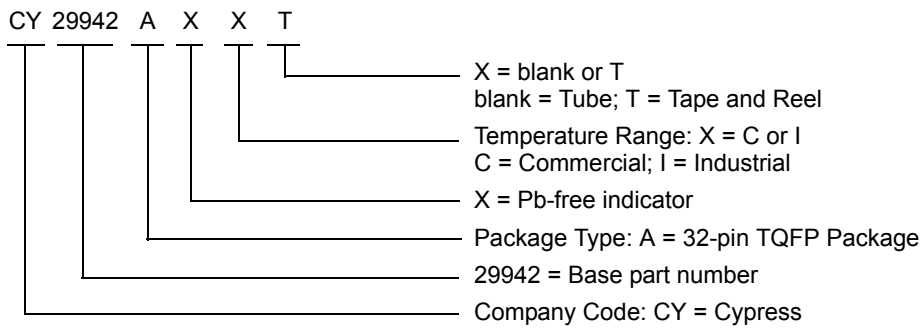
Figure 5. Output-to-Output Skew $t_{sk(0)}$



Ordering Information

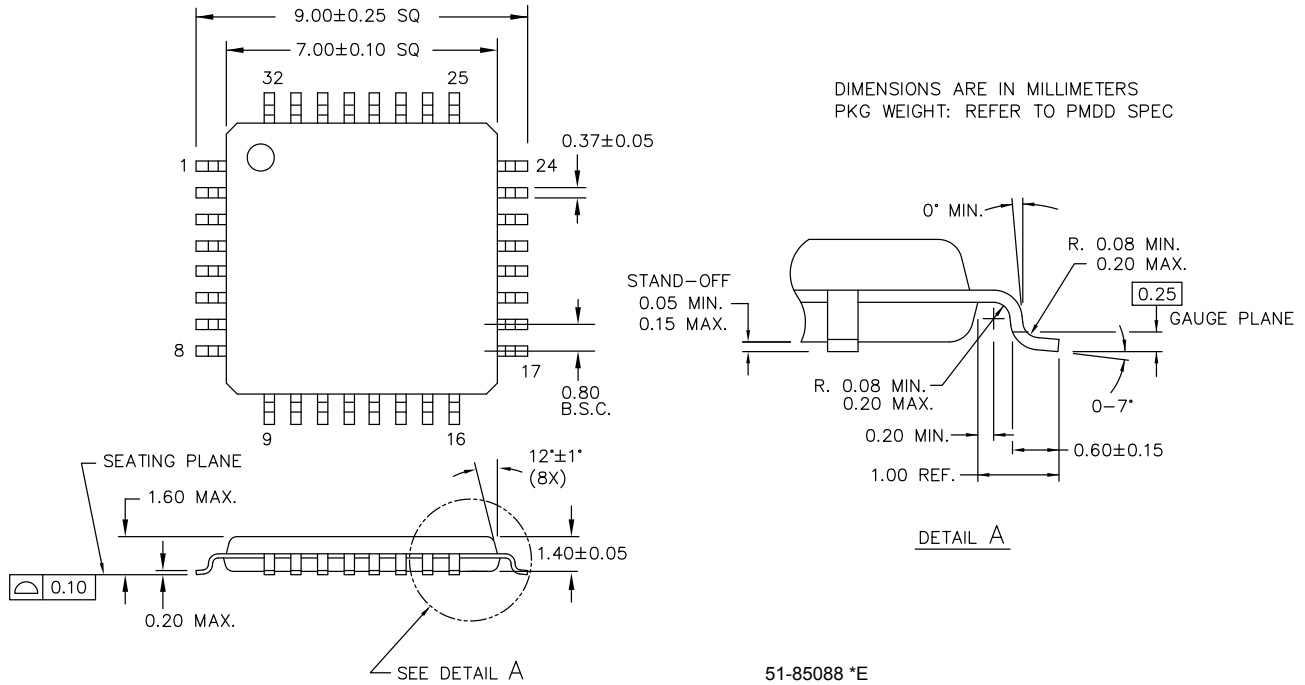
Part Number	Package Type	Production Flow
Pb-free		
CY29942AXI	32-pin TQFP	Industrial, -40 °C to 85 °C
CY29942AXIT	32-pin TQFP – Tape and Reel	Industrial, -40 °C to 85 °C
CY29942AXC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY29942AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 6. 32-pin TQFP (7 × 7 × 1.4 mm) A3214 Package Outline, 51-85088



Acronyms

Acronym	Description
LVC MOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor-Transistor Logic
OE	Output Enable
PLL	Phase-Locked Loop
TQFP	Thin Quad Flat Pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY29942, 1:18 Clock Distribution Buffer				
Document Number: 38-07284				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	111095	BRK	02/07/02	New data sheet.
*A	116777	HWT	08/14/02	Added a Commercial Temp. Range in the Ordering Information
*B	122876	RBI	12/21/02	Add power up requirements to maximum rating information.
*C	334117	RGL	See ECN	Added Lead-free devices Added typical value for output-output skew
*D	2761988	KVM	09/10/09	Ordering Information table: fixed typo and removed obsolete CY29942ACT. Changed Lead-free to Pb-free.
*E	2899304	BASH / CXQ	03/25/2010	Removed CY29942AC part from Ordering Information. Updated package diagram.
*F	3034172	CXQ	09/21/2010	Changed spec title. Updated format of "Features", changed wording in "Functional Description". Removed note 1, added info into Table 1 directly. Removed reference to multiple supplies, power supply sequencing from Absolute Maximum Ratings. Removed reference to V_{DDC} from AC/DC Electrical Specs tables. Added condition $OE = V_{SS}$ for I_{DDQ} in DC Electrical Specs table. Fixed formatting in AC/DC Electrical specs tables. Changed t_{SKEW} to $t_{SK(O)}$ to match Figure 6. Added Ordering Code Definitions . Added Acronyms and Units of Measure sections. Minor edits.
*G	3548252	PURU	03/12/2012	Changed LQFP to TQFP throughout document.
*H	4149208	CINM	10/07/2013	Updated Package Drawing and Dimensions : spec 51-85088 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*I	4586288	CINM	12/03/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Ordering Information : Removed the prune part numbers CY29942AI and CY29942AIT.
*J	5258930	PSR	05/04/2016	Added Thermal Resistance . Updated to new template.
*K	5500790	PAWK	10/28/2016	Sunset Review - No content change.
*L	5972824	AESATMP8	11/21/2017	Updated logo and Copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2002-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View CY29942AXCT on WIN SOURCE](#)
- ⊖ [Cypress Semiconductor Corp Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management