



**THE DATASHEET OF
PE42521C-Z**



Product Description

The PE42521 SPDT absorptive RF switch is designed for use in test/ATE and other high performance wireless applications. This broadband general purpose switch maintains excellent RF performance and linearity from 9 kHz through 13 GHz. This switch is a pin-compatible upgraded version of PE42552 with fast switching time and higher power handling of 36 dBm continuous wave (CW) and 38.5 dBm instantaneous power in 50Ω @ 4 GHz. The PE42521 exhibits high isolation, fast settling time, and is offered in a 3x3 mm QFN package.

The PE42521 is manufactured on pSemi's UltraCMOS[®] process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- HaRP™ technology enhanced
 - Fast settling time of 2 μs
 - No gate and phase lag
 - No drift in insertion loss and phase
- Fast switching time of 500 ns
- High power handling @ 4 GHz in 50Ω
 - 36 dBm CW
 - 38.5 dBm instantaneous power
 - 26 dBm terminated port
- High linearity
 - 65 dBm IIP3
- Low insertion loss
 - 0.75 dB @ 3 GHz
 - 1.15 dB @ 10 GHz
 - 1.85 dB @ 13 GHz
- High isolation
 - 44 dB @ 3 GHz
 - 30 dB @ 10 GHz
 - 17 dB @ 13 GHz
- ESD performance
 - 3kV HBM on RF pins to GND
 - 1.5kV HBM on all pins

Figure 1. Functional Diagram

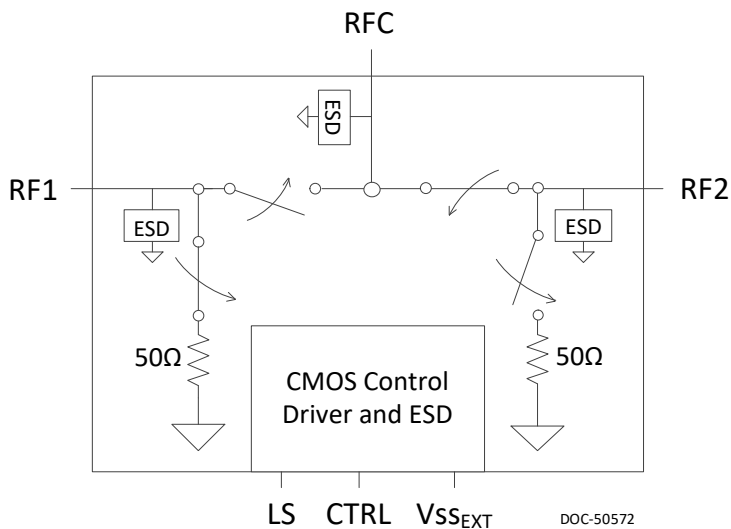


Figure 2. Package Type
16-lead 3x3 mm QFN



Table 1. Revision History

| Document Revision | Date | Change Description |
|-------------------|---------------|---------------------------|
| DOC-79380-2 | February 2024 | Table 4, Operating Ranges |

Table 2. Electrical Specifications @ 25°C, V_{DD} = 3.3V, V_{SS}EXT = 0V or V_{DD} = 3.4V, V_{SS}EXT = -3.4V, (Z_S = Z_L = 50Ω) unless otherwise noted

| Parameter | Path | Condition | Min | Typ | Max | Unit |
|---|---------|---------------------------------------|-------|--------|--------|----------|
| Operation frequency | | | 9 kHz | | 13 GHz | As shown |
| Insertion loss | RFC-RFX | 9 kHz – 10 MHz | | 0.60 | 0.80 | dB |
| | | 10 MHz – 3 GHz | | 0.75 | 1.00 | dB |
| | | 3 GHz – 7.5 GHz | | 0.95 | 1.20 | dB |
| | | 7.5 GHz – 10 GHz | | 1.15 | 1.40 | dB |
| | | 10 GHz – 12 GHz | | 1.75 | 2.20 | dB |
| | | 12 GHz – 13 GHz | | 1.85 | 2.60 | dB |
| Isolation | RFX-RFX | 9 kHz – 10 MHz | 70 | 90 | | dB |
| | | 10 MHz – 3 GHz | 46 | 49 | | dB |
| | | 3 GHz – 7.5 GHz | 35 | 37 | | dB |
| | | 7.5 GHz – 10 GHz | 23 | 26 | | dB |
| | | 10 GHz – 12 GHz | 16 | 19 | | dB |
| | | 12 GHz – 13 GHz | 14 | 17 | | dB |
| Isolation | RFC-RFX | 9 kHz – 10 MHz | 80 | 90 | | dB |
| | | 10 MHz – 3 GHz | 42 | 44 | | dB |
| | | 3 GHz – 7.5 GHz | 39 | 41 | | dB |
| | | 7.5 GHz – 10 GHz | 26 | 30 | | dB |
| | | 10 GHz – 12 GHz | 18 | 21 | | dB |
| | | 12 GHz – 13 GHz | 14 | 17 | | dB |
| Return loss (active port) | RFC-RFX | 9 kHz – 10 MHz | | 23 | | dB |
| | | 10 MHz – 3 GHz | | 19 | | dB |
| | | 3 GHz – 7.5 GHz | | 16 | | dB |
| | | 7.5 GHz – 10 GHz | | 21 | | dB |
| | | 10 GHz – 12 GHz | | 10 | | dB |
| | | 12 GHz – 13 GHz | | 15 | | dB |
| Return loss (common port) | RFC-RFX | 9 kHz – 10 MHz | | 23 | | dB |
| | | 10 MHz – 3 GHz | | 19 | | dB |
| | | 3 GHz – 7.5 GHz | | 16 | | dB |
| | | 7.5 GHz – 10 GHz | | 21 | | dB |
| | | 10 GHz – 12 GHz | | 10 | | dB |
| | | 12 GHz – 13 GHz | | 16 | | dB |
| Return loss (terminated port) | RFX | 9 kHz – 10 MHz | | 32 | | dB |
| | | 10 MHz – 3 GHz | | 23 | | dB |
| | | 3 GHz – 7.5 GHz | | 18 | | dB |
| | | 7.5 GHz – 10 GHz | | 11 | | dB |
| | | 10 GHz – 12 GHz | | 6 | | dB |
| | | 12 GHz – 13 GHz | | 5 | | dB |
| Input 0.1 dB compression point ¹ | RFC-RFX | 600 MHz – 13 GHz | | Fig. 5 | | dBm |
| Input IP2 | RFC-RFX | 834 MHz, 1950 MHz | | 120 | | dBm |
| Input IP3 | RFC-RFX | 834 MHz, 1950 MHz, and 2700 MHz | | 65 | | dBm |
| Settling time | | 50% CTRL to 0.05 dB final value | | 2 | 4 | μs |
| Switching time | | 50% CTRL to 90% or 10% of final value | | 500 | 700 | ns |

Note 1: The input 0.1 dB compression point is a linearity figure of merit. Refer to Table 3 for the RF input power P_{IN} (50Ω)

Figure 3. Pin Configuration (Top View)

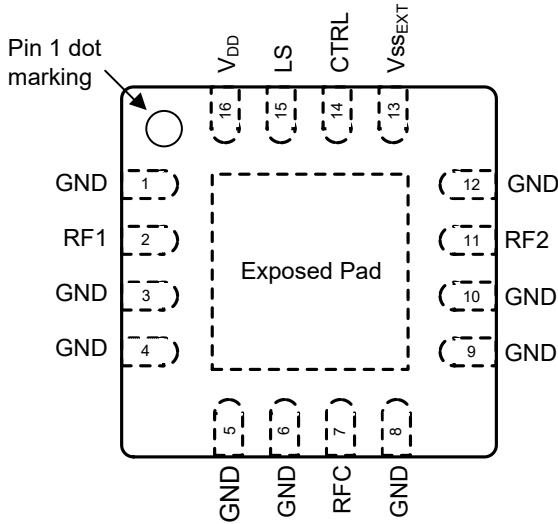


Table 3. Pin Descriptions

| Pin # | Pin Name | Description |
|-----------------------------|----------------------|--|
| 2 | RF1 ¹ | RF port 1 |
| 1, 3, 4, 5, 6, 8, 9, 10, 12 | GND | Ground |
| 7 | RFC ¹ | RF common |
| 11 | RF2 ¹ | RF port 2 |
| 13 | VSS_EXT ² | External Vss negative voltage control |
| 14 | CTRL | Digital control logic input |
| 15 | LS | Logic Select - used to determine the definition for the CTRL pin (see Table 5) |
| 16 | VDD | Supply voltage |
| Pad | GND | Exposed pad: ground for proper operation |

Notes: 1. RF pins 2, 7, and 11 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met
2. Use VSS_EXT (pin 13) to bypass and disable internal negative voltage generator. Connect VSS_EXT (pin 13) to GND (VSS_EXT = 0V) to enable internal negative voltage generator

Table 4. Operating Ranges

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------|------|-----|--------|------|
| Supply voltage (normal mode, VSS_EXT = 0V) ¹ | VDD | 2.3 | | 5.5 | V |
| Supply voltage (bypass mode, VSS_EXT = -3.4V, VDD ≥ 3.4V for full spec. compliance) ² | VDD | 2.7 | 3.4 | 5.5 | V |
| Negative supply voltage (bypass mode) ² | VSS_EXT | -3.6 | | -3.2 | V |
| Supply current (normal mode, VSS_EXT = 0V) ¹ | IDD | | 120 | 200 | μA |
| Supply current (bypass mode, VSS_EXT = -3.4V) ² | IDD | | 50 | 80 | μA |
| Negative supply current (bypass mode, VSS_EXT = -3.4V) ² | ISS | -40 | -16 | | μA |
| Digital input high (CTRL) | VIH | 1.07 | | 3.6 | V |
| Digital input low (CTRL) | VIL | -0.3 | | 0.68 | V |
| Digital input current | ICTRL | | | 10 | μA |
| RF input power, CW (RFC-RFX) ³ | PIN-CW | | | | |
| 9 kHz ≤ 600 MHz | | | | Fig. 4 | dBm |
| 600 MHz ≤ 4 GHz | | | | 36 | dBm |
| 4 GHz ≤ 13 GHz | | | | Fig. 5 | dBm |
| RF input power, pulsed (RFC-RFX) ⁴ | PIN-PULSED | | | | |
| 9 kHz ≤ 600 MHz | | | | Fig. 4 | dBm |
| 600 MHz ≤ 13 GHz | | | | Fig. 5 | dBm |
| RF input power, hot switch, CW ³ | PIN-HOT | | | | |
| 9 kHz ≤ 10 MHz | | | | Fig. 4 | dBm |
| 10 MHz ≤ 13 GHz | | | | 20 | dBm |
| RF input power into terminated ports, CW (RFX) ³ | PIN-TERM | | | | |
| 9 kHz ≤ 30 MHz | | | | Fig. 4 | dBm |
| 30 MHz ≤ 13 GHz | | | | 26 | dBm |
| Operating temperature range | TOP | -40 | +25 | +85 | °C |

Notes: 1. Normal mode: connect VSS_EXT (pin 13) to GND (VSS_EXT = 0V) to enable internal negative voltage generator
2. Bypass mode: use VSS_EXT (pin 13) to bypass and disable internal negative voltage generator
3. 100% duty cycle, all bands, 50W
4. Pulsed, 5% duty cycle of 4620 μs period, 50W

Table 5. Absolute Maximum Ratings

| Parameter/Condition | Symbol | Min | Max | Unit | | |
|---|-----------------|------|------------------|------------|--------|-----|
| Supply voltage | V_{DD} | -0.3 | 5.5 | V | | |
| Digital input voltage (CTRL) | V_{CTRL} | -0.3 | 3.6 | V | | |
| LS input voltage | V_{LS} | -0.3 | 3.6 | V | | |
| RF input power, CW (RFC-RFX) ¹ | P_{IN-CW} | | Fig. 4 36 | dBm | | |
| 9 kHz ≤ 600 MHz | | | | | Fig. 5 | dBm |
| 600 MHz ≤ 4 GHz 4 GHz ≤ 13 GHz | | | | | | |
| RF input power, pulsed (RFC-RFX) ² | $P_{IN-PULSED}$ | | Fig. 4 Fig. 5 | dBm dBm | | |
| 9 kHz ≤ 600 MHz 600 MHz ≤ 13 GHz | | | | | | |
| RF input power into terminated ports, CW (RFX) ¹ | $P_{IN,TERM}$ | | Fig. 4 26 | dBm dBm | | |
| 9 kHz ≤ 30 MHz 30 MHz ≤ 13 GHz | | | | | | |
| Storage temperature range | T_{ST} | -65 | +150 | °C | | |
| ESD voltage HBM ³ | $V_{ESD,HBM}$ | | 3000 1500 | V V | | |
| RF pins to GND All pins | | | | | | |
| ESD voltage MM ⁴ , all pins | $V_{ESD,MM}$ | | 200 | V | | |
| ESD voltage CDM ⁵ , all pins | $V_{ESD,CDM}$ | | 1000 | V | | |

Notes: 1. 100% duty cycle, all bands, 50Ω

- 2. Pulsed, 5% duty cycle of 4620 μs period, 50Ω
- 3. Human Body Model (MIL-STD 883 Method 3015)
- 4. Machine Model (JEDEC JESD22-A115)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS[®] device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS[®] devices are immune to latch-up.

Switching Frequency

The PE42521 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 13 = GND). The rate at which the PE42521 can be switched is only limited to the switching time (*Table 1*) if an external negative supply is provided (pin 13 = $V_{SS,EXT}$).

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its

Optional External Vss Control ($V_{SS,EXT}$)

For proper operation, the $V_{SS,EXT}$ control pin must be grounded or tied to the V_{SS} voltage specified in *Table 3*. When the $V_{SS,EXT}$ control pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, $V_{SS,EXT}$ can be applied externally to bypass the internal negative voltage

Spurious Performance

The typical spurious performance of the PE42521 is -135 dBm when $V_{SS,EXT} = 0V$ (pin 13 = GND). If further improvement is desired, the internal negative voltage generator can be disabled by setting $V_{SS,EXT} = -3.4V$.

Table 6. Control Logic Truth Table

| LS | CTRL | RFC-RF1 | RFC-RF2 |
|----|------|---------|---------|
| 0 | 0 | off | on |
| 0 | 1 | on | off |
| 1 | 0 | on | off |
| 1 | 1 | off | on |

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42521 in the 16-lead 3x3 mm QFN package is MSL3.

Logic Select (LS)

The Logic Select feature is used to determine the definition for the CTRL pin.

Figure 4. Power De-rating Curve for 9 kHz – 600 MHz (50Ω)

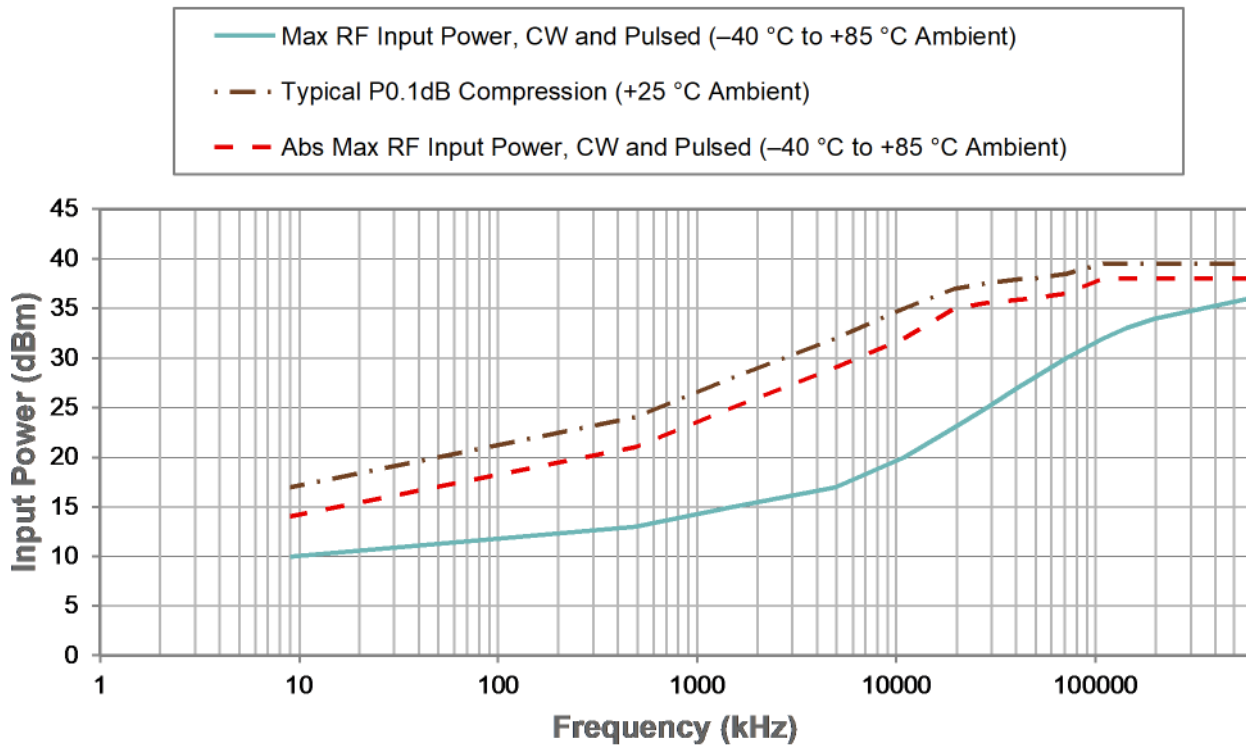


Figure 5a. Power De-rating Curve for 600 MHz – 13 GHz @ 25°C Ambient (50Ω)

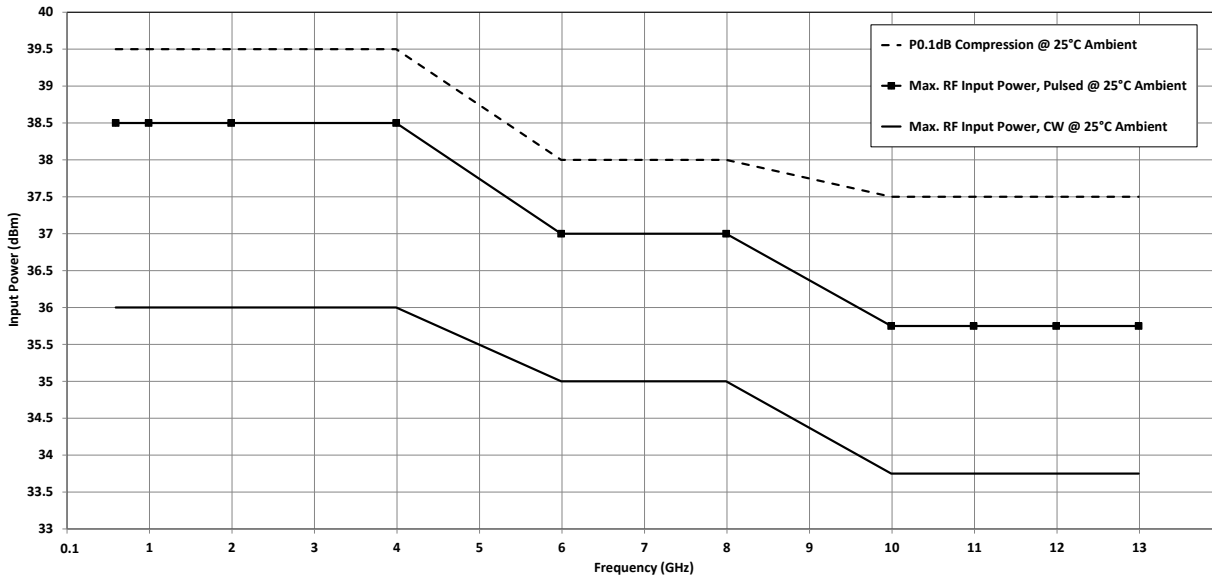
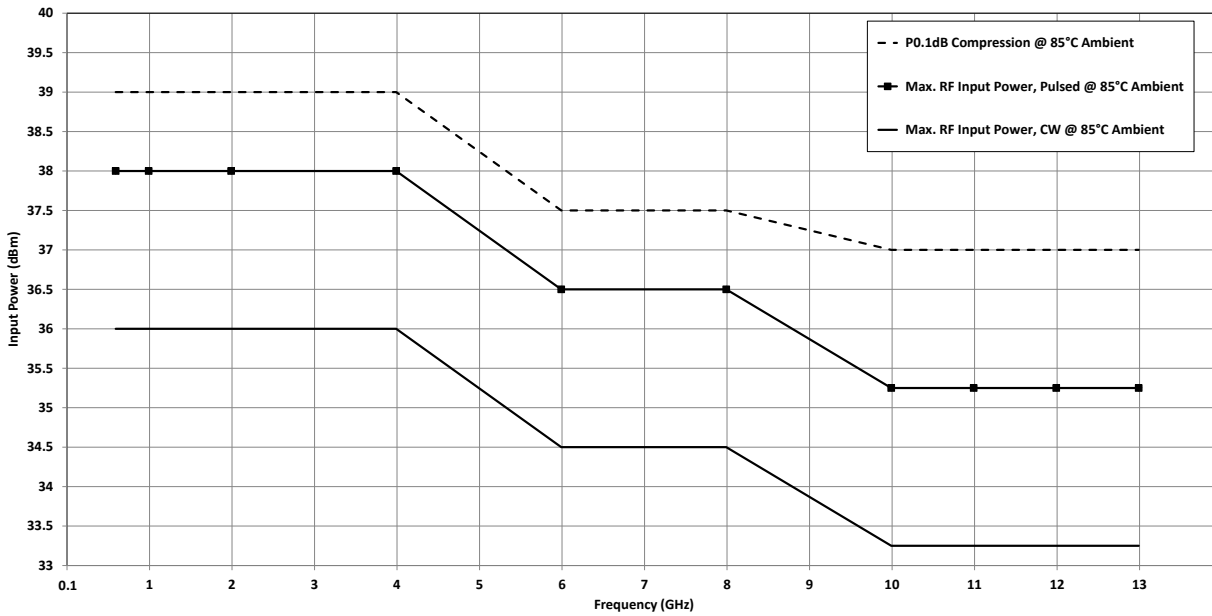


Figure 5b. Power De-rating Curve for 600 MHz – 13 GHz @ 85°C Ambient (50Ω)



Typical Performance Data @ 25°C and $V_{DD} = 3.4V$ unless otherwise specified

Figure 6. Insertion Loss vs. Temp (RFC–RF1)

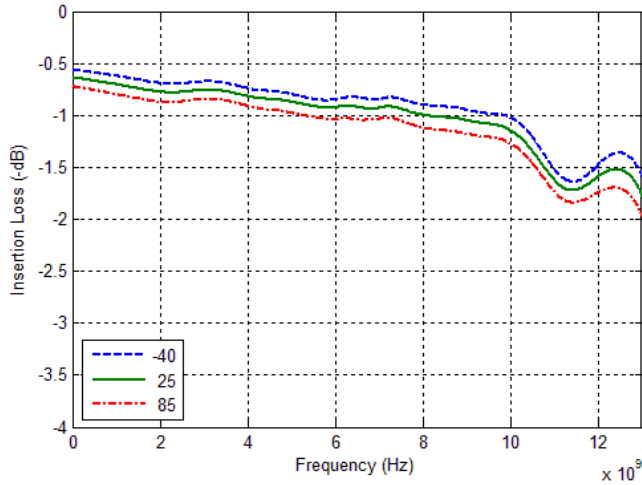


Figure 7. Insertion Loss vs. V_{DD} (RFC–RF1)

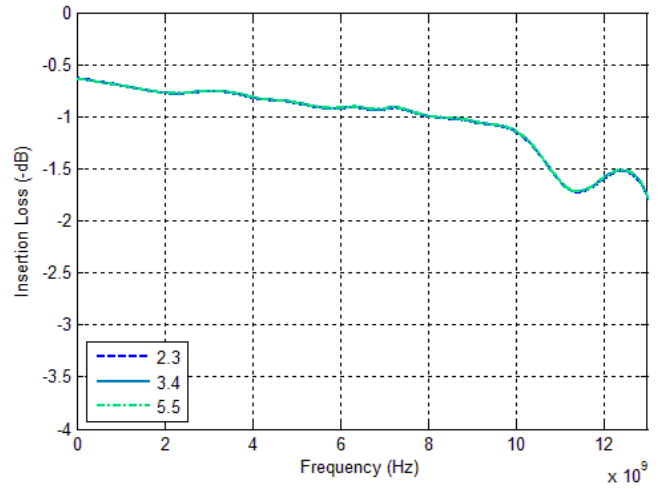


Figure 8. Insertion Loss vs. Temp (RFC–RF2)

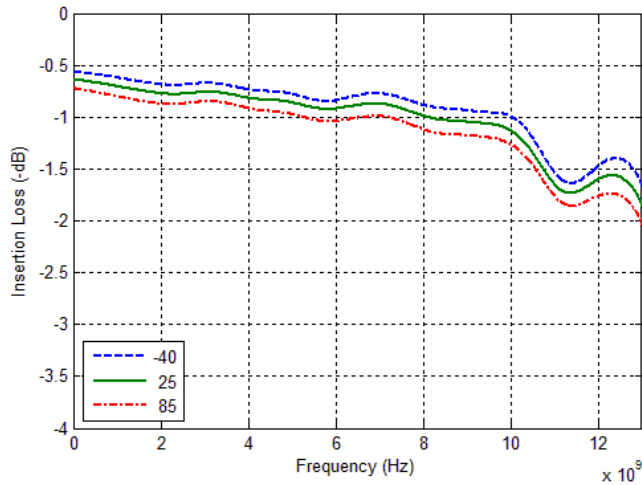
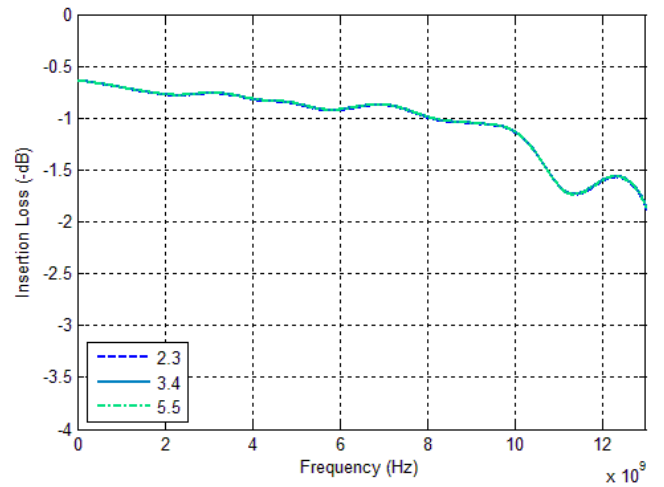


Figure 9. Insertion Loss vs. V_{DD} (RFC–RF2)



Typical Performance Data @ 25°C and $V_{DD} = 3.4V$ unless otherwise specified

Figure 10. RFC Port Return Loss vs. Temp (RF1 Active)

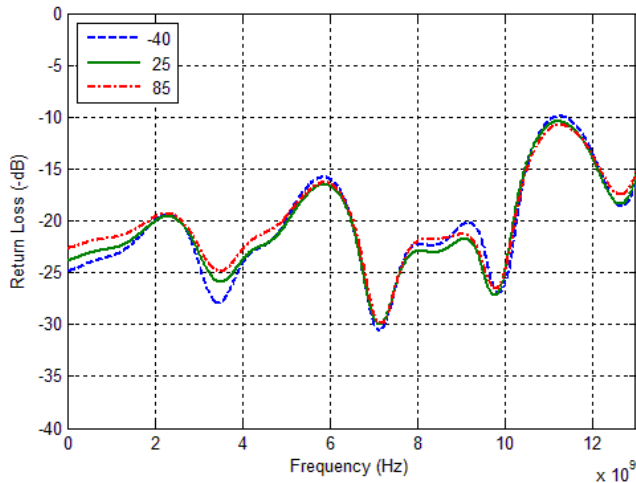


Figure 11. RFC Port Return Loss vs. V_{DD} (RF1 Active)

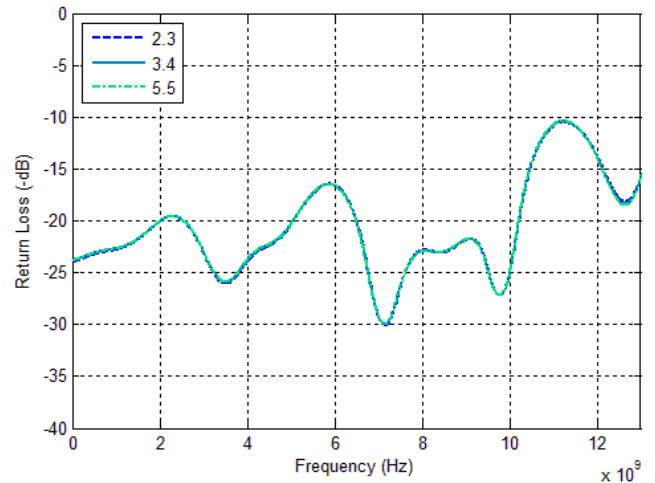


Figure 12. RFC Port Return Loss vs. Temp (RF2 Active)

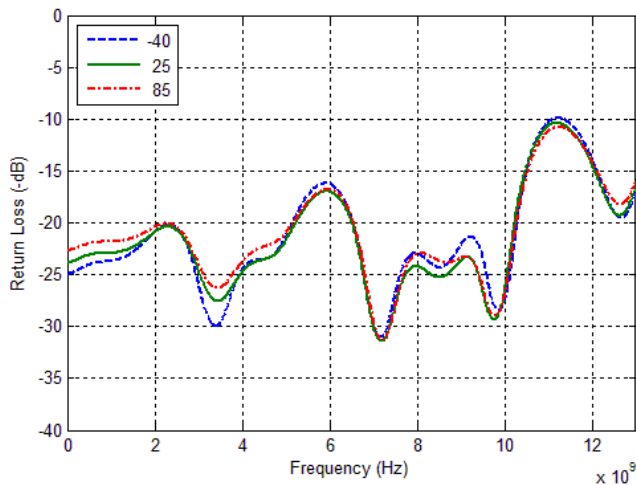
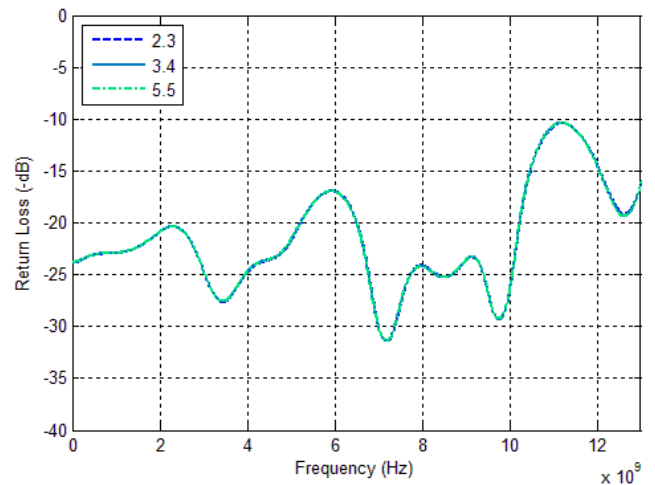


Figure 13. RFC Port Return Loss vs. V_{DD} (RF2 Active)



Typical Performance Data @ 25°C and $V_{DD} = 3.4V$ unless otherwise specified

Figure 14. Active Port Return Loss vs. Temp (RF1 Active)

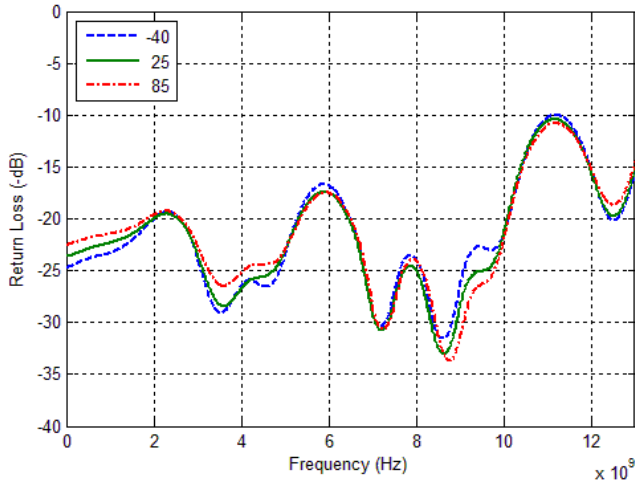


Figure 15. Active Port Return Loss vs. V_{DD} (RF1 Active)

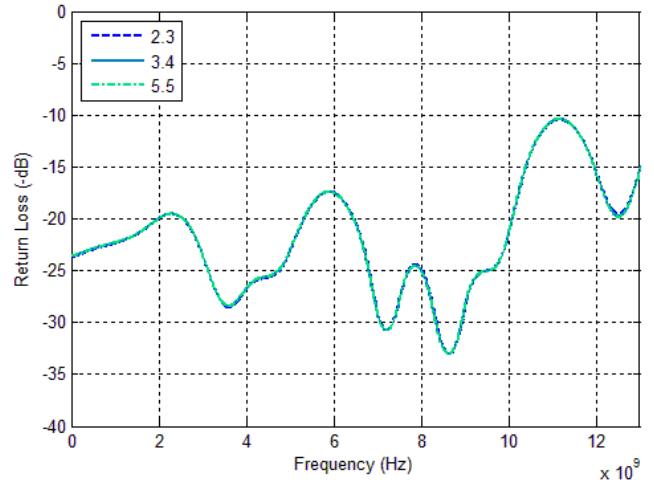


Figure 16. Active Port Return Loss vs. Temp (RF2 Active)

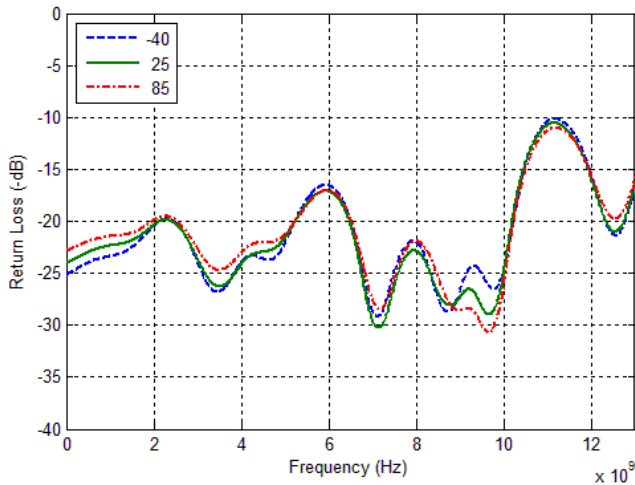
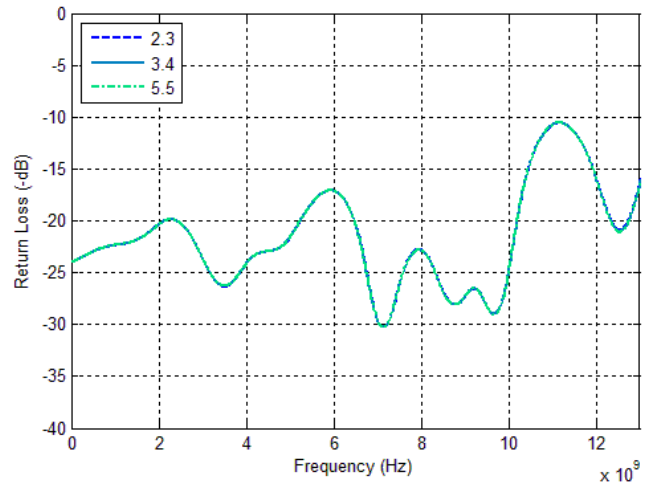


Figure 17. Active Port Return Loss vs. V_{DD} (RF2 Active)



Typical Performance Data @ 25°C and $V_{DD} = 3.4V$ unless otherwise specified

Figure 18. Terminated Port Return Loss vs. Temp (RF1 Active)

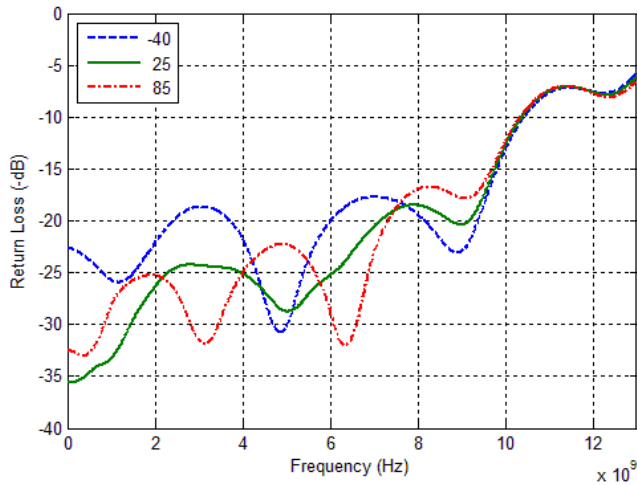


Figure 19. Terminated Port Return Loss vs. V_{DD} (RF1 Active)

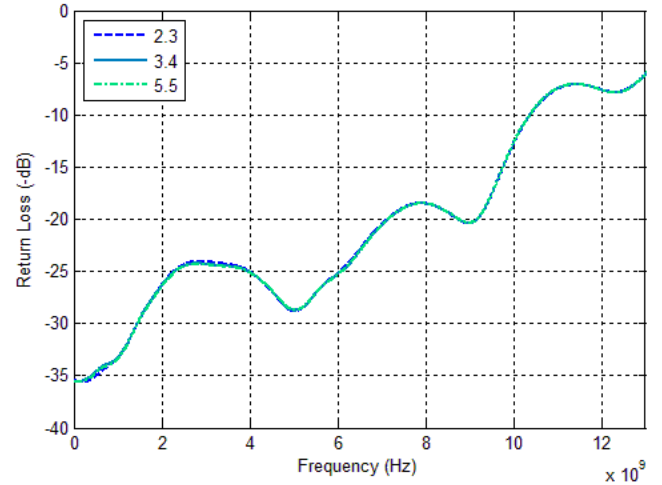


Figure 20. Terminated Port Return Loss vs. Temp (RF2 Active)

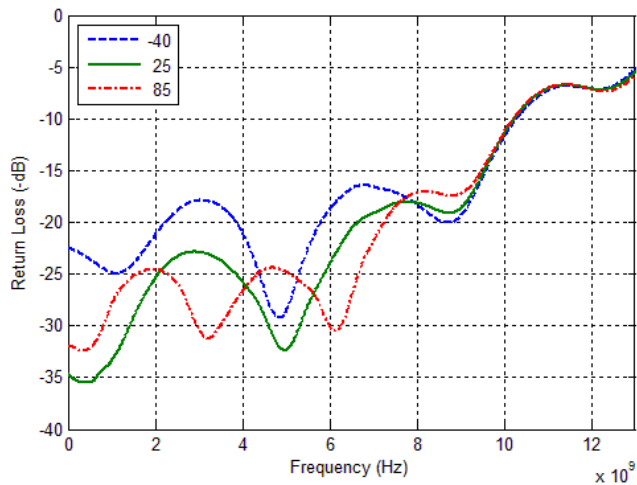
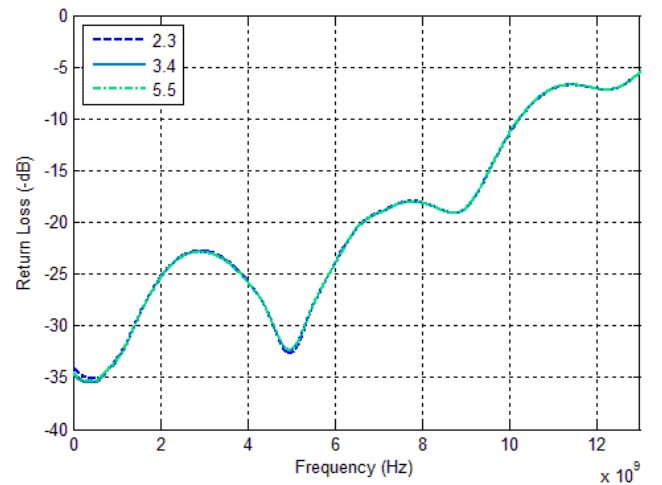


Figure 21. Terminated Port Return Loss vs. V_{DD} (RF2 Active)



Typical Performance Data @ 25°C and $V_{DD} = 3.4V$ unless otherwise specified

Figure 22. Isolation vs. Temp (RF1–RF2, RF1 Active)

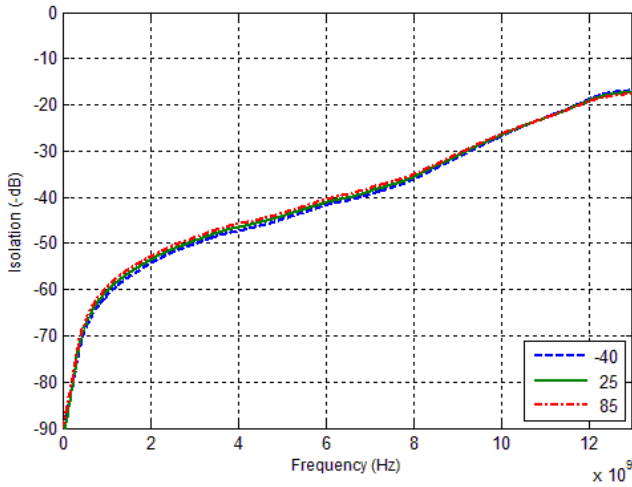


Figure 23. Isolation vs. V_{DD} (RF1–RF2, RF1 Active)

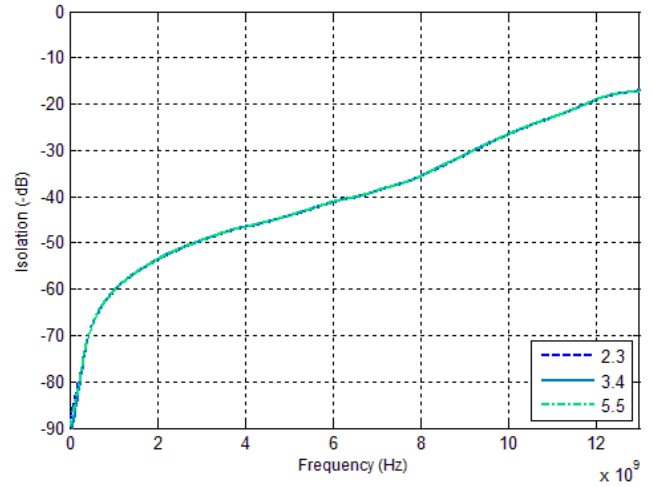


Figure 24. Isolation vs. Temp (RF2–RF1, RF2 Active)

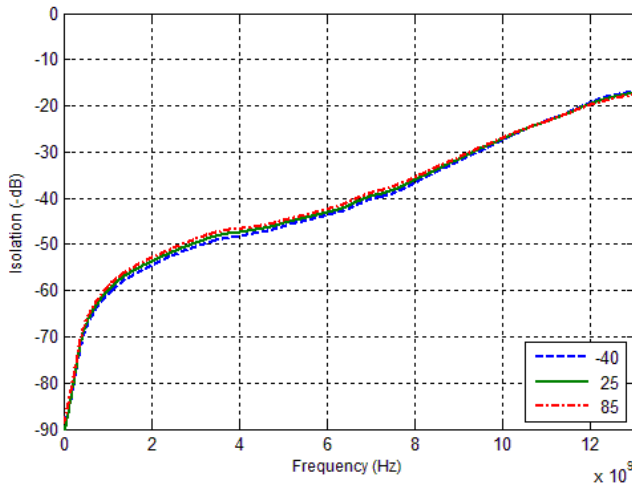
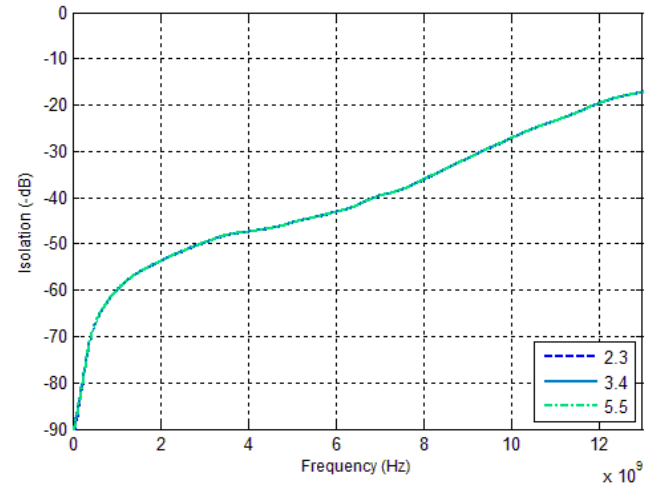


Figure 25. Isolation vs. V_{DD} (RF2–RF1, RF2 Active)



Typical Performance Data @ 25°C and $V_{DD} = 3.4V$ unless otherwise specified

Figure 26. Isolation vs. Temp
(RFC–RF2, RF1 Active)

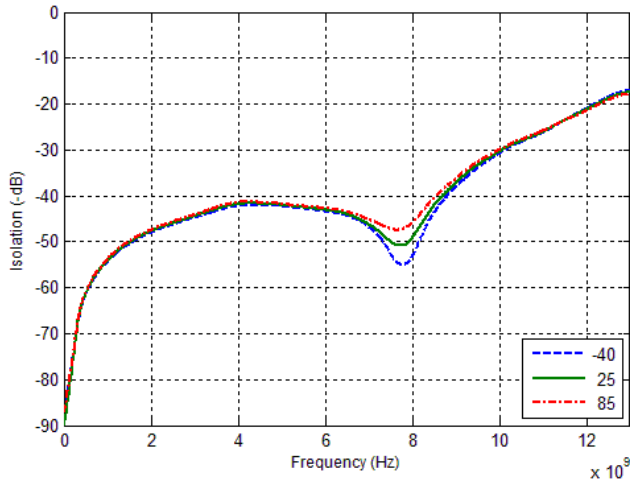


Figure 27. Isolation vs. V_{DD}
(RFC–RF2, RF1 Active)

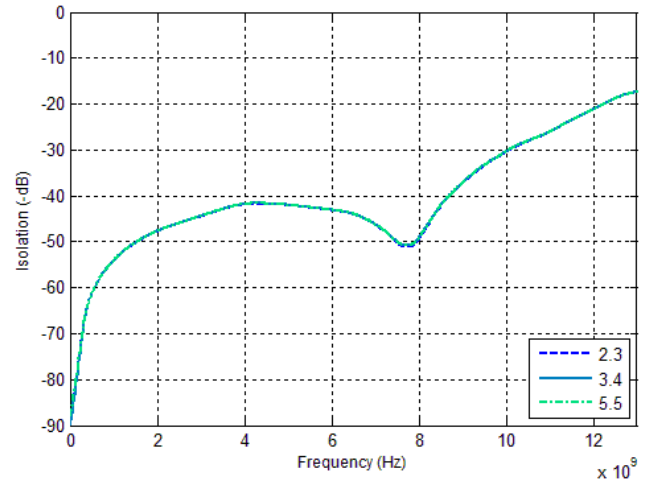


Figure 28. Isolation vs. Temp
(RFC–RF1, RF2 Active)

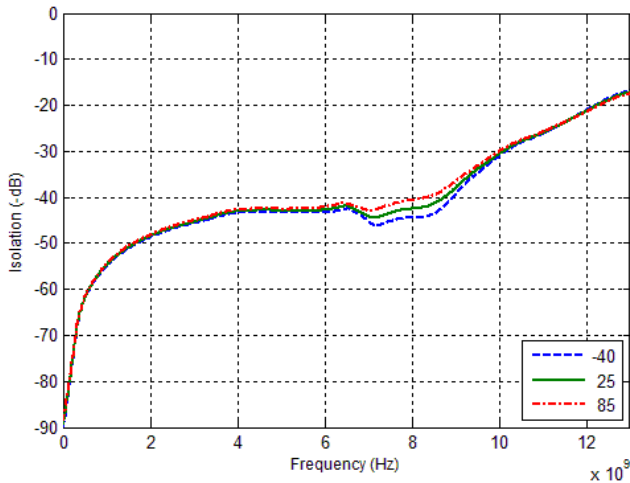
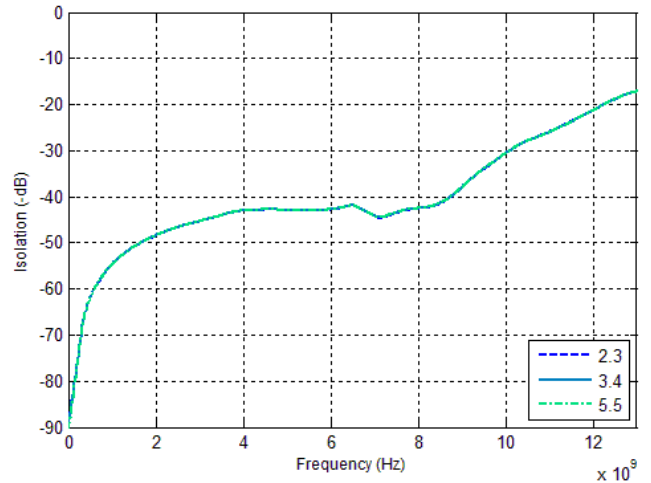


Figure 29. Isolation vs. V_{DD}
(RFC–RF1, RF2 Active)

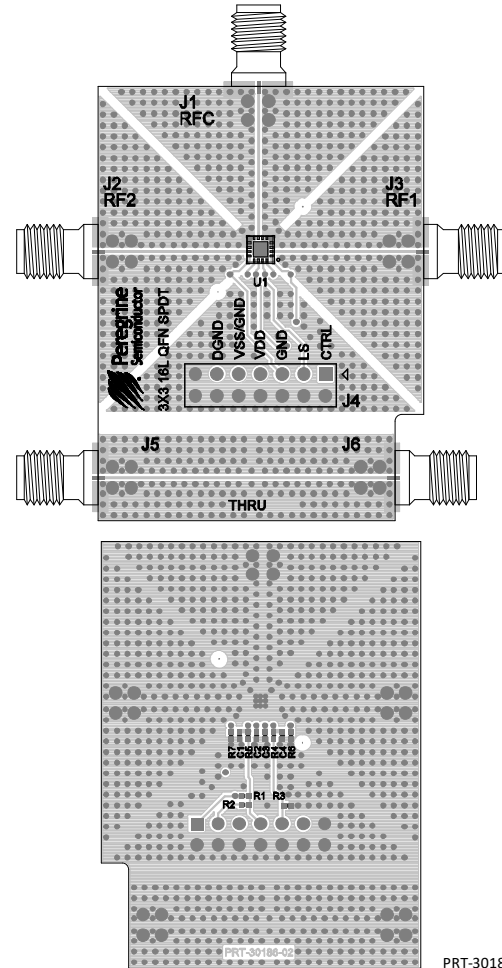


Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of pSemi's PE42521. The RF common port is connected through a 50Ω transmission line via the SMA connector, J1. RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which can be used to de-embed the loss of the PCB. J4 provides DC and digital inputs to the device.

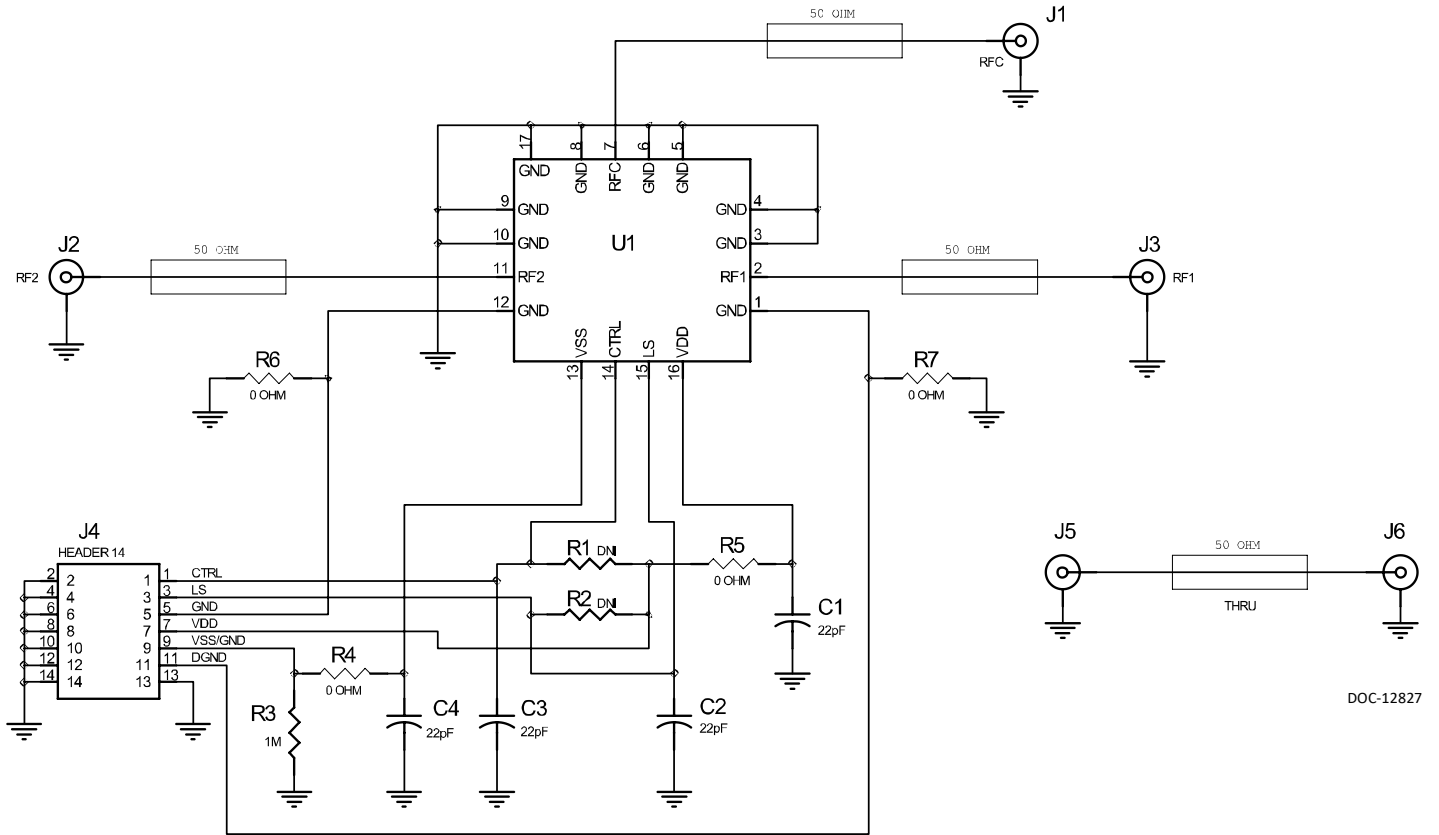
For the true performance of the PE42521 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

Figure 30. Evaluation Kit Layout



PRT-30186

Figure 31. Evaluation Board Schematic



- Notes:
1. Use PRT-30186-02 PCB
 2. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD)

Figure 32. Package Drawing
16-lead 3x3 mm QFN

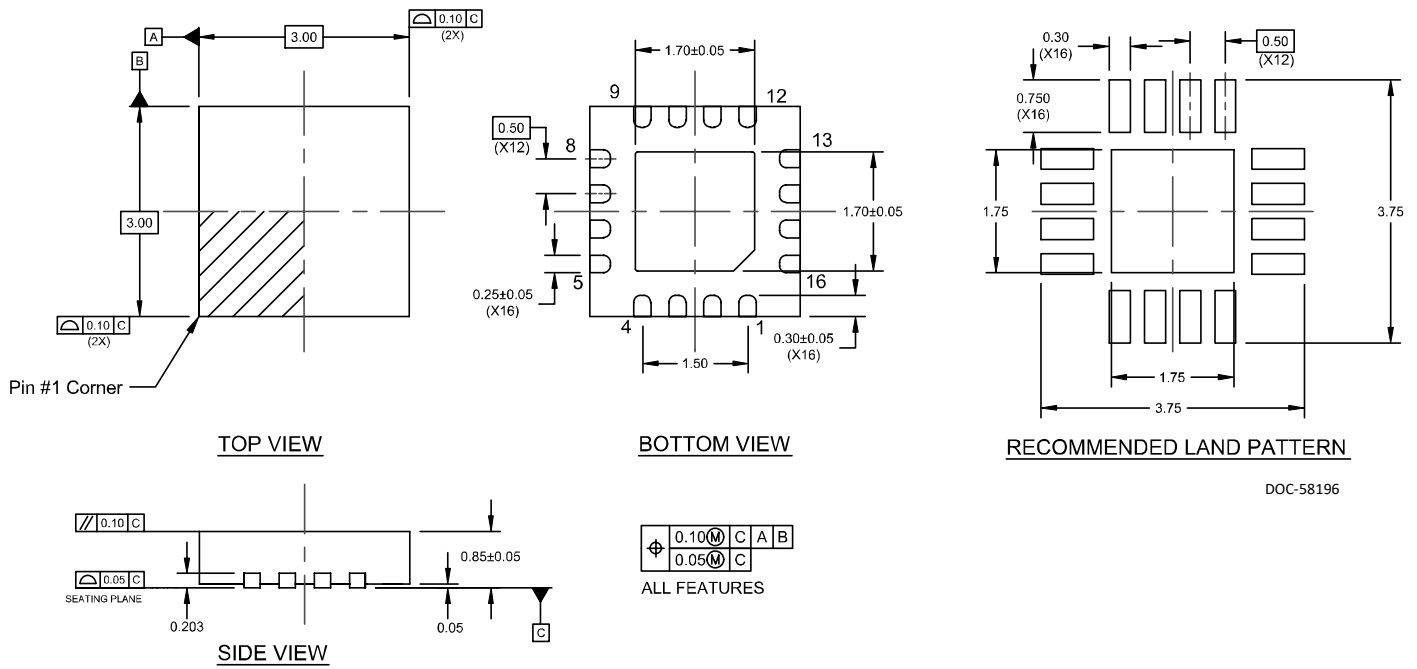
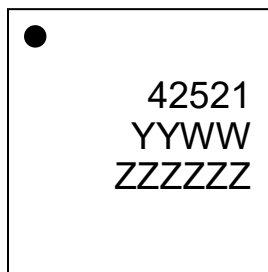


Figure 33. Top Marking Specifications



DOC-66053

- = Pin 1 designator
- YY = Last two digits of assembly year
- WW = Assembly work week
- ZZZZZZ = Assembly lot code (maximum six characters)

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