THE DATASHEET OF

SI4012-A0-GT

Si4021 Universal ISM Band FSK Transmitter

DESCRIPTION

Silicon Labs' Si4021 is a single chip, low power, multi-channel FSK transmitter designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 433, 868, and 915 MHz bands. Used in conjunction with Si4020, Silicon Labs' FSK receiver, the Si4021 transmitter features EZRadio™ technology, which produces a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation. The Si4021 builds on the features presented by the Si4020 by offering a higher output power and an improved phase noise characteristic. The Si4021 shares the same pinout and control command set as the Si4020. The Si4021 offers all of the frequencies as the Si4020, with the exception of the 315 MHz band.

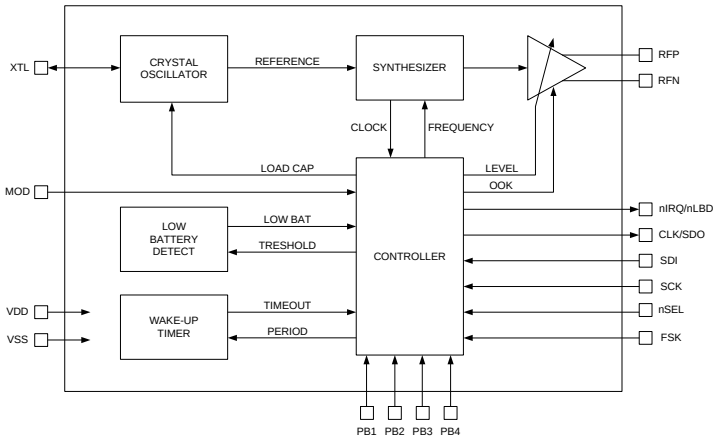
The Si4021 features a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading and interference to achieve robust wireless links. In addition, highly stable and accurate FSK modulation is accomplished by direct closed-loop modulation with bit rates up to 115.2 kbps. The PLL's high resolution allows the use of multiple channels in any of the bands.

The integrated power amplifier of the transmitter has an open-collector differential output that directly drive a loop antenna with programmable output level. No additional matching network is required. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and de-tuning due to the "hand effect".

For low-power applications, the device supports automatic activation from sleep mode. Active mode can be initiated by several wake-up events (on-chip timer timeout, low supply voltage detection, or activation of any of the four push-button inputs).

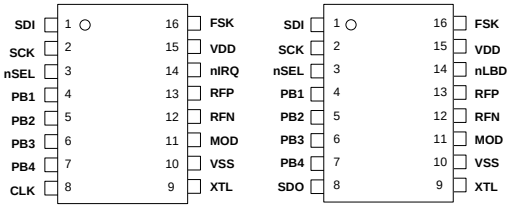
The Si4021's on-chip digital interface supports both a microcontroller mode and an EEPROM mode. The latter allows complete data transmitter operation without a microcontroller (both control commands and data are read from the EEPROM). Any wake-up event can start a transmission of the corresponding data stored in the EEPROM.

FUNCTIONAL BLOCK DIAGRAM



Si4021

PIN ASSIGNMENT



Microcontroller Mode EEPROM Mode

This document refers to Si4021-IC Rev A1.
See www.silabs.com/integration for any applicable errata. See back page for ordering information.

FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- Stable and accurate FSK modulation with programmable deviation
- Programmable PLL loop bandwidth
- Direct loop antenna drive
- Automatic antenna tuning circuit
- Programmable output power level
- Alternative OOK support
- EEPROM mode supported
- SPI bus for applications with microcontroller
- Clock output for microcontroller
- Integrated programmable crystal load capacitor
- Multiple event handling options for wake-up activation
- Push-button event handling with switch de-bounce
- Wake-up timer
- Low battery detection
- 2.2 to 5.4 V supply voltage
- Low power consumption
- Low standby current (0.3 µA)
- Compact 16-pin TSSOP package
- Transmit bit synchronization

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED DESCRIPTION

The Si4021 FSK transmitter is designed to cover the unlicensed frequency bands at 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows the usage of multiple channels in any of the bands. The FSK deviation is selectable (from 30 to 210 kHz with 30 kHz increments) to accommodate various bandwidth, data rate and crystal tolerance requirements, and it is also highly accurate due to the direct closed-loop modulation of the PLL. The transmitted digital data can be sent asynchronously through the FSK pin or over the control interface using the appropriate command.

The RF VCO in the PLL performs automatic calibration, which requires only a few microseconds. To ensure proper operation in the programmed frequency band, the RF VCO is automatically calibrated upon activation of the synthesizer. If temperature or supply voltage change significantly or operational band has changed, VCO recalibration is recommended.. Recalibration can be initiated at any time by switching the synthesizer off and back on again.

RF Power Amplifier (PA)

The power amplifier has an open-collector differential output and can directly drive a loop antenna with a programmable output power level. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and the so-called "hand effect."

The transmitters can operate in On-Off Keying (OOK) mode by switching the power amplifier on and off. When the appropriate control bit is set using the *Power Setting Command*, the FSK pin becomes an enable input (active high) for the power amplifier.

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet.

The transmitters can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. When the chip receives a *Sleep Command* from the microcontroller and turns itself off, it provides several further clock pulses ("clock tail") for the microcontroller to be able to go to idle or sleep mode. The length of the clock tail is programmable.

Low Battery Voltage Detector

The low battery voltage detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level. The detector circuit has 50 mV hysteresis.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 µA typical) and can be programmed from 1 ms to several days with an accuracy of ±5%.

It calibrates itself to the crystal oscillator at every startup, and then every 30 seconds. When the oscillator is switched off, the calibration circuit switches on the crystal oscillator only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing. The auto calibration feature can be disabled by setting the a bit in the *Low Battery Detector Command*.

Event Handling

In order to minimize current consumption, the device supports sleep mode. Active mode can be initiated by several wake-up events: timeout of wake-up timer, detection of low supply voltage, pressing any of the four push-button inputs, or through the serial interface. The push-button inputs can be driven by a logic signal from a microcontroller or controlled directly by normally open switches. Pull-up resistors are integrated.

If any wake-up event occurs, the wake-up logic generates an interrupt, which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the transmitters by the microcontroller through the nIRQ pin.

Interface

An SPI compatible serial interface lets the user select the operating frequency band and center frequency of the synthesizer, polarity and deviation of FSK modulation, and output power level. Division ratio for the microcontroller clock, wake-up timer period, and low battery detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode.

EEPROM Mode

In simple applications, the on-chip digital controller provides the transmitters with direct interface to a serial (SPI) EEPROM. In this case, no external microcontroller is necessary. Wake-up events initiate automatic readout of the assigned command sequence from EEPROM memory. For every event, there is a dedicated starting address available in the EEPROM.

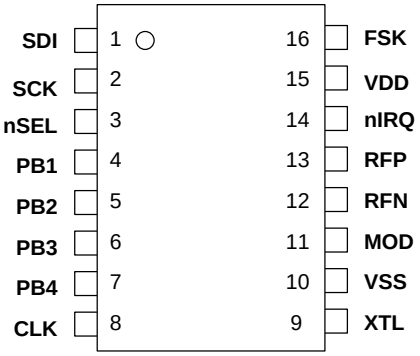
Programming the EEPROM is very simple. Any control command can be programmed in the EEPROM sequentially (same as in microcontroller mode).

The internal power-on reset (POR) is a dedicated event, which can be used to program the basic settings of the transmitters. In this case the chip starts to read out the preprogrammed data from the 00h address in EEPROM. Data can be transmitted with the help of the *Data Transmit Command*, which tells the transmitters how many bytes must be transmitted. The whole process finishes with a *Sleep Command.*

PACKAGE PIN DEFINITIONS, MICROCONTROLLER MODE

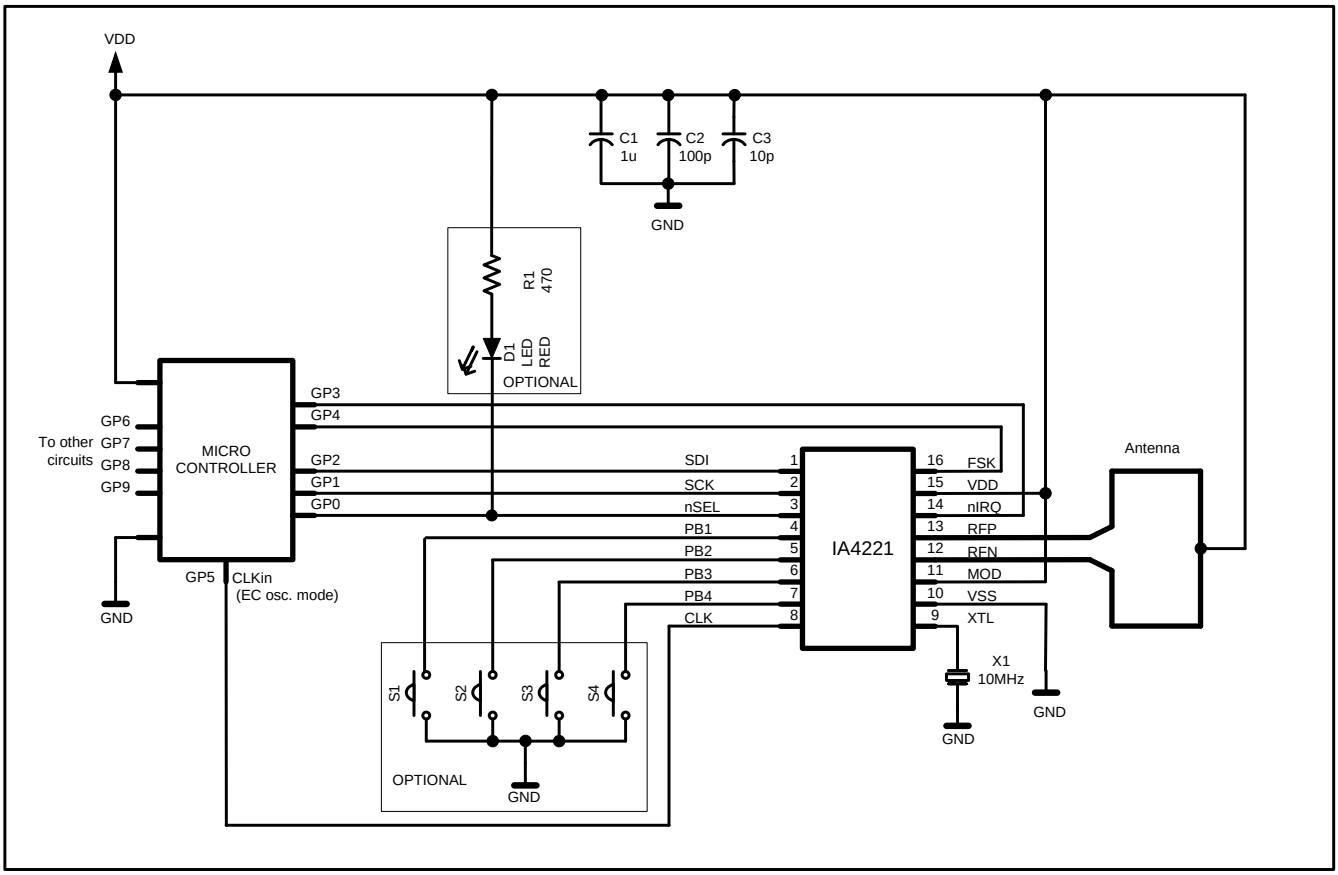
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output

Microcontroller Mode Pin Assignment



Pin	Name	Type	Function
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of serial control interface (active low)
4	PB1	DI	Push-button input #1 (active low with internal pull-up resistor)
5	PB2	DI	Push-button input #2 (active low with internal pull-up resistor)
6	PB3	DI	Push-button input #3 (active low with internal pull-up resistor)
7	PB4	DI	Push-button input #4 (active low with internal pull-up resistor)
8	CLK	DO	Microcontroller clock (1 MHz-10 MHz)
9	XTL	AIO	Crystal connection (other terminal of crystal to VSS)
10	VSS	S	Ground reference
11	MOD	DI	Connect to logic high (microcontroller mode)
12	RFN	AO	Power amplifier output (open collector)
13	RFP	AO	Power amplifier output (open collector)
14	nIRQ	DO	Interrupt request output for microcontroller (active low) and status read output
15	VDD	S	Positive supply voltage
16	FSK	DI	Serial data input for FSK modulation

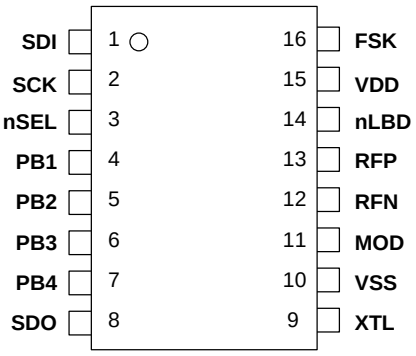
Typical Application, Microcontroller Mode



PACKAGE PIN DEFINITIONS, EEPROM MODE

Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output

EEPROM Mode Pin Assignment



Pin	Name	Type	Function
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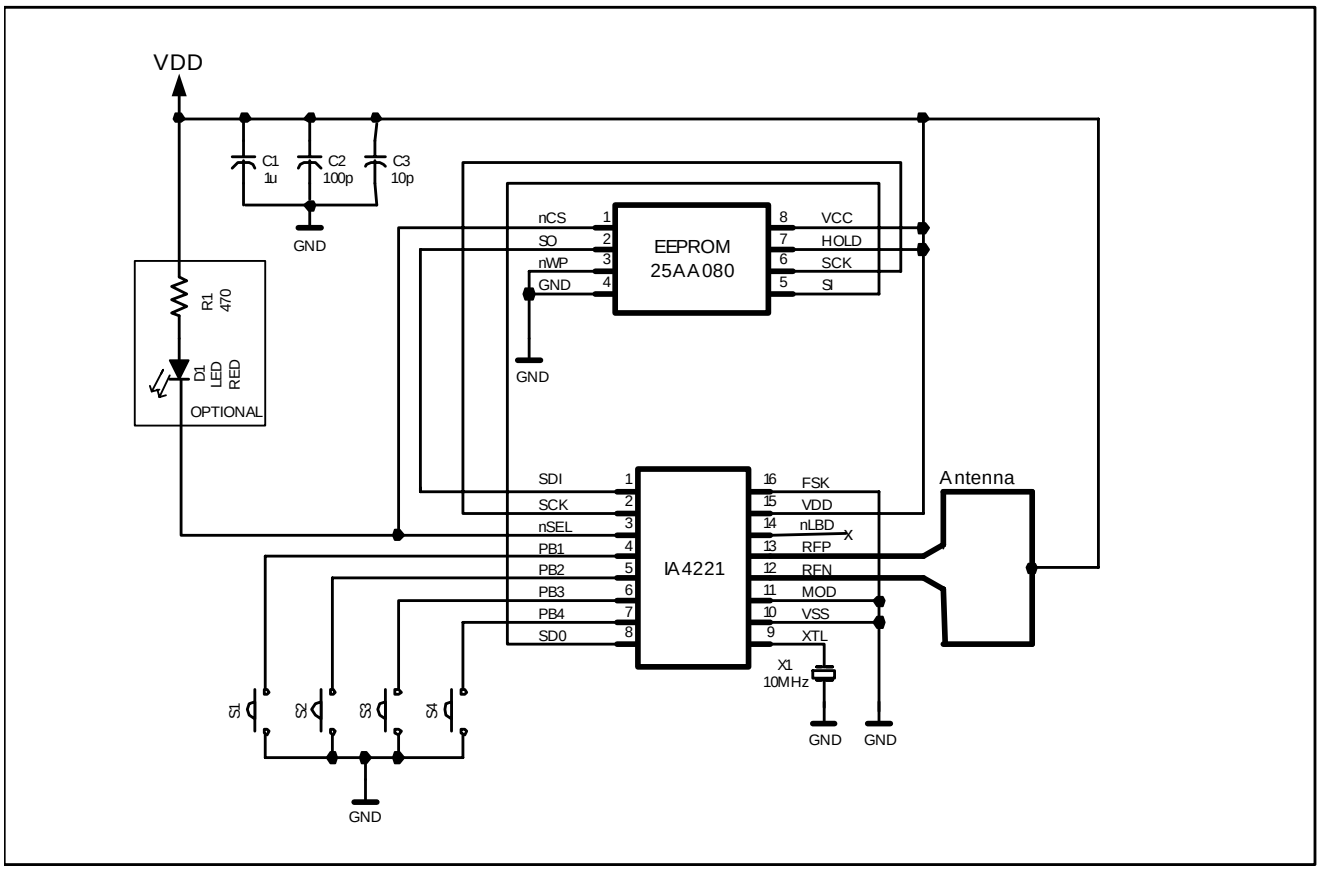
5	PB2	DI	Push-button input #2 (active low with internal pull-up resistor)
6	PB3	DI	Push-button input #3 (active low with internal pull-up resistor)
7	PB4	DI	Push-button input #4 (active low with internal pull-up resistor)
8	SDO	DO	Data output of serial control interface
9	XTL	AIO	Crystal connection (other terminal of crystal to VSS)
10	VSS	S	Ground reference
11	MOD	DI	Connect to logic low (EEPROM mode)
12	RFN	AO	Power amplifier output (open collector)
13	RFP	AO	Power amplifier output (open collector)
14	nLBD	DO	Low battery voltage detector output (active low)
15	VDD	S	Positive supply voltage
16	FSK	DI	Not used, connect to VDD or VSS

Typical Application, EEPROM Mode



GENERAL DEVICE SPECIFICATIONS

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin except open collector outputs	-0.5	V_{dd}+0.5	V
V_{oc}	Voltage on open collector outputs	-0.5	6.0	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	°C
T_{ld}	Lead temperature (soldering, max 10 s)		260	°C

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	5.4	V
V_{oc}	Voltage on open collector outputs (Max 6.0 V)	V_{dd} - 1	V_{dd} + 1	V
T_{op}	Ambient operating temperature	-40	85	°C

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typical conditions: T_{op} = 27 °C; V_{dd} = V_{oc} = 2.7 V)

DC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
$I_{dd\_TX\_0}$	Supply current (TX mode, Pout = 0 dBm)	433 MHz band		12		mA
		868 MHz band		14		
		915 MHz band		15		
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, Pout = P_{max})	433 MHz band		21		mA
		868 MHz band		23		
		915 MHz band		24		
I_{pd}	Standby current in sleep mode (Note 1)	All blocks disabled		0.3		µA
I_{wt}	Wake-up timer current consumption			1.5		µA
I_{lb}	Low battery detector current consumption			0.5		µA
I_x	Idle current	Only crystal oscillator is on		1.5		mA
V_{lba}	Low battery detection accuracy			+/-3		%
V_{lb}	Low battery detector threshold	Programmable in 0.1 V steps	2.25		5.35	V
V_{il}	Digital input low level				0.3*V_{dd}	V
V_{ih}	Digital input high level		0.7*V_{dd}			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	V_{ih} = V_{dd}, V_{dd} = 5.4 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

Note for table above is on page 7.

AC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	Crystal operation mode is parallel (Note 2)	8	10	12	MHz
f_o	Transmitter frequency	433 MHz band, 2.5 kHz resolution	430.24		439.75	
		868 MHz band, 5.0 kHz resolution	860.48		879.51	
		915 MHz band, 7.5 kHz resolution	900.72		929.27	
t_{lock}	PLL lock time	Frequency error < 10 kHz after 10 MHz step, POR default PLL setting (Note 7)		20		µs
t_{sp}	PLL startup time	After turning on from idle mode, with crystal oscillator already stable, POR default PLL setting (Note 7)			250	µs
I_{OUT}	Open collector output current (Note 3)	At all bands	0.5		6	mA
P_{maxL}	Available output power (433 MHz band)	With opt. antenna impedance (Note 4)		8		dBm
P_{maxH}	Available output power (868 and 915 MHz band)	With opt. antenna impedance (Note 4)		6		dBm
P_{out}	Typical output power	Selectable in 3 dB steps (Note 3)	P_{max}-21		P_{max}	dBm
P_{sp}	Spurious emission	At max power with loop antenna (Note 5)			-50	dBc
C_o	Output capacitance (set by the automatic antenna tuning circuit)	At low bands	1.5	2.3	3.1	pF
		At high bands	1.6	2.2	2.8	
Q_o	Quality factor of the output capacitance		16	18	22	
L_{out}	Output phase noise	100 kHz from carrier		-85		dBc/Hz
		1 MHz from carrier (Note 7)		-105		
BR_{FSK}	FSK bit rate	(Note 7)			115.2	kbps
BR_{OOK}	OOK bit rate				512	kbps
df_{fsk}	FSK frequency deviation	Programmable in 30 kHz steps	30		210	kHz
C_{xl}	Crystal load capacitance	Programmable in 0.5 pF steps, tolerance +/- 10%	8.5		16	pF
	See Crystal Selection Guidelines					
t_{POR}	Internal POR timeout (Note 6)	After V_{dd} has reached 90% of final value			150	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms (Note 8)		1.5	5	ms
t_{PBt}	Wake-up timer accuracy	Crystal oscillator must be enabled to ensure proper calibration at startup (Note 8)		+/-10		%
$t_{wake-up}$	Programmable wake-up time		1		$5 \cdot 10^{11}$	ms
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns

All notes for table above are on page 7.

Note 1: Using a CR2032 battery (225 mAh capacity), the expected battery life is greater than 2 years using a 60-second wake-up period for sending 100 byte packets in length at 19.2 kbps with +3 dBm output power in the 915 MHz band.

Note 2: Using anything but a 10 MHz crystal is allowed but not recommended because all crystal-referred timing and frequency parameters will change accordingly.

Note 3: Adjustable in 8 steps.

Note 4: Optimal antenna admittance/impedance for the Si4021:

	Yantenna [S]	Zantenna [Ohm]	Lantenna [nH]
434 MHz	1.3E-3 - j6.3E-3	31 + j152	58.00
868 MHz	1.35E-3 - j1.2E-2	9 + j82	15.20
915 MHz	1.45E-3 - j1.3E-2	8.7 + j77	13.60

Note 5: With selective resonant antennas (see: Application Notes available from http://www.silabs.com/integration).

Note 6: During this period, no commands are accepted by the chip. For detailed information see the *Reset modes* section.

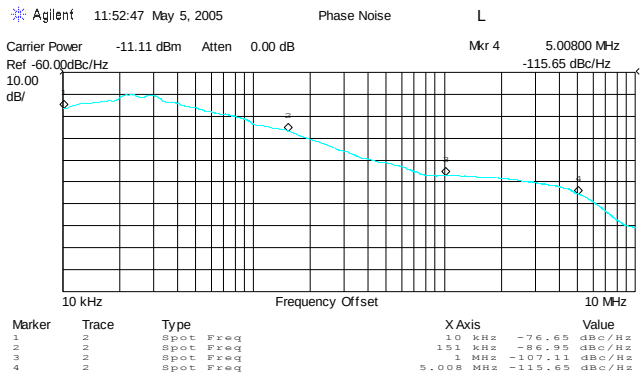
Note 7: The maximum FSK bitrate and the Output phase noise are dependent on the on the actual setting of the *PLL Setting Command*.

Note 8: The crystal oscillator start-up time strongly depends on the capacitance seen by the oscillator. Using low capacitance and low ESR crystal is recommended. When designing the PCB layout keep the trace connecting to the crystal short to minimize stray capacitance.

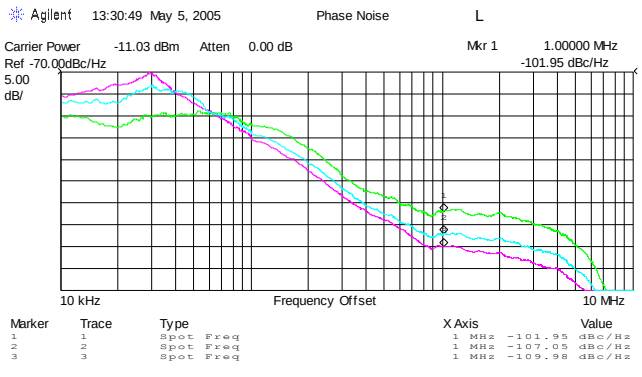
TYPICAL PERFORMANCE DATA

Phase noise measurements in the 868 MHz ISM band

50% Charge pump current setting (Ref. level: -60 dBc/Hz, 10 dB/div)



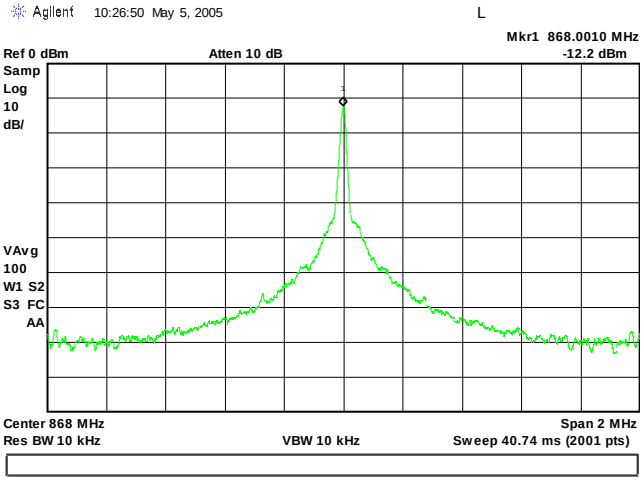
100, 50, 33% Charge pump current settings (Ref. level: -70 dBc/Hz, 5 dB/div)



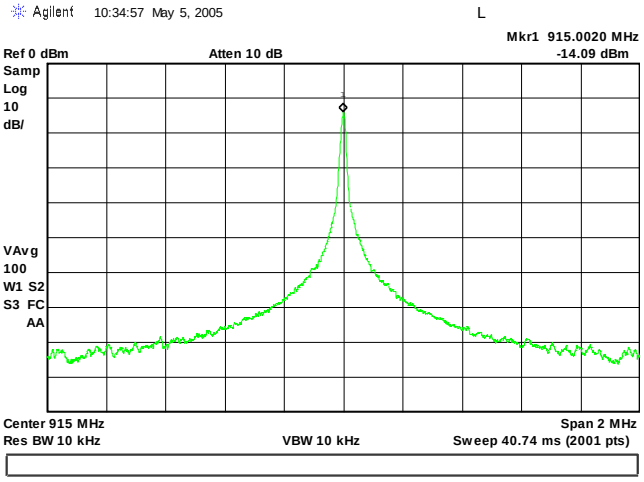
Unmodulated RF Spectrum

The output spectrum is measured at different frequencies. The output is loaded with 50 Ohms through a matching network.

At 868 MHz

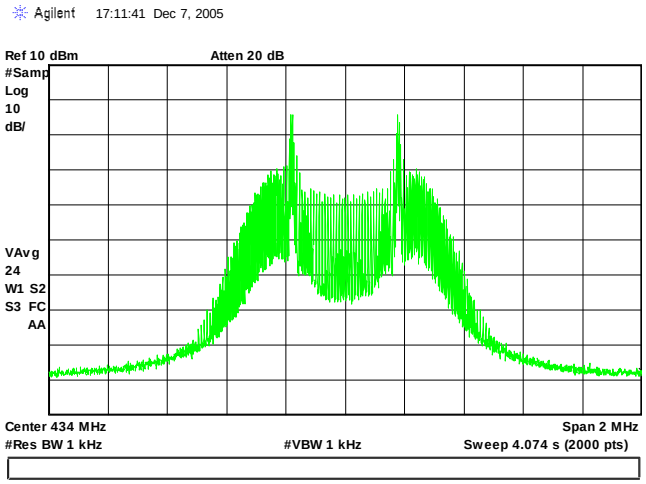


At 915 MHz

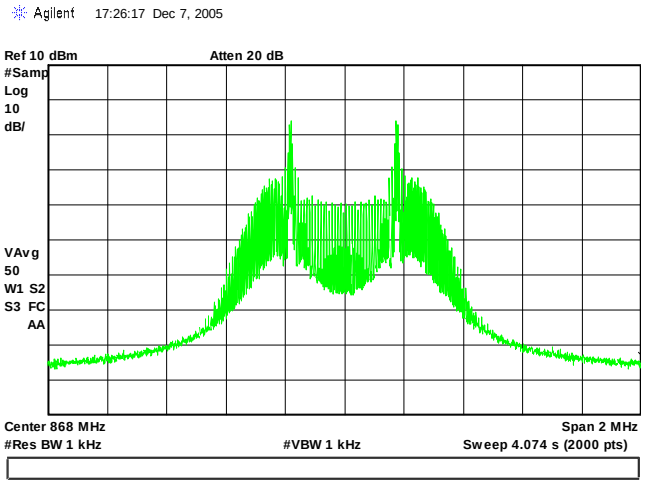


Modulated RF Spectrum

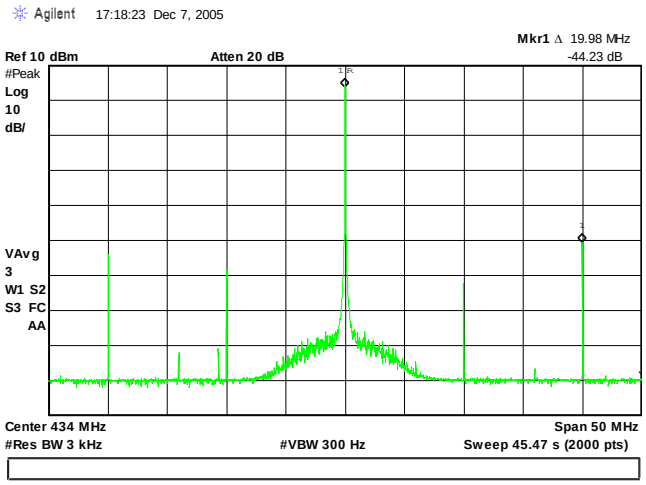
At 433 MHz with 180 kHz Deviation at 64 kbps



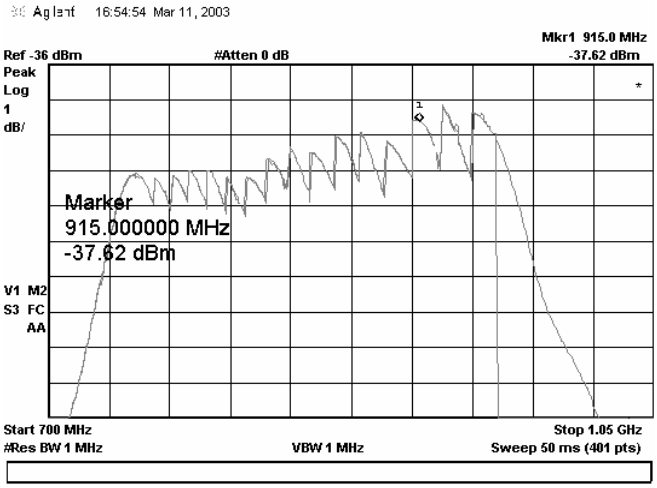
At 868 MHz with 180 kHz Deviation at 64 kbps



Spurious RF Spectrum With 10 MHz CLK Output Enabled at 433 MHz



Antenna Tuning Characteristics 750–970 MHz



The antenna tuning characteristics was recorded in “max-hold” state of the spectrum analyzer. During the measurement, the transmitters were forced to change frequencies by forcing an external reference signal to the XTL pin. While the carrier was changing the antenna tuning circuit switched trough all the available states of the tuning circuit. The graph clearly demonstrates that while the complete output circuit had about a 40 MHz bandwidth, the tuning allows operating in a 220 MHz band. In other words, the tuning circuit can compensate for 25% variation in the resonant frequency due to any process or manufacturing spread.

CONTROL INTERFACE

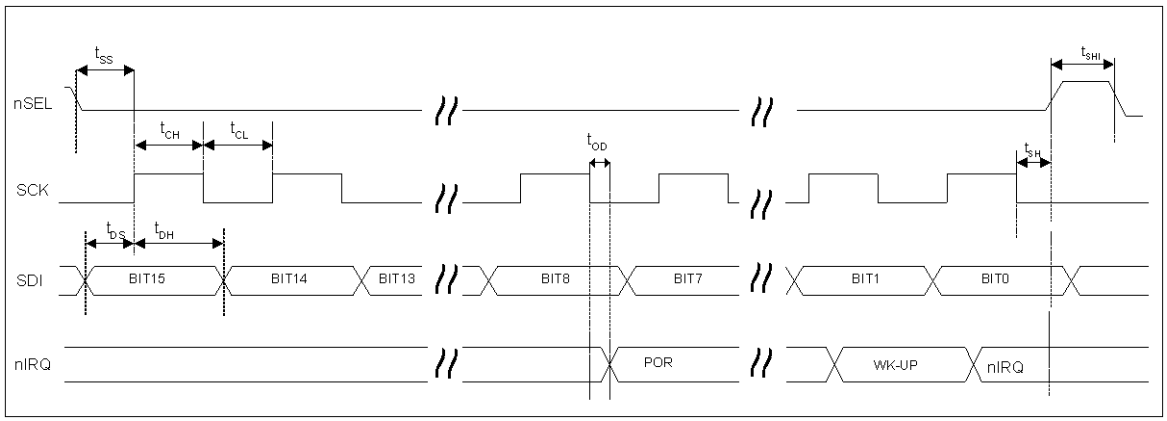
Commands to the transmitters are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control and command registers.

The status information or received data can be read serially over the IRQ pin. Bits are shifted out upon the falling edge of CLK signal

Timing Specification

Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10
t_{BL}	Push-button input low time	25

Timing Diagram



Control Commands

	Control Command	Related Parameters/Functions	Related control bits
1	Configuration Setting Command	Frequency band, microcontroller clock output, crystal load capacitance, frequency deviation	b1 to b0, d2 to d0, x3 to x0, ms, m2 to m0
2	Power Management Command	Crystal oscillator, synthesizer, power amplifier, low battery detector, wake-up timer, clock output buffer	a1 a0, ex, es, ea, eb, et, dc
3	Frequency Setting Command	Carrier frequency	f11 to f0
4	Data Rate Command	Bit rate	r7 to r0
5	Power Setting Command	Nominal output power, OOK mode	ook, p2 to p0
6	Low Battery Detector Command	Low battery threshold limit, transmit bit synchronizer, wake-up timer calibration	dwc, ebs, t4 to t0
7	Sleep Command	Length of the clock tail after power down	s7 to s0
8	Push-Button Command	Push-button related functions	p4, d1 to d0, b4 to b1, bc
9	Wake-Up Timer Command	Wake-up time period	r4 to r0, m7 to m0
10	Data Transmit Command	Data transmission	
11	Status Register Command	Transmitter status read	
12	PLL Setting and Reset Mode Command	PLL bandwidth, reset mode	bw1 to bw0, dr

Note: In the following tables the POR column shows the default values of the command registers after power-on.

1. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	d2	d1	d0	x3	x2	x1	x0	ms	m2	m1	m0	8080h

b1	b0	Frequency Band {MHz]
0	0	315
0	1	433
1	0	868
1	1	915

d2	d1	d0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
…				
1	1	1	0	15.5
1	1	1	1	16.0

The resulting output frequency can be calculated as:

$f_{out} = f_0 - (-1)^{SIGN} * (M + 1) * (30\ kHz)$

where:

f_0 is the channel center frequency (see the next command)
M is the three bit binary number <*m2 : m0*>
SIGN = (*ms*) XOR (FSK input)

Note:

- Use M in a range from 0 to 6.

2. Power Management Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	a1	a0	ex	es	ea	eb	et	dc	C000h

Bits 5-0, enable the corresponding block of the transmitters, i.e. the crystal oscillator is enabled by the *ex* bit, the synthesizer by *es*, the power amplifier by *ea* and the low battery detector by *eb*, while the wake-up timer by *et*. The bit *dc* disables the clock output buffer.

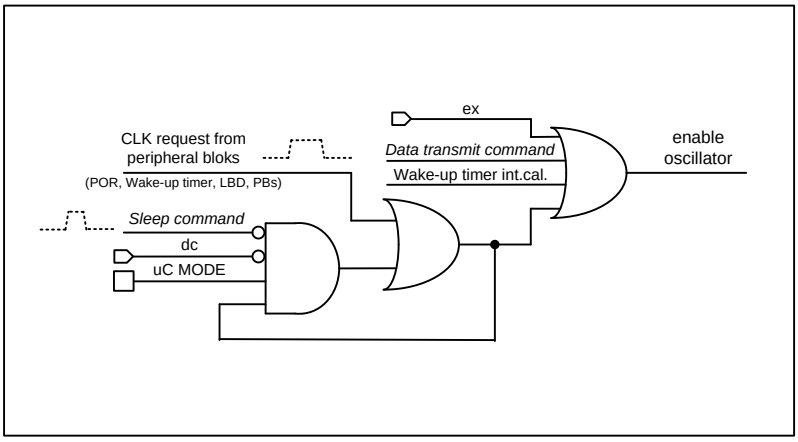
When receiving the *Data Transmit Command*, the chip supports automatic on/off control over the crystal oscillator, the PLL and the PA.

If bit *a1* is set, the crystal oscillator and the synthesizer are controlled automatically. *Data Transmit Command* starts up the crystal oscillator and as soon as a stable reference frequency is available the synthesizer starts. After a subsequent delay to allow locking of the PLL, if *a0* is set the power amplifier is turned on as well.

Note:

- To enable the automatic internal control of the crystal oscillator, the synthesizer and the power amplifier, the corresponding bits (*ex, es, ea*) must be zero in the *Power Management Command*.
- In microcontroller mode, the *ex* bit should be set in the *Power Management Command* for the correct control of *es* and *ea*. The oscillator can be switched off by clearing the *ex* bit after the transmission.
- In EEPROM operation mode after an identified *Data Transmit Command* the internal logic switches on the synthesizer and PA. At the end of *Data Transmit Command* header if necessary the current clock cycle is automatically extended to ensure the PLL stabilization and RF power ramp-up.
- In EEPROM operation mode the internal logic switches off the PA when the given number of bytes is transmitted. (See: *Data Transmit Command* in EEPROM operation.)
- When the chip is controlled by a microcontroller, the *Sleep Command* can be used to indicate the end of the data transmission process, because in microcontroller mode the *Data Transmit Command* does not contain the length of the TX data.
- For processing the events caused by the peripheral blocks (POR, LBD, wake-up timer, push-buttons) the chip requires operation of the crystal oscillator. This operation is fully controlled internally, independently from the status of the *ex* bit, but if the dc bit is zero, the oscillator remains active until *Sleep Command* is issued. (This command can be considered as an event controller reset.)

Oscillator control logic



3. Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A7D0h

The 12-bit parameter of the *Frequency Setting Command <f11 : f0>* has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as:

$$f_0 = 10\ \text{MHz} * C1 * (C2 + F/4000)$$

The constants C1 and C2 are determined by the selected band as:

Band [MHz]	C1	C2
433	1	43
868	2	43
915	3	30

Note:

- For correct operation of the frequency synthesizer, the frequency and band of operation need to be programmed **before** the synthesizer is started. Directly after activation of the synthesizer, the RF VCO is calibrated to ensure proper operation in the programmed frequency band.

4. Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	r7	r6	r5	r4	r3	r2	r1	r0	C800h

In EEPROM mode the transmitted bit rate is determined by the 8-bit value R (bits *<r7 : r0>*) as:

$$BR = 10\ \text{MHz} / 29 / (R+1)$$

Apart from setting custom values, the standard bit rates from 2.4 to 115.2 kbps can be approximated with minimal error. The commands are read out with a different fixed bit rate:

$$F_{sck} = 10\ \text{MHz} / 29 / 3\ \ [\sim 115.2\ \text{kHz}]$$

Note:

- PLL bandwidth should be set according the data rate. Please see the *PLL Setting Command*.

5. Power Setting Command

bit	7	6	5	4	3	2	1	0	POR
	1	0	1	1	ook	p2	p1	p0	B0h

The bit *ook* enables the OOK mode for the PA, in this case the data to be transmitted are received through the FSK pin.

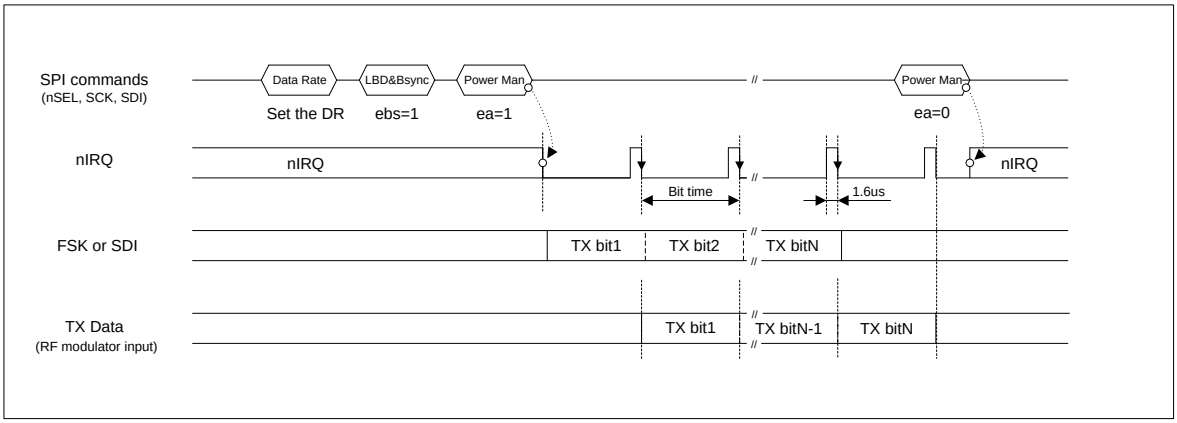
p2	p1	p0	Relative Output Power [dB]
0	0	0	0
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-18
1	1	1	-21

The output power is given in the table as relative to the maximum available power, which depends on the actual antenna impedance. (See: Antenna Application Note available from **www.silabs.com/integration**).

6. Low Battery Detector Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	dwc	0	ebs	t4	t3	t2	t1	t0	C200h

Bit 7 <*dwc*> Disables the Wake-up timer periodical (every 30 second) calibration if this bit is set.
Bit 5 <*ebs*> Enables the TX bit synchronization circuit. The data rate must be set by the Data Rate Command.



The 5-bit value T of <*t4 : t0*> determines the threshold voltage V_{lb} of the detector:

$$V_{lb} = 2.25\ V + T * 0.1\ V$$

7. Sleep Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0	C410h

The effect of this command depends on the *Power Management Command*. It immediately disables the power amplifier (if *a0*=1 and *ea*=0) and the synthesizer (if *a1*=1 and *es*=0). Stops the crystal oscillator after S periods of the microcontroller clock (if *a1*=1 and *ex*=0) to enable the microcontroller to execute all necessary commands before entering sleep mode itself. The 8-bit value S is determined by bits <*s7 : s0*>.

8. Push-Button Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	1	0	p4	d1	d0	b4	b3	b2	b1	bc	CA00h

If the corresponding bit was set (*b1-b4*) the event remains active while the button is pressed. In EEPROM mode, the chip is continuously performing the routine assigned to the push-button while it is pressed. In microcontroller mode, the chip continuously generates interrupts on nIRQ until the push-button is released. Weak pull-up currents are switched off when *bc* is high.

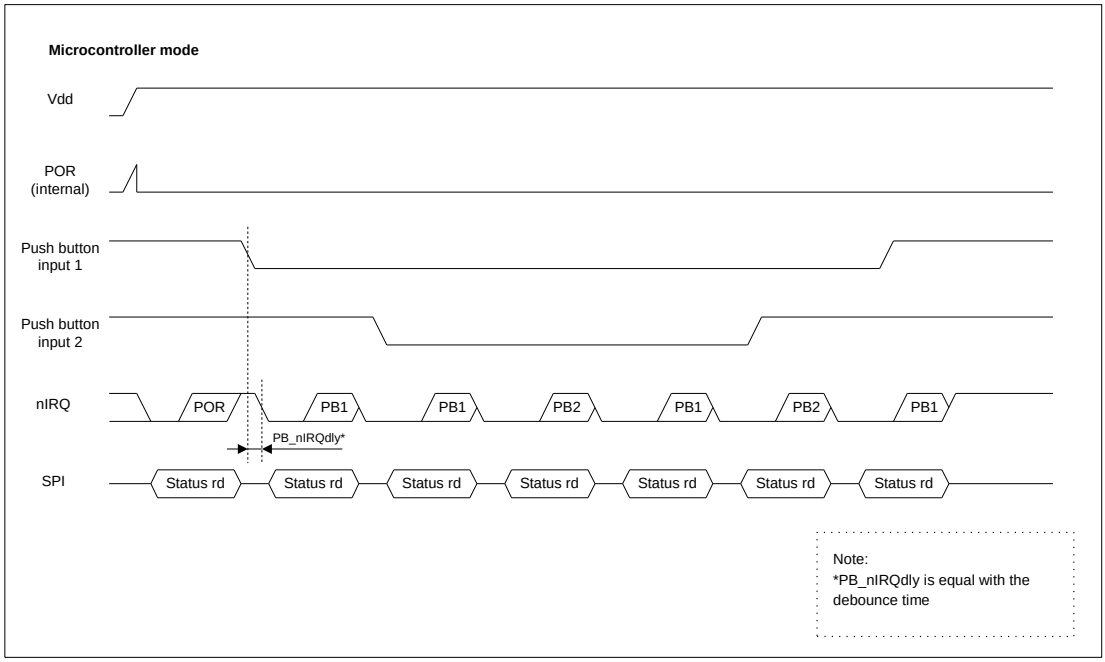
The *d0, d1* bits set the de-bouncing time period:

d1	d0	De-bouncing Time [ms]
0	0	160
0	1	40
1	0	10
1	1	0 (Bypassed)

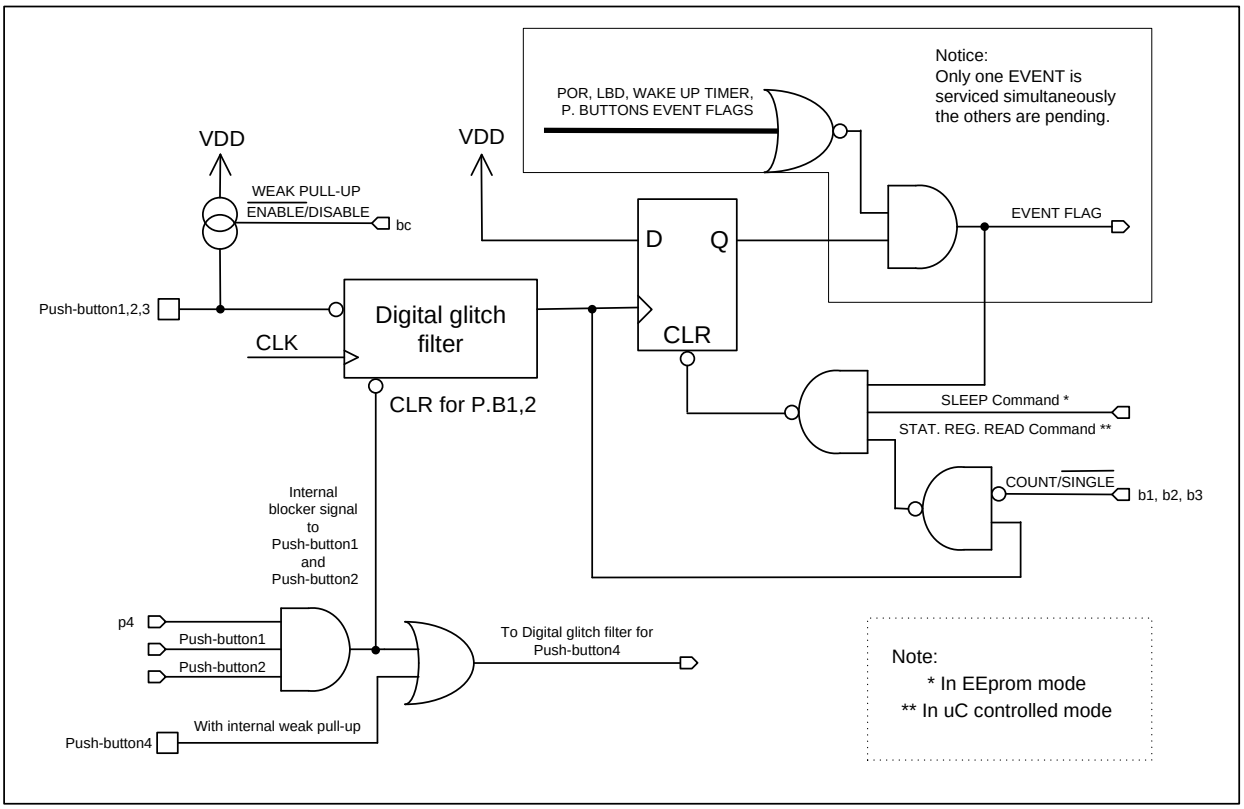
Note:

- Until the de-bouncing time has expired, the crystal oscillator remains switched on, independent of the status of the *ex* bit in the *Power Management Command*. (Because the circuit uses the crystal oscillator signal for timing.)
- If the *p4* bit is set, the controller performs the routine assigned to the fourth button when PB1 and PB2 are pressed down simultaneously. With the addition of this feature, there is a way to build a device that uses 3 buttons, but performs 4 functions.
- It is possible to detect multiple pressed push-buttons, in both modes. In EEPROM mode the controller executes sequentially all the routines belonging to the pressed buttons.

Simultaneously Pressed Push-Button Detect by Microcontroller



Simplified Block Diagram of Push-Button 1–4 Inputs



9. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E000h

The wake-up time period can be calculated as:

$$T_{wake\text{-}up} = M * 2^R \text{ [ms]} ,$$

where M is defined by the <*m7 : m0*> digital value and R is defined by the <*r4 : r0*> digital value.

The value of R should be in the range of 0 and 23. The maximum achievable wake-up time period can be up to 24 days.

Note:

- For continual operation the *et* bit should be cleared and set at the end of every cycle.

Software reset: Sending FE00h command to the chip triggers software reset. For more details see the *Reset modes* section.

10. Data Transmit Command

In EEPROM operation mode:

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	n7	n6	n5	n4	n3	n2	n1	n0	- -

In microcontroller slave mode:

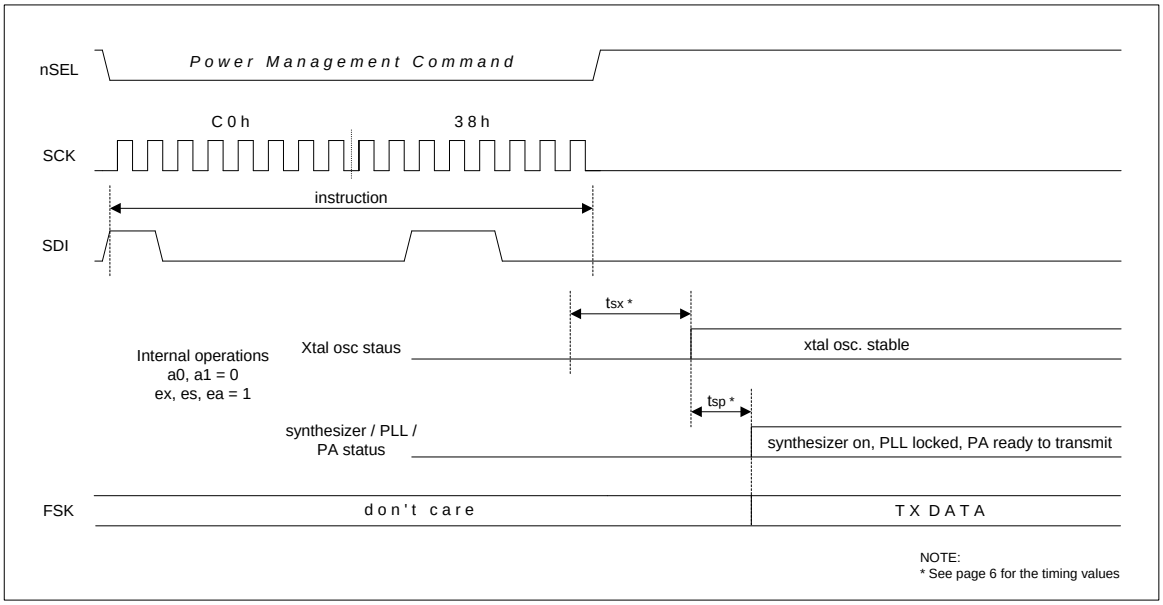
bit	7	6	5	4	3	2	1	0
	1	1	0	0	0	1	1	0

This command indicates that the following bitstream coming in via the serial interface is to be transmitted. In EEPROM mode, the 8-bit value N of bits <*n7 : n0*> contains the number of data bytes to follow.

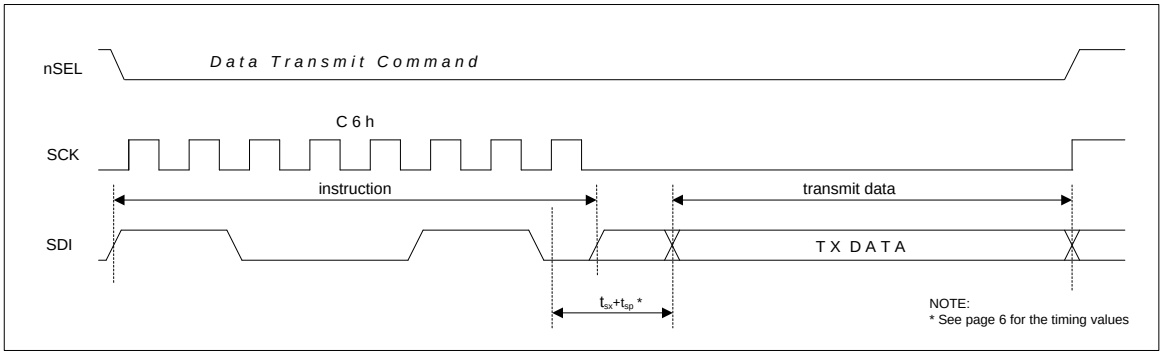
Note:

- This command is not needed if the transmitters' power management bits (*ex, es, ea*) are fully controlled by the microcontroller and TX data comes through the FSK pin.
- If the crystal oscillator was formerly switched off (*ex*=0), the internal oscillator needs t_{sx} time, to switch on. The actual value depends on the type of quartz crystal used.
- If the synthesizer was formerly switched off (*es*=0), the internal PLL needs t_{sp} startup time. Valid data can be transmitted only when the internal locking process is finished.
- In EEPROM mode, before issuing the *Data Transmit Command*, the power amplifier must be enabled, with the *ea* or *a0* bit in the *Power Management Command*.
- In EEPROM mode, when N bytes have been read and transmitted the controller continues reading the EEPROM and processing the data as control commands. This process stops after *Sleep Command* has been read from the EEPROM.

Data Transmit Sequence Through the FSK Pin



Data Transmit Sequence Through the SDI Pin



Note:

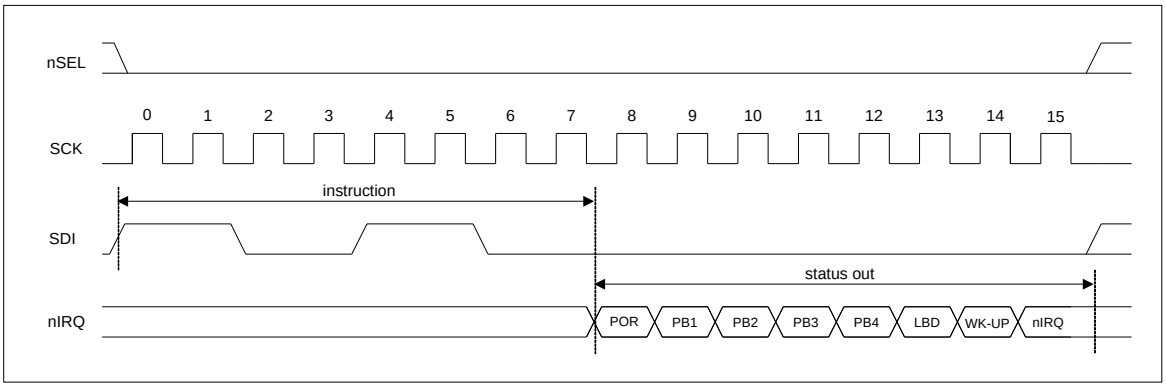
- Do not send CLK pulses with the TX data bits, otherwise they will be interpreted as commands.
- This mode is not SPI compatible, therefore it is not recommended in microcontroller mode.
- If the crystal oscillator and the PLL are running, the t_{sx}+t_{sp} delay is not needed.

11. Status Register Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	- -

With this command, it is possible to read the chip's status register through the nIRQ pin. This command clears the last serviced interrupt and processing the next pending one will start (if there is any).

Status Register Read Sequence



12. PLL Setting and Reset Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	1	0	0	1	0	bw1	bw0	0	0	0	0	dr	0	D200h

Bits 7-6 <*bw1 : bw0*> select the PLL bandwidth:

bw1	bw0	Max datarate [kbps]	Phase Noise at 1MHz offset [dBc/Hz] (typical)	Charge pump current
0	1	19.2	-112	25%
1	1	38.4	-110	33%
0	0	68.9	-107	50%
1	0	115.2	-102	100%

Bit 1 (*dr*): Disables the highly sensitive RESET mode. If this bit is cleared, a 600 mV glitch in the power supply may cause a system reset. For more detailed description see the *Reset modes* section.

EEPROM MODE

In this mode, the transmitters can operate with a standard at least 1 kbyte serial EEPROM with an SPI interface, and no microcontroller is necessary. The following events cause wake-up of the device:

Event Number N	EEPROM entry point	Description
0	0000h	power-on
1	0080h	low level on input PB1
2	0100h	low level on input PB2
3	0180h	low level on input PB3
4	0200h	low level on input PB4
5	0280h	low supply voltage level
6	0300h	wake-up timer timeout

After any of these events, the crystal oscillator turns on and the device starts to read bytes from the EEPROM continuously (block read) starting from address N * 128 (decimal) and executes them as commands as described in the previous section.

Note: Zero bytes can be put in the EEPROM for timing purposes. Never put more than 31 consecutive zero bytes into the EEPROM's active region (between the actual entry point and the closing Sleep Command).

Example EEPROM Hexa Content

Power-On Reset:

00000000	C0	C4	CA	1E	C8	23	C4	00	00	00	00	00	00	00	00	00
00000010	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000020	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000030	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000070	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Short Explanation:

Data in Address, Command, and Parameter fields are hexadecimal values.

For the detailed description of the control command bits, see previous section.

Address	Command	Parameter	Related Control Command	Remarks
00–01	C0	C4	Power Management	Crystal– Synthesizer – Power Amplifier auto on/off mode enable
02–03	CA	1E	Push Button	Continuous execution for all push buttons
04–05	C8	23	Bit Rate	BR=10M/29/(35+1)~9600 bps
06-07	C4	00	Sleep	Power down

Push-button 1:

00000080	88	72	A6	10	C6	60	55	55	55	55	55	55	55	55	55	55
00000090	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
000000A0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
000000B0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
000000C0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
000000D0	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
000000E0	55	55	55	55	55	55	C4	00	00	00	00	00	00	00	00	00
000000F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Short Explanation:

Address	Command	Parameter	Related Control Command	Remarks
80–81	8	872	Configuration Control	433MHz band, Xtal C_L=12pF f_{dev}=90kHz
82–83	A	610	Frequency	f_c=(43+1552/4000)*10MHz
84–85	C6	60	Data Transmit	Transmit the next 96 bytes
86–E5		60x55		Data
E6–E7	C4	00	Sleep	Power down, go to address 80

Note: This routine is repeatedly executed while PB1 is pressed, because continuous execution was selected at POR (CA1E code issued in the power-on reset section before).

RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the Si4021 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 100 ohms ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup. It is recommended to keep the PCB parasitic capacitances on the XTL pin as low as possible.

The crystal frequency is used as the reference of the PLL, which generates the RF carrier frequency (f_c). Therefore f_c is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable carrier frequency error.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate:	**2.4 kbps**	Transmitter Deviation [+/- kHz]						
		30	**60**	**90**	**120**	**150**	**180**	**210**
	433 MHz	20	50	75	100	100	100	100
	868 MHz	10	25	40	60	75	100	100
	915 MHz	10	25	40	50	75	75	100

Bit Rate:	**9.6 kbps**	Transmitter Deviation [+/- kHz]						
		30	**60**	**90**	**120**	**150**	**180**	**210**
	433 MHz	15	50	75	100	100	100	100
	868 MHz	8	25	40	60	75	75	100
	915 MHz	8	25	40	50	70	75	100

Bit Rate:	**38.4 kbps**	Transmitter Deviation [+/- kHz]						
		30	**60**	**90**	**120**	**150**	**180**	**210**
	433 MHz	don't use	20	50	75	100	100	100
	868 MHz	don't use	10	30	40	60	75	100
	915 MHz	don't use	10	25	40	60	75	75

Bit Rate:	**115.2 kbps**	Transmitter Deviation [+/- kHz]						
		30	**60**	**90**	**120**	**150**	**180**	**210**
	433 MHz	don't use	don't use	don't use	don't use	30	50	100
	868 MHz	don't use	don't use	don't use	don't use	20	30	50
	915 MHz	don't use	don't use	don't use	don't use	15	30	50

Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C_0.

Note:

- There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.

RESET MODES

The chip will enter into reset mode if any of the following conditions are met:

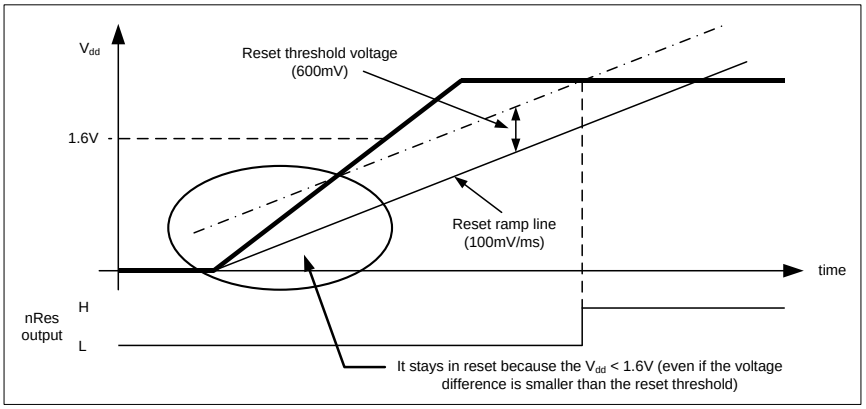
- Power-on reset: During a power up sequence until the V_{dd} has reached the correct level and stabilized
- Power glitch reset: Transients present on the V_{dd} line
- Software reset: Special control command received by the chip

Power-on reset

After power up the supply voltage starts to rise from 0V. The reset block has an internal ramping voltage reference (reset-ramp signal), which is rising at 100mV/ms (typical) rate. The chip remains in reset state while the voltage difference between the actual V_{dd} and the internal reset-ramp signal is higher than the reset threshold voltage, which is 600 mV (typical). As long as the V_{dd} voltage is less than 1.6V (typical) the chip stays in reset mode regardless the voltage difference between the V_{dd} and the internal ramp signal.

The reset event can last up to 150ms supposing that the V_{dd} reaches 90% its final value within 1ms. During this period the chip does not accept control commands via the serial control interface.

Power-on reset example:



Power glitch reset

The internal reset block has two basic mode of operation: normal and sensitive reset. The default mode is sensitive, which can be changed by the appropriate control command (see *Related control commands* at the end of this section). In normal mode the power glitch detection circuit is disabled.

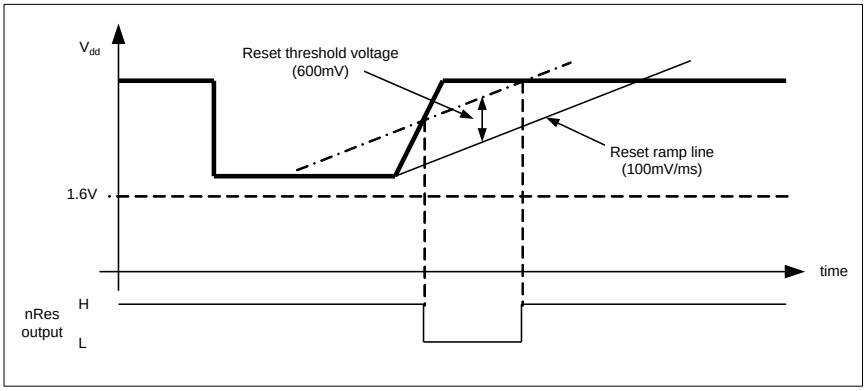
There can be spikes or glitches on the V_{dd} line if the supply filtering is not satisfactory or the internal resistance of the power supply is too high. In such cases if the sensitive reset is enabled an (unwanted) reset will be generated if the positive going edge of the V_{dd} has a rising rate greater than 100mV/ms and the voltage difference between the internal ramp signal and the V_{dd} reaches the reset threshold voltage (600 mV). Typical case when the battery is weak and due to its increased internal resistance a sudden decrease of the current consumption (for example turning off the power amplifier) might lead to an increase in supply voltage. If for some reason the sensitive reset cannot be disabled step-by-step decrease of the current consumption (by turning off the different stages one by one) can help to avoid this problem.

Any negative change in the supply voltage will not cause reset event unless the V_{dd} level reaches the reset threshold voltage (250mV in normal mode, 1.6V in sensitive reset mode).

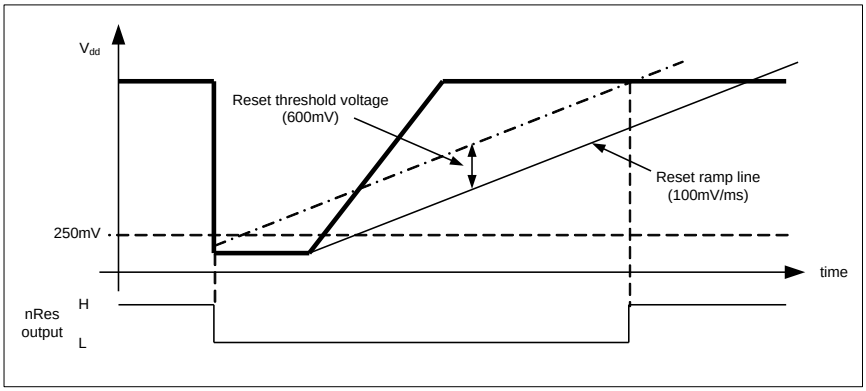
If the sensitive mode is disabled and the power supply turned off the V_{dd} must drop below 250mV in order to trigger a power-on reset event when the supply voltage is turned back on. If the decoupling capacitors keep their charges for a long time it could happen that no reset will be generated upon power-up because the power glitch detector circuit is disabled.

Note that the reset event reinitializes the internal registers, so the sensitive mode will be enabled again.

Sensitive Reset Enabled, Ripple on V_{dd}:



Sensitive reset disabled:



Software reset

Software reset can be issued by sending the appropriate control command (described at the end of the section) to the chip. The result of the command is the same as if power-on reset was occurred.

V_{dd} line filtering

During the reset event (caused by power-on, fast positive spike on the supply line or software reset command) it is very important to keep the V_{dd} line as smooth as possible. Noise or periodic disturbing signal superimposed the supply voltage may prevent the part getting out from reset state. To avoid this phenomenon use adequate filtering on the power supply line to keep the level of the disturbing signal below $10mV_{p-p}$ in the DC – 50kHz range for 200ms from V_{dd} ramp start.. Typical example when a switch-mode regulator is used to supply the radio, switching noise may be present on the V_{dd} line. Follow the manufacturer's recommendations how to decrease the ripple of the regulator IC and/or how to shift the switching frequency.

Related control commands

"PLL setting and Reset Mode Command"

Setting bit<1> to high will change the reset mode to normal from the default sensitive.

"SW Reset Command"

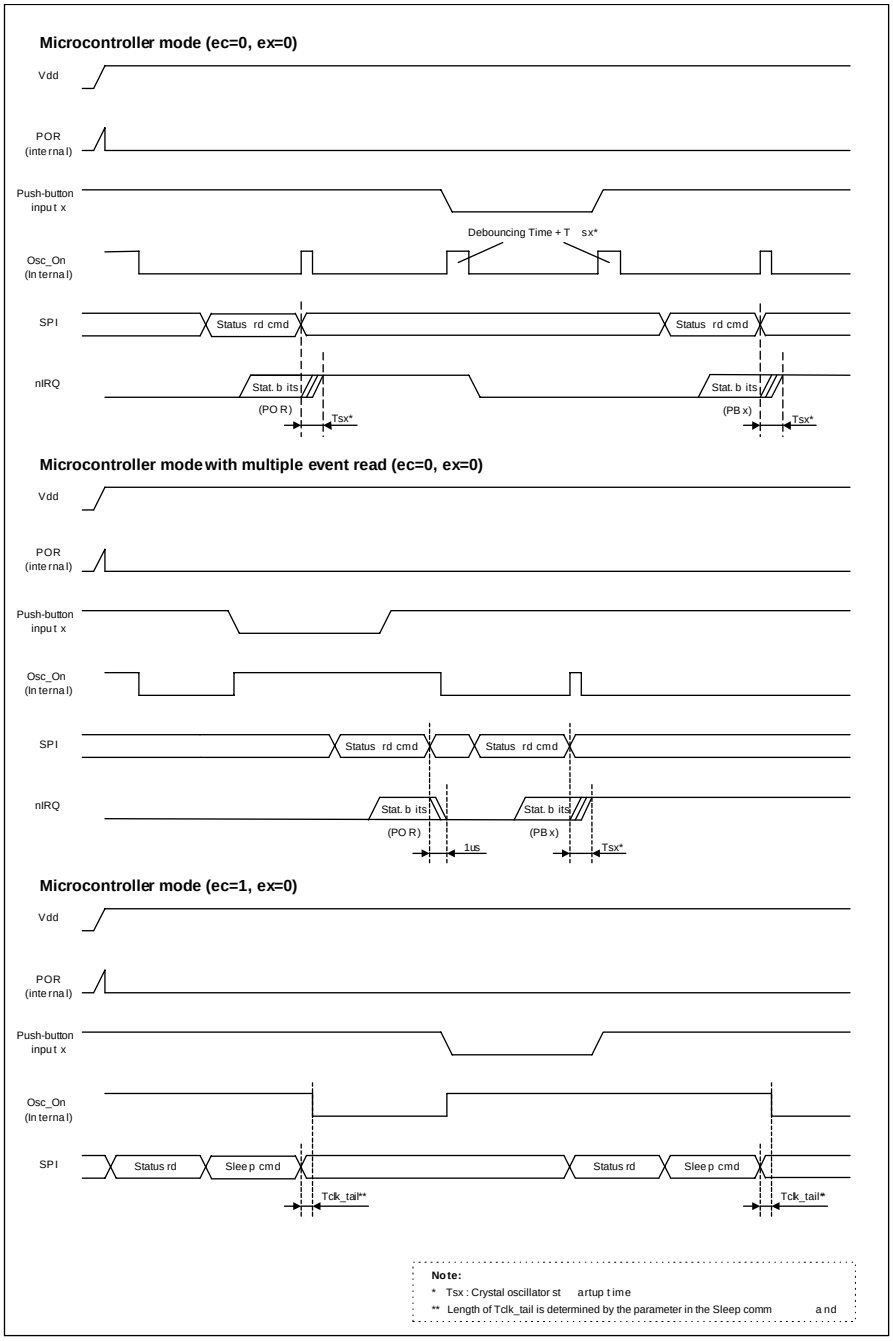
Issuing FE00h command will trigger software reset. See the *Wake-up Timer Command*.

SIMPLIFIED INTERNAL CONTROL AND TIMING

The internal controller uses the clock generated by the crystal oscillator to sequentially process the various events and to de-bounce the push-button (PB) inputs. If the oscillator is not running, internal logic automatically turns it on temporarily and then off again. Such events are: any wake-up event (POR, PB press, wake-up timer timeout and low supply voltage detection), PB release and status read request by the microcontroller.

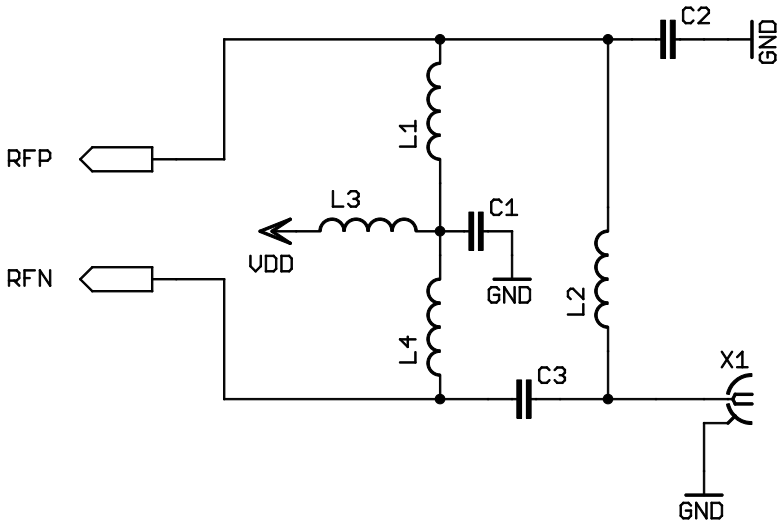
If two wake-up events occur in succession, the crystal oscillator stays on until the next status read (acknowledgment of the first event).

Simplified Internal Control and Timing Diagrams



MATCHING NETWORK FOR A 50 OHM SINGLE ENDED OUTPUT

Matching Network Schematic



Si4021	L1 [nH]	L2 [nH]	L3 [nH]	L4 [nH]	C1 [pF] (Note 1)	C1 [pF] (Note 2)	C2 [pF]	C3 [pF]	C4 [pF] (Note 3)
433 MHz	16	47	390	16	3.3	3.3	6.0	2.7	220
868 MHz	5.1	24	100	5.1	2	1.5	2.2	1.2	47
915 MHz	4.3	24	100	4.3	2	1.8	2.2	1.2	33

Note 1: 1 mm thick board

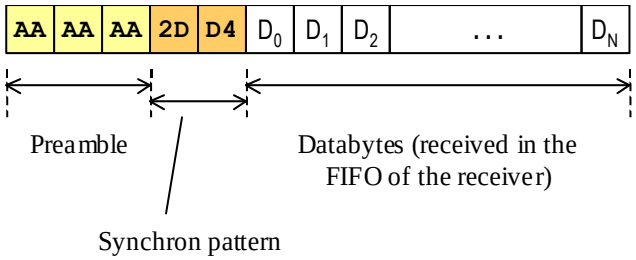
Note 2: 1.5 mm thick board

Note 3: C4 must be connected parallel to the supply decoupling capacitors (10nF + 2.2µF recommended) as close as possible to the VDD and VSS pins

EXAMPLE APPLICATIONS: DATA PACKET TRANSMISSION

Data packet structure

An example data packet structure using the IA422x – IA4320 pair for data transmission. This packet structure is an example of how to use the high efficiency FIFO mode at the receiver side:



The first 3 bytes compose a 24 bit length '01' pattern to let enough time for the clock recovery of the receiver to lock. The next two bytes compose a 16 bit synchron pattern which is essential for the receiver's FIFO to find the byte synchron in the received bit stream. The synchron patters is followed by the payload. The first byte transmitted after the synchron pattern (D_0 in the picture above) will be the first received byte in the FIFO.

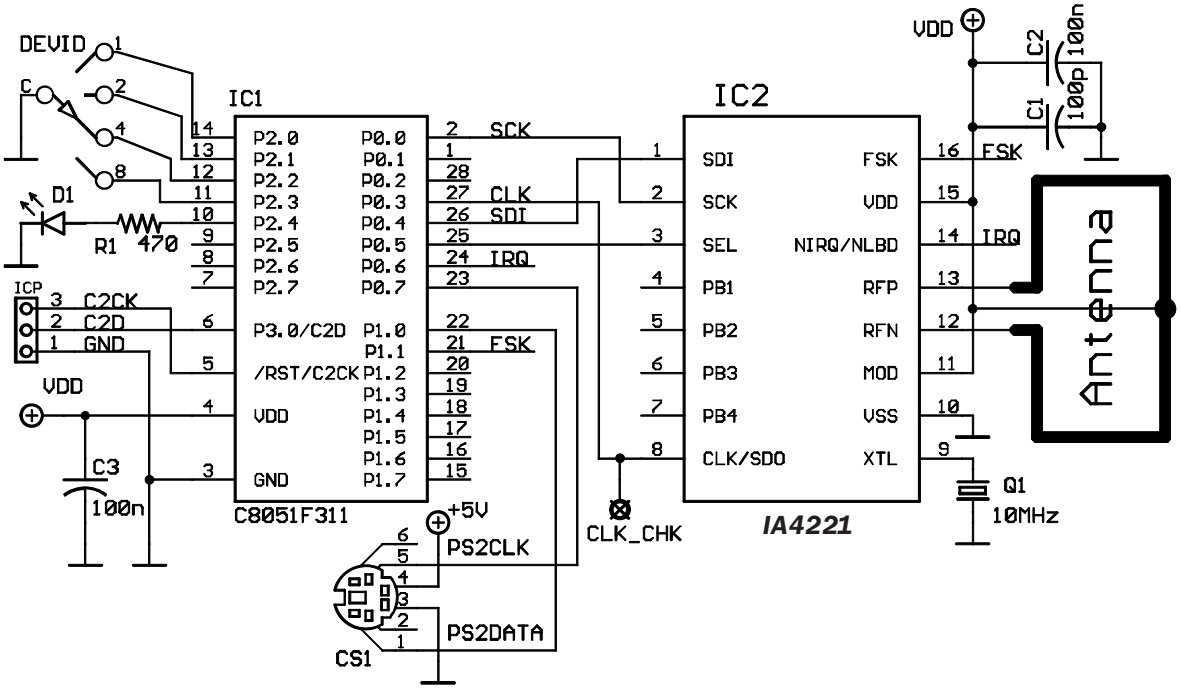
Important: The bytes of the data stream should follow each other continuously, otherwise the clock recovery circuit of the receiver side will be unable to track.

Further details of packet structures can be found in the IA ISM-UGSB1 software development kit manual.

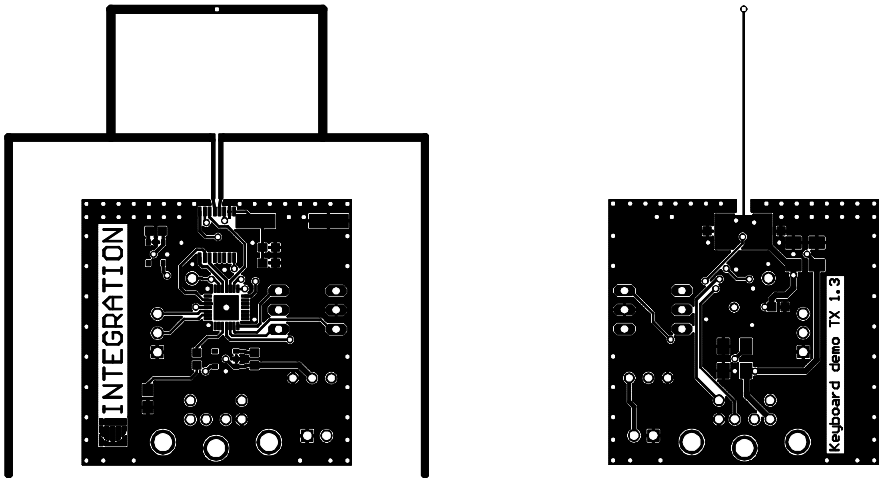
EXAMPLE APPLICATIONS

For Microcontroller Mode

Schematic



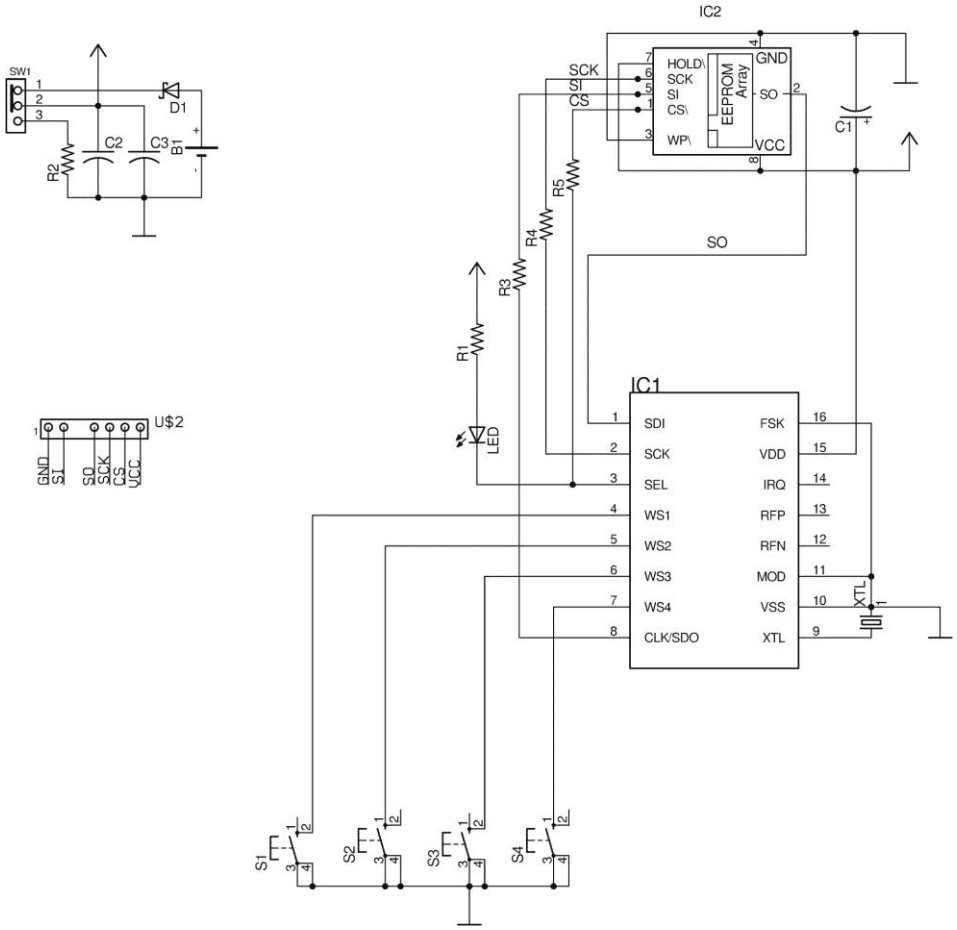
PCB Layout of Keyboard Transmitter Demo Circuit Using Microcontroller Mode (operating in the 915 MHz band)



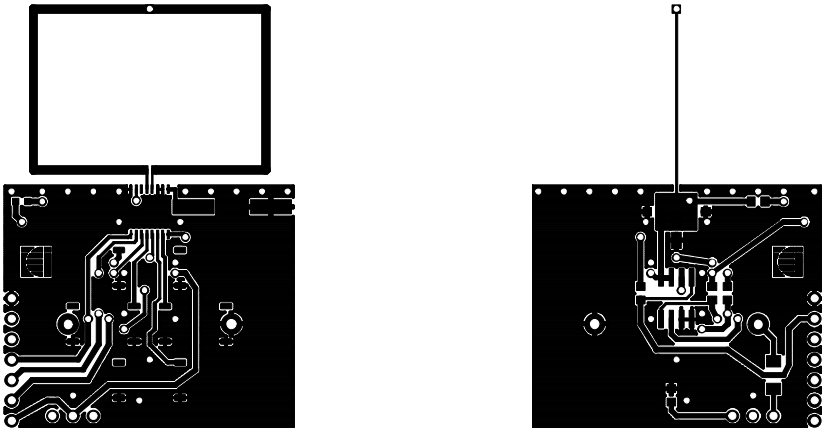
Top Layer *Bottom Layer*

For EEPROM Mode

Schematic



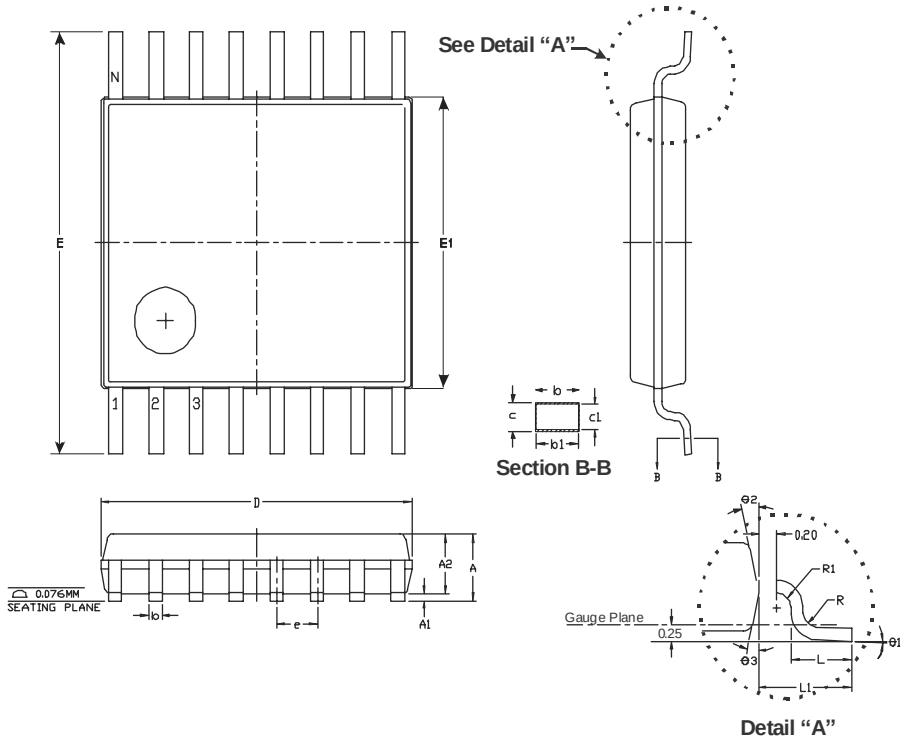
PCB Layout of Push-Button Transmitter Demo Circuit Using EEPROM Mode (operating in the 434 MHz band)



Top Layer *Bottom Layer*

PACKAGE INFORMATION

16-pin TSSOP



Symbol	Dimensions in mm			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			1,20			0,047
A1	0,05		0,15	0,002		0,006
A2	0,80	0,90	1,05	0,031	0,035	0,041
b	0,19		0,30	0,007		0,012
b1	0,19	0,22	0,25	0,007	0,009	0,010
c	0,09		0,20	0,004		0,008
c1	0,09		0,16	0,004		0,006
D	4,90	5,00	5,10	0,193	0,197	0,201
e	0.65 BSC.			0.026 BSC.		
E	6.40 BSC.			0.252 BSC.		
E1	4,30	4,40	4,50	0,169	0,173	0,177
L	0,50	0,60	0,75	0,020	0,024	0,030
L1	1.00 REF.			0.39 REF.		
R	0,09			0,004		
R1	0,09			0,004		
θ1	0		8	0		8
θ2	12 REF.			12 REF.		
θ3	12 REF.			12 REF.		

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RELATED PRODUCTS AND DOCUMENTS

Si4021 Universal ISM Band FSK Transmitter

DESCRIPTION	ORDERING NUMBER	
Si4021 16-pin TSSOP	Si4021-IC CC16	Rev A1
die	see Silicon Labs	

Demo Boards and Development Kits

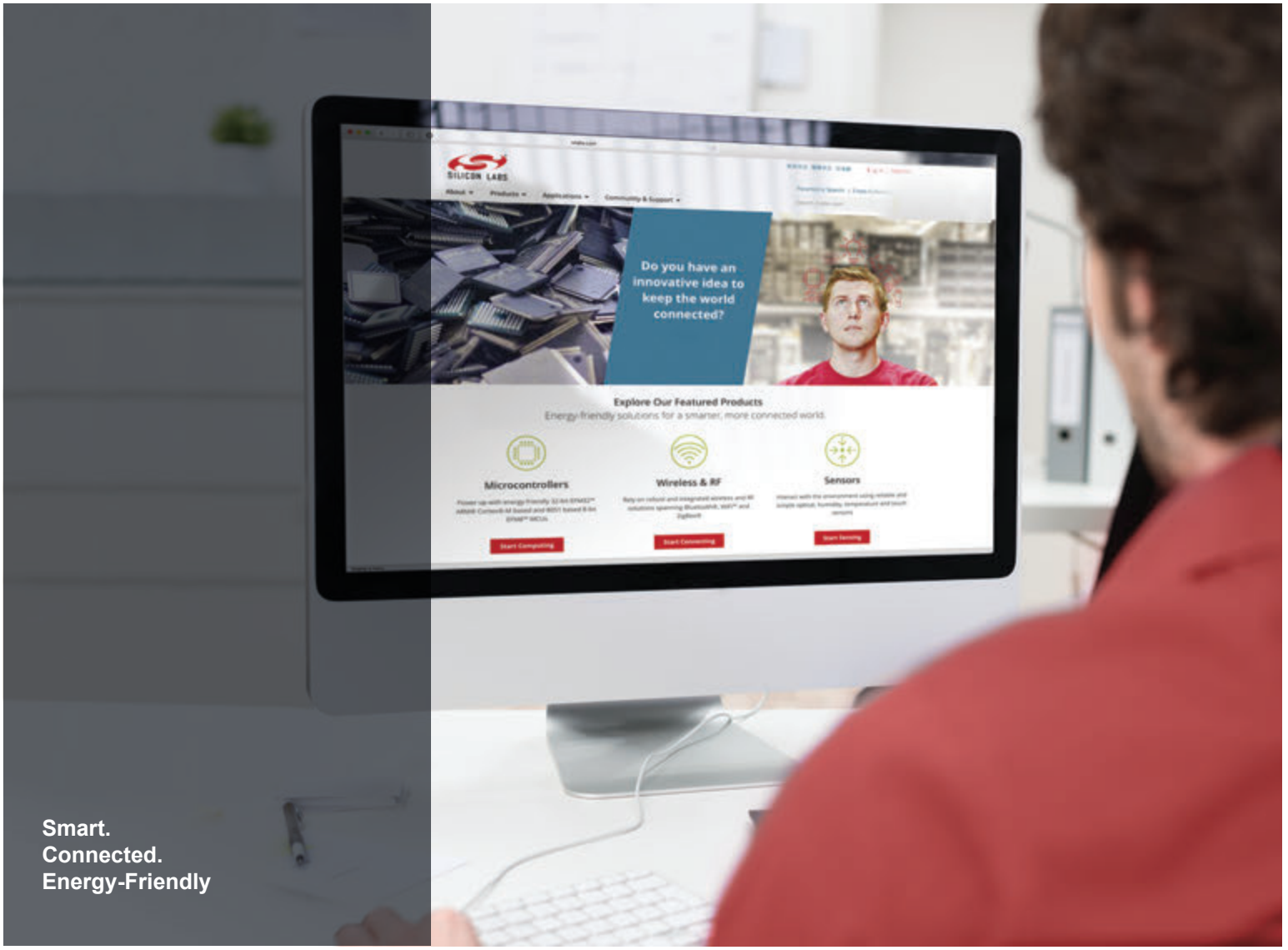
DESCRIPTION	ORDERING NUMBER
Development Kit	IA ISM – DK
Remote Temp. Monitoring Station	IA ISM – DATD

Related Resources

DESCRIPTION	ORDERING NUMBER
Antenna Selection Guide	IA ISM – AN1
Antenna Development Guide	IA ISM – AN2
IA4320 Universal ISM Band FSK Receiver	See www.silabs.com/integration for details

Note: Volume orders must include chip revision to be accepted.

Silicon Labs, Inc.
400 West Cesar Chavez
Austin, Texas 78701
Tel: 512.416.8500
Fax: 512.416.9669
Toll Free: 877.444.3032
www.silabs.com/integration
wireless@silabs.com



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