THE DATASHEET OF

SL3S1204FUD/BG/S1Z

SL3S1204

UCODE 7

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241340

Product data sheet
COMPANY PUBLIC

1 General description

NXP's UCODE 7 IC is the leading-edge EPC Gen2 RFID chip that offers best-in-class performance and features for use in the most demanding RFID tagging applications.

Particularly well suited for inventory management application, like e.g Retail and Fashion, with its leading edge RF performance for any given form factor, UCODE 7 enables long read distance and fast inventory of dense RFID tag population. With its broadband design, it offers the possibility to manufacture true global RFID label with best-in-class performance over worldwide regulations.

The device also provides a pre-serialized 96-bit EPC and a Parallel encoding feature. For applications where the same 58-bit Stock Keeping Unit (SKU) needs to be encoded on multiple tags, at the same time, a combination of both features improves and simplifies the tag initialization process.

On top UCODE 7 offers a Tag Power Indicator for RFID tag initialization optimization and a Product Status Flag for Electronic Article Surveillance (EAS) application.

2 Features and benefits

2.1 Key features

- Read sensitivity -21 dBm
- Write sensitivity -16 dBm
- Parallel encoding mode: 100 items in 60ms
- Encoding speed: 16 bits per millisecond
- Innovative functionalities
  - Tag Power Indicator
  - Pre-serialization for 96-bit EPC
  - Integrated Product Status Flag (PSF)
- Compatible with single-slit antenna
- Up to 128-bit EPC
- 96-bit Unique Tag Identifier (TID) factory locked, including 48-bit unique serial number
- EPC Gen2 v2.0 ready

2.1.1 Memory

- Up to 128-bit of EPC memory
- Supports pre-serialization for 96-bit EPC
- 96-bit Tag IDentifier (TID) factory locked
- 48-bit unique serial number factory-encoded into TID
- No User Memory
- 32-bit kill password to permanently disable the tag
- 32-bit access password
- Wide operating temperature range: -40 °C up to +85 °C
- Minimum 100.000 write cycle endurance

2.2 Key benefits

2.2.1 End user benefit

- Long READ and WRITE ranges due to leading edge chip sensitivity
- Very fast bulk encoding
- Product identification through unalterable extended TID range, including a 48-bit serial number
- Reliable operation in dense reader and noisy environments through high interference rejection

2.2.2 Antenna design benefits

- High sensitivity enables smaller and cost efficient antenna designs for the same retail category
- Tag Power Indicator features enables very high density of inlay on rolls without cross-talk issues during writing/encoding

- The different input capacitance for the single slit antenna solution provides an additional possibility in tuning of the impedance for the antenna design

2.2.3 Label manufacturer benefit

- Large RF pad-to-pad distance to ease antenna design
- Symmetric RF inputs are less sensitive to process variation
- Single slit antenna for a more mechanically stable antenna connection
- Pre-serialization of the 96-bit EPC
- Extremely fast encoding of the EPC content

2.3 Supported features

- All mandatory commands of EPC global specification V.1.2.0 are implemented including:
  - (Perma)LOCK
  - Kill Command
- The following optional commands are implemented in conformance with the EPC specification:
  - Access
  - BlockWrite (2 words, 32-bit)
- Product Status Flag bit: enables the UHF RFID tag to be used as EAS (Electronic Article Surveillance) tag without the need for a back-end data base.
- Tag Power Indicator: enables the reader to select only ICs/tags that have enough power to be written to.
- Parallel encoding: allows for the ability to bring (multiple) tag(s) quickly to the OPEN state and hence allowing single tags to be identified simply, without timing restrictions, or multiple tags to be e.g. written to at the same time, considerably reducing the encoding process

All supported features of UCODE 7 can be activated using standard EPCglobal READ / WRITE / ACCESS / SELECT commands. No custom commands are needed to take advantage of all the features in case of unlocked EPC memory. The parallel encoding feature may however require a firmware upgrade of the reader to use its full potential.

3 Applications

3.1 Markets

- Retail/Fashion (apparel, footwear, jewelry, cosmetics)
- Fast Moving Consumer Goods

3.2 Applications

- Retail Inventory management
- Supply chain management
- Loss prevention
- Asset management

Outside the applications mentioned above, please contact NXP Semiconductors for support.

4 Ordering information

Table 1. Ordering information

Type number	Package			
	Name	IC type	Description	Version
SL3S1204FUD/BG1	Wafer	UCODE 7	bumped die on sawn 8" 120 µm wafer 7 µm Polyimide spacer	not applicable
SL3S1204FUD/HA1	Wafer	UCODE 7	die with large pads 3 µm Au, 10 µm Polyimide spacer on sawn 8" 120 µm wafer	not applicable
SL3S1204FUD2/BG1	Wafer	UCODE 7	bumped die on sawn 12" 120 µm wafer 7 µm Polyimide spacer	not applicable
SL3S1204FTB0/1	XSON6	UCODE 7	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886F1

5 Marking

Table 2. Marking codes

Type number	Marking code	Comment	Version
SL3S1204FTB0/1	YM	UCODE 7	SOT886

6 Block diagram

The SL3S1204 IC consists of three major blocks:

- Analog Interface
- Digital Control
- EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader which is then processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital section includes the state machines, processes the protocol and handles communication with the EEPROM, which contains the EPC and the user data.

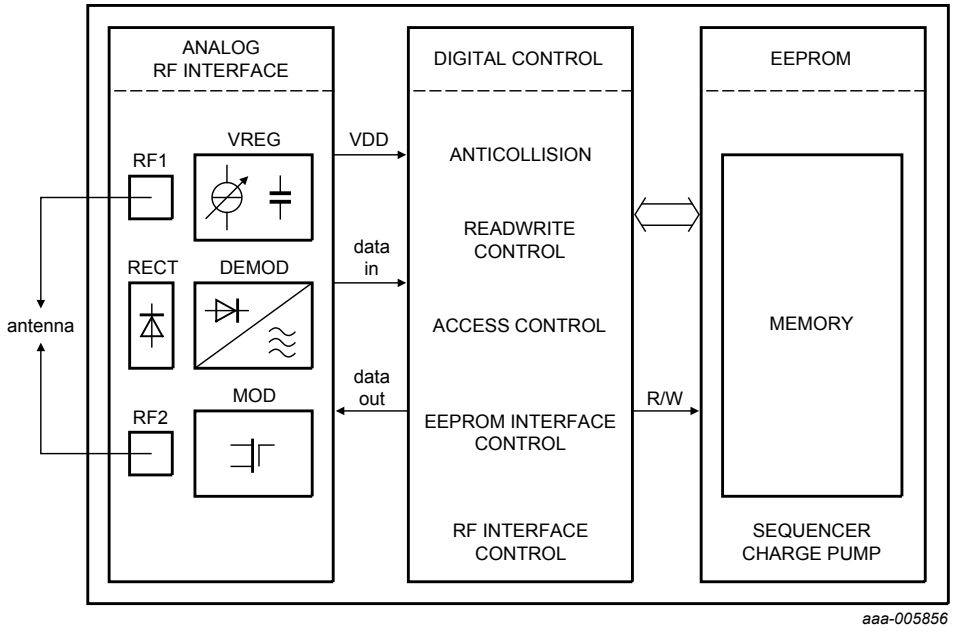


Figure 1. Block diagram of UCODE 7 IC

7 Pinning information

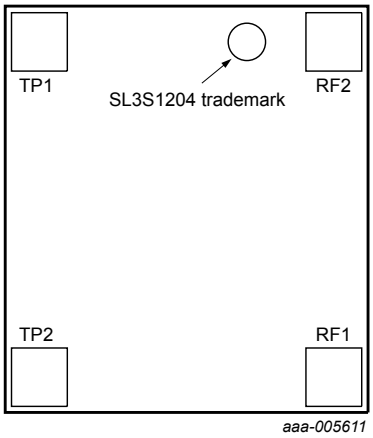


Figure 2. Pinning bare die

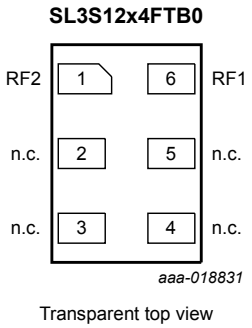


Figure 3. Pin configuration for SOT886

7.1 Pin description

Table 3. Pin description bare die

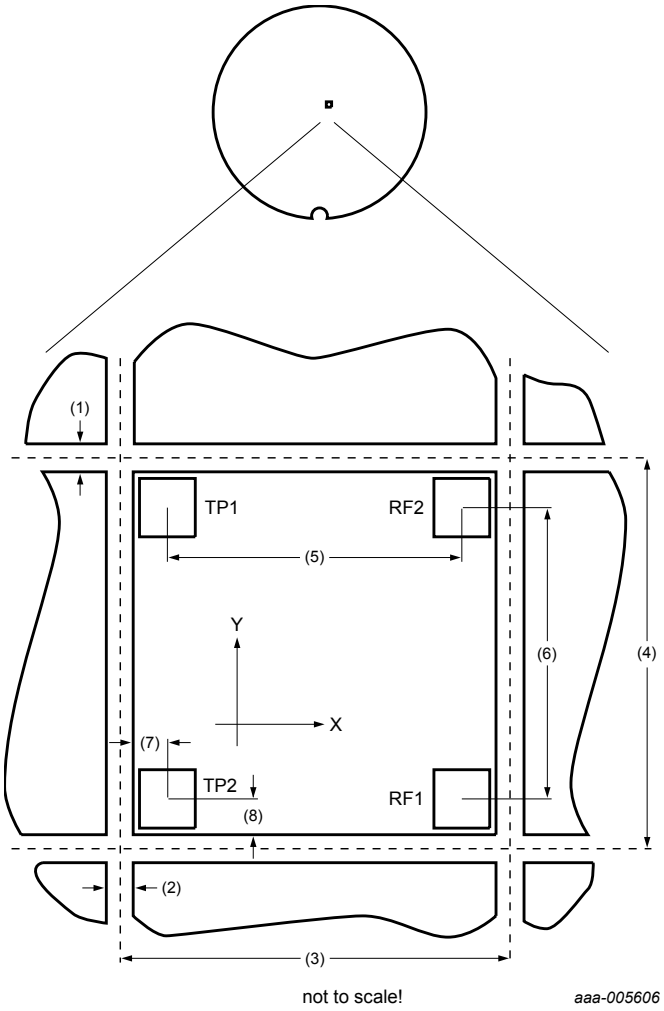
Symbol	Description
TP1	test pad 1
RF1	antenna connector 1
TP2	test pad 2
RF2	antenna connector 2

Table 4. Pin description SOT886

Pin	Symbol	Description
1	RF2	antenna connector
2	n.c.	not connected
3	n.c.	not connected
4	n.c.	not connected
5	n.c.	not connected
6	RF1	antenna connector

8 Wafer layout

8.1 Wafer layout 8 inch



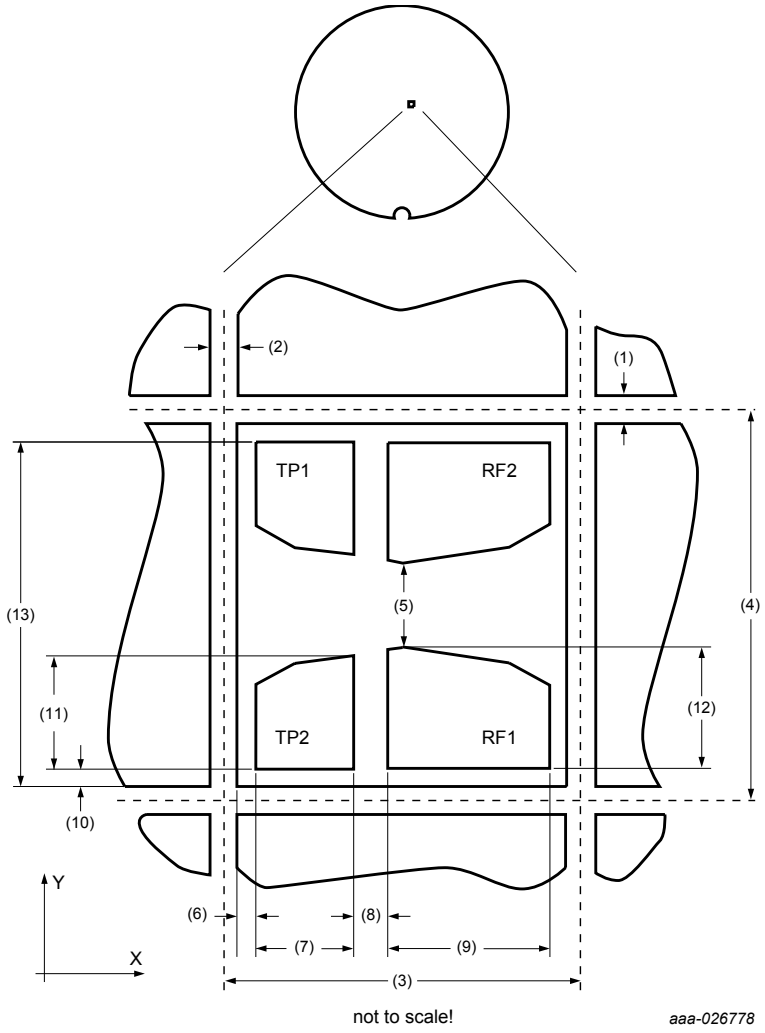
1. Die to Die distance (metal sealring - metal sealring) 21,4 µm, (X-scribe line width: 15 µm)
2. Die to Die distance (metal sealring - metal sealring) 21,4 µm, (Y-scribe line width: 15 µm)
3. Chip step, x-length: 460 µm
4. Chip step, y-length: 505 µm
5. Bump to bump distance X (TP1 - RF2): 358 µm
6. Bump to bump distance Y (RF1 - RF2): 403 µm
7. Distance bump to metal sealring X: 40,3 µm (outer edge - top metal)
8. Distance bump to metal sealring Y: 40,3 µm

Bump size X x Y: 60 µm x 60 µm

Remark: TP1 and TP2 are electrically disconnected after dicing

Figure 4. UCODE 7 8 inch wafer layout

8.2 Wafer layout 8 inch with large pads

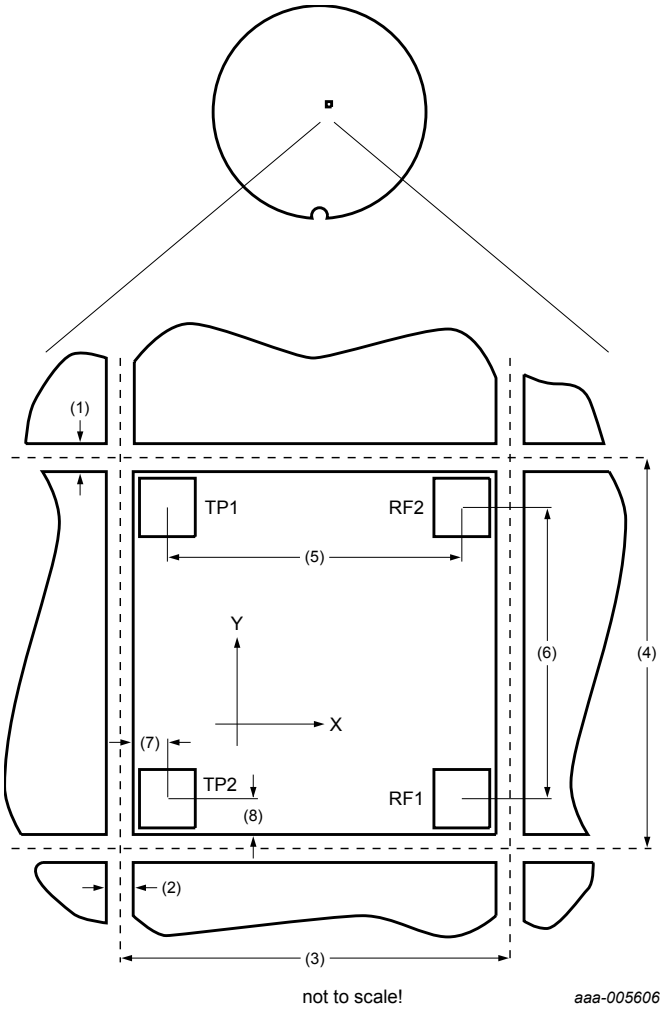


1. Die to Die distance (metal sealring - metal sealring) 21,4 µm, (Y-scribe line width: 15 µm)
2. Die to Die distance (metal sealring - metal sealring) 21,4 µm, (X-scribe line width: 15 µm)
3. Chip step, x-length: 460 µm
4. Chip step, y-length: 505 µm
5. Bump to bump distance Y (RF1 - RF2): 115 µm
6. Distance bump to metal sealring X: 23,5 µm
7. Bump size (TP1, TP2) X: 130 µm
8. Bump to bump distance X (RF1 - TP2): 50 µm
9. Bump size (RF1, RF2) X: 218 µm
10. Distance bump to metal sealring Y: 23,5 µm
11. Bump size (TP1, TP2) Y: 153,1 µm
12. Bump size (RF1, RF2) Y: 164 µm
13. Distance bump to metal sealring Y: 466,5 µm

Remark: TP1 and TP2 are electrically disconnected after dicing

Figure 5. UCODE 7 8 inch wafer layout with large pads

8.3 Wafer layout 12 inch



1. Die to Die distance (metal sealring - metal sealring) 39 µm, (X-scribe line width: 35 µm)
2. Die to Die distance (metal sealring - metal sealring) 39 µm, (Y-scribe line width: 35 µm)
3. Chip step, x-length: 480 µm
4. Chip step, y-length: 525µm
5. Bump to bump distance X (TP1 - RF2): 358 µm
6. Bump to bump distance Y (RF1 - RF2): 403 µm
7. Distance bump to metal sealring X: 40,3 µm (outer edge - top metal)
8. Distance bump to metal sealring Y: 40,3 µm

Bump size X x Y: 60 µm x 60 µm

Remark: TP1 and TP2 are electrically disconnected after dicing

Figure 6. UCODE 7 12 inch wafer layout

9 Mechanical specification

The UCODE 7 wafers are available in 120 µm thickness. The 120 µm thick wafer is enhanced with 7µm /10µm Polyimide spacer resulting in less coupling between the antenna and the active circuit, leaving more room for process control (like pressure).

9.1 Wafer specification

9.1.1 8 inch Wafer, Standard bumps

See [2].

Table 5. Specifications

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	200 mm (8") unsawn - 205 mm typical sawn on foil
Thickness	
SL3S1204FUD/BG	120 µm ± 15 µm
Number of pads	4
Pad location	non diagonal / placed in chip corners
Distance pad to pad RF1-RF2	403.0 µm
Distance pad to pad TP1-RF2	358.0 µm
Process	CMOS 0.14 µm
Batch size	25 wafers
Potential good dies per wafer	126.524
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 µm, R_t max. 5 µm
Chip dimensions	
Die size excluding scribe	0.490 mm × 0.445 mm = 0.218 mm^2
Scribe line width:	x-dimension = 15 µm
	y-dimension = 15 µm
Passivation on front	
Type	Sandwich structure
Material	PE-Nitride (on top)
Thickness	1.75 µm total thickness of passivation
Polyimide spacer	7 µm ± 1 µm
Au bump	

Bump material	> 99.9 % pure Au
Bump hardness	35 – 80 HV 0.005
Bump shear strength	> 70 MPa
Bump height	
SL3S1204FUD/BG	25 µm[1]
Bump height uniformity	
within a die	± 2 µm
– within a wafer	± 3 µm
– wafer to wafer	± 4 µm
Bump flatness	± 1.5 µm
Bump size	
– RF1, RF2	60 × 60 µm
– TP1, TP2	60 × 60 µm
Bump size variation	± 5 µm

[1] Because of the 7 µm spacer, the bump will measure 18 µm relative height protruding the spacer.

9.1.2 8 inch Wafer, Large pads

See [2].

Table 6. Specifications

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	200 mm (8") unsawn - 205 mm typical sawn on foil
Thickness	
SL3S1204FUD/HA	120 µm ± 15 µm
Number of pads	4
Pad location	non diagonal / placed in chip corners
Process	CMOS 0.14 µm
Batch size	25 wafers
Potential good dies per wafer	126.524
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 µm, R_t max. 5 µm
Chip dimensions	
Die size excluding scribe	0.490 mm × 0.445 mm = 0.218 mm^2
Scribe line width:	x-dimension = 15 µm

	y-dimension = 15 µm
Passivation on front	
Type	Sandwich structure
Material	PE-Nitride (on top)
Thickness	1.75 µm total thickness of passivation
Polyimide spacer	10 µm ± 2 µm
Au Pad	
Pad material	> 99.9 % pure Au
Pad hardness	35 – 80 HV 0.005
Pad shear strength	> 70 MPa
Pad height	
SL3S1204FUD/HA	3 µm
Pad height uniformity	
within a die	max. 2 µm
– within a wafer	max. 4 µm
Pad flatness	max. 3 µm
Pad size	
– RF1, RF2 (max. details see wafer layout)	218 × 164 µm
– TP1, TP2 (max. details see wafer layout)	130 × 153.1 µm
Pad size variation	± 5 µm

9.1.3 12 inch Wafer

See [4]

Table 7. Specifications

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	300 mm (12") unsawn and sawn on foil
Thickness	
SL3S1204FUD2	120 µm ± 15 µm
Number of pads	4
Pad location	non diagonal / placed in chip corners
Distance pad to pad RF1-RF2	403.0 µm
Distance pad to pad TP1-RF2	358.0 µm
Process	CMOS 0.14 µm
Batch size	25 wafers
Potential good dies per wafer	264.696
Wafer backside	

Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 µm, R_t max. 5 µm
Chip dimensions	
Die size excluding scribe	0.490 mm × 0.445 mm = 0.218 mm^2
Scribe line width:	x-dimension = 35 µm
	y-dimension = 35 µm
Passivation on front	
Type	Sandwich structure
Material	PE-Nitride (on top)
Thickness	1.75 µm total thickness of passivation
Polyimide spacer	7 µm ± 1 µm
Au bump	
Bump material	> 99.9 % pure Au
Bump hardness	35 – 80 HV 0.005
Bump shear strength	> 70 MPa
Bump height	
SL3S1204FUD2	25 µm[1]
Bump height uniformity	
within a die	± 2 µm
– within a wafer	± 3 µm
– wafer to wafer	± 4 µm
Bump flatness	± 1.5 µm
Bump size	
– RF1, RF2	60 × 60 µm
– TP1, TP2	60 × 60 µm
Bump size variation	± 5 µm

[1] Because of the 7 µm spacer, the bump will measure 18 µm relative height protruding the spacer.

9.1.4 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See [2]

See [4]

9.1.5 Map file distribution

See [2]

See [4]

10 Functional description

10.1 Air interface standards

The UCODE 7 fully supports all parts of the "Specification for RFID Air Interface EPCglobal, EPC Radio-Frequency Identity Protocols, Class-1 Generation-2 UHF RFID, Protocol for Communications at 860 MHz to 960 MHz, Version 1.2.0".

10.2 Power transfer

The interrogator provides an RF field that powers the tag, equipped with a UCODE 7. The antenna transforms the impedance of free space to the chip input impedance in order to get the maximum possible power for the UCODE 7 on the tag.

The RF field, which is oscillating on the operating frequency provided by the interrogator, is rectified to provide a smoothed DC voltage to the analog and digital modules of the IC.

The antenna that is attached to the chip may use a DC connection between the two antenna pads. Therefore the UCODE 7 also enables loop antenna design.

10.3 Data transfer

10.3.1 Interrogator to tag Link

An interrogator transmits information to the UCODE 7 by modulating an UHF RF signal. The UCODE 7 receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the interrogator's RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least one inventory round. It communicates to the UCODE 7 by modulating an RF carrier.

For further details refer to [1]. Interrogator-to-tag (R=>T) communications.

10.3.2 Tag to interrogator Link

Upon transmitting a valid command an interrogator receives information from a UCODE 7 tag by transmitting an unmodulated RF carrier and listening for a backscattered reply. The UCODE 7 backscatters by switching the reflection coefficient of its antenna between two states in accordance with the data being sent. For further details refer to [1], chapter 6.3.1.3.

The UCODE 7 communicates information by backscatter-modulating the amplitude and/or phase of the RF carrier. Interrogators shall be capable of demodulating either demodulation type.

The encoding format, selected in response to interrogator commands, is either FM0 baseband or Miller-modulated subcarrier.

10.4 Supported commands

The UCODE 7 supports all **mandatory** EPCglobal V1.2.0 commands including

- Kill command

- (perma) LOCK command

In addition the UCODE7 supports the following **optional** commands:

- ACCESS
- Block Write (32 bit)

10.5 UCODE 7 memory

The UCODE 7 memory is implemented according EPCglobal

Class1Gen2 and organized in three banks:

Table 8. UCODE 7 memory sections

Name	Size	Bank
Reserved memory (32 bit ACCESS and 32 bit KILL password)	64 bit	00b
EPC (excluding 16 bit CRC-16 and 16 bit PC)	128 bit	01b
UCODE 7 Configuration Word	16 bit	01b
TID (including permalocked unique 48 bit serial number)	96 bit	10b

The logical address of all memory banks begin at zero (00h).

In addition to the three memory banks one configuration word to handle the UCODE 7 specific features is available at EPC bank 01 address bit-200h. The configuration word is described in detail in 9.6.

The TID complies to the extended tag Identification scheme according GS1 EPC Tag Data Standard 1.6.

10.5.1 UCODE 7 overall memory map

Table 9. UCODE 7 overall memory map

Bank address	Memory address	Type	Content	Initial	Remark
Bank 00	00h to 1Fh	reserved	kill password	all 00h	unlocked memory
	20h to 3Fh	reserved	access password	all 00h	unlocked memory
Bank 01 EPC	00h to 0Fh	EPC	CRC-16: refer to [1]		memory mapped calculated CRC
	10h to 14h	EPC	EPC length	00110b	unlocked memory
	15h	EPC	UMI	0b	unlocked memory
	16h	EPC	XPC indicator	0b	hardwired to 0
	17h to 1Fh	EPC	numbering system indicator	00h	unlocked memory
	20h to 9Fh	EPC	EPC	[1]	unlocked memory
Bank 01 Config Word	200h	EPC	RFU	0b	locked memory
	201h	EPC	RFU	0b	locked memory
	202h	EPC	Parallel encoding	0b	Action bit[2]
	203h	EPC	RFU	0b	locked memory
	204h	EPC	Tag Power Indicator	0b	Action bit[2]

Bank address	Memory address	Type	Content	Initial	Remark
	205h	EPC	RFU	0b	locked memory
	206h	EPC	RFU	0b	locked memory
	207h	EPC	RFU	0b	locked memory
	208h	EPC	RFU	0b	locked memory
	209h	EPC	max. backscatter strength	1b	permanent bit[3]
	20Ah	EPC	RFU	0b	locked memory
	20Bh	EPC	RFU	0b	locked memory
	20Ch	EPC	RFU	0b	locked memory
	20Dh	EPC	RFU	0b	locked memory
	20Eh	EPC	RFU	0b	locked memory
	20Fh	EPC	PSF alarm flag	0b	Permanent bit[3]
Bank 10 TID	00h to 07h	TID	allocation class identifier	1110 0010b	locked memory
	08h to 13h	TID	tag mask designer identifier	1000 0000 0110b	locked memory
	14h	TID	config word indicator	1b[4]	locked memory
	14h to 1Fh	TID	tag model number	TMNR[5]	locked memory
	20h to 2Fh	TID	XTID header	2000h	locked memory
	30h to 5Fh	TID	serial number	SNR	locked memory

[1] HEX E280 6890 0000 nnnn nnnn nnnn
where n are the nibbles of the SNR from the TID
[2] Action bits: meant to trigger a feature upon a SELECT command on the related bit ref feature control mechanism, seeSection 10.6.1
[3] Permanent bit: permanently stored bits in the memory; Read/Writeable according EPC bank lock status, see Section 10.6.1
[4] Indicates the existence of a Configuration Word at the end of the EPC number
[5] See Figure 7

10.5.2 UCODE 7 TID memory details

	First 48 bit of TID memory	Class ID	Mask Designer ID	Model Number			XTID Header
				Config Word Indicator	Sub Version Nr.	Version (Silicon) Nr.	
UCODE 7	E28068902000	E2h	806h	1b	0001b	0010000b	2000h

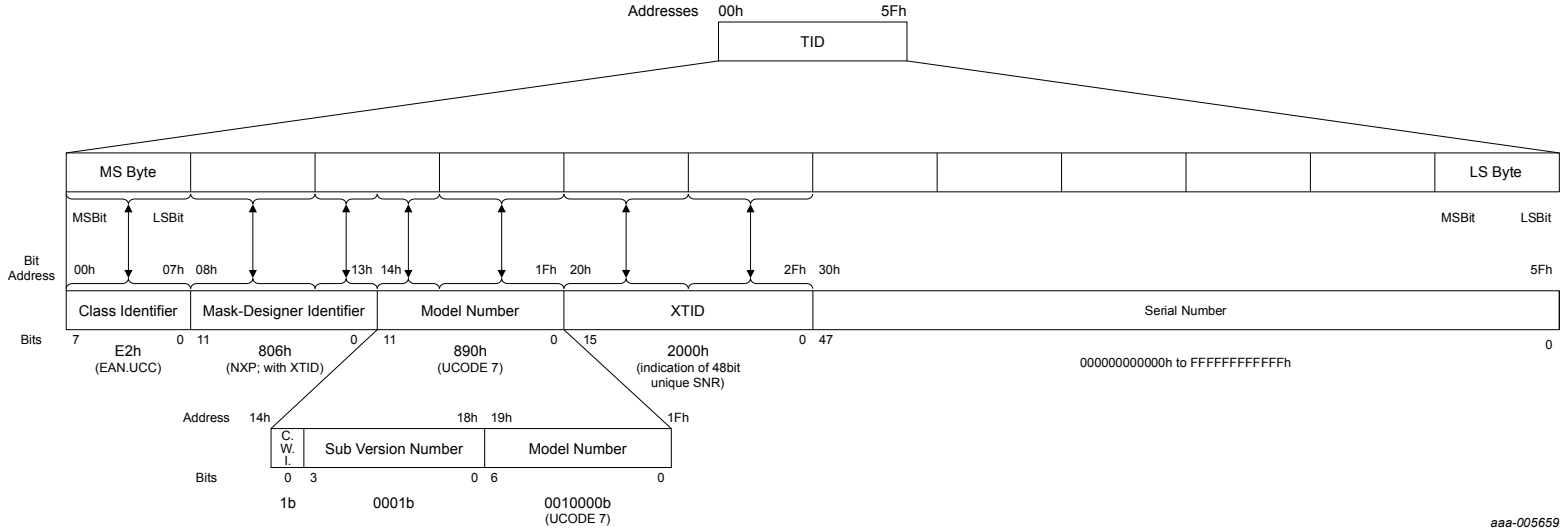


Figure 7. UCODE 7 TID memory structure

10.6 Supported features

The UCODE 7 is equipped with a number of additional features, which are implemented in such a way that standard EPCglobal READ / WRITE / ACCESS / SELECT commands can be used to operate these features.

The Configuration Word, as mentioned in the memory map, describes the additional features located at address 200h of the EPC memory.

Bit 14h of the TID indicates the existence of a Configuration Word. This flag will enable the selection of configuration word enhanced transponders in mixed tag populations.

Please refer to [3] for additional reference.

10.6.1 UCODE 7 features control mechanism

The different features of the UCODE 7 can be activated / de-activated by addressing or changing the content of the corresponding bit in the configuration word located at address 200h in the EPC memory bank (see Table 10). The de-activation of the action bit features will only happen after chip reset.

Table 10. Configuration word UCODE 7

Locked memory		Action bit	Locked memory	Action bit	Locked memory		
RFU	RFU	Parallel encoding	RFU	Tag Power Indicator	RFU	RFU	RFU
0	1	2	3	4	5	6	7

Table 11. Configuration word UCODE 7 ... continued

Locked memory	Permanent bit	Locked memory					Permanent bit
RFU	max. backscatter strength	RFU	RFU	RFU	RFU	RFU	PSF Alarm bit
8	9	10	11	12	13	14	15

The configuration word contains 2 different type of bits:

- **Action bits**: meant to trigger a feature upon a SELECT command on the related bit:
  Parallel encoding
  Tag Power indicator
- **Permanent bits**: permanently stored bits in the memory
  Max. Backscatter Strength
  PSF Alarm bit

The activation or the de-activation of the feature behind the permanent bits happens only when attempting to write a "1" value to the related bit (value toggling) - writing "0" value will have no effect.

If the feature is activated, the related bit will be read with a "1" value and, if de-activated, with a "0" value.

The permanent bits can only be toggled by using standard EPC WRITE (not a BlockWrite) if the EPC bank is unlocked or within the SECURED state if the EPC is locked. If the EPC is perma locked, they cannot be changed.

Action bits will trigger a certain action only if the pointer of the SELECT command exactly matches the action-bit address (i.e. 202h or 204h), if the length=1 and if mask=1b

(no multiple trigger of actions possible within one single SELECT command).

After issuing a SELECT to any action bits an interrogator shall transmit CW for RTCal [1] + 80 µs before sending the next command.

If the truncate bit in the SELECT command is set to "1" the SELECT will be ignored.

A SELECT on action bits will not change the digital state of the chip.

The action bits can be triggered regardless if the EPC memory is unlocked, locked or permalocked.

10.6.2 Backscatter strength reduction

The UCODE 7 features two levels of backscatter strengths. Per default maximum backscatter is enabled in order to enable maximum read rates. When clearing the flag the strength can be reduced if needed.

10.6.3 Pre-serialization of the 96-bit EPC

Description

The 96-bit EPC, which is the initial EPC length settings of UCODE7, will be delivered pre-serialized with the 48-bit serial number from the TID.

Use cases and benefits

With a pre-serialized EPC, the encoding process of the tags with UCODE 7 gets simpler and faster as it only needs to encode the SKU (58-bit header of the EPC).

10.6.4 Parallel encoding

Description

This feature of the UCODE 7 can be activated by the "Parallel encoding bit" in the Configuration-Word located at (202h).

Upon issuing a EPC SELECT command on the "Parallel encoding bit", in a population of UCODE 7 tags, a subsequent QUERY brings all tags go the OPEN state with a specific handle ("AAAAh").

Once in the OPEN state, for example a WRITE command will apply to all tags in the OPEN state (see Figure 9). This parallel encoding is considerably lowering the encoding time compared to a standard implementation (see Figure 8).

The amount of tags that can be encoded at the same time will depend on the strength of the reader signal. Since all tags will backscatter their ACKNOWLEDGE (ACK) response at the same time, the reader will observe collision in the signal from the tags.

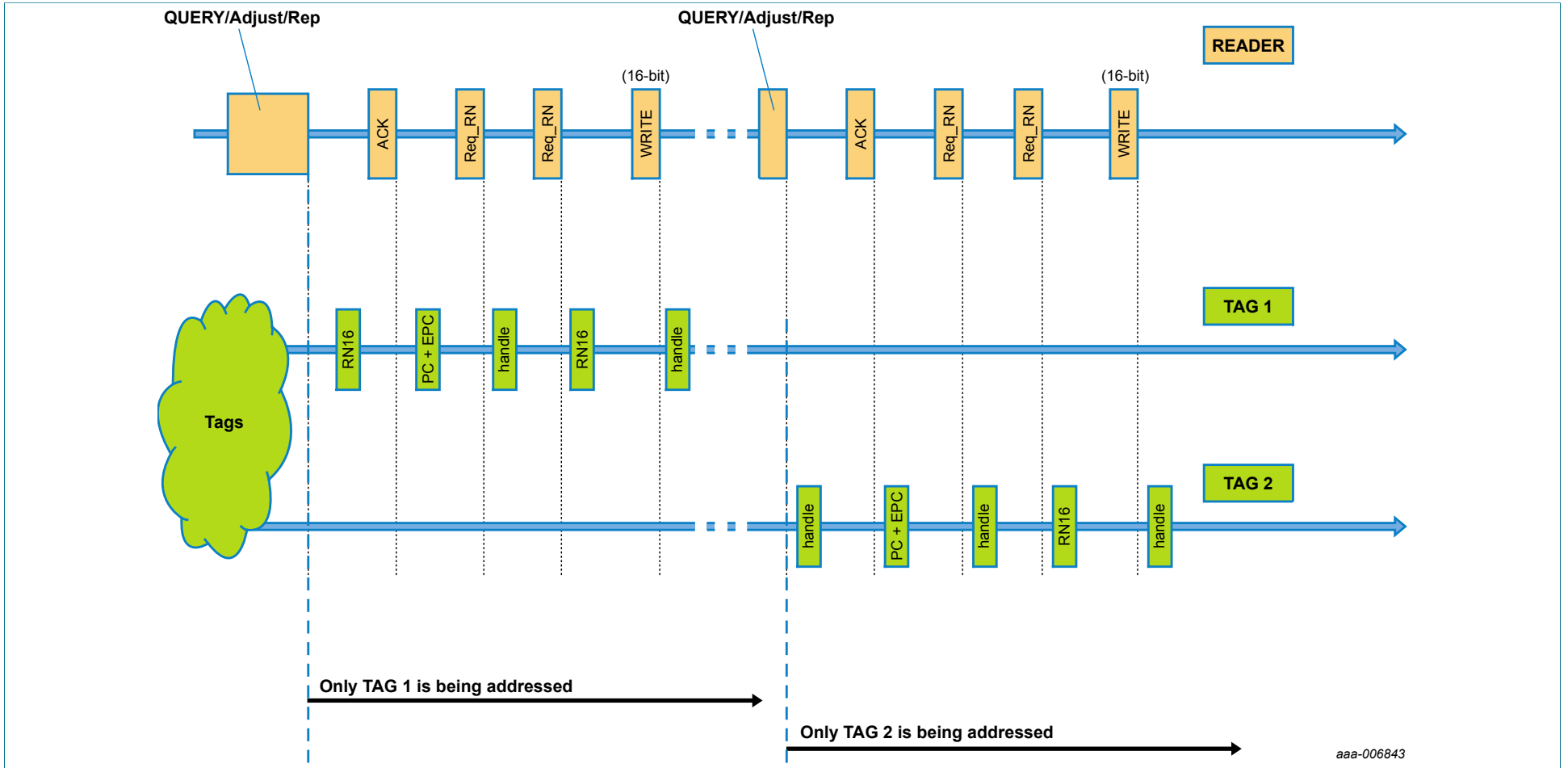


Figure 8. Example of 16-bit Write command with standard EPC Gen 2 commands

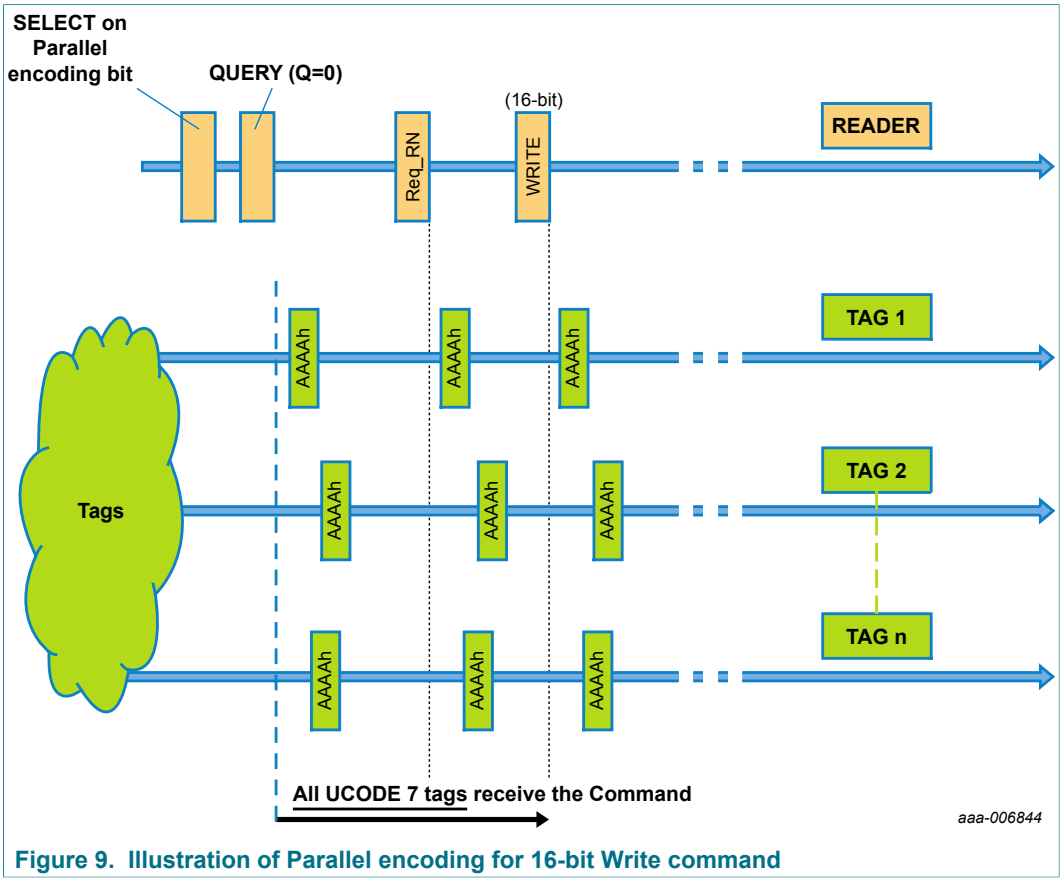


Figure 9. Illustration of Parallel encoding for 16-bit Write command

Use cases and benefits

Parallel encoding feature of UCODE 7 can enable ultra fast bulk encoding.

Taking in addition advantage of the pre-serialization scheme of UCODE 7, the same SKU can be encoded in multiple tags as the EPC will be delivered pre-serialized already.

In the case of only one tag answering (like in printer encoding), this feature could be used to save some overhead in commands to do direct EPC encoding after the handle reply.

Since this is a UCODE 7 specific feature the use of this features requires support on the reader side.

10.6.5 Tag Power Indicator

Description

Upon a SELECT command on the "Tag Power Indicator", located in the config word 204h, an internal power check on the chip is performed to see if the power level is sufficient to perform a WRITE command. The decision level is defined as nominal WRITE sensitivity minus 1dB. In the case there is enough power, the SELECT command is matching and non-matching if not enough power. The tag can then be singulated by the standard inventory procedure.

Use cases and benefits

This feature gives the possibility to select only the tag(s) that receive enough power to be written during e.g. printer encoding in a dense environment of tags even though the reader may read more than one tag (see Figure 10 for illustration). The power level still needs to be adjusted to transmit enough writing power to one tag only to do one tag singulation.

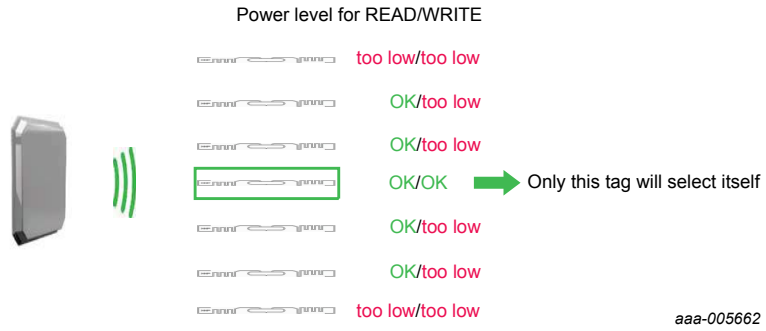


Figure 10. Selection of tags with Tag Power Indicator feature

10.6.6 Product Status Flag (PSF)

Description

The PSF is a general purpose bit located in the Configuration word at address 20Fh with a value that can be freely changed.

Use cases and benefits

The PSF bit can be used as an EAS (Electronic Article Surveillance) flag, quality checked flag or similar.

In order to detect the tag with the PSF activated, a EPC SELECT command selecting the PSF flag of the Configuration word can be used. In the following inventory round only PSF enabled chips will reply their EPC number.

10.6.7 Single-slit antenna solution

Description

In UCODE 7 the test pads TP1 and TP2 are electrically disconnected meaning they are not electrically active and can be safely short-circuited to the RF pads RF1 and RF2 (see Figure 11).

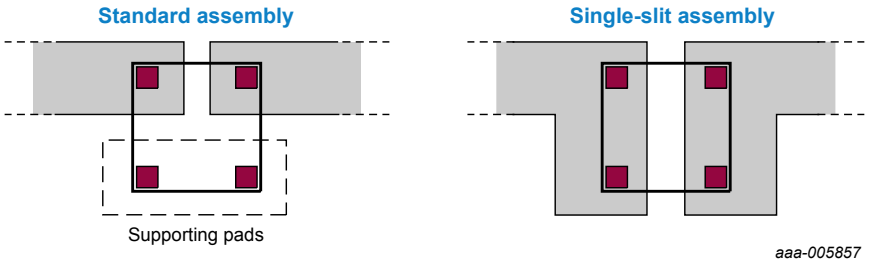


Figure 11. Standard antenna design versus single-slit antenna

Uses cases and benefits

Using single-slit antenna enables easier assembly and antenna design. Inlay manufacturer will only have to take care about one slit of the antenna instead of two in case all pads need to be disconnected from each other.

Additionally single-slit antenna assembly and the related increased input capacitance (see Table 13) can be used advantageously over the standard antenna design as additional room for optimization to different antenna design.

11 Limiting values

Table 12. Limiting values[1][2]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Voltages are referenced to RFN

Symbol	Parameter	Conditions		Min	Max	Unit
Bare die limitations						
T_{stg}	storage temperature			-55	+125	°C
T_{amb}	ambient temperature			-40	+85	°C
V_{ESD}	electrostatic discharge voltage	Human body model	[3][4]	-	± 2	kV
Pad limitations						
P_i	input power	maximum power dissipation, RFP pad		-	100	mW

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

[3] ANSI/ESDA/JEDEC JS-001

[4] For ESD measurement, the die chip has been mounted into a CDIP20 package.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

12 Characteristics

12.1 UCODE 7 bare die characteristics

Table 13. UCODE 7 RF interface characteristics (RF1, RF2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			840	-	960	MHz
						-	
$P_{i(min)}$	minimum input power	READ sensitivity	[1][2][3]	-	-21	-	dBm
$P_{i(min)}$	minimum input power	WRITE sensitivity	[4]	-	-16	-	dBm
t 16bit	Encoding speed	16-bit	[5]	-	1	-	ms
		32-bit (block write)	[5]	-	1.8	-	ms
C_i	Chip input capacitance	parallel	[2][6]	-	0.63	-	pF
Z	Chip impedance	866 MHz	[2][6]	-	14.5-j293	-	Ω
		915 MHz	[2][6]	-	12.5-j277	-	Ω
		953 MHz	[2][6]	-	12.5-j267	-	Ω
Z	Typical assembled impedance [7]	915MHz	[8]	-	18-j245		Ω
Z	Typical assembled impedance [7] in case of single-slit antenna assembly	915MHz	[8][9]	-	13.5-j195	-	Ω
C_i	Chip input capacitance, Large Pads	parallel	[2][6]	-	0.68	-	pF
Z	Chip impedance, Large Pads	866 MHz	[2][6]	-	12.6-j267	-	Ω
		915 MHz	[2][6]	-	11.8-j254	-	Ω
		953 MHz	[2][6]	-	11.5-j244	-	Ω
Tag Power Indicator mode							
$P_{i(min)}$	minimum input power level to be able to select the tag		[4]	-	-15	-	dBm

[1] Power to process a QUERY command
[2] Measured with a 50 Ω source impedance directly on the chip
[3] Results in approximately -21,5dBm tag sensitivity with a 2dBi gain antenna
[4] Tag sensitivity on a 2dBi gain antenna
[5] When the memory content is "0000...".
[6] At minimum operating power
[7] Assuming a 80fF additional input capacitance, 250fF in case of single slit antenna
[8] The antenna shall be matched to this impedance
[9] Depending on the specific assembly process, sensitivity losses of few tenths of dB might occur

Table 14. UCODE 7 memory characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
EEPROM characteristics							
t_{ret}	retention time	$T_{amb} \leq 55$ °C		20	-	-	year
$N_{endu(W)}$	write endurance			100k	-	-	cycle

12.2 UCODE 7 SOT886 characteristics

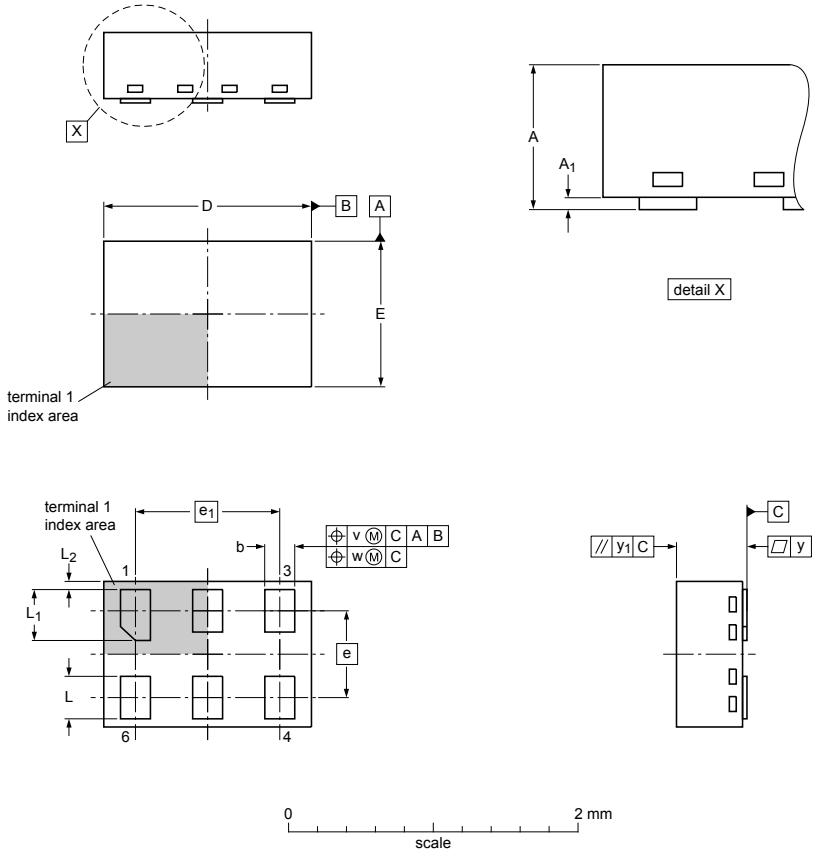
Table 15. UCODE 7 RF interface characteristics (RF1, RF1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{i(min)}$	minimum input power	READ sensitivity	[1][2]	-	-21	-	dBm
Z	impedance	915 MHz	[3]	-	12.8 -j248	-	Ω

[1] Power to process a Query command.
[2] Measured with a 50 Ω source impedance.
[3] At minimum operating power.

13 Package outline

XSON6: plastic, extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.45 x 0.5 mm **SOT886-1**



Dimensions (mm are the original dimensions)

Unit	A	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
max	0.50	0.05	0.25	1.50	1.05			0.35	0.40	0.10				
mm nom			0.20	1.45	1.00	0.6	1.0	0.30	0.35	0.05	0.10	0.05	0.05	0.05
min		0.00	0.17	1.40	0.95			0.27	0.32	0.02				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot886-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886-1						~~13-07-03~~ 13-07-10

Figure 12. Package outline SOT886

14 Packing information

14.1 Wafer

See [2]

See [4]

14.2 SOT886

See: www.nxp.com/packages/SOT886.html

15 Abbreviations

Table 16. Abbreviations

Acronym	Description
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DSB-ASK	Double Side Band-Amplitude Shift Keying
DC	Direct Current
EAS	Electronic Article Surveillance
EEPROM	Electrically Erasable Programmable Read Only Memory
EPC	Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number)
FM0	Bi phase space modulation
G2	Generation 2
IC	Integrated Circuit
PIE	Pulse Interval Encoding
PSF	Product Status Flag
RF	Radio Frequency
UHF	Ultra High Frequency
SECS	Semi Equipment Communication Standard
TID	Tag IDentifier

16 References

[1] EPCglobal: EPC Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 1.1.0 (December 17, 2005)

[2] Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1093**[1]

[3] Application note - AN11274 – FAQ on UCODE 7

[4] Data sheet - Delivery type description – General specification for 12" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1862**

1 ** ... document version number

17 Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SL3S1204 v. 4.0	20190305	Product data sheet	-	SL3S1204 v. 3.9
Modifications:	• Section 16 updated			
SL3S1204 v. 3.9	20170321	Product data sheet	-	SL3S1204 v. 3.8
Modifications:	• Introduction of Large Pads • Table 1 :updated • Section 8.2: added • Section 9.1.2: added • Table 13: updated			
SL3S1204 v. 3.8	20161011	Product data sheet	-	SL3S1204 v. 3.7
Modifications:	• Figure 7: updated • Figure 12: updated • Editorial changes			
SL3S1204 v. 3.7	20160718	Product data sheet	-	SL3S1204 v. 3.6
Modifications:	• Update Automatic Pre-serialization functionality • Figure 7 - change of TID			
SL3S1204 v. 3.6	20160524	Product data sheet	-	SL3S1204 v. 3.5
Modifications:	• Introduction of 12 inch wafer delivery • Section 8.3: added • Section 9.1.3: added • Section 14.2: added • Table 15: impedance value added			
SL3S1204 v. 3.5	20150706	Product data sheet	-	SL3S1204 v. 3.4
Modifications:	• SOT886 package added			
SL3S1204 v. 3.4	20141017	Product data sheet	-	SL3S1204 v. 3.3
Modifications:	• Table 9: corrected • Editorial changes			
SL3S1204 v. 3.3	20131217	Product data sheet	-	SL3S1204 v. 3.2
Modifications:	• Figure 7: Automatic self pre-serialization scheme for 96-bit EPC: corrected			
SL3S1204 v. 3.2	20131120	Product data sheet	-	SL3S1204 v. 3.1
Modifications:	• Security level changed from "COMPANY PROPRIETARY" to "COMPANY PUBLIC"			
SL3S1204 v. 3.1	20130603	Product data sheet	-	241330
Modifications:	• Security level changed from "COMPANY CONFIDENTIAL" to "COMPANY PROPRIETARY"			
241330	20130522	Product data sheet	-	241312
Modifications	• Editorial changes • Figure 4: updated • Table 9: updated • Table 10: updated • Table 13: updated			
241312	20130422	Objective data sheet		241311

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications	• Editorial changes • Figure 7: updated • Figure 7: Automatic self pre-serialization scheme for 96-bit EPC: updated • Figure 10: updated • Figure 11: updated			
241311	20130325	Objective data sheet		241310
Modifications	General Update			
241310	20130226	Objective data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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