

PE42441

UltraCMOS® SP4T RF Switch
10 MHz – 8 GHz

Product Description

The PE42441 is a HaRP™ technology-enhanced absorptive SP4T RF switch designed for use in various switching applications spanning multiple markets including wireless infrastructure, broadband, and wireless connectivity.

This switch has four symmetric RF ports and delivers low insertion loss and exceptional isolation. An on-chip CMOS decode logic facilitates a two-pin low voltage CMOS control interface. In addition, no external blocking capacitors are required if 0 VDC is present on RF ports.

The PE42441 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- Four symmetric 50Ω absorptive ports
- High isolation
 - 45 dB @ 3 GHz
 - 39 dB @ 6 GHz
 - 31 dB @ 8 GHz
- Low insertion loss
 - 0.8 dB @ 3 GHz
 - 1.0 dB @ 6 GHz
 - 1.2 dB @ 8 GHz
- High linearity
 - 58 dBm IIP3 @ 8 GHz
 - 110 dBm IIP2 @ 8 GHz
- 1.8V control logic compatible
- ESD performance
 - 2 kV HBM on all pins
 - 100V MM on all pins
 - 1 kV CDM on all pins

Figure 1. Functional Diagram

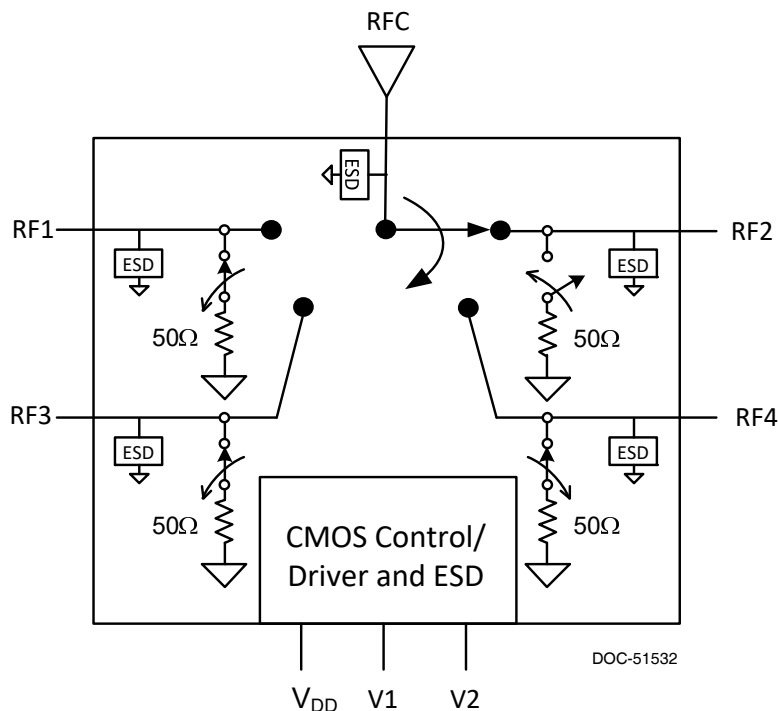


Figure 2. Package Type

32-lead 5x5 mm LGA

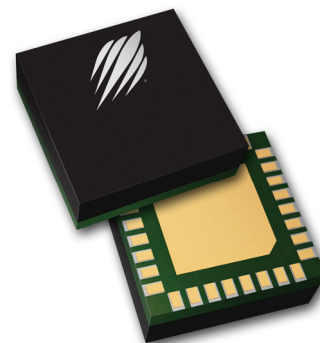


Table 1. Electrical Specifications @ 25°C, V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise specified

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			10 MHz		8 GHz	
Insertion loss	RFC-RFX	10 MHz – 3000 MHz		0.8	1.1	dB
		3000 MHz – 6000 MHz		1.0	1.3	dB
		6000 MHz – 7500 MHz		1.1	1.5	dB
		7500 MHz – 8000 MHz		1.2	1.6	dB
Isolation (active port to terminated port)	RFX-RFX	10 MHz – 3000 MHz	40	45		dB
		3000 MHz – 6000 MHz	34	39		dB
		6000 MHz – 7500 MHz	27	32		dB
		7500 MHz – 8000 MHz	25	31		dB
Isolation (common port to active port)	RFC-RFX	10 MHz – 3000 MHz	40	45		dB
		3000 MHz – 6000 MHz	28	33		dB
		6000 MHz – 7500 MHz	24	29		dB
		7500 MHz – 8000 MHz	21	27		dB
Return loss (common port)	RFX	10 MHz – 3000 MHz		23		dB
		3000 MHz – 6000 MHz		18		dB
		6000 MHz – 7500 MHz		14		dB
		7500 MHz – 8000 MHz		13		dB
Return loss (active port)	RFX	10 MHz – 3000 MHz		23		dB
		3000 MHz – 6000 MHz		18		dB
		6000 MHz – 7500 MHz		17		dB
		7500 MHz – 8000 MHz		16		dB
Return loss (terminated port)	RFX	10 MHz – 3000 MHz		18		dB
		3000 MHz – 6000 MHz		13		dB
		6000 MHz – 7500 MHz		11		dB
		7500 MHz – 8000 MHz		10		dB
Input 0.1 dB compression point ¹	RFC-RFX	10 MHz – 8000 MHz		31		dBm
Input IP3	RFC-RFX	8000 MHz		58		dBm
Input IP2	RFC-RFX	8000 MHz		110		dBm
Switching time		50% CTRL to 90% or 10% RF		5	8	μs
Settling time		50% CTRL to 0.05 dB final value (–40 to +85°C) rising edge		14	18	μs
		50% CTRL to 0.05 dB final value (–40 to +85°C) falling edge		15	45	μs

Note 1: The input 0.1dB compression point is a linearity figure of merit. Refer to Table 3 for the operating RF input power (50Ω).

Figure 3. Pin Configuration (Top View)

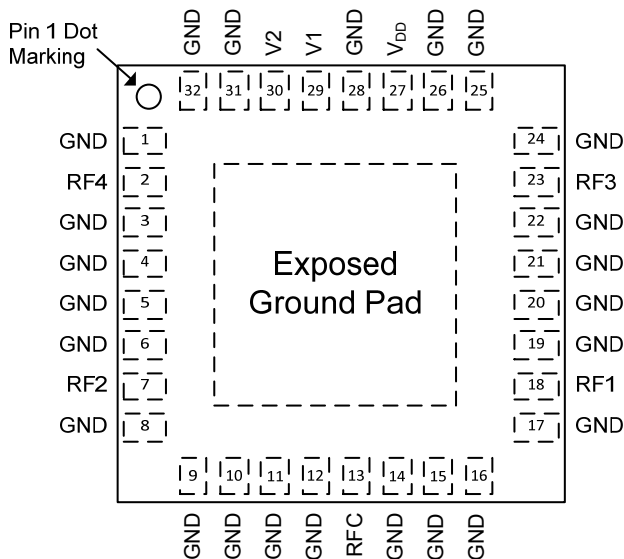


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 3-6, 8, 9-12, 14-17, 19-22, 24-26, 28, 31, 32	GND	Ground
2	RF4 ¹	RF port
7	RF2 ¹	RF port
13	RFC ¹	RF common
18	RF1 ¹	RF port
23	RF3 ¹	RF port
27	V _{DD}	Supply voltage
29	V1	Digital control logic input 1
30	V2	Digital control logic input 2
Pad	GND	Exposed pad: Ground for proper operation

Note 1: RF pins 2, 7, 13, 18, and 23 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DD}	3.0	3.3	3.55	V
Supply current	I _{DD}		90	160	μA
Digital input high (V1, V2)	V _{IH}	1.2	1.5	V _{DD}	V
Digital input low (V1, V2)	V _{IL}	0	0	0.4	V
Digital input current	I _{CTRL}			1	μA
RF input power, CW ¹ 10 MHz – 8 GHz	P _{MAX,CW}			See Fig. 4	dBm
RF input power into terminated ports, CW 10 MHz – 8 GHz	P _{MAX,TERM}			+20	dBm
Operating temperature range	T _{OP}	-40		+85	°C

Notes: 1. 100% duty cycle (-40 to +85°C, 1:1 VSWR)

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V _{DD}	-0.3	4.0	V
Digital input voltage (V1, V2)	V _{CTRL}	-0.3	4.0	V
Maximum input power 10 MHz – 8 GHz	P _{MAX,ABS}		See Fig. 4	dBm
Storage temperature range	T _{ST}	-60	+150	°C
ESD voltage HBM ¹ , all pins	V _{ESD,HBM}		2	kV
ESD voltage MM ² , all pins	V _{ESD,MM}		100	V
ESD voltage CDM ³ , all pins	V _{ESD,MM}		1	kV

Notes: 1. Human Body Model (MIL-STD 883 Method 3015.7)
2. Machine Model (JEDEC JESD22-A115-A)
3. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Switching Frequency

The PE42441 has a maximum 25 kHz switching rate. Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Table 5. Truth Table

State	V1	V2
RF1 on	0	0
RF2 on	1	0
RF3 on	0	1
RF4 on	1	1

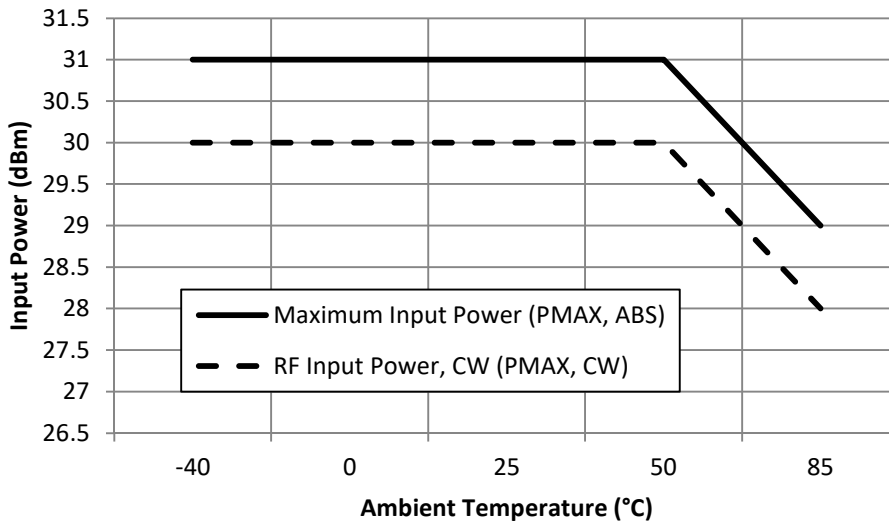
Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42441 in the 32-lead 5x5 mm LGA package is MSL3.

Spurious Performance

The typical spurious performance of the PE42441 is -159 dBm/Hz.

Figure 4. Power De-rating Curve vs Temperature



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ unless otherwise specified

Figure 5. Insertion Loss (RFC-RFX)

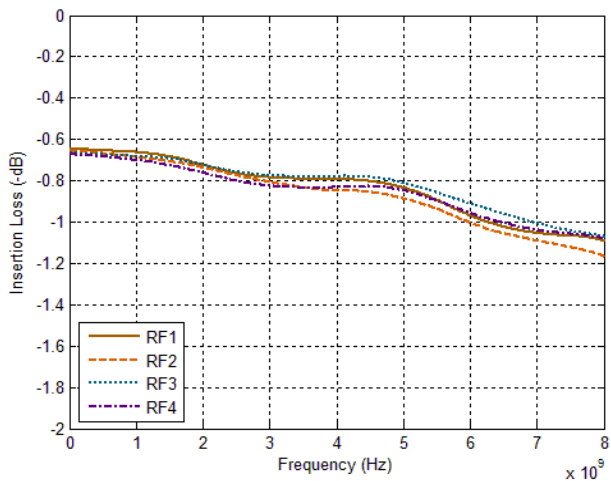


Figure 6. Insertion Loss vs. Temp (RFC-RFX)

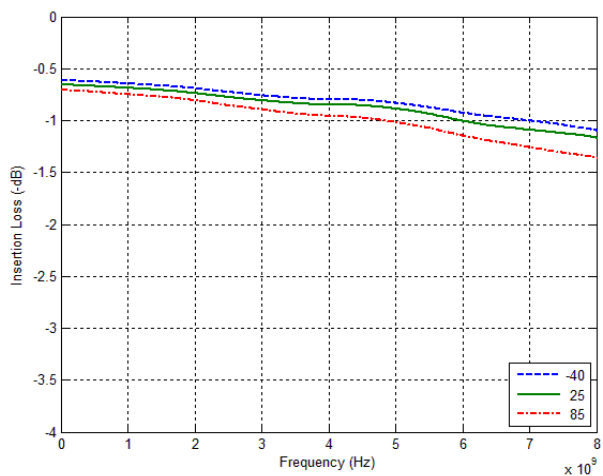
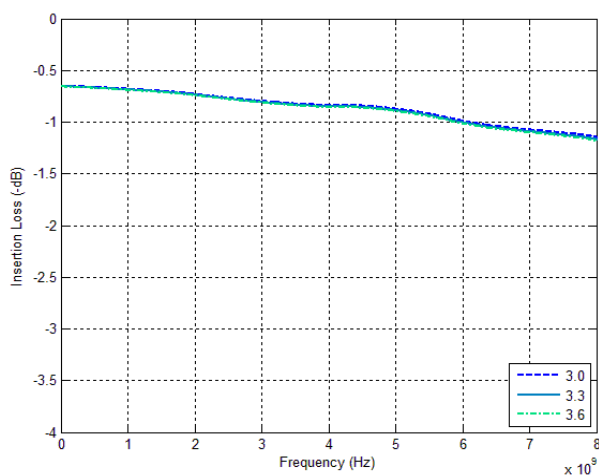


Figure 7. Insertion Loss vs. V_{DD} (RFC-RFX)



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, unless otherwise specified

Figure 8. RFC Port Return Loss vs. Temp

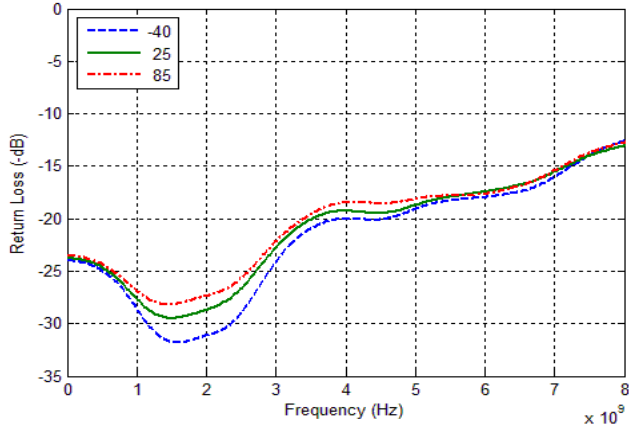


Figure 9. RFC Port Return Loss vs. V_{DD}

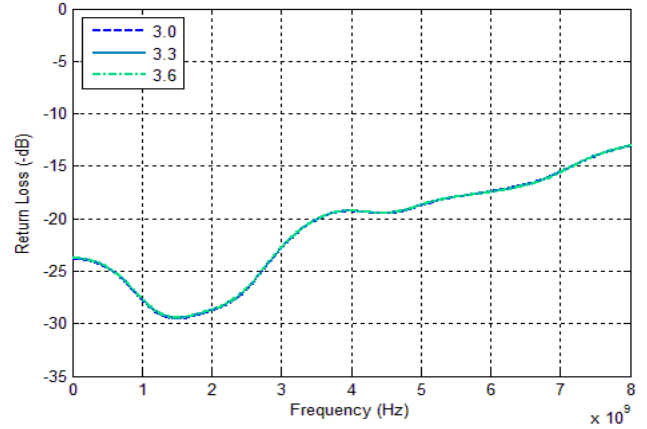


Figure 10. Active Port Return Loss vs. Temp

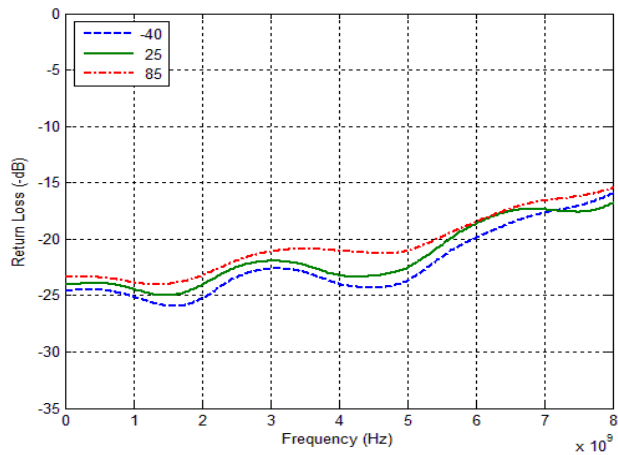
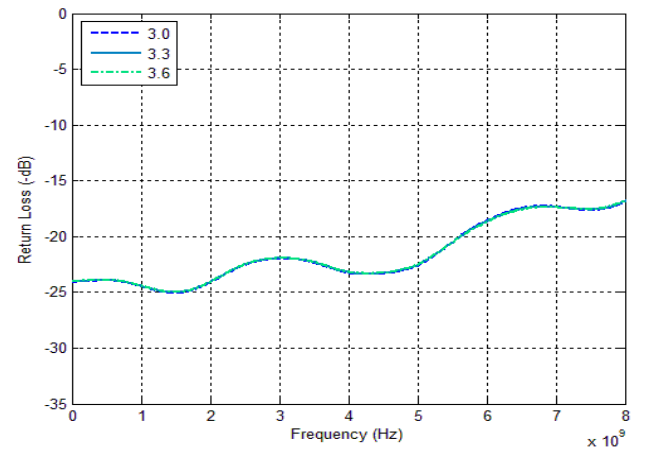


Figure 11. Active Port Return Loss vs. V_{DD}



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, unless otherwise specified

Figure 12. Terminated Port Return Loss vs. Temp

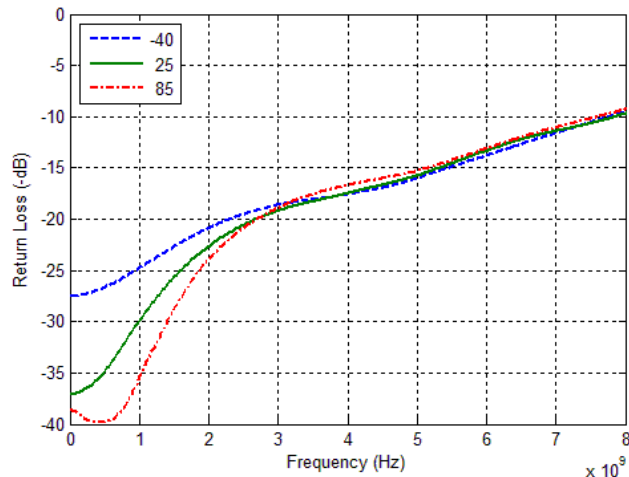


Figure 13. Terminated Port Return Loss vs. V_{DD}

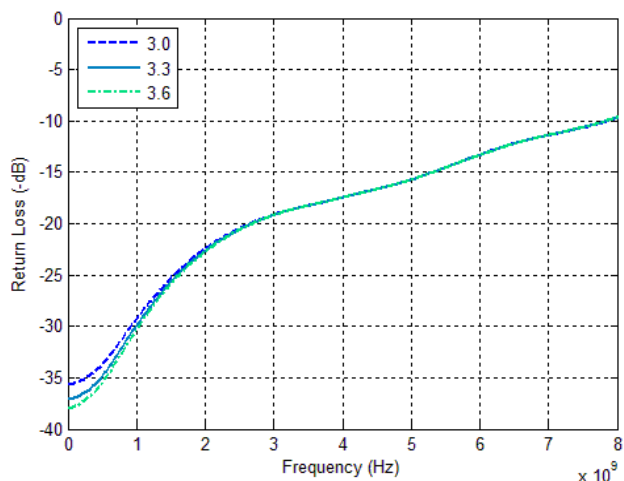


Figure 14. Isolation vs. Temp (RFX-RFX)

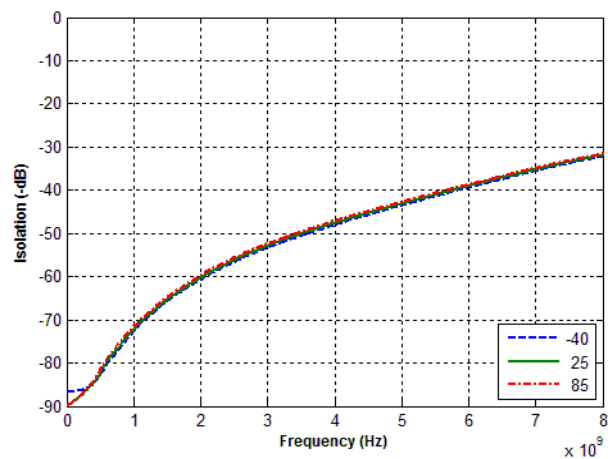
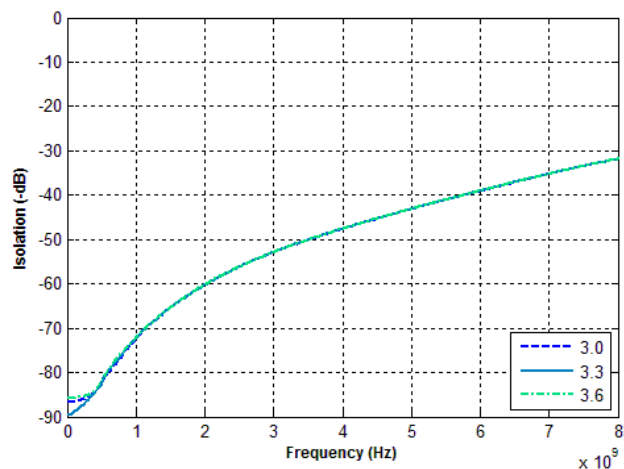


Figure 15. Isolation vs. V_{DD} (RFX-RFX)



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, unless otherwise specified

Figure 16. Isolation vs. Temp (RFC-RFX)

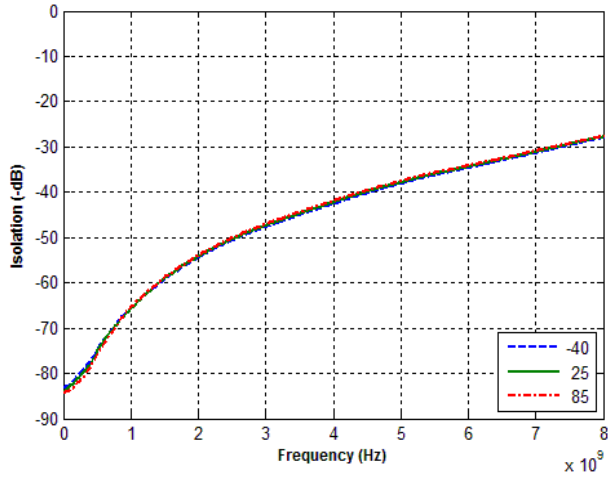


Figure 17. Isolation vs. V_{DD} (RFC-RFX)

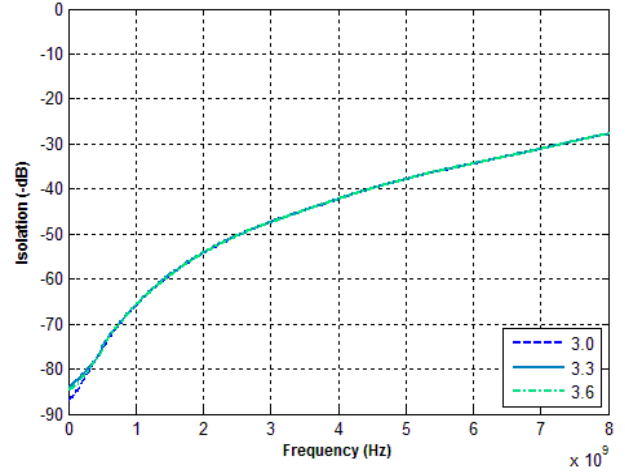
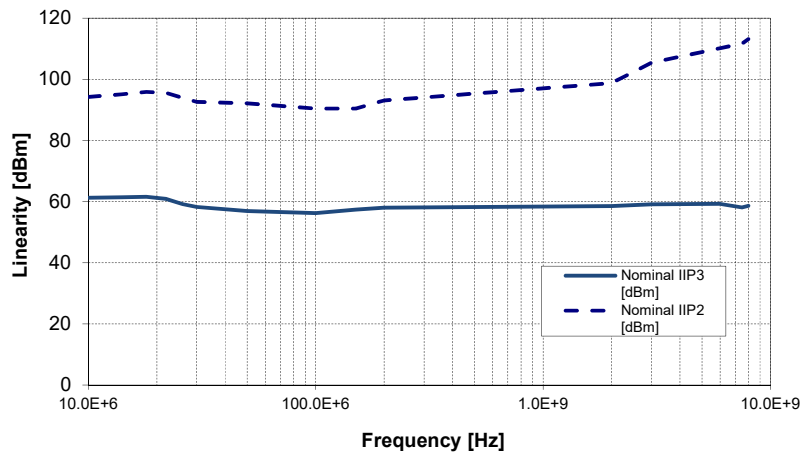


Figure 18. Linearity Performance

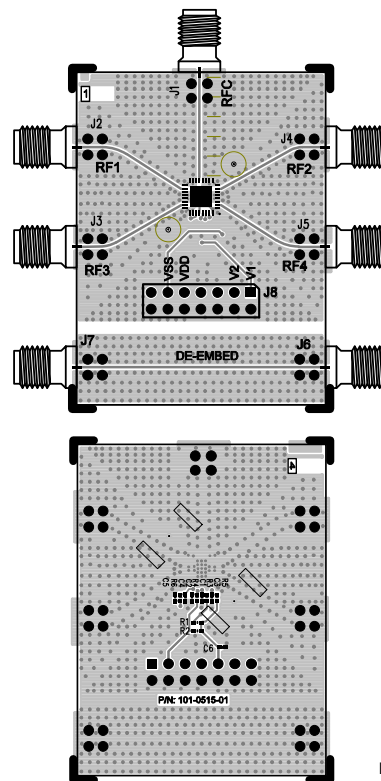


Evaluation Kit

The SP4T switch EK Board was designed to ease customer evaluation of pSemi’s PE42441. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1, RF2, RF3 and RF4 are connected through 50Ω transmission lines via SMA connectors J2, J4, J3 and J5, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

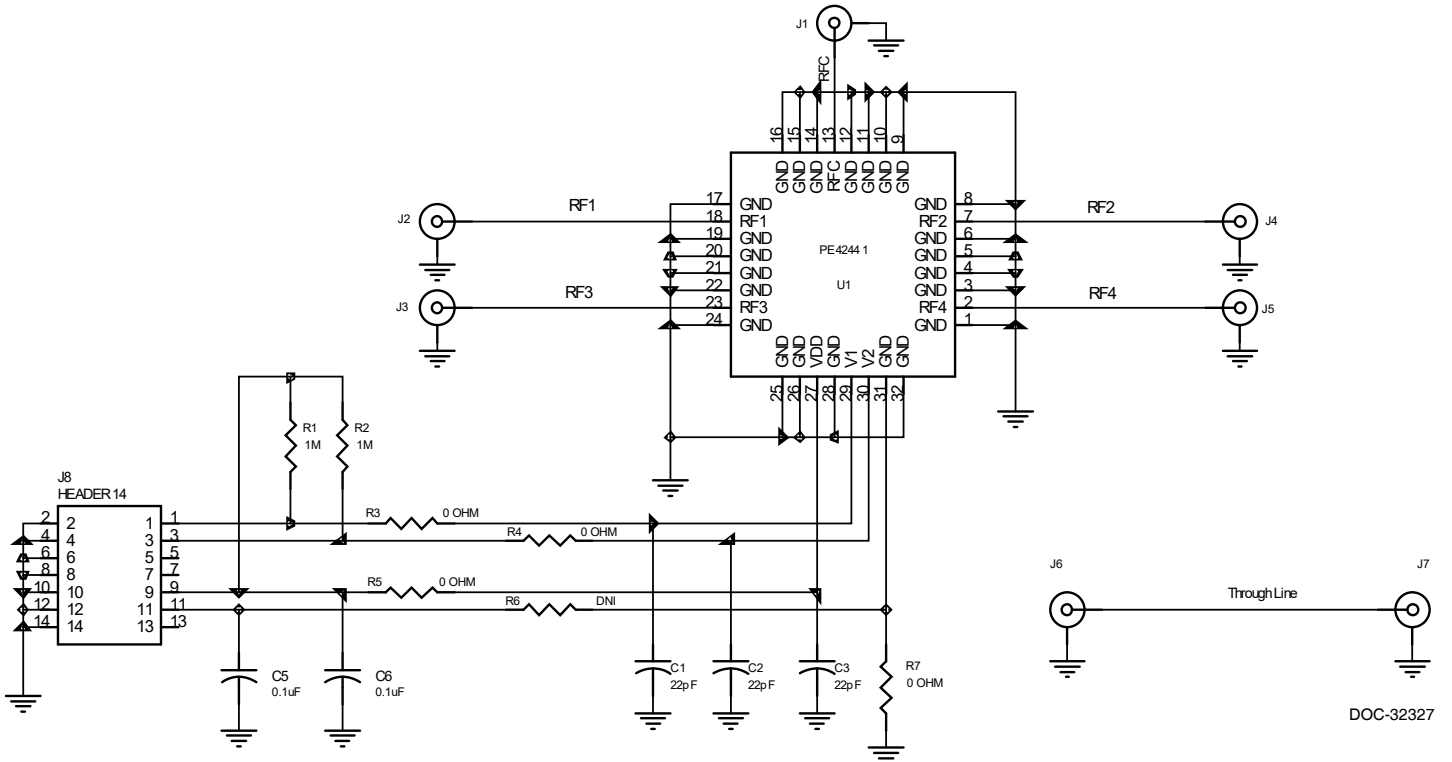
The board is constructed of a four metal layer material with a total thickness of 62 mils. The dual clad top RF layer is Rogers RO4003 material with an 8 mil RF core and $\epsilon_r = 3.55$. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 15 mils, trace gaps of 10 mils, and metal

Figure 19. Evaluation Board Layouts



PRT-28605

Figure 20. Evaluation Board Schematic



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