THE DATASHEET OF

SI32260CPB21BC0EVB

Si32260/1

SINGLE-CHIP DUAL PROSLIC®

Si32260/1 Features

- Two complete FXS channels in a single 6 x 8 mm or 8 x 8 mm package
- Performs all BORSCHT functions
- Ideal for short- or long-loop applications
- Ultra low power consumption
- Internal balanced or unbalanced ringing
- Patented low power ringing
- Adaptive ringing
- Simplified configuration and diagnostics
  - Supported by ProSLIC API
  - GR-909 loop diagnostics
  - Audio diagnostics with loopback
  - Integrated test load
- Wideband voice support
- On-hook transmission
- Loop or ground start operation
- Smooth polarity reversal
- Pulse metering
- PCM and SPI bus digital interfaces with programmable interrupts
- Software-programmable parameters:
  - Ringing frequency, amplitude, cadence, and waveshape
  - Two-wire ac impedance
  - Transhybrid balance
  - DC current loop feed (10–45 mA)
  - Loop closure and ring trip thresholds
  - Ground key detect threshold
- Integrated dc-dc controllers with direct connection to MOSFET
- Three high voltage supply options
  - Full tracking
  - Tracking shared supplies
  - Fixed rail
- DTMF generator/decoder
- A-Law/μ-Law companding, linear PCM
- GCI/IOM-2 mode support
- 3.3 V operation
- Pb-free/RoHS-compliant packaging

Applications

- VoIP gateways and routers
- xDSL IADs
- Optical Network Terminals/Units (ONT/U)
- Analog Terminal Adapters (ATA)
- Cable eMTA
- Wireless Fixed Terminals (WFT)
- Wireless Local Loop (WLL)
- WiMAX CPE
- Private Branch Exchange (PBX)
- VoIP MDU gateways

Description

The Si32260/1 Dual ProSLIC® devices, in a single package, implement two complete foreign exchange station (FXS) telephony interfaces. The Si32260/1 devices operate from a 3.3 V supply and have standard PCM/SPI or GCI (8x8 mm package only) bus digital interfaces. A pair of built-in dc-dc converter controllers can be used to automatically generate the optimal battery voltage required for each line-state, optimizing efficiency and minimizing heat generation.

The Si32260/1 devices are designed to operate not only with a tracking battery supply for each channel for lowest power consumption, but also with shared battery supplies, for lowest cost. When used with shared battery supplies, the internal dc-dc controller operates in Tracking Shared Supply (TSS) mode to deliver power consumption lower than typical fixed voltage shared rail designs (shared supplies are not currently supported by the 6 x 8 mm package option).

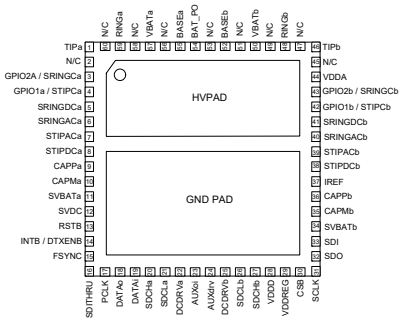
Self-testing and metallic loop testing (MLT) (e.g., GR-909) is facilitated by the built-in DSP, monitor ADC, and test load. The devices are available with linefeed voltage ratings of –110 V (Si32260) or –140 V (Si32261) to support high voltage ringing, and both devices support wideband audio for better-than-PSTN voice quality. The Si32260/1 devices are available in a 6 x 8 mm 47-pin QFN package or an 8 x 8 mm 60-pin QFN package.

Ordering Information

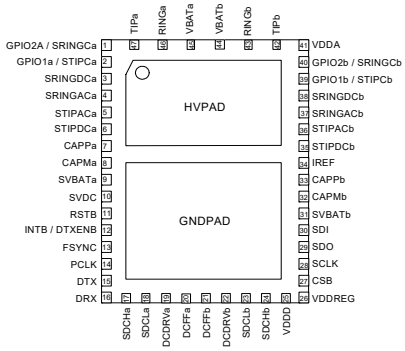
See page 45.

Pin Assignments

Si32260/1 8x8 mm



Si32260/1 6x8 mm



Patents pending

Functional Block Diagram

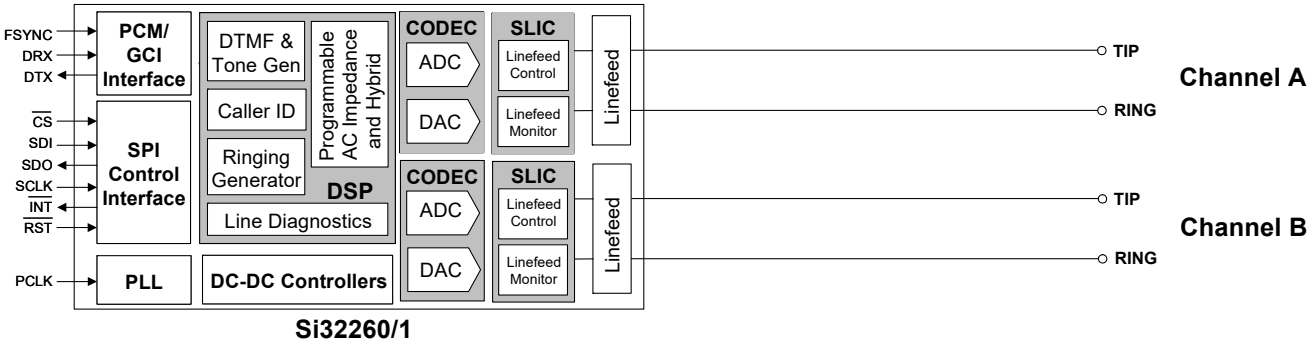


Table of Contents

1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A	F-grade	0	25	70	°C
		G-grade	–40	25	85	°C
Silicon Junction Temperature, QFN-60, QFN-47	T_{JHV}	Linefeed Die	—	—	145[2]	°C
Supply Voltage, Si32260/1	V_{DDD}, V_{DDA}		3.13	3.3	3.47	V
Battery Voltage, Si32260[3]	V_{BAT}		–110	—	–15	V
Battery Voltage, Si32261[3]	V_{BAT}		–140	—	–15	V

Notes:
1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Except during ringing.
3. Operation at minimum voltage dependent upon loop conditions and dc-dc converter configuration.

Table 2. AC Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Compression	2-Wire – PCM	Figure 5	—	—	
Single Frequency Distortion (0 dBm0 input)	0 Hz to 4 kHz	—	—	–40	dBm0
	0 Hz – 12 kHz	—	—	–28	dBm0
Signal-to-(Noise + Distortion) Ratio[1]	200 Hz to 3.4 kHz D/A or A/D 8-bit Active off-hook, and OHT, any Z_T	Figure 4	—	—	
Audio Tone Generator Signal-to-Distortion Ratio[1]	0 dBm0, Active off-hook, and OHT, any Z_T	46	—	—	dB
Intermodulation Distortion		—	—	–41	dB
Gain Accuracy[1]	2-Wire to PCM or PCM to 2-Wire 1014 Hz, any gain setting	–0.2	—	0.2	dB
Attenuation Distortion vs. Freq.	0 dBm0[5]	See Figure 6 and 7			

Notes:
1. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
2. The quantization errors inherent in the μ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
3. V_{DDD}, V_{DDA} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
4. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
5. 0 dBm0 is equal to 0 dBm into 600 Ω.

Table 2. AC Characteristics (Continued)

Parameter	Test Condition	Min	Typ	Max	Unit
Group Delay vs. Frequency		See Figure 8 and 9			
Gain Tracking[2]	1014 Hz sine wave, reference level –10 dBm Signal level:				
	3 dB to –37 dB	—	—	0.25	dB
	–37 dB to –50 dB	—	—	0.5	dB
	–50 dB to –60 dB	—	—	1.0	dB
Round-Trip Group Delay	1014 Hz, Within same time-slot	—	450	500	µs
2-Wire Return Loss[3]	200 Hz to 3.4 kHz	26	30	—	dB
Transhybrid Balance[3]	300 Hz to 3.4 kHz	26	30	—	dB
Noise Performance					
Idle Channel Noise[4]	C-Message weighted	—	8	12	dBrnC
	Psophometric weighted	—	–82	–78	dBmP
PSRR from V_{DDD}, V_{DDA} @ 3.3 V	RX and TX, 200 Hz to 3.4 kHz	—	55	—	dB
Longitudinal Performance					
Longitudinal to Metallic/PCM Balance (forward or reverse)	200 Hz to 1 kHz	58	60	—	dB
	1 kHz to 3.4 kHz	53	58	—	dB
Metallic/PCM to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING	—	50	—	Ω
Longitudinal Current Capability	Active off-hook 60 Hz Reg 73 = 0x0B	—	25	—	mA

Notes:

1. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
2. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
3. V_{DDD}, V_{DDA} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
4. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
5. 0 dBm0 is equal to 0 dBm into 600 Ω.

Table 3. Power Supply Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply currents: Reset	I_{DD}	V_T and V_R = Hi-Z , RST = 0	—	3.5	—	mA
	I_{VBAT}		—	0	—	mA
Supply currents: High Impedance, Open	I_{DD}	V_T and V_R = Hi-Z	—	23	—	mA
	I_{VBAT}		—	0.6	—	mA
Supply currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V, Automatic Power Save Mode enabled	—	10	—	mA
	I_{VBAT}		—	0.4	—	mA
Supply currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V, Automatic Power Save Mode disabled	—	35	—	mA
	I_{VBAT}		—	2.2	—	mA
Supply currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V V_R or V_T = Hi-Z, Automatic Power Save Mode enabled	—	10	—	mA
	I_{VBAT}		—	0.4	—	mA
Supply currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V V_R or V_T = Hi-Z, Automatic Power Save Mode enabled	—	35	—	mA
	I_{VBAT}		—	1.5	—	mA
Supply currents: Forward/Reverse OHT, On-hook	I_{DD}	V_{TR} = 48 V	—	53	—	mA
	I_{VBAT}		—	3	—	mA
Supply currents: Forward/Reverse Active, Off-hook	I_{DD}	I_{LOOP} = 20 mA R_{LOAD} = 200 Ω	—	54	—	mA
	I_{VBAT}		—	2.2 + I_{LOOP}	—	mA
Supply currents: Ringing	I_{DD}	V_{TR} =55V_{RMS} + 0 V_{DC}, balanced, sinusoidal, f = 20 Hz, R_{LOAD} = 5 REN = 1400 Ω	—	40	—	mA
	I_{VBAT}		—	38	—	mA

Notes:

1. All specifications are for a single channel of Si3226x with a tracking flyback dc-dc converter, when both channels are in the same operating state.
2. I_{LOOP} is the dc current in the subscriber loop during the off-hook state.

Table 4. Linefeed Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Loop Resistance	R_{LOOP}	$R_{DC,MAX}$ = 430 Ω I_{LOOP} = 18 mA, V_{BAT} = –52 V, R_{PROT} = 0 Ω	—	—	2000	Ω
DC Feed Current		Differential	—	—	45	mA
		Common Mode	—	—	30	mA
		Differential + Common Mode	—	—	45	mA
DC Loop Current Accuracy		I_{LIM} = 18 mA	—	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	—	—	4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	160	—	640	Ω
DC On-Hook Voltage Accuracy—Ground Start	V_{OHTO}	$I_{RING}<I_{LIM}$; V_{RING} wrt ground, V_{RING} = –51 V	—	—	4	V
DC Output Resistance—Ground Start	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	160	—	640	Ω
DC Output Resistance—Ground Start	R_{TOTO}	TIP to ground	400	—	—	kΩ
Loop Closure Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ground Key Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ring Trip Threshold Accuracy		AC detection, V_{RING} = 70 Vpk, no offset, I_{TH} = 80mA	—	—	4	mA
		DC detection, 20 V dc offset, I_{TH} = 13 mA	—	—	1	mA
		DC Detection, 48 V DC offset, R_{loop} = 1500 Ω	—	—	3	mA
Ringing Amplitude*	$V_{RINGING}$	Si32260 Open circuit, V_{BAT} = –110 V	—	–108	—	V_{PK}
		Si32261 Open circuit, V_{BAT} = –140 V	—	–136	—	V_{PK}
Sinusoidal Ringing Total Harmonic Distortion	R_{THD}	Si32260 : 60 V_{RMS}, 15 V_{OFFSET}, 0–5 REN	—	1	—	%
		Si32261 : 55 V_{RMS}, 48 V_{OFFSET}, 0–5 REN				
Ringing Frequency Accuracy		f = 16 Hz to 60 Hz	—	—	1	%

***Note:** Ringing amplitude is set for 108 or 128 V peak and measured at TIP-RING using no series protection resistance.

Table 4. Linefeed Characteristics (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ringing Cadence Accuracy		Accuracy of ON/OFF times	—	—	50	ms
Loop Voltage Sense Accuracy		$V_{TIP} - V_{RING}$ = 48 V	—	2	4	%
Loop Current Sense Accuracy		I_{LOOP} = 18 mA	—	7	10	%
Power Alarm Threshold Accuracy		Power Threshold = 1.0 W V_{BAT} = –56 V, I_{LDDD} = 40 mA, R_{LOAD} = 600 Ω	—	15	—	%
Test Load Impedance	R_{TEST}	HVIC_STATE_SPARE[23] = 1; $\lvert V_{T/R} \rvert \leq 50$ V	1.0	—	3.0	kΩ
Test Load Voltage	V_{TL}	HVIC_STATE_SPARE[23] = 1	±5		±50	V
***Note:** Ringing amplitude is set for 108 or 128 V peak and measured at TIP-RING using no series protection resistance.						

Table 5. Digital I/O Characteristics

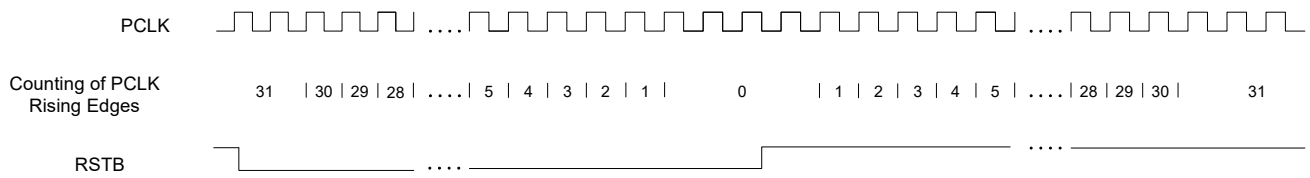
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	V_{DD}	V
Low Level Input Voltage	V_{IL}		0	—	0.8	V
High Level Output Voltage	V_{OH}	DTX, SDO, SDITHRU, GPIO1/STIPC, GPIO2/SRINGC: I_O = –4 mA	V_{DD} – 0.6	—	—	V
Low Level Output Voltage	V_{OL}	DTX, SDO, $\overline{INT}$, SDITHRU, GPIO1/STIPC, GPIO2/SRINGC: I_O = 4 mA	—	—	0.4	V
SDITHRU and $\overline{RST}$ Internal Pullup Current			33	42	80	µA
Input Leakage Current	I_L		—	—	10	µA

Table 6. Charge Pump Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage (DCDRVa/b, DCFFa/b)	V_{CP}		2 x V_{DD} – 1	—	2xV_{DD}	V
Output Current	I_{CP}		—	—	3*	mA
***Note:** Peak drive current capability is >60 mA.						

Table 7. Switching Characteristics—General Inputs*

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width	t_{rl}	33/PCLK	—	—	µs
***Note:** All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DD} – 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.					



Note: The count of PCLK rising edges during reset will be skewed by 1-2 clocks based on the internal sampling of reset.

Figure 1. Reset Timing Diagram

Table 8. Switching Characteristics—SPI

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		62	—	—	ns
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, CSB Rise to SDO Tristate	t_{d3}		—	—	20	ns
Setup Time, CSB to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, CSB to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Chip Selects	t_{cs}		220	—	—	ns
SDI to SDITHRU Propagation Delay	t_{d4}		—	4	10	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_{DDD} - 0.4$ V, $V_{IL} = 0.4$ V.
2. Characteristics for outputs specified with CL = 20 pF.

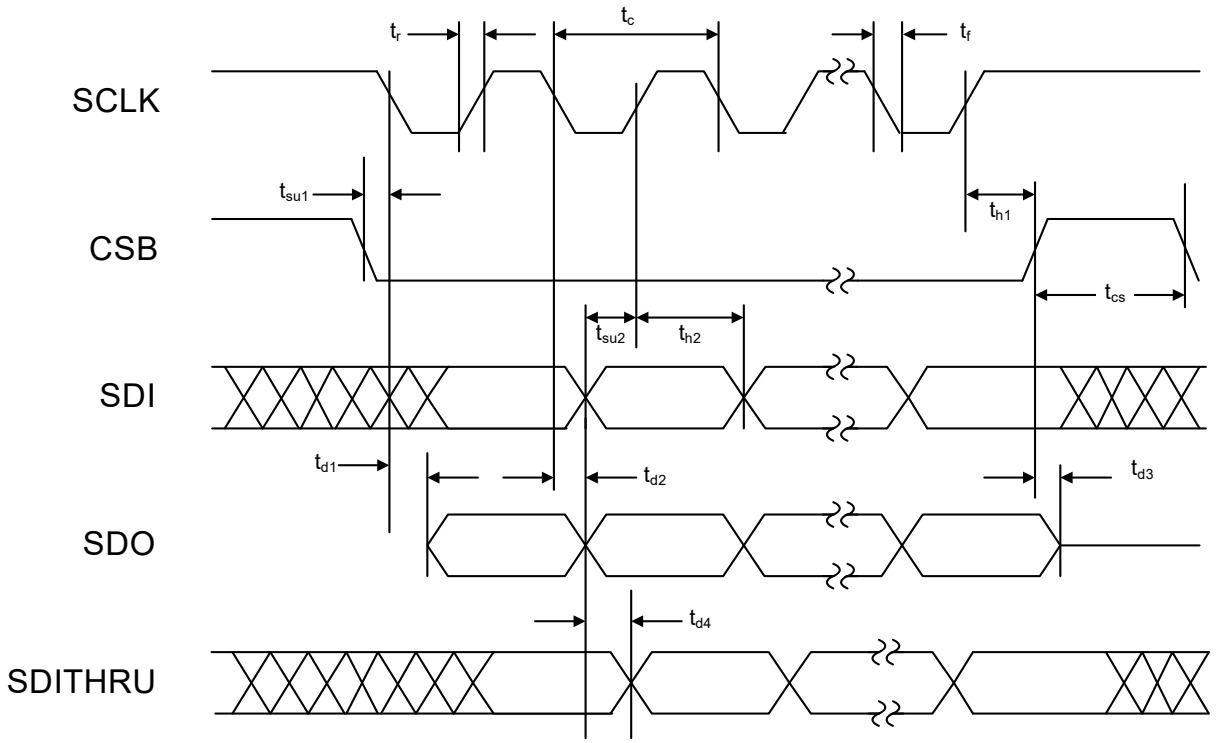


Figure 2. SPI Timing Diagram

Table 9. Switching Characteristics—PCM Highway Interface[1]

Parameter	Symbol	Test Condition	Min[2]	Typ[2]	Max[2]	Unit
PCLK Period	t_p		122	—	1953	ns
PCLK Jitter Tolerance	t_{jitter}				8	ns_{RMS}
Valid PCLK Inputs[3]			— — — — — — — —	512 768 1.024 1.536 1.544 2.048 4.096 8.192	— — — — — — — —	kHz kHz MHz MHz MHz MHz MHz MHz
FSYNC Period[4]	t_{fs}		—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
FSYNC Jitter Tolerance[5]	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tri-state[6]	t_{d3}		—	—	20	ns
Setup Time, FSYNC to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, FSYNC to PCLK Fall	t_{h1}		20	—	—	ns
Setup Time, DRX to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, DRX to PCLK Fall	t_{h2}		20	—	—	ns
FSYNC Pulse Width	t_{wfs}		t_p	—	125 µs–t_p	

Notes:
1. Characteristics for outputs specified with CL = 20 pF.
2. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} – V_{I/O} – 0.4$ V, $V_{IL} = 0.4$ V.
3. A constant PCLK and FSYNC are required.
4. FSYNC source is assumed to be 8 kHz under all operating conditions.
5. FSYNC Jitter Tolerance relative to PCLK.
6. Specification applies to PCLK fall to DTX tristate when that mode is selected.

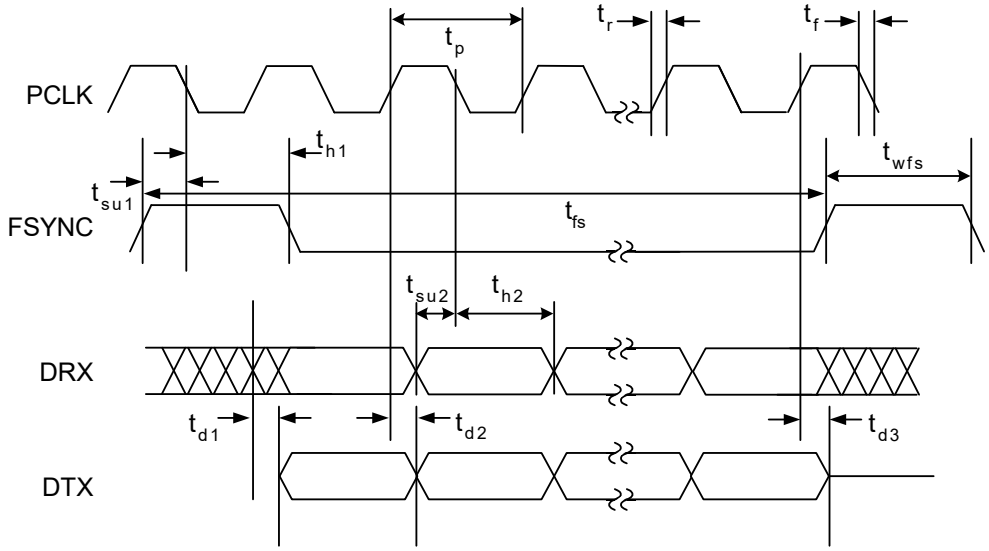


Figure 3. PCM Highway Interface Timing Diagram

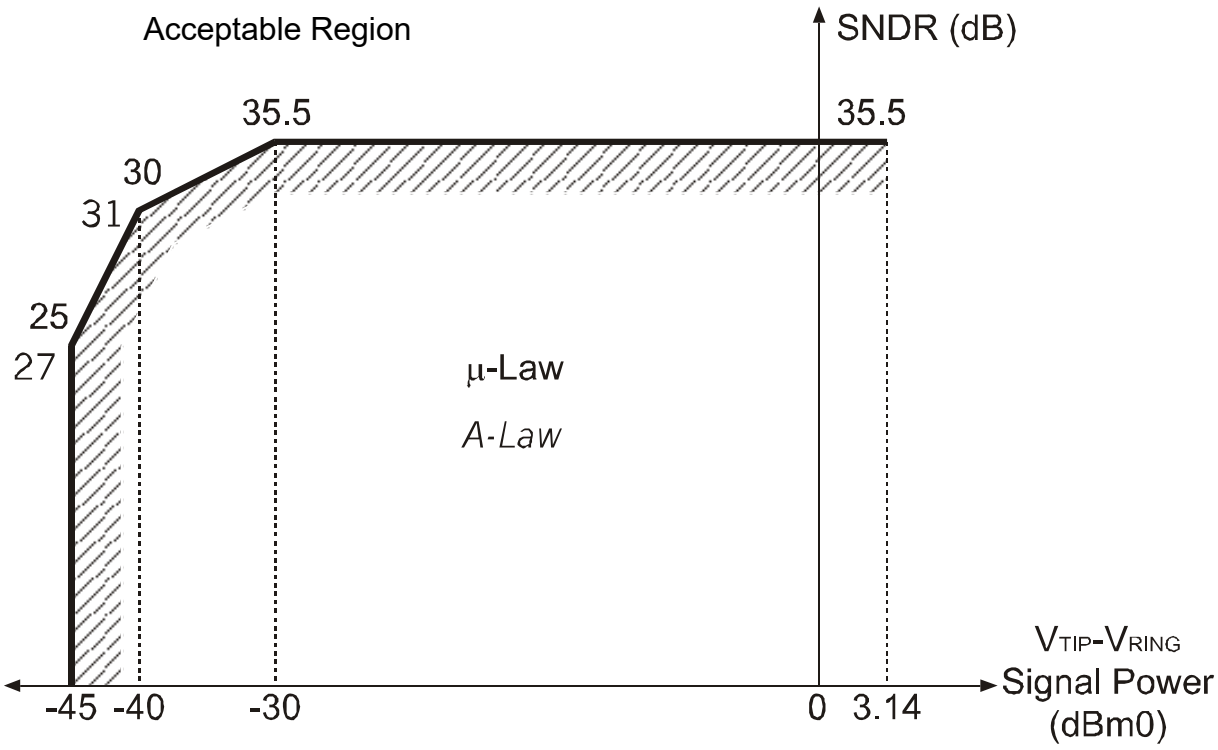


Figure 4. Transmit and Receive Path SNDR

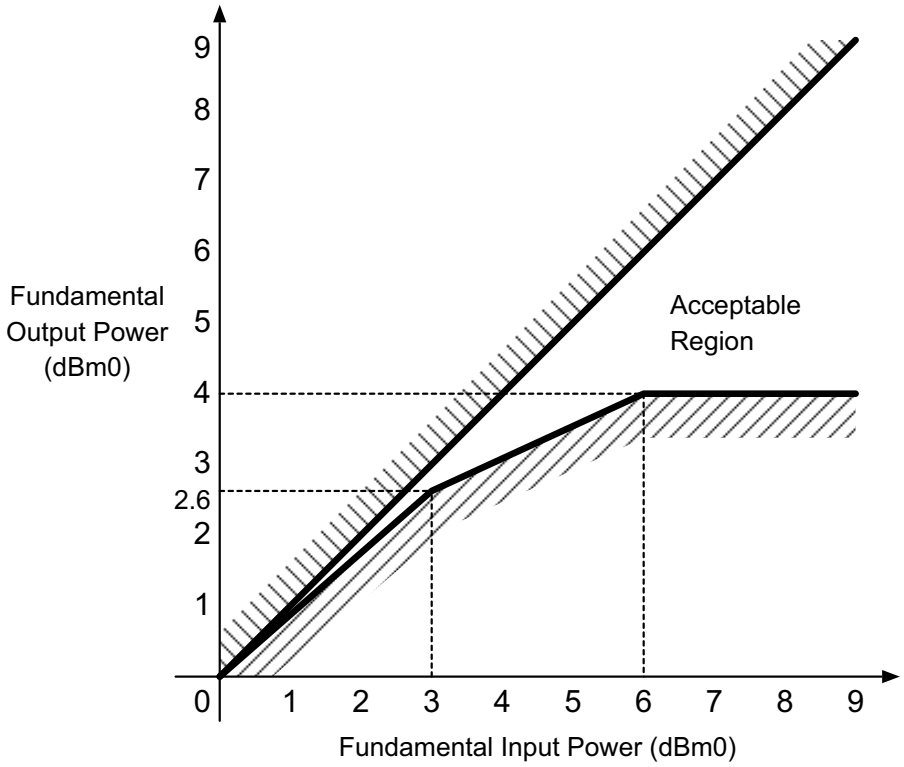


Figure 5. Overload Compression Performance

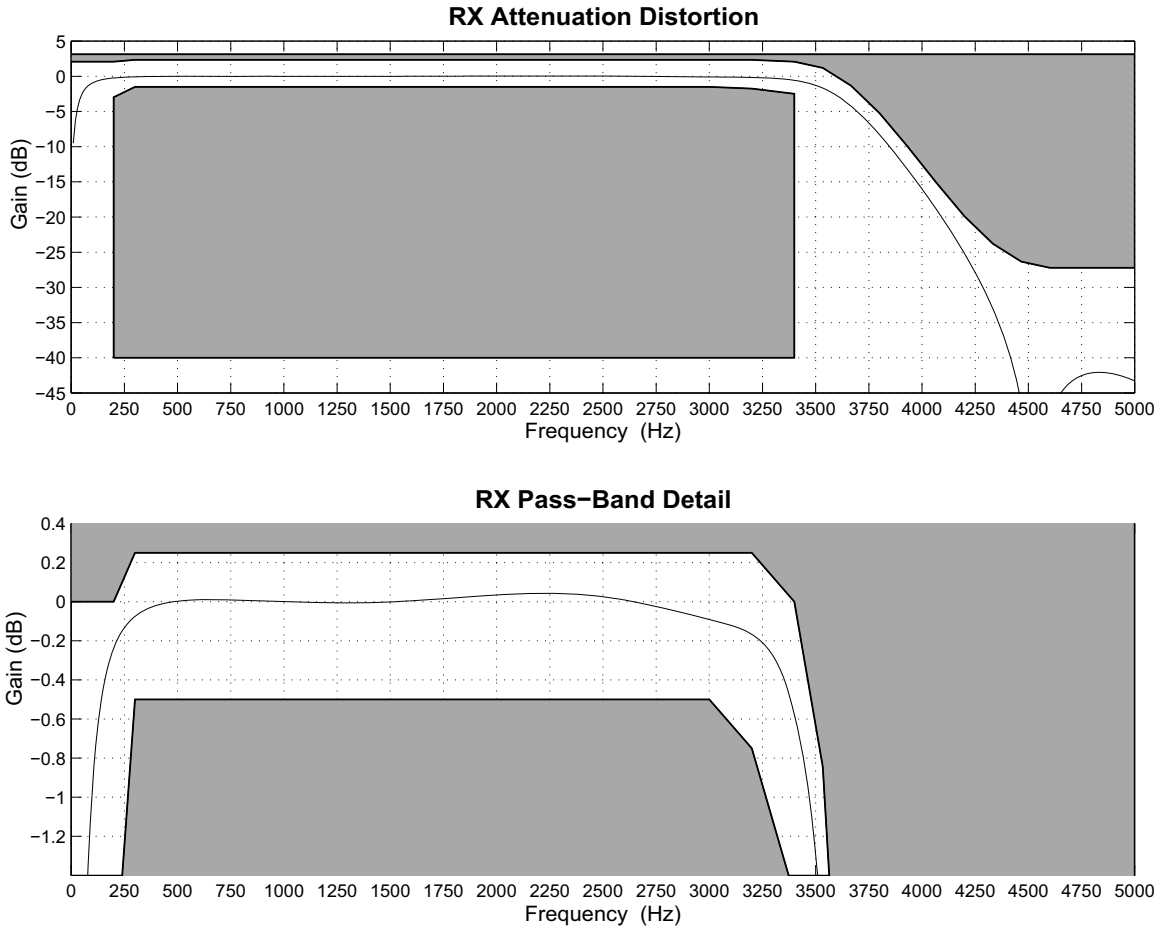


Figure 6. Receive Path Frequency Response

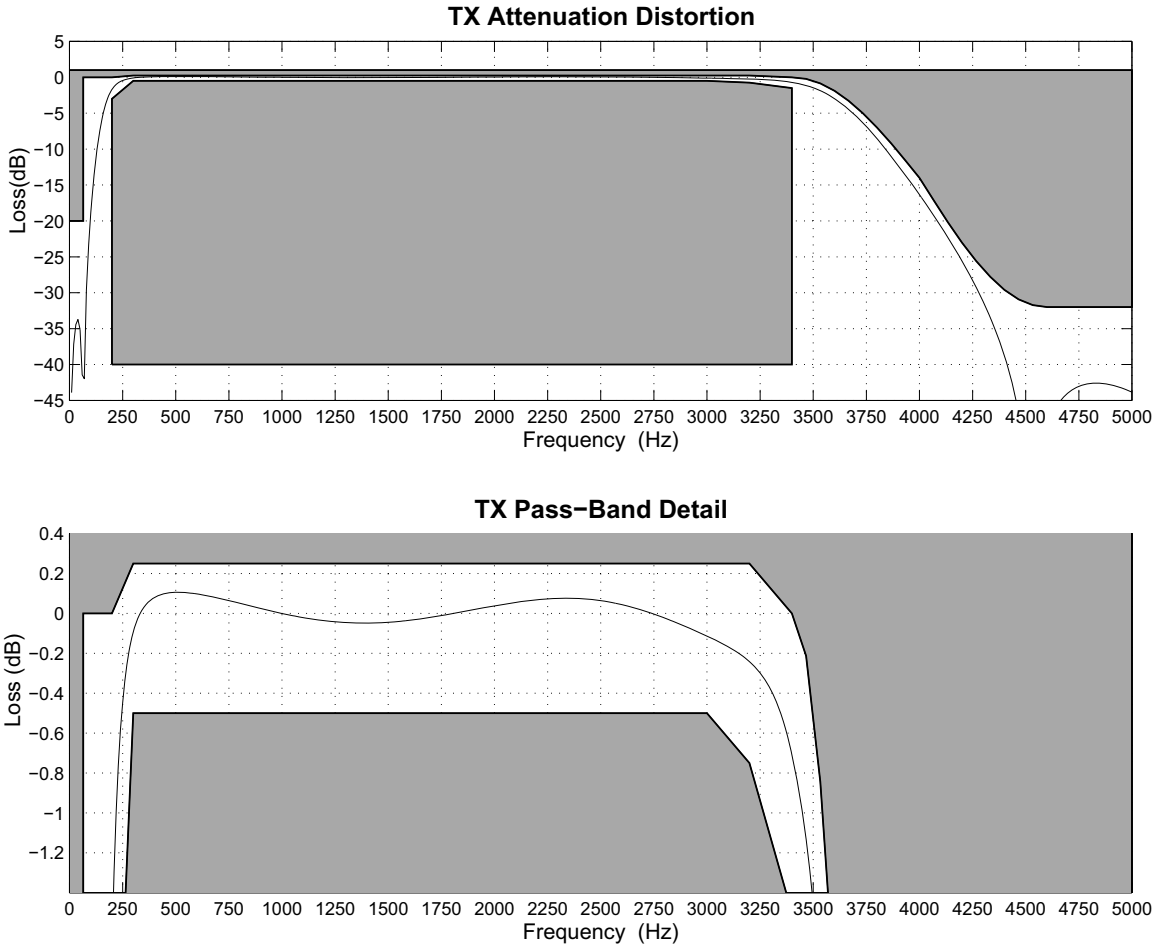


Figure 7. Transmit Path Frequency Response

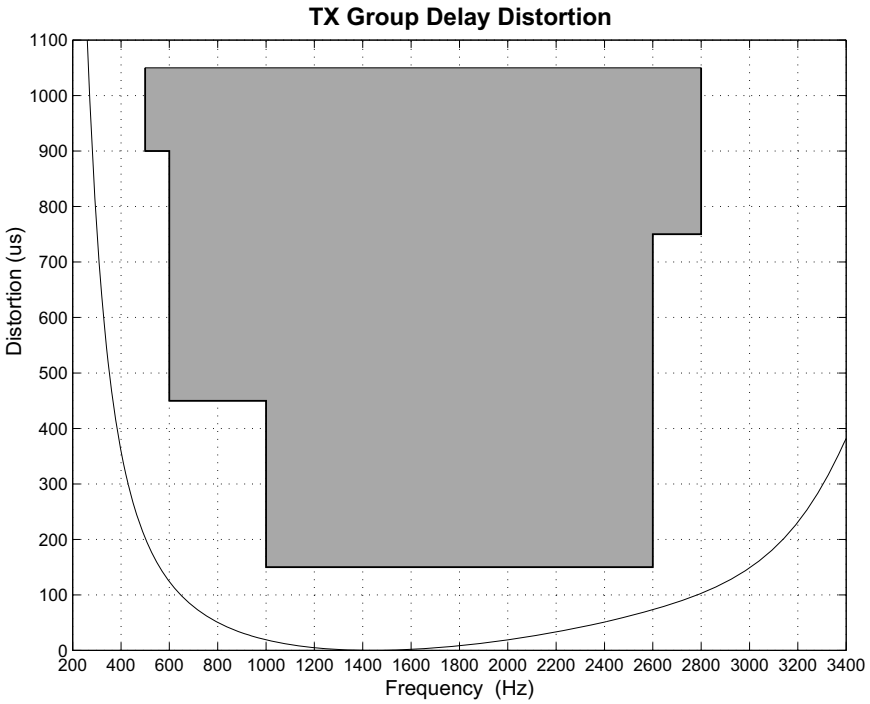


Figure 8. Transmit Group Delay Distortion

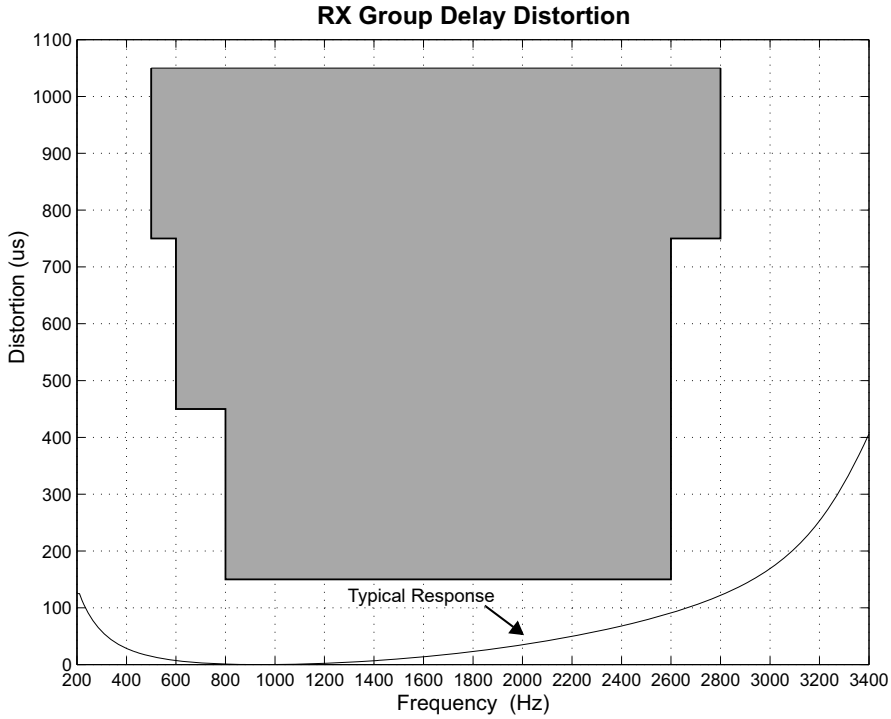


Figure 9. Receive Group Delay Distortion

Table 10. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Typical* QFN-60	θ_{JA}		42	°C/W
	θ_{JB}		19	
	θ_{JC}		12	
Thermal Resistance, Typical* QFN-47	θ_{JA}		48	°C/W
	θ_{JB}		22	
	θ_{JC}		14	
Maximum Junction Temperature, QFN-60, QFN-47(Linefeed Die)	T_{JHV}	Continuous	145	°C
Maximum Junction Temperature QFN-60,QFN-47 (Low Voltage Die)	T_{JLV}		125	°C

***Note:**

1. The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed correctly. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane. Thermal resistance values are empirical measurements taken from Skyworks Solutions EVBs.
2. Operation of the Si3226x above 125 °C junction temperature may degrade device reliability.
3. The Si3226x linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold. The thermal shutdown threshold should normally be set to 145 °C; when in the ringing state with cadence the thermal shutdown may be set to 200 °C. For optimal reliability, long term operation of the Si3226x linefeed above 150 °C junction temperature should be avoided.

Table 11. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Value	Unit
Storage Temperature Range	T_{STG}		–55 to 150	°C
Continuous Power Dissipation[2,3] QFN-60	P_D	T_A = 85 °C	1.4	W
Continuous Power Dissipation QFN-47	P_D	T_A = 85 °C	1.25	W
Supply Voltage	V_{DDD}, V_{DDA}		–0.5 to 4.0	V
Digital Input Voltage	V_{IND}		–0.3 to 3.6	V
Battery Supply Voltage[4], Si32260	V_{BAT}		+0.4 to –115	V

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.
2. Operation of the Si32260/1 low voltage die above 125 °C junction temperature may degrade device reliability.
3. Si32260/1 linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold.
4. The dv/dt of the voltage applied to the V_{BAT} pins must be limited to 10 V/µs.
5. Specification requires circuit for surge event as shown in typical application circuit. Refer to “AN381: Si3226x ProSLIC Designer’s Guide.”

Table 11. Absolute Maximum Ratings[1] (Continued)

Parameter	Symbol	Test Condition	Value	Unit
Battery Supply Voltage[4], Si32261	V_{BAT}		+0.4 to –142	V
TIP or RING Voltage, Si32260[5]	V_{TIP}, V_{RING}		+0.4 to –130	V
TIP or RING Voltage, Si32261[5]	V_{TIP}, V_{RING}		+0.4 to –142	V
TIP, RING Current	I_{TIP}, I_{RING}		±100	mA

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.
2. Operation of the Si32260/1 low voltage die above 125 °C junction temperature may degrade device reliability.
3. Si32260/1 linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold.
4. The dv/dt of the voltage applied to the V_{BAT} pins must be limited to 10 V/µs.
5. Specification requires circuit for surge event as shown in typical application circuit. Refer to “AN381: Si3226x ProSLIC Designer’s Guide.”

2. Typical Application Circuits

2.1. Flyback Tracking DC-DC Converter

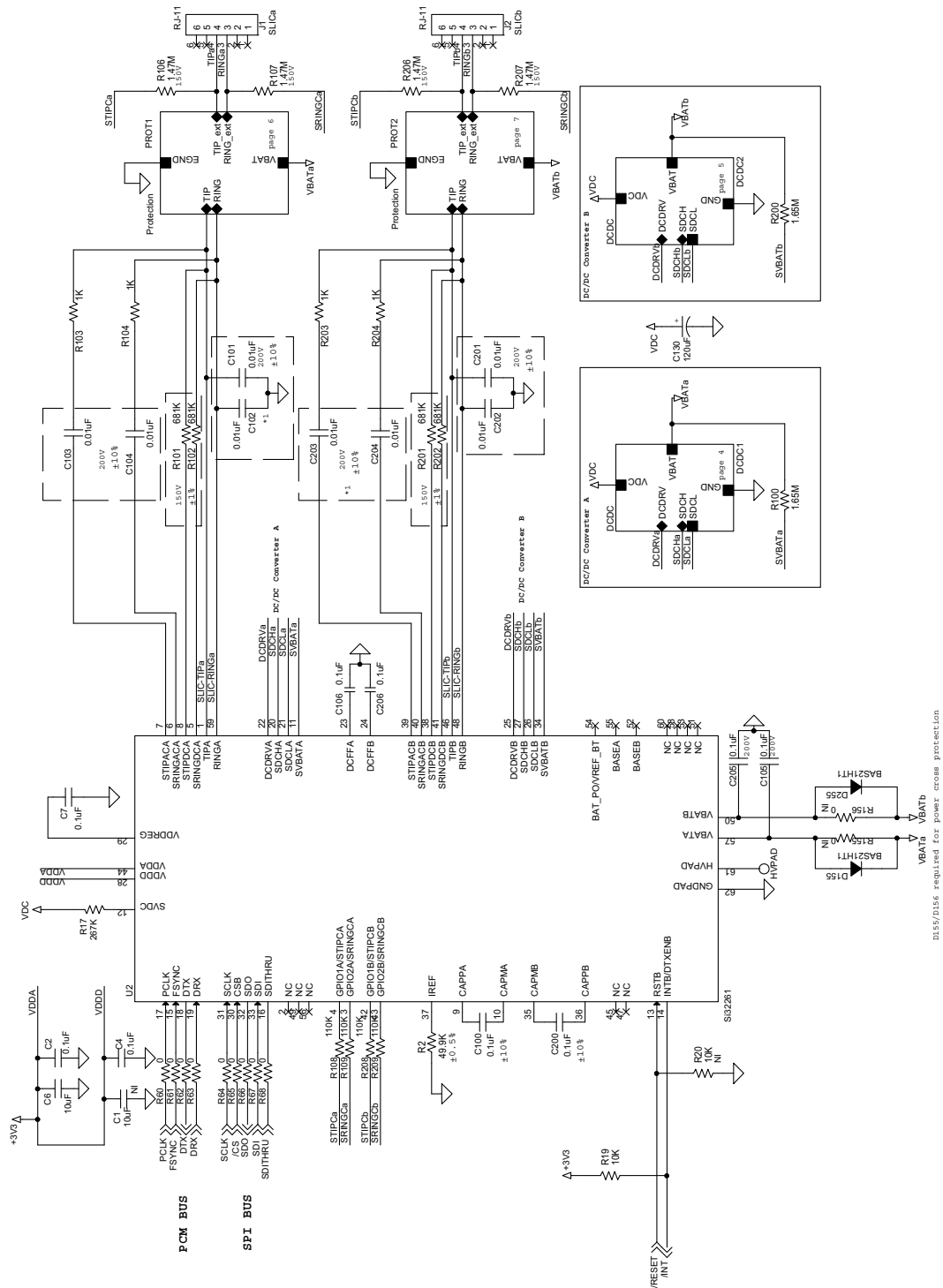


Figure 10. Flyback Tracking DC-DC Converter Top Level Schematic

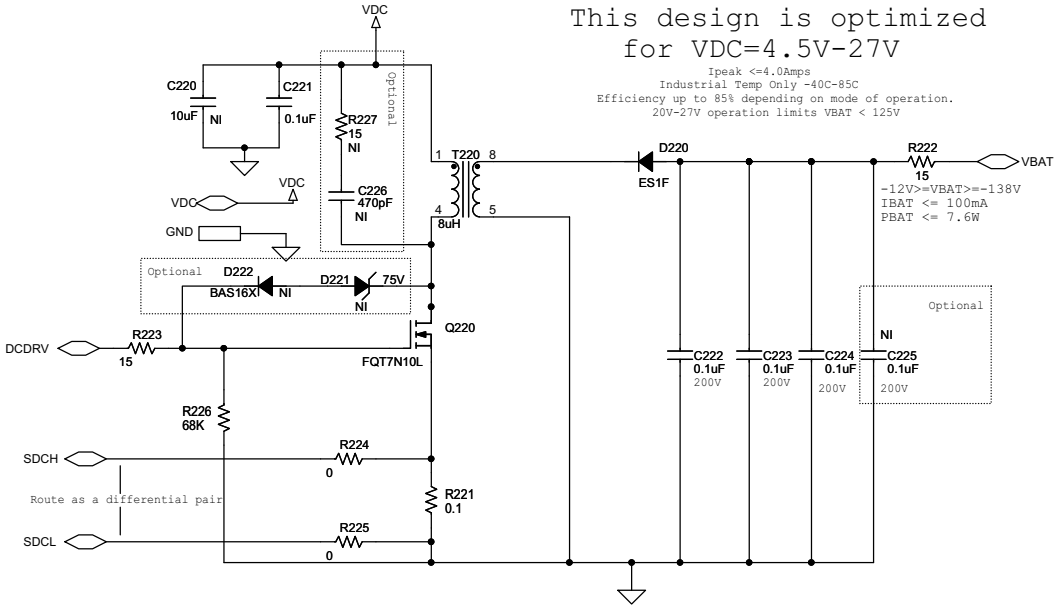


Figure 11. Flyback Tracking DC DC1

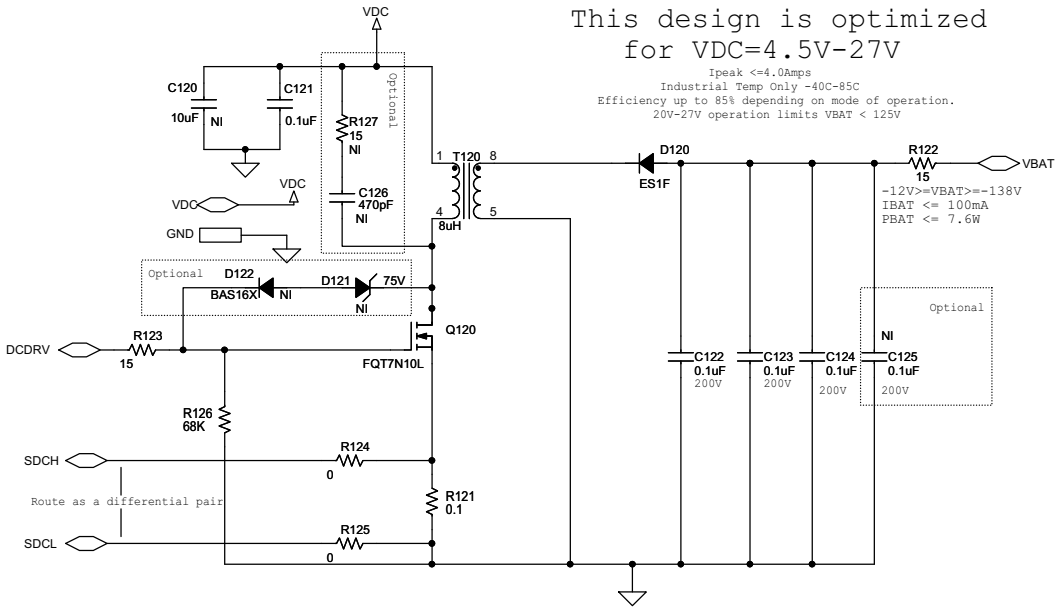


Figure 12. Flyback Tracking DC DC2

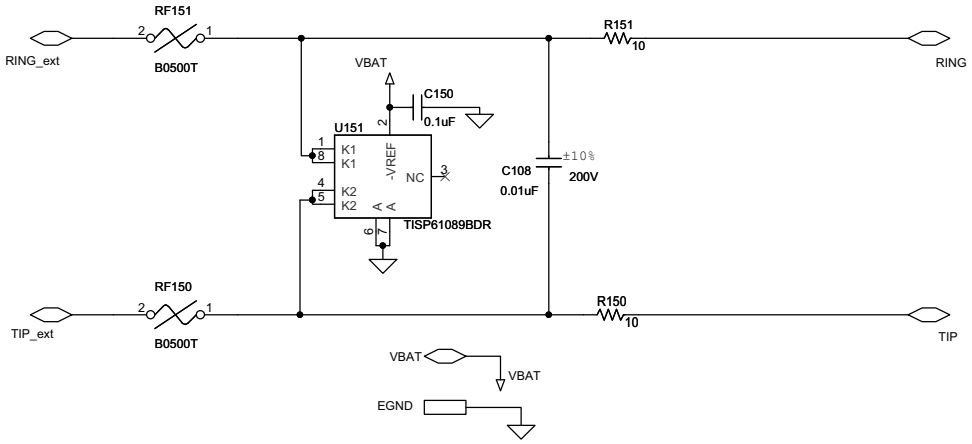


Figure 13. Flyback Protection 1

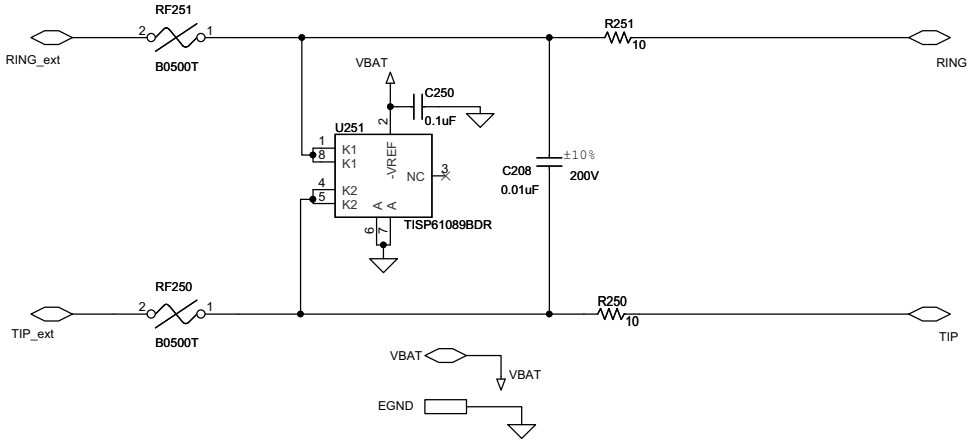


Figure 14. Flyback Protection 2

2.2. Low Cost Quasi Ćuk (LCQC)

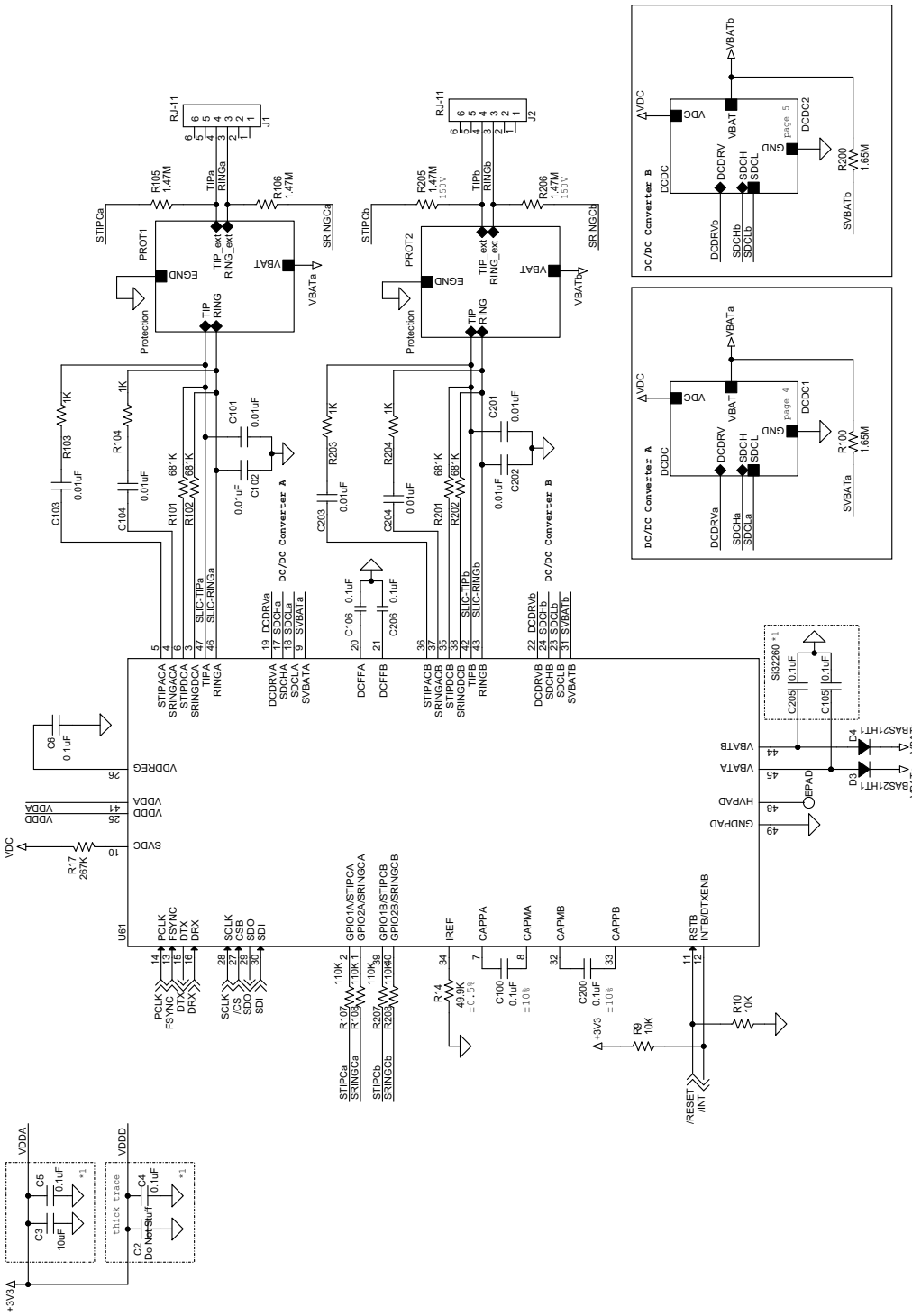


Figure 15. Top Level Schematic—Low Cost Quasi Ćuk (LCQC)

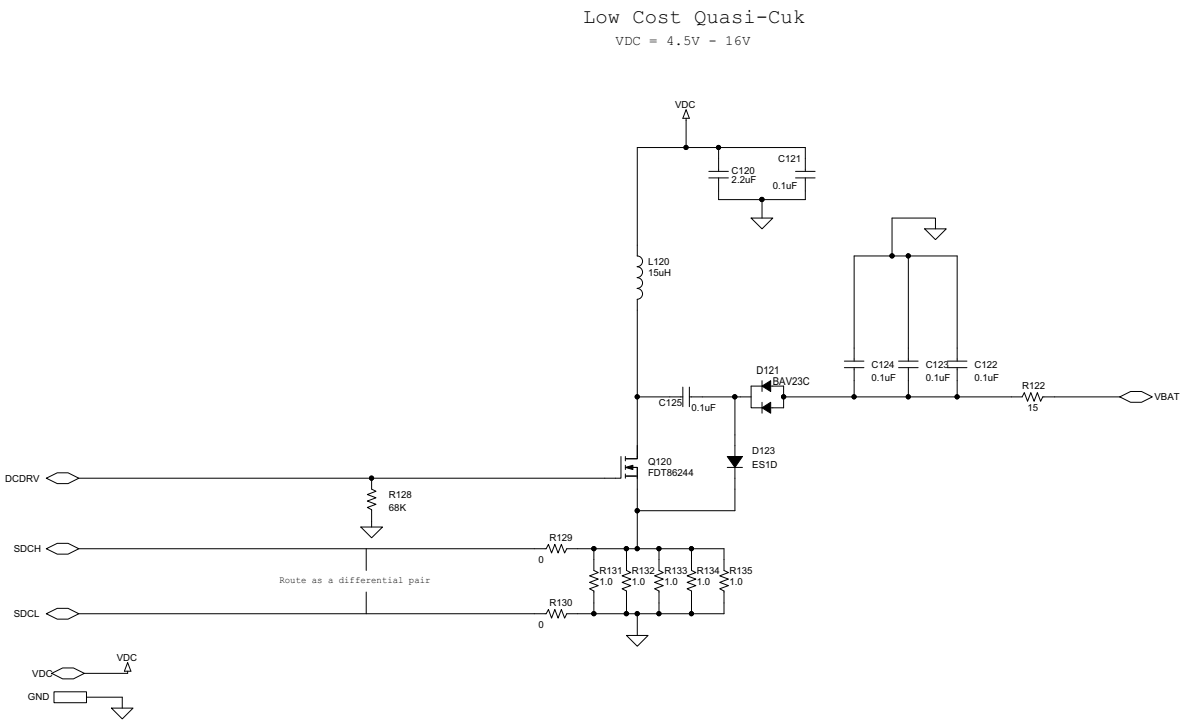


Figure 16. Low Cost Quasi Ćuk (LCQC) DC-DC 1

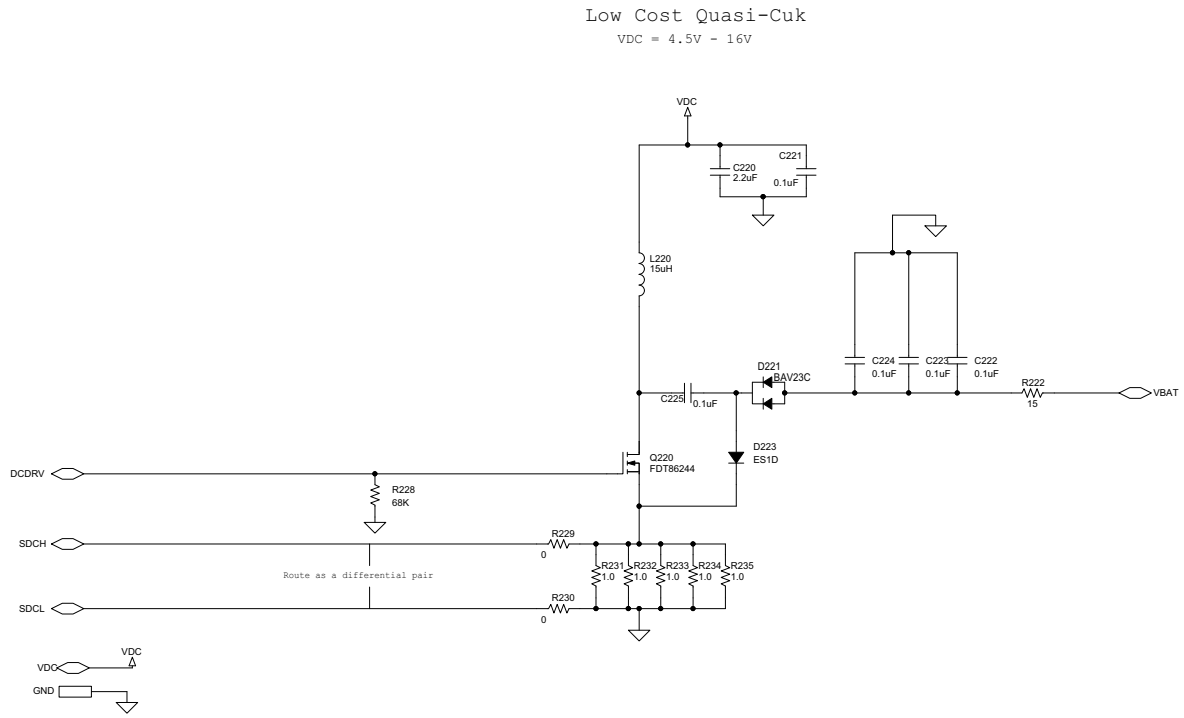


Figure 17. Low Cost Quasi Ćuk (LCQC) DC-DC 2

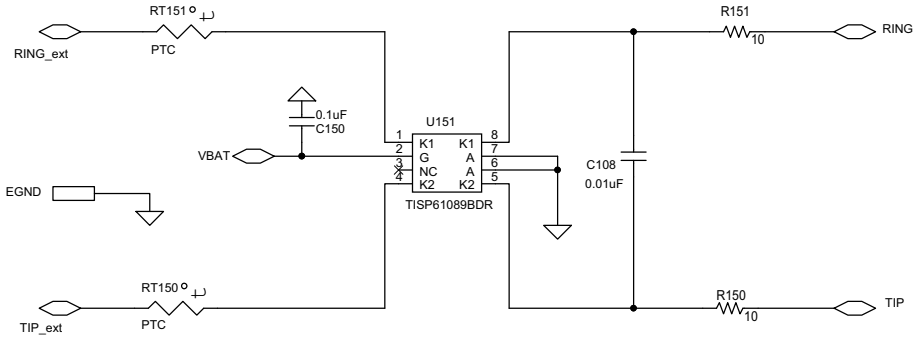


Figure 18. Low Cost Quasi Ćuk (LCQC) Protection 1

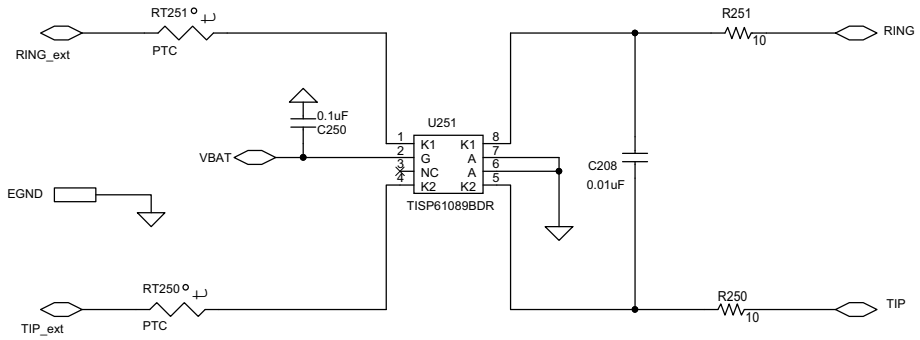


Figure 19. Low Cost Quasi Ćuk (LCQC) Protection 2

3. Bill of Materials

Table 12. Flyback Tracking DC-DC Converter Bill of Materials—Top Level

Reference	Description	Mfr Part Number	Manufacturer
C1 (NI)	CAP, 10 µF, 6.3 V, ±20%, X5R, 0603	C0603X5R6R3-106M	Venkel
D2 (NI)	DIO, DUAL Common ANODE, 200 V, 400 mA, SOT23	BAV23A	Diodes Inc.
D155 D255 (NI)	DIO, SINGLE, 250 V, 200 mA, SOT323	BAS21HT1	On Semi
R20 (NI)	RES, 10K, 1/16W, ±5%, ThickFilm, 0402	CR0402-16W-103J	Venkel
C2 C4 C7 C100 C106 C200 C206	CAP, 0.1 µF, 10 V, ±10%, X7R, 0402	C0402X7R100-104K	Venkel
C6	CAP, 10 µF, 6.3 V, ±20%, X5R, 0603	C0603X5R6R3-106M	Venkel
C101 C102 C103 C104 C201 C202 C203 C204	CAP, 0.01 µF, 200 V, ±10%, X7R, 0805	C0805X7R201-103K	Venkel
C105 C205	CAP, 0.1 µF, 200V, ±20%, X7R, 1206	C1206X7R201-104M	Venkel
J1 J2	1 Port SMT RJ11	5555077-2	AMP
R2	RES, 49.9K, 1/16W, ±0.5%, ThickFilm, 0603	CR0603-16W-4992D	Venkel
R17	RES, 267K, 1/10W, ±1%, ThickFilm, 0805	CR0805-10W-2673F	Venkel
R19	RES, 10K, 1/16W, ±5%, ThickFilm, 0402	CR0402-16W-103J	Venkel
R60 R61 R62 R63 R64 R65 R66 R67 R68	RES, 0 Ω, 1A, ThickFilm, 0402	CR0402-16W-000	Venkel
R100 R200	RES, 1.65M, 1/10W, ±1%, ThickFilm, 0805	CR0805-10W-1654F	Venkel
R101 R102 R201 R202	RES, 681K, 1/10W, ±1%, ThickFilm, 0805	CR0805-10W-6813F	Venkel
R103 R104 R203 R204	RES, 1K, 1/10W, ±1%, ThickFilm, 0603	CR0603-10W-1001F	Venkel
R106 R107 R206 R207	RES, 1.47M, 1/8W, ±1%, ThickFilm, 1206	CR1206-8W-1474F	Venkel
R108 R109 R208 R209	RES, 110K, 1/16W, ±1%, ThickFilm, 0402	CR0402-16W-1103F	Venkel
R155 R156	RES, 0 Ω, 2A, ThickFilm, 0805	CR0805-10W-000	Venkel
U1	IC, Dual SLIC, Integrated Linefeed, PCM, Bat Tracking	Si32261-C-GM	Skyworks Solutions

Table 13. Flyback Tracking DC-DC Converter Bill of Materials—DC-DC

Reference	Description	Mfr Part Number	Manufacturer
C120 C220 (NI)	CAP, 10 µF, 25 V, ±20%, X7R, 1210	C1210X7R250-106M	Venkel
C125 C225 (NI)	CAP, 0.1 µF, 200 V, ±20%, X7R, 1206	C1206X7R201-104M	Venkel
C126 C226 (NI)	CAP, 470 pF, 100 V, ±10%, X7R, 0603	C0603X7R101-471K	Venkel
D121 D221 (NI)	DIO, ZENER, 75 V, 200 mW, SOD323	BZX384C75-V	Vishay
D122 D222 (NI)	DIO, SWITCH, 200mA, 75 V, SOD523	BAS16XV2T1G	On Semi
R127 R227 (NI)	RES, 15 Ω, 1/2W, ±5%, ThickFilm, 1210	CR1210-2W-150J	Venkel
C121 C221	CAP, 0.1 µF, 50 V, ±10%, X7R, 0603	C0603X7R500-104K	Venkel
C122 C123 C124 C222 C223 C224	CAP, 0.1 µF, 200 V, ±20%, X7R, 1206	C1206X7R201-104M	Venkel
C130	CAP, 120 µF, 63 V, ±20%, AL, 8X16MM, Low Impedance	EEUFC1J121	Panasonic
D120 D220	DIO, FAST, 300V, 1A, SMA	ES1F	Fairchild
Q120 Q220	TRANSISTOR, MOSFET, N-CHNL, 2.0W Switching, Logic Level, SOT223	FQT7N10L	Fairchild
R121 R221	RES, 0.1 Ω, 1/2W, ±1%, ThickFilm, 1210	LCR1210-R100F	Venkel
R122 R222	RES, 15 Ω, 1/2W, ±5%, ThickFilm, 1210	CR1210-2W-150J	Venkel
R123 R223	RES, 15 Ω, 1/16W, ±1%, ThickFilm, 0402	CR0402-16W-15R0F	Venkel
R124 R125 R224 R225	RES, 0 Ω, 1A, ThickFilm, 0402	CR0402-16W-000	Venkel
R126 R226	RES, 68K, 1/16W, ±5%, ThickFilm, 0402	CR0402-16W-683J	Venkel
T120 T220	TRANSFORMER, Flyback, 8.0uH Primary, 100nH Leakage, 1:3, 1 Tap, SMT	UTB01890s	UMEC

Table 14. Flyback Tracking DC-DC Converter Bill of Materials—Protection

C108 C208	CAP, 0.01 µF, 200 V, ±10%, X7R, 0805	C0805X7R201-103K	Venkel
C150 C250	CAP, 0.1 µF, 200 V, ±20%, X7R, 1206	C1206X7R201-104M	Venkel
RF150 RF151 RF250 RF251	FUSE, 0.5A, 600 V	B0500T	Bourns
R150 R250	RES, 10 Ω, 1/10W, ±1%, ThickFilm, 0805	CR0805-10W-10R0F	Venkel
R151 R251	RES, 10 Ω, 1/10W, ±1%, ThickFilm, 0805	CR0805-10W-10R0F	Venkel
U151 U251	SLIC Protector	TISP61089BDR	Bourns

Table 15. Low Cost Quasi Ćuk (LCQC) DC-DC Converter Bill of Materials—Top Level

Reference	Description	Mfr Part Number	Manufacturer
C2 (NI)	10UF, 6.3V, 20%, X5R, 0603	C0603X5R6R3-106M	Venkel
C3	10UF, 6.3V, 20%, X5R, 0603	C0603X5R6R3-106M	Venkel
C4 C5 C6 C100 C106 C200 C206	0.1UF, 10V,10%, X7R, 0402	C0402X7R100-104K	Venkel
C105 C205	0.1UF, 250V, 10%, X7T, 0805	C2012X7T2E104K	Tdk Corporation
C101 C102 C103 C104 C201 C202 C203 C204	.01UF, 200V, 10%, X7R, 0805	C0805X7R201-103K	Venkel
R107 R108 R207 R208	110K 1%	CR0402-16W-1103F	Venkel
R14	49.9K, 1/16W, 0.5%, 0603	CR0603-16W-4992D	Venkel
R9 R10	10K, 1/16W, 5%, 0402	CR0402-16W-103J	Venkel
R100 R200	1.65M, 1/10W, 1%, 0805	CR0805-10W-1654F	Venkel
R105 R106 R205 R206	1.47M, 1/8W, 1%, 1206	CR1206-8W-1474F	Venkel
R103 R104 R203 R204	1K, 1/16W, 1%, 0402	CR0402-16W-1001F	Venkel
R101 R102 R201 R202	681K, 1/10W, 1%, 0805	CR0805-10W-6813F	Venkel
R17	267K, 1/16W, 1%, 0402	CR0402-16W-2673F	Venkel
D3 D4	BAS21HT1	BAS21HT1	On Semi
J1 J2	RJ-11	5555077-2	Tyco
U61	SI32260	SI32260-C-GM2	Skyworks Solutions

Table 16. Low Cost Quasi Ćuk (LCQC) DC-DC Converter Bill of Materials—DC-DC

Reference	Description	Mfr Part Number	Manufacturer
C120 C220	2.2uf, 16V,20%, X7R, 0805	C0805X7R160-225M	Venkel
C121 C221	0.1uf, 25V,20%, X7R, 0603	C0603X7R250-104M	Venkel
C122 C123 C124 C125 C222 C223 C224 C225	0.1uf, 250V, 10%, X7T, 0805	C2012X7T2E104K	TDK Corporation
D121 D221	BAV23C	BAV23C	Diodes Inc.
D123 D223	ES1D	ES1D	Diodes Inc.
L120 L220	15uH, 1.6A, 20%, shielded	NR 6028T 150M	Taiyo Yuden
Q120 Q220	FDT86244, 2.8A, 150V N-CHAN	FDT86244	Fairchild
R128 R228	68k, 1/16W, 5%, 0402	CR0402-16W-683J	Venkel
R129 R130 R229 R230	0 ohm, 1A, 0402	CR0402-16W-000	Venkel
R131 R132 R133 R134 R135 R231 R232 R233 R234 R235	1.0 ohm, 1/16W, 1%, 0402	CR0402-16W-1R00F	Venkel
R122 R222	15 ohm, 1/10W, 1%, 0805	CR0805-10W-15R0F	Venkel

Table 17. Low Cost Quasi Ćuk (LCQC) DC-DC Converter Bill of Materials—Protection

Reference	Description	Mfr Part Number	Manufacturer
C108 C208	.01uf, 200V, 10%, X7R, 0805	C0805X7R201-103K	Venkel
C150 C250	0.1uf, 250V, 10%, X7T, 0805	C2012X7T2E104K	TDK Corporation
R150 R151 R250 R251	10 ohm, 1%, 0805	CR0805-10W-10R0F	Venkel
RT150 RT151 RT250 RT251	PTC, 3A, 250V	MF-SM013/250V	Bourns
U151 U251	TISP61089BDR	TISP61089BDR	Bourns

4. Functional Description

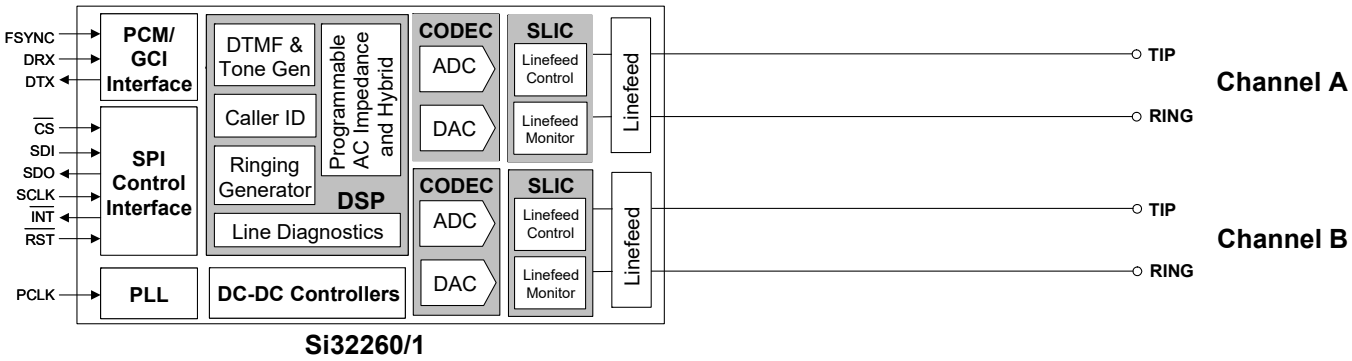


Figure 20. Functional Block Diagram

The Si32260/1 dual ProSLIC devices provide all SLIC, codec, DTMF detection, and signal generation functions needed for two complete analog telephone interfaces. They perform all battery, over-voltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions, and also support extensive metallic loop testing capabilities.

The Si32260/1 both provide a standard voice-band (200 Hz–3.4 kHz) audio codec and, optionally, an audio codec with both wideband (50 Hz–7 kHz) and standard voiceband modes. The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality while the standard voice-band mode provides standard telephony audio bandwidth.

The Si32260/1 devices incorporate two programmable dc-dc converter controllers that can operate in either battery tracking mode or a shared rail mode. In both the battery tracking and the shared rail modes the dc-dc converter controllers react to line conditions to provide the optimal battery voltage required for each line-state. Multiple Si32260/1 devices can also operate from fixed rail supplies controlled either by one of the integrated dc-dc controllers or by an external dc-dc controller. The Si32260/1 devices are available with voltage ratings of –110 or –140 V to support a wide range of ringing voltages. See Section "8. Ordering Guide," on page 45 for the voltage rating of each version.

Programmable on-hook voltage, programmable offhook loop current, reverse battery operation, loop or ground start operation, and on-hook transmission are supported. Loop current and voltage are continuously monitored by an integrated monitoring ADC. The Si32260/1 dual ProSLIC devices support balanced and unbalanced 5 REN ringing with or without a programmable dc offset, and can operate in low power ringing and adaptive ringing modes. The available offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements.

5. FXS Features

5.1. DC Feed Characteristics

ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics.

When in the active state, the ProSLIC operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in Figure 21. The constant-voltage region has a low resistance, typically 160 Ω. The constant-current region approximates infinite resistance.

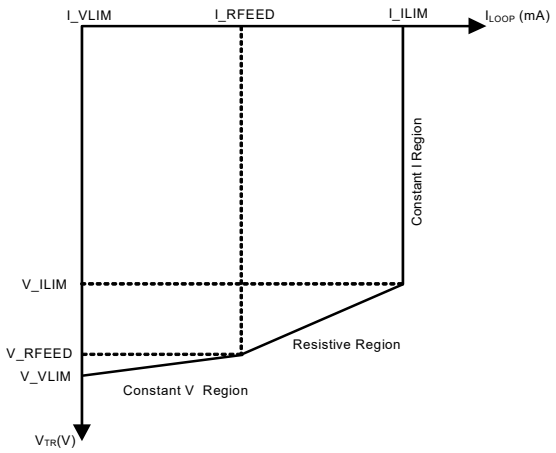


Figure 21. Dual ProSLIC DC Feed Characteristics

5.2. Linefeed Operating States

The linefeed interface includes nine different register-programmable operating states as listed in Table 18. The Open state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

5.3. Line Voltage and Current Monitoring

The ProSLIC continuously monitors the TIP, RING, and battery voltages and currents via an on-chip ADC and stores the resulting values in individual RAM locations. Additionally, the loop voltage (V_{TIP}–V_{RING}), loop current, and longitudinal current values are calculated based on the TIP and RING measurements and are stored in unique register locations for further processing. The ADC updates all registers at a rate of 2 kHz or greater.

5.4. Power Monitoring and Power Fault Detection

The Si32260/1 line monitoring functions are used to continuously protect against excessive power conditions. The Si32260/1 contains on-chip, analog sensing diodes that turn off the device when a preset temperature threshold is exceeded.

If the Si32260/1 detects a fault condition or overpower condition, it automatically sets that line to the open state and generates a "power alarm" interrupt.

The interrupt can be masked, but masking the automatic transition to open is not recommended.

The various power alarms and linefeed faults supporting automatic intervention are described below.

1. Total power exceeded.
2. Excessive foreign current or voltage on TIP and/or RING.
3. Thermal shutdown event.

5.5. Thermal Overload Shutdown

If the die temperature exceeds the maximum junction temperature threshold (TJmax) of 145 or 200 °C, depending on the operating state, the device has the ability to shut itself down to a low-power state without user intervention.

Table 18. Linefeed Operating States

Linefeed State	Description
Open	Output is high-impedance and all line supervision functions are powered down. Audio is not transmitted. This is the default state after powerup or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in line diagnostics mode as a high impedance state during linefeed testing. A power fault condition may also force the device into the open state.
Forward Active Reverse Active	Linefeed circuitry and audio are active. In Forward Active state, the TIP lead is more positive than the RING lead; in Reverse Active state, the RING lead is more positive than the TIP lead. Loop closure and ground key detect circuitry are active.
Forward OHT Reverse OHT	Provides data transmission during an on-hook loop condition (e.g., transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the TIP lead is more positive than the RING lead; in Reverse OHT state, the RING lead is more positive than the TIP lead.
TIP Open	Provides an active linefeed on the RING lead and sets the TIP lead to high impedance (>400 kΩ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.
RING Open	Provides an active linefeed on the TIP lead and sets the RING lead to high impedance (>400 kΩ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.
Ringing	Drives programmable ringing signal onto TIP and RING leads with or without dc offset.
Line Diagnostics	The channel is put into diagnostic mode. In this mode, the channel has special diagnostic resources available.

5.6. Loop Closure Detection

The Si32260/1 provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two unique thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status, and a maskable interrupt bit is also provided.

5.7. Ground Key Detection

The Si32260/1 provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two unique thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status, and a maskable interrupt bit is also provided.

5.8. Ringing Generation

The Si32260/1 provides the ability to generate a programmable sinusoidal or trapezoidal ringing waveform, with or without dc offset. The ringing frequency, wave shape, cadence, and offset are all register-programmable. Three ringing modes are supported: balanced, unbalanced, and low-power ringing (LPR). Figure 22 illustrates the fundamental differences between the three ringing modes.

The dual ProSLIC's adaptive ringing capability allows further power savings to be realized in systems designed for long loop applications. In a long loop system, it may be necessary to generate a large ringing voltage to ensure that sufficient voltage is presented to a phone at the far end of the loop. However, in situations when a short loop is connected to an FXS interface that was designed with the ability to ring long loops, the large ringing voltage in combination with a low resistance load will result in excessive and unnecessary power consumption. Skyworks Solutions' Si32260/1 dual ProSLICs eliminate this unnecessary power consumption with their adaptive ringing capability. The ProSLIC automatically senses when excessive power is being consumed in the line feed circuit (due to the lower resistance of a short loop) and will iteratively reduce the ringing amplitude to a voltage that is appropriate for the load.

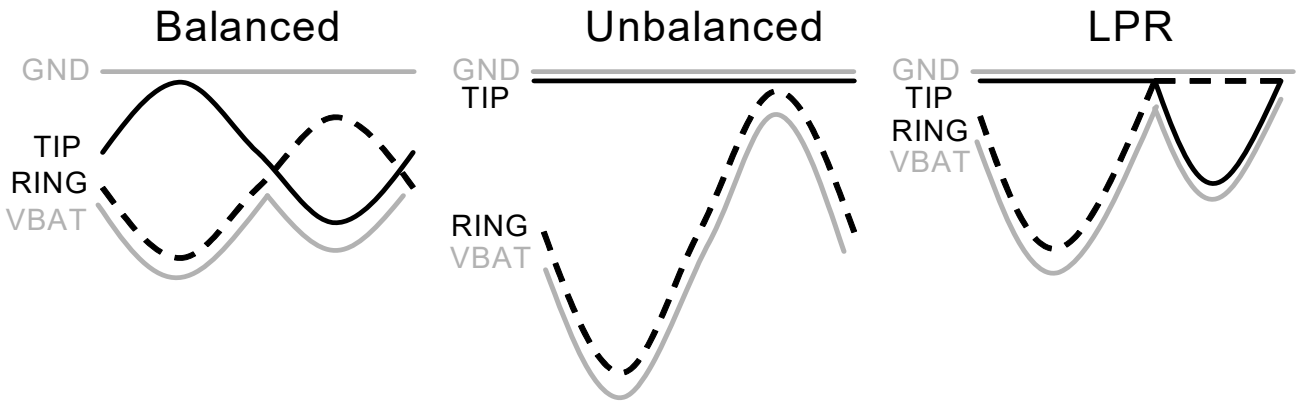


Figure 22. Ringing Modes

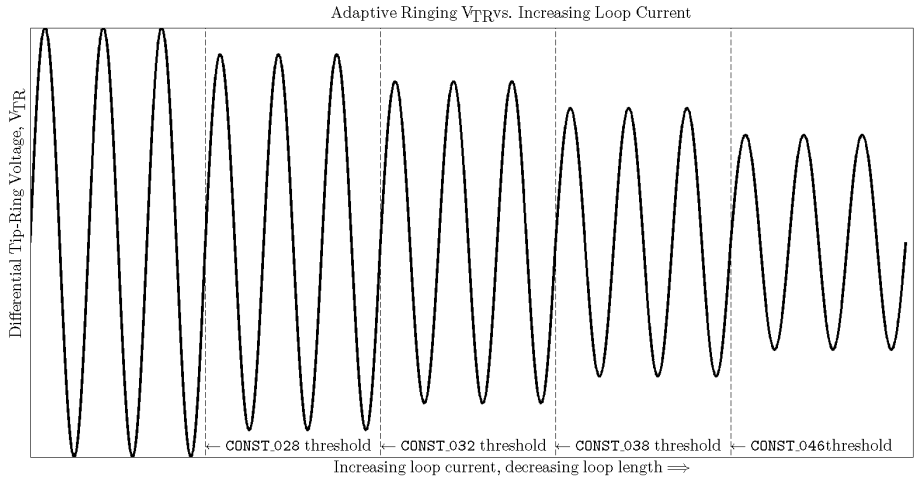


Figure 23. Adaptive Ringing

5.9. Polarity Reversal

The Si32260/1 supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

5.10. Two-Wire Impedance Synthesis

The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Si32260/1 to the reference impedance. Most real or complex two-wire impedances can be generated by using the coefficient generator software to simulate the desired line conditions and generate the required register coefficients.

5.11. Transhybrid Balance Filter

The trans-hybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path. The coefficient generator software is used to optimize the filter coefficients.

5.12. Tone Generators

The Si32260/1 includes two digital tone generators that allow a wide variety of single- or dual-tone frequency and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.

5.13. DTMF Detection

The Dual ProSLIC performs DTMF detection.

5.14. Pulse Metering

The pulse metering system for the Si32260/1Si32260/1 is designed to inject a 12 or 16 kHz billing tone into the audio path with maximum amplitude of 0.5 V_{RMS} at TIP and RING into a 200 Ω ac load impedance. The tone is generated in the DSP via a table lookup that guarantees spectral purity by not allowing drift. The tone will ramp up until it reaches a host-programmed threshold, at which point it will maintain that level until instructed to ramp down, thus creating a trapezoidal envelope.

See AN381 for additional details and considerations on Pulse Metering.

5.15. DC-DC Controller

The Si3226x integrates two dc-dc controllers that can be used to control external dc-dc converters to generate high voltage supplies to the SLIC channels.

The integrated line feeds are designed to work with either a single tracking high voltage input, one for each channel, or with two high voltage supplies shared by both channels.

In tracking mode, the VBATa and VBATb inputs are each directly connected to the high voltage output of two tracking dc-dc converters, one for channel A and one for channel B. In tracking mode, the VBAT voltage for each channel is optimized to minimize power consumption by closely tracking the SLIC state, even tracking the ringing waveforms (see section 2.1 for schematics).

In shared supply mode, a single flyback dc-dc converter generates two rails using two taps on the dc-dc converter's transformer. External power offloading transistors are used to lower the power dissipated inside the Si3226x device by shunting excess power away. In tracking shared supply (TSS) mode, in a two channel implementation, the dc-dc converter is controlled by the integrated dc-dc controller which allows the high voltage and low voltage outputs from the dc-dc converter to track the combined state of the two channels of the Si3226x ProSLIC, including the ringing waveforms. Using the same schematic, the TSS mode of operation reduces system power consumption significantly when compared to typical fixed rail shared supply designs (see section 2.2 for schematics).

Both of the dc-dc controller outputs DCDRVa/b are driven by an internal charge pump which allows them to connect directly to the gate of the MOSFET switch of a flyback (transformer based) dc-dc converter. This connection eliminates the need for the MOSFET pre-drive circuit that is required when VTH is greater than VDD. See Table 7.

5.16. Wideband Audio

The Si32260/1 dual ProSLIC devices support a software-selectable wideband (50 Hz–7 kHz) and narrowband (200 Hz–3.4 kHz) audio codec. The wideband mode provides an expanded audio band at a 16-bit, 16 kHz sample rate for enhanced audio quality while maintaining standard telephony audio compatibility. In wideband operation, two time slots are used to transmit the wideband signal and each slot contains 8-bits of the 16-bit sample. These two time slots are transmitted and received half a frame apart, but within the same 8 kHz frame.

5.17. In-Circuit and Metallic Loop Testing (MLT)

A rich set of features is provided for in-circuit testing of the FXS system and the connected telephone line (MLT):

- Tone generators
- Audio diagnostic filters
- Digital and analog loop-back modes
- Internal test load
- Monitor ADC
- DSP algorithms

Using these facilities, it is possible to test the Si32260/1's dc-dc converter, codec, line-feed, PCM bus interface, DSP, SPI bus interface, and call progress state-machine as well as testing the connected telephone line and external protection circuitry.

The audio diagnostic filters on the FXS are intended to provide programmable filtering of the TX digital audio signal and calculate the peak and/or average signal power of the filters' outputs. The signal powers are then compared to programmable thresholds. The programmable filters can be used to band-pass filter a certain tone or notch out certain tones, so that the signal power measurements are frequency selective. This filtering is useful in a telephony system because it can measure harmonic distortion, intermodulation, noise, etc.

The Si32260/1 incorporates an internal test load with a 2.2 kΩ nominal value that can be connected across Tip/Ring (Figure 24). The audio diagnostics system and built-in test load can be used to test the FXS interface (Si32260/1) itself without requiring an external load, a connected line, or any relays. This facility can be used for production and in-service testing of such things as:

- Dial tone draw/break
- Audio quality measurements
- Pulse digit detection
- DC feed
- Ringtrip
- Polarity reversal
- Transmission loss

MLT, e.g., GR-909, is facilitated by the built-in DSP, monitor ADC, and test load. They provide the ability to detect multiple fault conditions within the CPE as well as on the Tip/Ring pair (T-R). Thirteen different measured and/or calculated parameters are reported by the Monitor ADC. Host software for use in conjunction with the ProSLIC API is available from Skyworks Solutions. Typical MLT tests include:

- Hazardous Potential Test – This checks for ac voltage > 50 V_{RMS} or dc voltage > 135 V between Tip and Ground (T-G) or Ring and Ground (R-G).
- Foreign Electromotive Force Test – Checks T-G or R-G for ac voltage > 10 V_{RMS} or dc voltage > 6 V. Uses same threshold as for hazardous voltage test.
- Resistive Faults Test – Checks for dc resistance from T-R, T-G or R-G. Any measurement < 150 kΩ is considered a resistive fault.
- Receiver-Off-Hook Test – Distinguishes between a T-R resistive fault and an off-hook condition.
- Ringers Test – Measures the magnitude of the connected ring load (REN) across T-R. Results are > 0.175 REN and < 5 REN for a valid load
- AC Line Impedance (line length) – T-R, T-G, and R-G. Generates a tone at several specific frequencies (audio band) and measures the reflected signal amplitude (complex spectrum) that comes back (with transhybrid balance filter disabled). The reflected signal is then used to calculate the line impedance based on certain assumptions of wire gauge, etc.
- Line Capacitance – T-R, T-G, R-G. Generates a linear ramp function with polarity reversal, and measures the time constant.

Diagnostic information is available even in the presence of fault conditions that cause the system's protection devices (fuses, PTCs, etc.) to open. A high-impedance sensing path (pins SRINGC and STIPC) can be used to measure the conditions on Tip/Ring even when the FXS system is effectively disconnected from the line. No relay is required and this sensing path inherently meets Dielectric Withstand per GR-49 (> 1000 V).

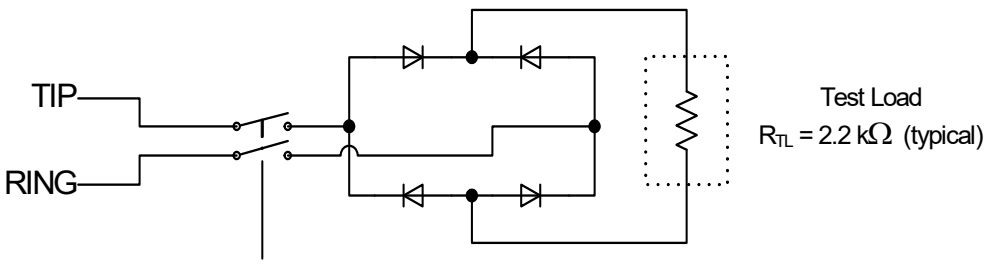


Figure 24. Si32260/1 Internal Test Load Circuit

6. System Interfaces

6.1. SPI Control Interface

The controller interface to the Si32260/1 is a 4-wire interface modeled after microcontroller and serial peripheral devices. The interface consists of a clock (SCLK), chip select (CS), serial data input (SDI), and serial data output (SDO). In addition, the ProSLIC devices feature a serial data through output (SDITHRU 8x8 mm package only) to support operation of up to 16 channels using a single chip select line. Each FXS port occupies one SPI channel. The device operates with both 8-bit and 16-bit SPI controllers.

6.2. PCM Interface and Companding

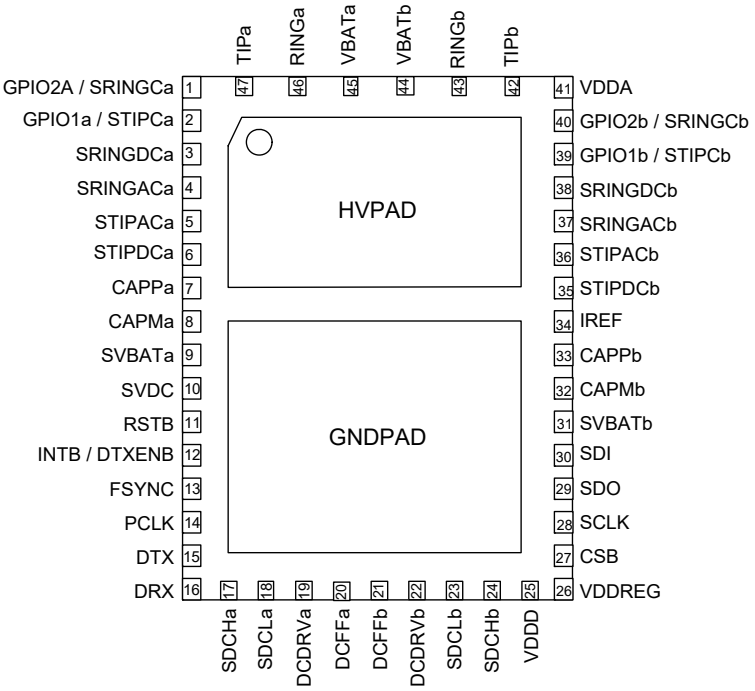
The Si32260/1 contains a flexible, programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled by the PCM clock (PCLK) and frame sync (FSYNC) inputs as well as the PCM Mode Select, PCM Transmit Start, and PCM Receive Start settings.

The interface can be configured to support from 8 to 128 8-bit time slots in each 125 µs frame, corresponding to a PCM clock (PCLK) frequency range of 512 kHz to 8.192 MHz. 1.544 MHz is also supported.

The Si32260/1 supports both µ-255 Law (µ-Law) and A-law companding formats in addition to 16-bit linear data mode with no companding.

7. Pin Descriptions: Si32260/1

7.1. Si32260/61 6x8 mm Package

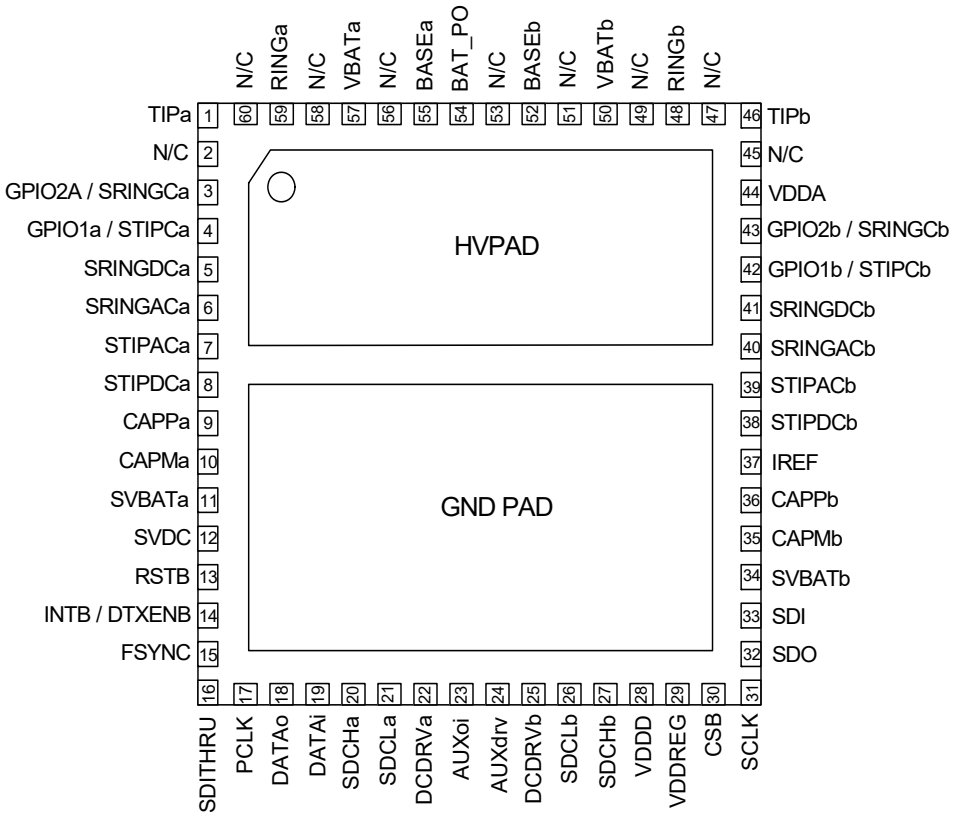


Pin #	Pin Name	Description
1	GPIO2a/SRINGCa	**General Purpose I/O** or **RING Coarse Sense Input—Channel A.** RING channel A Voltage sensing outside protection circuit.
2	GPIO1a/STIPCa	**General Purpose I/O** or **TIP Coarse Sense Input—Channel A.** TIP channel A voltage sensing outside protection circuit.
3	SRINGDCa	**RING DC Sense Input—Channel A.** Analog dc input to sense voltage on the channel A RING lead.
4	SRINGACa	**RING AC Sense Input—Channel A.** Analog ac input to sense voltage on the channel A RING lead.
5	STIPACa	**TIP AC Sense Input—Channel A.** Analog ac input to sense voltage on the channel A TIP lead.
6	STIPDCa	**TIP DC Sense Input—Channel A.** Analog dc input to sense voltage on the channel A TIP lead.
7	CAPPa	**SLIC Stabilization Capacitor—Channel A.** Capacitor used in low pass filter.
8	CAPMa	**SLIC Stabilization Capacitor—Channel A.** Capacitor used in low pass filter.
9	SVBATa	**VBAT Sense—Channel A.** Input to sense voltage on V_{BAT}.
10	SVDC	**DC-DC Input Voltage Sensor**. Senses V_{DC} input to dc-dc converters.

Pin #	Pin Name	Description
11	RSTB	**Reset Input.** Active low input. Hardware reset used to place all control registers in the default state.
12	INTB/DTXENB	**Interrupt Output** or **Transmit PCM Data Output Enable.** Maskable interrupt output or output enable for PCM data output. Open drain output for wire-ORed operation.
13	FSYNC	**Frame Sync Clock Input.** 8 kHz frame synchronization signal for the PCM bus. May be short or long pulse format.
14	PCLK	**PCM Bus Clock Input.** Clock input for PCM bus timing.
15	DTX	**Transmit PCM Data Output.** Output data to PCM bus.
16	DRX	**Transmit PCM Data Input**. Input data from PCM bus.
17	SDCHa	**DC Monitor—Channel A.** DC-DC converter monitor input used to detect overcurrent situations.
18	SDCLa	**DC Monitor—Channel A.** DC-DC converter monitor input used to detect overcurrent situations.
19	DCDRVa	**DC Drive—Channel A.** DC-DC converter control signal output which drives external transistor.
20	DCFFa	**DC Flexible Function—Channel A.** DC-DC controller flexible function I/O—channel A.
21	DCFFb	**DC Flexible Function—Channel B**. DC-DC controller flexible function I/O—channel B.
22	DCDRVb	**DC Drive—Channel B.** DC-DC converter control signal output which drives external transistor.
23	SDCLb	**DC Monitor—Channel B**. DC-DC converter monitor input used to detect overcurrent situations.
24	SDCHb	**DC Monitor—Channel B.** DC-DC converter monitor input used to detect overcurrent situations.
25	VDDD	**IC Voltage Supply**. Digital power supply for internal digital circuitry.
26	VDDREG	**Regulated Core Power Supply.**
27	CSB	**Chip Select Input**. Active low. When inactive, SCLK and SDI are ignored and SDO is high impedance. When active, the serial port is operational.
28	SCLK	**Serial Port Bit Clock Input.** Serial port clock input. Controls the serial data on SDO and latches the data on SDI.
29	SDO	**Serial Port Data Output.** Serial port control data output.

Pin #	Pin Name	Description
30	SDI	**Serial Port Data Input.** Serial port control data input.
31	SVBATb	**VBAT Sense—Channel B.** Input to sense voltage on V_{BAT}.
32	CAPMb	**SLIC Stabilization Capacitor—Channel B.** Capacitor used in low pass filter.
33	CAPPb	**SLIC Stabilization Capacitor—Channel B.** Capacitor used in low pass filter.
34	IREF	**Current Reference Input.** Connects to an external resistor used to provide a high accuracy reference current.
35	STIPDCb	**TIP DC Sense Input—Channel B.** Analog dc input to detect voltage on the channel B TIP lead.
36	STIPACb	**TIP AC Sense Input—Channel B.** Analog ac input to sense voltage on the channel B TIP lead.
37	SRINGACb	**RING AC Sense Input—Channel B.** Analog ac input to sense voltage on the channel B RING lead.
38	SRINGDCb	**RING DC Sense Input—Channel B.** Analog dc input to sense voltage on the channel B RING lead.
39	GPIO1b/STIPCb	**General Purpose I/O** or **TIP Coarse Sense Input—Channel B.** TIP channel A voltage sensing outside protection circuit.
40	GPIO2b/SRINGCb	**General Purpose I/O** or **RING Coarse Sense Input—Channel B.** RING channel A Voltage sensing outside protection circuit.
41	VDDA	**Analog Supply Voltage.** Analog power supply for internal analog circuitry.
42	TIPb	**TIP Terminal—Channel B.** Connect to the TIP lead of the channel B subscriber loop.
43	RINGb	**RING Terminal—Channel B**. Connect to the RING lead of the channel B subscriber loop.
44	VBATb	**Battery Voltage Supply—Channel B.** Connect to battery supply for Channel B.
45	VBATa	**Battery Voltage Supply—Channel A.** Connect to battery supply for Channel A.
46	RINGa	**RING Terminal—Channel A.** Connect to the RING lead of the channel A subscriber loop.
47	TIPa	**TIP Terminal—Channel A.** Connect to the TIP lead of the channel A subscriber loop.
48	HVPAD	**Exposed paddle.** Connect to electrically-isolated low thermal impedance inner layer and/or backside thermal plane using multiple thermal vias.
49	GNDPAD	**Exposed paddle.** Connect to ground.

7.2. Si32260/61 8x8 mm Package



Pin #	Pin Name	Description
1	TIPa	**TIP Terminal—Channel A.** Connect to the TIP lead of the channel A subscriber loop.
2	N/C	**No Connect.** This pin should be left unconnected.
3	GPIO2a/SRINGCa	**General Purpose I/O** or **RING Coarse Sense Input—Channel A.** RING channel A Voltage sensing outside protection circuit.
4	GPIO1a/STIPCa	**General Purpose I/O** or **TIP Coarse Sense Input—Channel A.** TIP channel A voltage sensing outside protection circuit.
5	SRINGDCa	**RING DC Sense Input—Channel A.** Analog dc input to sense voltage on the channel A RING lead.
6	SRINGACa	**RING AC Sense Input—Channel A.** Analog ac input to sense voltage on the channel A RING lead.
7	STIPACa	**TIP AC Sense Input—Channel A.** Analog ac input to sense voltage on the channel A TIP lead.
8	STIPDCa	**TIP DC Sense Input—Channel A.** Analog dc input to sense voltage on the channel A TIP lead.
9	CAPPa	**SLIC Stabilization Capacitor—Channel A.** Capacitor used in low pass filter.

Pin #	Pin Name	Description
10	CAPMa	**SLIC Stabilization Capacitor—Channel A.** Capacitor used in low pass filter.
11	SVBATa	**VBAT Sense—Channel A.** Input to sense voltage on V_{BAT}.
12	SVDC	**DC-DC Input Voltage Sensor**. Senses V_{DC} input to dc-dc converters.
13	$\overline{RST}$	**Reset Input.** Active low input. Hardware reset used to place all control registers in the default state.
14	INTB/DTXENB	**Interrupt Output** or **Transmit PCM Data Output Enable.** Maskable interrupt output or output enable for PCM data output. Open drain output for wire-ORed operation.
15	FSYNC	**Frame Sync Clock Input.** 8 kHz frame synchronization signal for the PCM bus. May be short or long pulse format.
16	SDITHRU	**SDI Pass-Through.** Cascaded SDI output signal for daisy-chain mode.
17	PCLK	**PCM Bus Clock Input.** Clock input for PCM bus timing.
18	DTX	**Transmit PCM Data Output.** Output data to PCM bus.
19	DRX	**Transmit PCM Data Input**. Input data from PCM bus.
20	SDCHa	**DC Monitor—Channel A.** DC-DC converter monitor input used to detect overcurrent situations.
21	SDCLa	**DC Monitor—Channel A.** DC-DC converter monitor input used to detect overcurrent situations.
22	DCDRVa	**DC Drive—Channel A.** DC-DC converter control signal output which drives external transistor.
23	DCFFa	**DC Flexible Function—Channel A.** DC-DC controller flexible function I/O—channel A.
24	DCFFb	**DC Flexible Function—Channel B**. DC-DC controller flexible function I/O—channel B.
25	DCDRVb	**DC Drive—Channel B.** DC-DC converter control signal output which drives external transistor.
26	SDCLb	**DC Monitor—Channel B**. DC-DC converter monitor input used to detect overcurrent situations.
27	SDCHb	**DC Monitor—Channel B.** DC-DC converter monitor input used to detect overcurrent situations.
28	VDDD	**IC Voltage Supply**. Digital power supply for internal digital circuitry.
29	VDDREG	**Regulated Core Power Supply.**

Pin #	Pin Name	Description
30	CSB	**Chip Select Input**. Active low. When inactive, SCLK and SDI are ignored and SDO is high impedance. When active, the serial port is operational.
31	SCLK	**Serial Port Bit Clock Input.** Serial port clock input. Controls the serial data on SDO and latches the data on SDI.
32	SDO	**Serial Port Data Output.** Serial port control data output.
33	SDI	**Serial Port Data Input.** Serial port control data input.
34	SVBATb	**VBAT Sense—Channel B.** Input to sense voltage on V_{BAT}.
35	CAPMb	**SLIC Stabilization Capacitor—Channel B.** Capacitor used in low pass filter.
36	CAPPb	**SLIC Stabilization Capacitor—Channel B.** Capacitor used in low pass filter.
37	IREF	**Current Reference Input.** Connects to an external resistor used to provide a high accuracy reference current.
38	STIPDCb	**TIP DC Sense Input—Channel B.** Analog dc input to detect voltage on the channel B TIP lead.
39	STIPACb	**TIP AC Sense Input—Channel B.** Analog ac input to sense voltage on the channel B TIP lead.
40	SRINGACb	**RING AC Sense Input—Channel B.** Analog ac input to sense voltage on the channel B RING lead.
41	SRINGDCb	**RING DC Sense Input—Channel B.** Analog dc input to sense voltage on the channel B RING lead.
42	GPIO1b/STIPCb	**General Purpose I/O** or **TIP Coarse Sense Input—Channel B.** TIP channel A voltage sensing outside protection circuit.
43	GPIO2b/SRINGCb	**General Purpose I/O** or **RING Coarse Sense Input—Channel B.** RING channel A Voltage sensing outside protection circuit.
44	VDDA	**Analog Supply Voltage.** Analog power supply for internal analog circuitry.
45	N/C	**No Connect.** This pin should be left unconnected.
46	TIPb	**TIP Terminal—Channel B.** Connect to the TIP lead of the channel B subscriber loop.
47	N/C	**No Connect.** This pin should be left unconnected.
48	RINGb	**RING Terminal—Channel B**. Connect to the RING lead of the channel B subscriber loop.
49	N/C	**No Connect.** This pin should be left unconnected.

Pin #	Pin Name	Description
50	VBATb	**Battery Voltage Supply—Channel B.** Connect to battery supply for Channel B.
51	N/C	**No Connect.** This pin should be left unconnected.
52	BASEb	**Offloading Base Control Output—Channel B**. Output to control base of power offloading transistor (fixed rail).
53	N/C	**No Connect.**
54	BAT_PO	**Power Offloading Battery Voltage Input**. Output from fixed rail dc-dc converter.
55	BASEa	**Offloading Base Control Output—Channel A.** Output to control base of power offloading transistor (fixed rail).
56	N/C	**No Connect.** This pin should be left unconnected.
57	VBATa	**Battery Voltage Supply—Channel A.** Connect to battery supply for Channel A.
58	N/C	**No Connect.** This pin should be left unconnected.
59	RINGa	**RING Terminal—Channel A.** Connect to the RING lead of the channel A subscriber loop.
60	N/C	**No Connect.** This pin should be left unconnected.
61	HVPAD	**Exposed paddle.** Connect to electrically-isolated low thermal impedance inner layer and/or backside thermal plane using multiple thermal vias.
62	GNDPAD	**Exposed paddle.** Connect to ground.

8. Ordering Guide

Table 19. Si32260/61 Ordering Guide[1]

P/N	Description	Package Type	Package Size	Number of pins	Max V_{BAT}	Temperature
Si32260-C-FM1	Dual wideband FXS, tracking or shared dc-dc	LGA[2]	8x8 mm	60	–110 V	0 to 70 °C
Si32260-C-GM1	Dual wideband FXS, tracking or shared dc-dc	LGA[2]	8x8 mm	60	–110 V	–40 to 85 °C
Si32261-C-FM1	Dual wideband FXS, tracking or shared dc-dc	LGA[2]	8x8 mm	60	–140 V	0 to 70 °C
Si32261-C-GM1	Dual wideband FXS, tracking or shared dc-dc	LGA[2]	8x8 mm	60	–140 V	–40 to 85 °C
Si32260-C-FM2	Dual wideband FXS, tracking dc-dc	LGA[2]	6x8 mm	47	–110 V	0 to 70 °C
Si32260-C-GM2	Dual wideband FXS, tracking dc-dc	LGA[2]	6x8 mm	47	–110 V	–40 to 85 °C
Si32261-C-FM2	Dual wideband FXS, tracking dc-dc	LGA[2]	6x8 mm	47	–140 V	0 to 70 °C
Si32261-C-GM2	Dual wideband FXS, tracking dc-dc	LGA[2]	6x8 mm	47	–140 V	–40 to 85 °C

Notes:
1. Adding the suffix "R" to the part number (e.g., Si32260-C-FM1R) denotes tape and reel.
2. LGA - Land Grid Array.

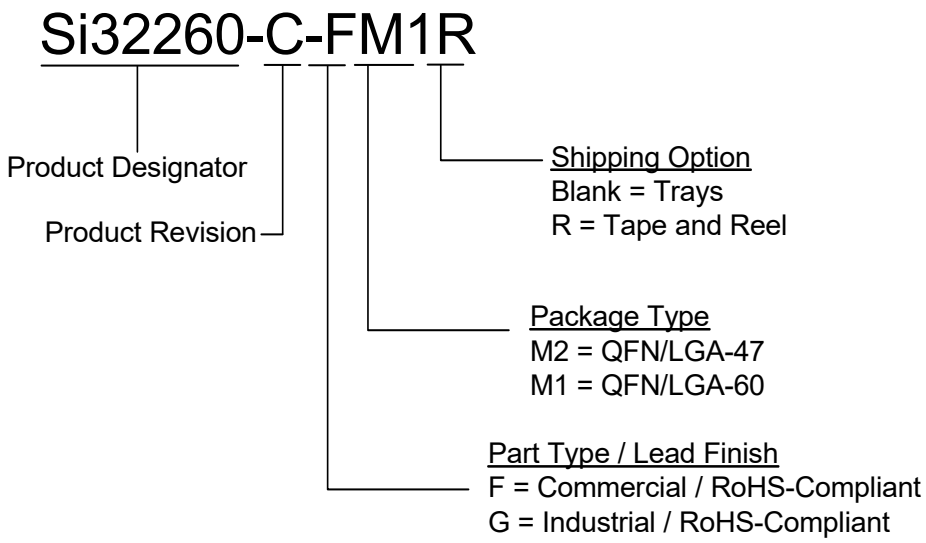
Table 20. Evaluation Kit Ordering Guide

Part Number	Supported ProSLIC	Description	V_{BAT} Max	Interface
Si32260CQC20SL0EVB	Si32260	Low cost quasi-Ćuk (NMOS FET/ Inductor based) full tracking dc-dc converter EVB	–110 V*	PCM/SPI to Voice Motherboard
Si32260CTS20SL0EVB	Si32260	Tracking Shared Supply (TSS) dc-dc converter EVB	–100 V	PCM/SPI to Voice Motherboard
Si32261CFB20SL0EVB	Si32260, Si32261	Flyback (transformer based) full tracking dc-dc converter EVB	–140 V	PCM/SPI to Voice Motherboard
Si32261CQC20SL0EVB	Si32260, Si32261	Quasi-Ćuk (NMOS FET/Inductor based) full tracking dc-dc converter EVB	–140 V	PCM/SPI to Voice Motherboard
***Note:** Supports VBAT up to –125 V with minor component substitutions (see AN381).				

9. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:



10. Package Outlines

10.1. 47-Pin QFN/LGA (6x8 mm)

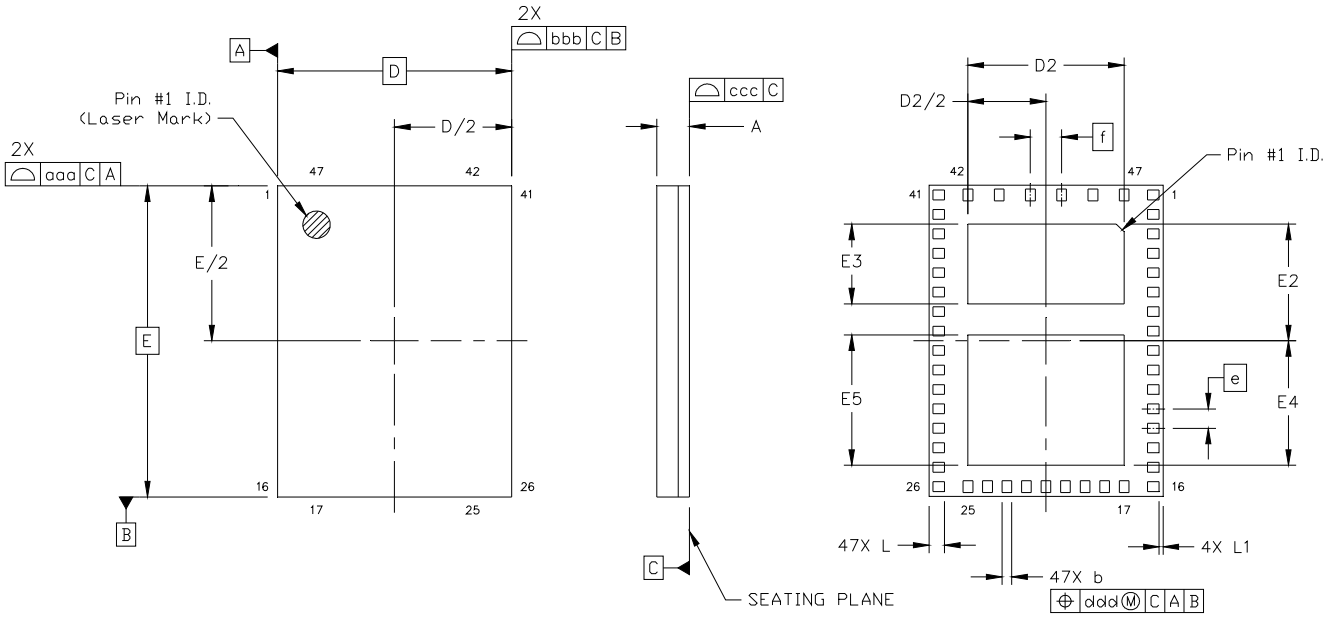


Figure 25. 47-pin QFN Package

Table 21. 47-Pin QFN Package Diagram Dimensions

Dimension	MIN	NOM	MAX	Dimension	MIN	NOM	MAX
A	0.74	0.84	0.94	E5	3.30	3.35	3.40
b	0.20	0.25	0.30	f	0.80 BSC		
D	6.00BSC			L	0.35	0.40	0.45
D2	3.95	4.00	4.05	L1	0.05	0.10	0.15
e	0.50 BSC			aaa	—	—	0.15
E	8.00 BSC			bbb	—	—	0.15
E2	2.95	3.10	3.25	ccc	—	—	0.10
E3	2.00	2.15	2.30	ddd	—	—	0.10
E4	3.15	3.20	3.25				

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2. 60-Pin QFN/LGA (8x8 mm)

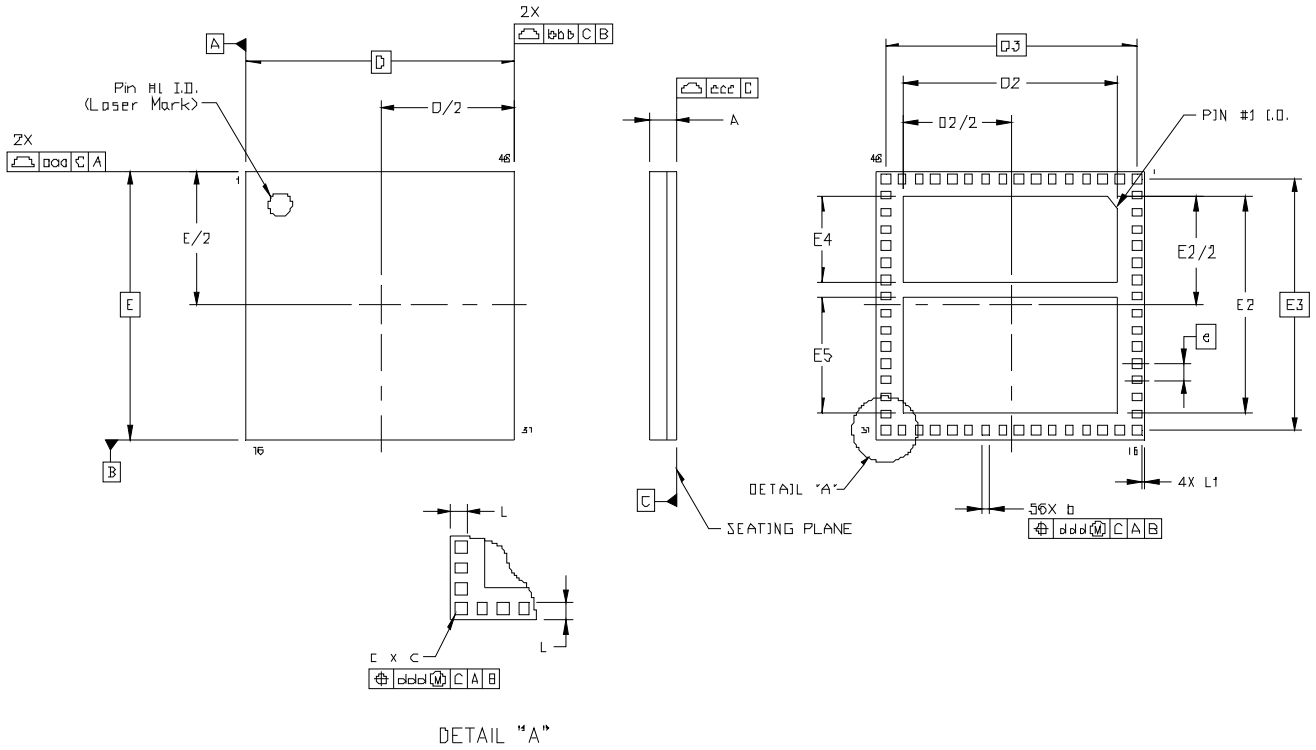


Figure 26. 60-Pin (QFN/LGA Package)

Table 22. 60-Pin QFN/LGA Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.74	0.84	0.94
b	0.20	0.25	0.30
c	0.25	0.30	0.35
D	8.00 BSC.		
D2	6.35	6.40	6.45
D3	7.50 BSC.		
e	0.50 BSC.		
E	8.00 BSC.		
E2	6.35	6.40	6.45

Dimension	Min	Nom	Max
E3	7.50 BSC.		
E4	2.46	2.51	2.56
E5	3.34	3.39	3.44
L	0.35	0.40	0.45
L1	0.05	0.10	0.15
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.3. 60-Pin QFN (8x8 mm)

Figure 27 illustrates the package details for the Si32260/1 60-Pin QFN. Table 23 lists the values for the dimensions shown in the illustration.

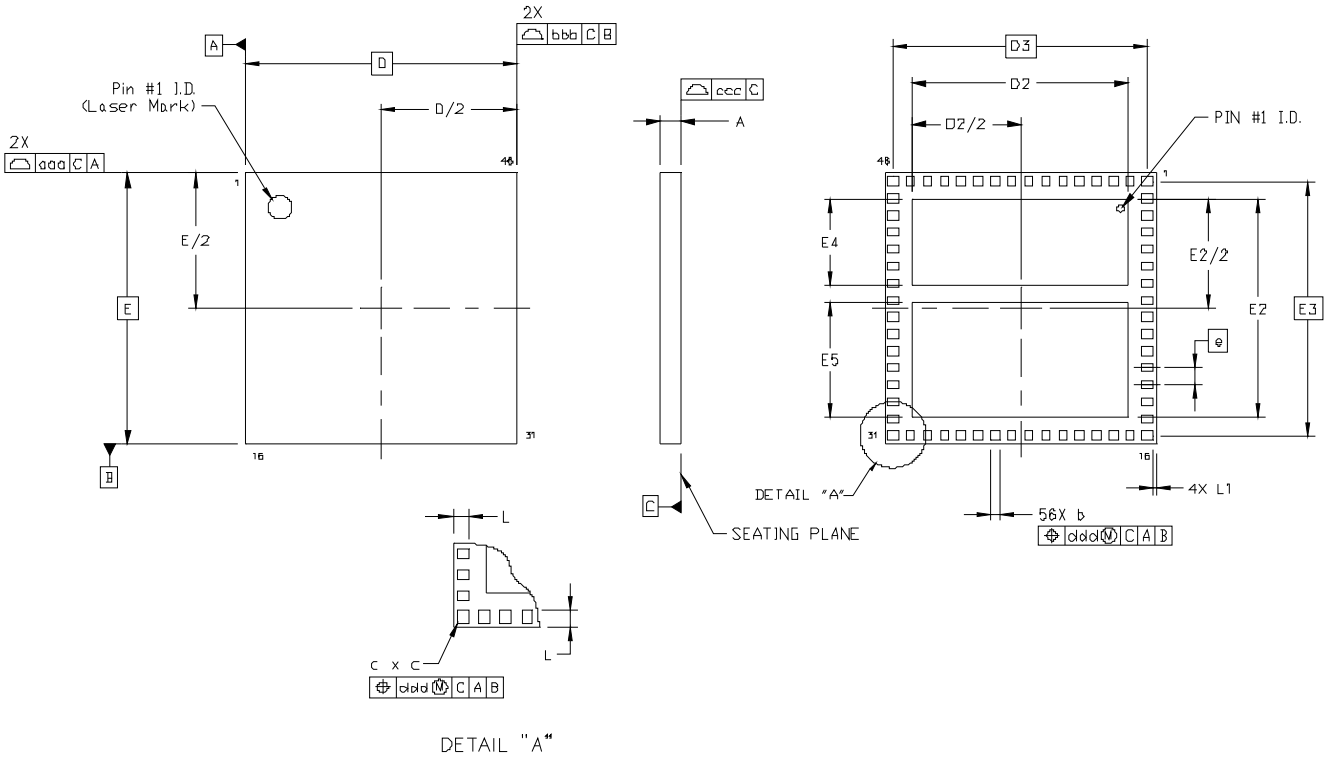


Figure 27. 60-Pin (QFN Package)

Table 23. 60-Pin QFN Package Diagram Dimensions

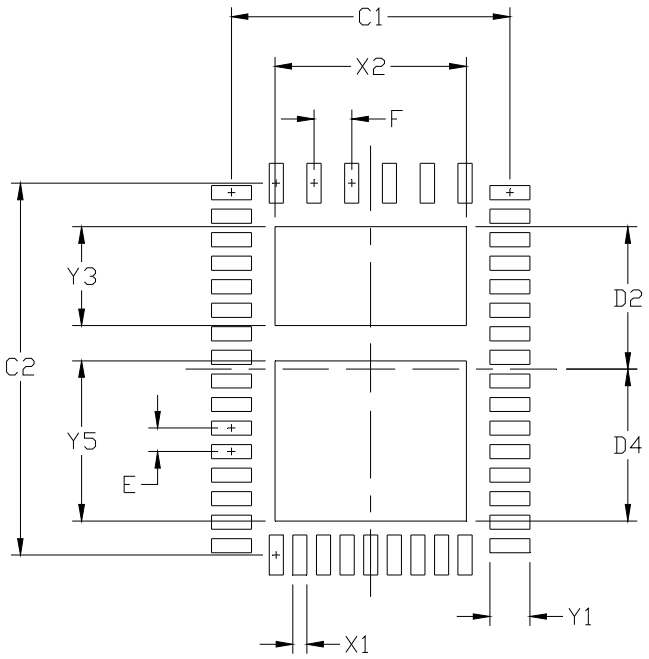
Dimension	Min	Nom	Max
A	0.60	0.65	0.70
b	0.20	0.25	0.30
c	0.25	0.30	0.35
D		8.00 BSC.	
D2	6.35	6.40	6.45
D3		7.50 BSC.	
e		0.50 BSC.	
E		8.00 BSC.	
E2	6.35	6.40	6.45

Dimension	Min	Nom	Max
E3		7.50 BSC.	
E4	2.46	2.51	2.56
E5	3.34	3.39	3.44
L	0.35	0.40	0.45
L1	0.05	0.10	0.15
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern—LGA Package

11.1. Land Pattern and Solder Mask Design–QFN-47 (6x8 mm)



Dimension	mm
C1	5.90
C2	7.90
D2	3.02
D4	3.22
E	0.50
F	0.80
X1	0.30
X2	4.05
Y1	0.85
Y3	2.10
Y5	3.40

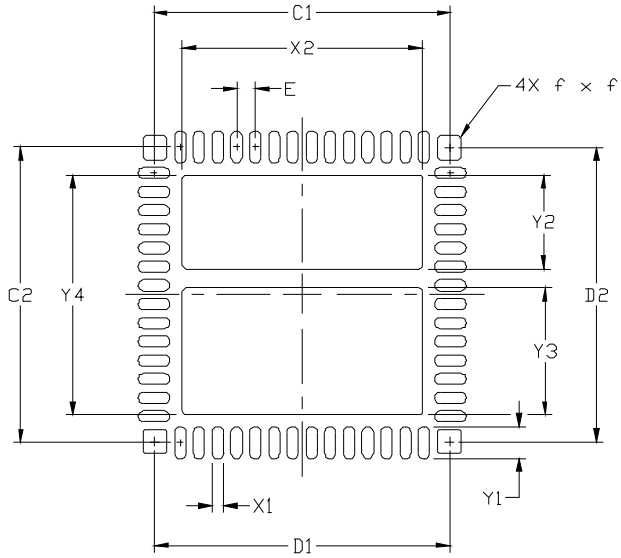
Notes:
General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

11.2. Land Pattern and Solder Mask Design–QFN-60 (8x8 mm)



Dimension	mm
C1	7.90
C2	7.90
D1	7.85
D2	7.85
E	0.50
f	0.65
X1	0.30
X2	6.35
Y1	0.85
Y2	2.46
Y3	3.39
Y4	6.37

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

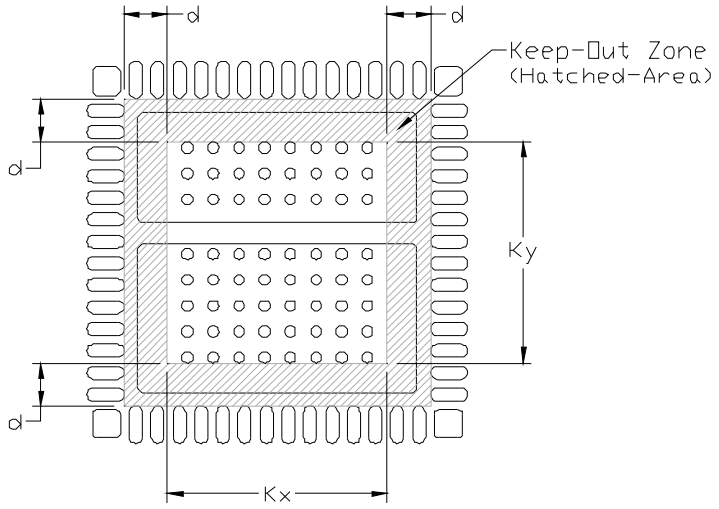
Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

11.3. Thermal via Layout–QFN-47 (6x8 mm)

The thermal via layout rules in section “11.4. Thermal via Layout–QFN-60 (8x8 mm)” for the QFN-60 package apply, except that it is not required to meet the minimum dimension d ≥ 1.0 mm for the via edge to pin pad metal spacing, as described in note 4.

11.4. Thermal via Layout–QFN-60 (8x8 mm)

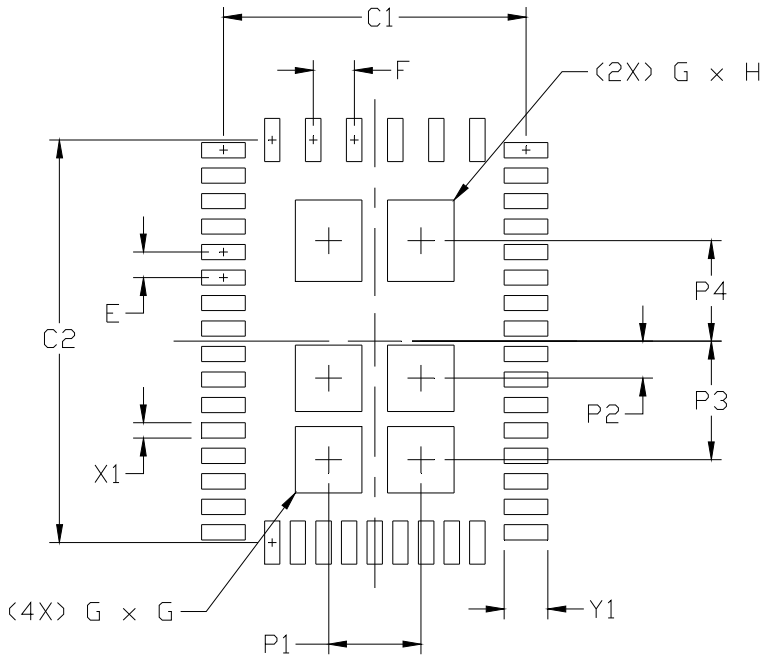


Dimension	Min	Max
d	1.00	—
Kx	—	5.05
Ky	—	5.05

Notes:

1. High-Tg PCB materials (Tg ≥ 170 °C) are recommended for Pb-Free reflow profiles, per standard industry practice.
2. The customer’s PCB design must provide sufficient thermal dissipation for high power operation of the device. See layout guidelines in application note, “AN381: Si3226x ProSLIC Designer’s Guide”, for further details.
3. A minimum of eight thermal vias are required in each center pad. The recommended via diameter is 0.20–0.30 mm (8–12 mils).
4. Thermal vias placed in the center pads *must* have a minimum spacing of 1.0 mm from the edge of the via to the closest pin pad metal (d ≥ 1.0 mm).
5. Vias may be placed as desired within the non-hatched area of the center pads.
6. Vias placed within the center pad areas *must* be either filled, or tented on the top side of the board, to prevent solder thieving from under the device.

11.5. Stencil Aperture Design–QFN-47 (6x8 mm)



Dimension	mm
C1	5.90
C2	7.90
E	0.50
F	0.80
G	1.30
H	1.80
P1	1.80
P2	0.73
P3	2.33
P4	2.08
X1	0.30
Y1	0.85

Notes:

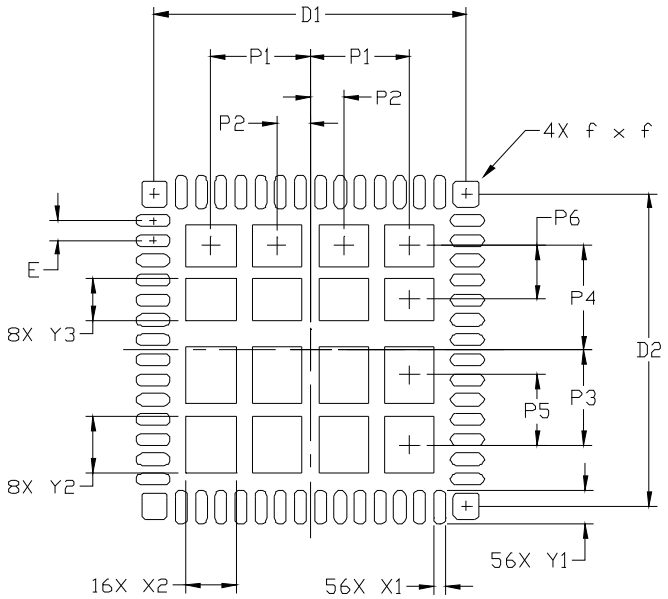
Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).

Card Assembly

3. A No-Clean, Type-3 solder paste is recommended.
4. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11.6. Stencil Aperture Design–QFN-60 (8x8 mm)



Dimension	mm
D1	7.85
D2	7.85
E	0.50
f	0.65
P1	2.50
P2	0.85
P3	2.38
P4	2.62
P5	1.76
P6	1.35
X1	0.30
X2	1.25
Y1	0.85
Y2	1.40
Y3	1.05

Notes:

Stencil Design

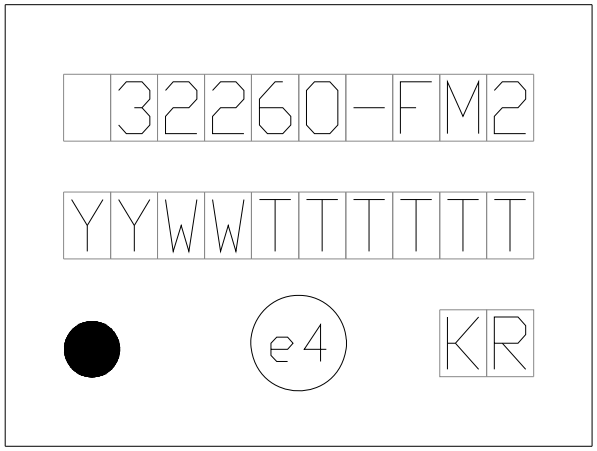
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).

Card Assembly

3. A No-Clean, Type-3 solder paste is recommended.
4. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Markings

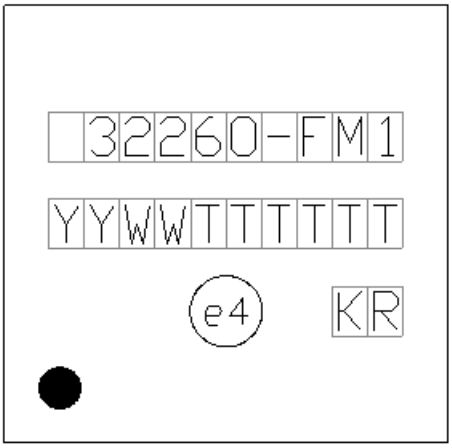
12.1. Top Marking (47-Pin LGA)



12.2. Top Marking Explanation (47-pin LGA)

Mark Method:	Laser	
Font Size:	2.0 Point (28 mils) Right-Justified	
Line 1 Marking:	Customer Part Number	32260-FM2
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 0.75 mm Diameter Lower-Left Justified	Pin 1 Identifier
	Circle = 1.3 mm Diameter Center-Justified	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	KR

12.3. Top Marking (60-Pin LGA)



12.4. Top Marking Explanation (60-Pin LGA)

Mark Method:	Laser	
Font Size:	2.0 Point (28 mils) Right-Justified	
Line 1 Marking:	**Device Part Number**	**Si32260-FM1**
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.3 mm Diameter Center-Justified	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	KR
Line 4 Marking:	Circle = 0.75 mm Diameter Lower Left-Justified	Pin 1 Identifier

13. Si3226x Support Documentation

- AN381: Si3226x ProSLIC Designer's Guide

Note: Refer to www.skyworksinc.com for a current list of support documents for this product family.

Document Change List:

Revision 0.1 to Revision 0.2

- Corrected (reversed) EPAD1 & EPAD2 in pin assignment drawings and pin descriptions
- Added table of charge pump characteristics
- Added PCLK jitter tolerance
- Updated flyback dc-dc converter application schematics and BOM
- Added fixed rail dc-dc converter application schematics and BOM
- Updated ordering guide to revision B
- Added package top markings information
- Added PCB land pattern and soldering notes

Revision 0.2 to Revision 0.3

- Added Tracking Shared Supply (TSS) mode
- Added thermal resistance and maximum continuous power dissipation
- Completed Table 3 with power consumption data
- Changed the name of the fixed rail dc-dc application circuit to Tracking Shared Supply (TSS)
- Corrected description of wideband operation
- Changed ordering information to revision C

Revision 0.3 to Revision 0.31

- Corrected IDD values in Table 3. They were showing IDD for two channels, now only one channel as specified.

Revision 0.31 to Revision 1.0

- Corrected Jitter Tolerance to be 8 ns_{RMS} maximum.
- Updated the protection schematics for the TSS dc-dc converter application. Pins "A" of the TISP61089BDR are now connected to GROUND, and the pin labeled "G" (the GATE) is now connected to VBAT.
- Updated order of data sheet elements in accordance with new style guide SOPs.
- Cosmetic updates to schematics and BOMs.
- Changed test load impedance to 2.2 kΩ (was listed as 5.3 kΩ or 600 Ω).
- Increased SDITHRU and $\overline{RST}$ maximum leakage current to 80 µA.
- Increased absolute maximum VBAT, TIP, and RING voltages to –142 V (was –140 V).
- Added absolute maximum positive voltage specs for TIP and RING of +0.4 V.

Revision 1.0 to Revision 1.1

- Added LGA package information

Revision 1.1 to Revision 1.2

- Added 6x8 mm QFN/LGA-47 package option
- Added theta jb and jc values (for all package sizes)
- Corrected some text formatting in the Power Supply Characteristics table and changed the off hook line feed current condition to 20 mA for consistency with other ProSLIC data sheets.
- Renamed EPADs to be more descriptive: HVPAD and GNDPAD.
- Updated EVB part numbers and added PMOS buck boost dual footprint EVB.
- Removed reset rise time spec from Table 7.

Revision 1.2 to Revision 1.3

- Corrected 6x8 mm package land pattern diagram in section 11.1 on p.52.

Revision 1.3 to Revision 1.4

- Updated EVB part numbers.
- Changed R_{TEST} (Test Load Impedance) specification in Table 4 to replace typical value with a range from minimum to maximum.
- Removed notes specifying voltage and temperature conditions for Tables 2 through 9.
- Replaced TSS DC-DC converter reference schematics and bill of materials with (Low Cost Quasi-Ćuk (LCQC) reference schematics and bill of materials.
- Removed NBA Part Numbers from Ordering Guide.
- Updated 6x8 LGA package dimension tolerances: Dimension E2 NOM changed from 3.00 to 3.10, and Max changed from 3.05 to 3.25. Dimension E3 NOM changed from 2.05 to 2.15, and Max from 2.10 to 2.30.
- Added section listing support documentation.
- Removed NBA package references throughout document.

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