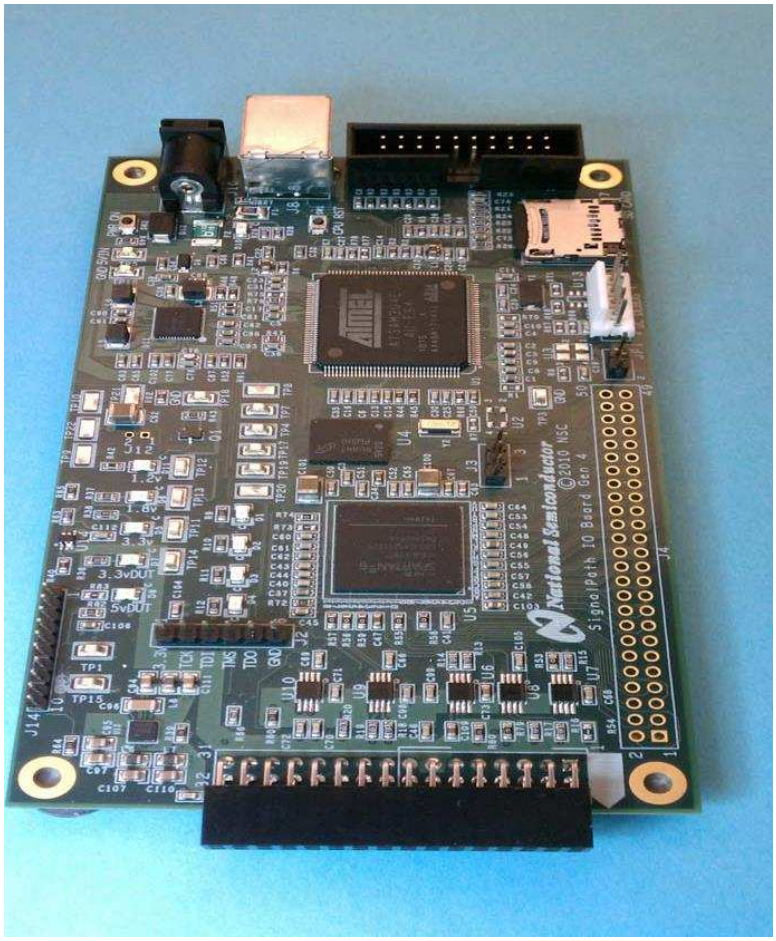
THE DATASHEET OF

SPIO-4/NOPB

SPIO-4 Precision Signal-Path Controller Board



This user's guide describes the characteristics, operation, and use of the SPIO-4 precision signal-path controller board. This document includes a schematic, reference printed circuit board (PCB) layouts, and a complete bill of materials (BOM).

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Trademarks

1 System Overview

The SPIO-4 is one of several National Semiconductor digital controller and capture boards that are used by multiple evaluation systems. The objective of these software and hardware evaluation systems is to allow our customers to easily and accurately evaluate TI's signal-path devices in a lab setting. At the time of the SPIO-4 release, two different evaluation system software applications and graphical user interfaces (GUIs) make use of this board: the WaveVision-5 and the Sensor AFE. The board ships with the current version of the WaveVision-5 software.

In addition to the controller and capture board (in this case, the SPIO-4) and the evaluation GUI software (for example, WaveVision-5 or Sensor AFE), the third essential element of an evaluation system is the device or signalpath evaluation board that plugs into the controller board. This evaluation board is generically referred to as the *DUT board*. Each DUT board comes with a user's guide that documents the specific features of the board. Each DUT board also comes with some software that the user must install before initial use. In the case of the WaveVision-5 GUI, this software is essentially a device-specific module that adds support for the future device evaluation boards. In the case of Sensor AFE device family, the evaluation board comes with a complete, custom Sensor AFE that is specifically paired with that device.

The WaveVision-5 and Sensor AFE GUI software have respective user's guide documents that describe how to interact with the respective GUI.

This user’s guide describes only the SPIO-4 board. The user is expected to refer to this guide only if necessary. The DUT user’s guide and the GUI user's guide are the primary documents that describe how to work with a TI signal-path evaluation board.

The latest version of this document may be obtained from the Texas Instruments web site at www.ti.com.

1.1 System Features

- Captures or sources multiple signal-path data streams and transfers them to and from the PC-based application software through a USB 2.0 connection (USB 1.1 compatible).
- Supports a jumper-less, plug-and-play configuration. The GUI automatically discovers the attached DUT board and loads the appropriate software module for it.
- Supports a wide variety of signal-path evaluation board through a standardized connector (GPSI- 16 or GPSI-32).
- Capable of storing up to 8 MBytes of signal-path data.
- DUT interface can be SPI, I^2C, or parallel.
- Powered either by PC via USB or external supply.

1.2 Packing List

The SPIO-4 kit (order number SPIO-4/NOPB) consists of the following components:

- SPIO-4 board
- USB cable
- User’s guide (this document)
- WaveVision-5 GUI software

1.3 Component Description

Table 1 describes both the onboard connectors and the main components used in the SPIO-4 system shown in Figure 4.

Table 1. Main Component Reference Designators

Component	Description
J1	Serial debug connector
J2	Header to provide access to the FPGA JTAG interface for debug
J3	Jumper to select J4 IO voltage (3.3 V or programmable)
J4 (DBG)	Debug and development connector(see Section 2.6)
J6 (GPSI-32)	GPSI-16/32 connector to DUT
J7 (micro_SD)	Holds the microSD card for storage or development purposes
J8 (USB)	USB cable connection
J9 (JTAG)	Atmel processor JTAG debug header
J10 (POWER)	5-v to 6-V power supply connection; optional (see Section 2.9)
J14 (USNAP)	Additional header providing power and serial interface to processor
JP1	Jumpers for test purposes only
U1	Atmel SAM3U processor
U4	8Mx16 PSRAM
U5	Xilinx Spartan LX16 FPGA
D1-D4	FPGA status LEDs (see Section 2.4)
D6	1.8-V PSRAM core voltage surface-mount power LED
D7	3.3-V DUT supply voltage surface-mount power LED
D8	5.0-V DUT supply voltage surface-mount power LED
D10	USB input power LED
D11	1.2-V FPGA Core voltage surface-mount power LED
SW1	Reset switch
SW2	Power on push-button

1.4 SPIO-4 Board Test Points

Table 2 describes the available test points.

Table 2. Test Points

Test Point	Description
TP1, TP3, TP16, TP18 (GND)	Ground test points
TP11	3.3-V digital I/O voltage for SPIO board
TP12	1.2 V for FPGA core voltage
TP13	1.8 V for PSRAM core voltage
TP14	3.3 V for DUT digital supply
TP15	5.0 V for DUT analog supply

2 System Functionality

2.1 System Block Diagram

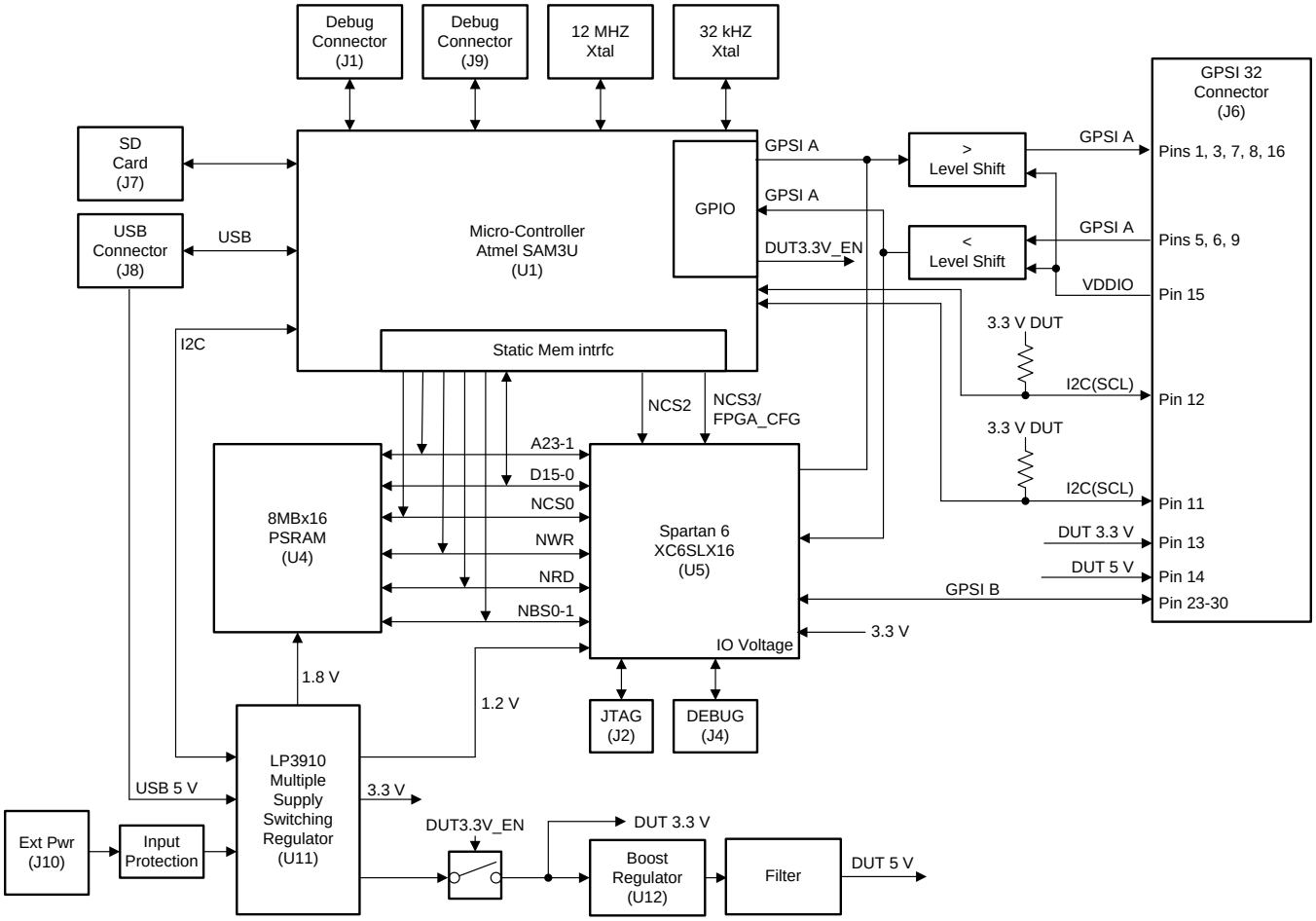

Figure 1. SPIO-4 System Block Diagram

2.2 General System Overview

The SPIO-4 board is controlled via the Atmel SAM3U, a microcontroller that is based on an ARM M3, 32-bit embedded core. This miscrocontroller provides the interface to the computer via a USB interface. The DUT board interfaces to the SPIO-4 via J6, the GPSI-16/32 connector. The GPSI-16/32 interface provides control, data and power to the DUT board. The interfaces on the GPSI-32 can be I^2C, SPI with multiple-device capability, or parallel interface. The dedicated I^2C interface on the GPSI-16/32 is primarily for control and DUT identification, while the dedicated SPI interface may be used for control or for data transfer. The I^2C interface is derived from the peripheral of the microcontroller. There can be a wide variety of SPI requirements for DUTs; therefore, the SPI interface can be provided via a processor peripheral and over the dedicated SPI lines as shown in this document, or the onboard Xilinx Spartan XC6SLX16 FPGA may be used. In fact, the FPGA may be used to implement DUT interfaces other than SPI, such as high-speed I^2C for data purposes, and parallel data-plus-clock interfaces. A large external SRAM 8Mx16 is connected to both the processor and the FPGA, and is used to provide additional device data storage in case the microcontroller or FPGA onboard memory is insufficient.

Power is provided to the system via the USB cable or external power jack. A switching regulator is used to produce the 3.3-V supply required by the microcontroller and GPSI-32 devices. A boost regulator creates the regulated 5-V supply required by the devices interfaced to the GPSI-32 connector.

2.3 Automatic Device Detection and Configuration

The SPIO-4 system supports automatic hardware detection and configuration of the device under test. The GUI software actually carries out the device detection and configuration task. The FPGA is reconfigured on-the-fly by the host PC when the SPIO-4 board is powered on, or whenever ADC evaluation boards are exchanged and SPIO-4 power is cycled.

Each DUT board has either an FPGA configuration file or a microcontroller firmware module unique to the board. The GUI software, in conjunction with the USB microcontroller, determines which DUT board has been plugged in. The GUI then loads a configuration file tailored for that DUT board into the FPGA, the microcontroller, or both.

Normally, the configuration process is totally transparent to the user, and requires no intervention. However, some devices may allow this process to be overridden. Refer to the evaluation board manual for more information.

NOTE: Many of our device evaluation boards do require jumper configurations to select channels, voltages, or other options. Please consult the manual that came with the evaluation board for specific information.

CAUTION

Be aware that DUT boards are ***NOT*** hot swappable. Power down both the SPIO-4 board and the DUT board prior to swapping DUT board.

2.4 LED Indicators

There are several LED indicators on the SPIO-4 board. The LED indicators described in Table 3 are driven directly by separate power rails on the SPIO-4 board. Those rails can only be controlled by the processor; therefore, the LEDs not only indicate a particular rails is powered on, but the LEDs also show the state of the SPIO-4 firmware, as shown in Table 3.

Table 3. LED Behavior

LED Number	Description
D10	Indicates power (USB or external) is present to SPIO board
D5	3.3-V digital I/O voltage for SPIO board is up (required for all operations)
D6	1.2 V for FPGA core voltage. Indicates processor has completed low-level hardware initialization, and is ready to program the FPGA.
D11	1.8 V for PSRAM core voltage. Indicates processor has completed low-level hardware initialization, and is able to use the PSRAM
D7 and D8	3.3-V and 5-V DUT supplies. Indicates the processor has detected a DUT board is inserted, and has powered the board.

2.5 DUT Interface (GPSI-16/32)

The SPIO-4 data capture board is connected to the DUT through the GPSI-16/32 (J6) connector. As described in this user's guide, the GPSI-32 interface provides control, data, and power to the DUT board. See Table 4 for signal specifics. The GPSI-16/32 interface also supports a subset called GPSI-16 that consists of the lower order pins 1 to 16. A given DUT board may use a 16-pin, GPSI-16 port only, or may use the whole 32-pin port. GPSI-16 has level shifters allowing some of the DUT interface voltages to go from 1.65-V to 5.5-V LVTTL levels under the direct control of the DUT board circuitry. To achieve that voltage range, the voltage level shifters are NOT bidirectional. A DUT board requiring bidirectional signals must use the upper-order portion of the GPSI-32. However, that upper-order portion of GPSI-32 requires adherence to 3.3-V LVTTL voltage levels because the upper-order portion does not have level shifters.

Figure 2 and Figure 3 show two photos demonstrating the proper mating of a GPSI16 and a GPSI32 DUT board to the SPIO4.

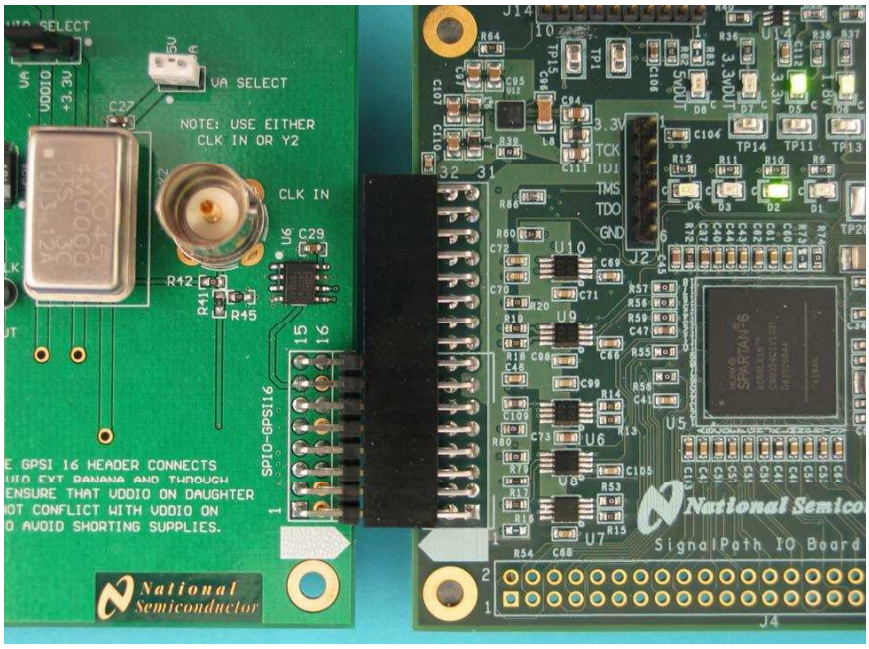

Figure 2. GPSI 16 DUT to SPIO4 Mating

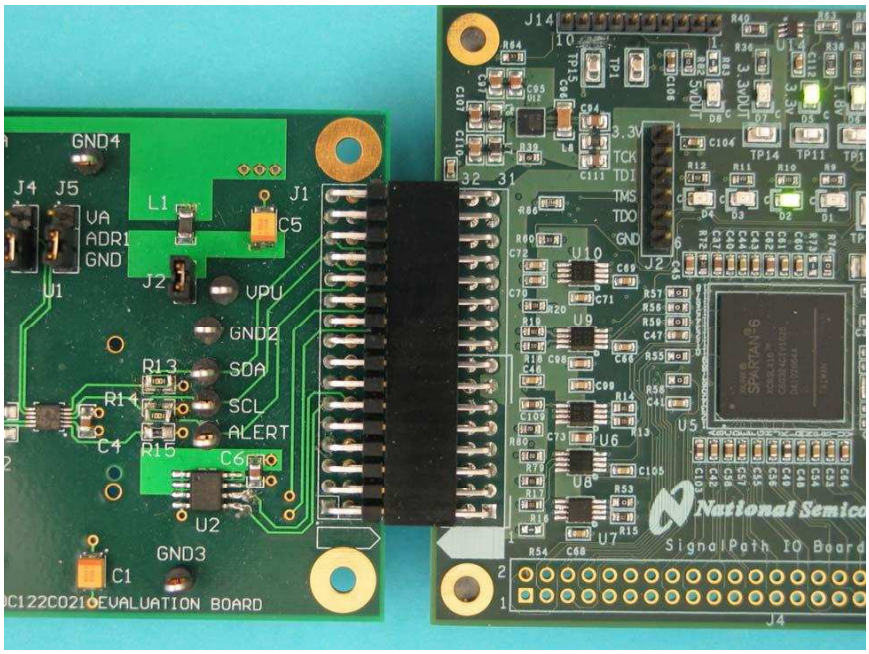

Figure 3. GPSI 32 DUT to SPIO4 Mating

2.5.1 Level Shifters

The board incorporates level shifters to allow flexible output voltages on the unidirectional SPI signals of GPSI-16 port, as shown in Figure 1. VDDIO, a supply voltage from the GPSI-16/32 connector coming from the DUT board, provides the voltage to the output side of the level translators. If the DUT has no special requirements for voltage and simply needs basic 3.3-V signal levels, the 3.3-V output from the GPSI connector can be connected to VDDIO on the DUT board. The level shifters are unidirectional. If VDDIO is not provided, the level shifters enter a shutdown state with all input pins in a tri-state condition. The state passed along to the processor in this case is logic low. Table 4 shows the full list of available level-shifter configurations.

Table 4. GPSI-32 Signals

Pin #	Signal Name	Signal Function	Voltage Level	Direction (From SPIO-4)
Pins 1-16 form the GPSI-16 subset:				
1	SCS0_A~	Serial Bus A – Chip select for device 0.	1.65 V to 5.5 V	Output
2	GND	Ground	N/A	N/A
3	SCK_A	Serial Bus A – Serial clock from the master to the device.	1.65 V to 5.5 V	Output
4	DUT_Present~	The DUT board grounds this pin. The SPIO-4 senses this pin to determine the DUT board presence.	N/A	Input
5	SMISO_A	Serial Bus A – Data from the slave (device) to the master. The device may implement this as a tri-state signal that can be driven by multiple devices on Serial Bus A in a bussed fashion. The pullup resistor, if required, is on the DUT board.	1.65 V to 5.5 V	Input
6	Dev_INT~/ SDRDY_A~	In certain applications, if required, this pin serves as the DRDY~ signal from the DUT to the SPIO-4. In other cases, this pin may be a general interrupt pin from the device to the SPIO-4. On the SPIO-4 board, this signal connects to an interrupt pin on the microcontroller.	1.65 V to 5.5 V	Input
7	SMOSI_A	Serial Bus A – Data from the master to the slave (device).	1.65 V to 5.5 V	Output
8	SCS1_A~	Serial Bus A – Chip select for device 1.	1.65 V to 5.5 V	Output
9	Ref_CLK	Reference clock from the DUT board to the SPIO-4 board. If not used, the DUT board should ground this pin.	1.65 V to 5.5 V	Input
10	GND	Ground	N/A	N/A
11	SDA	Data line of the I^2C bus. Pulled up to +3.3V_DUT on the SPIO-4 board through a 1.5-kΩ resistor.	3.3 V	Bidirectional
12	SCL	Clock line of the I^2C bus. Pulled up to +3.3V_DUT on the SPIO-4 board through a 1.5-kΩ resistor.	3.3 V	Bidirectional
13	+3.3V_DUT	Switched by the SPIO-4 conditional parameter on the DUT_Present pin. The ID EEPROM and the entire I^2C bus on the DUT board must be unconditionally powered by this supply. Maximum peak current = 50 mA (subject to total power budget limit of 200 mW over both supplies). Maximum capacitor loading for this node is not to exceed 50 µF.	3.3 V	Output
14	+5V_DUT	This supply is sourced by the SPIO-4 and is intended to power the core functionality of the DUT board, if desired. Nominal current = 35 mA. Maximum peak current = 50 mA (subject to total power budget limit of 200mW over both supplies). If power from the SPIO-4 is not required, the DUT board must leave this pin open. Maximum capacitor loading for this node is not to exceed 50 µF.	5.0 V	Output
15	VDDIO		1.65 V to 5.5 V	Input
16	SCS2_A~		1.65 V to 5.5 V	Output
17	DUT_PWR_Enable		3.3 V	Output
18		Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open. (Possible use: DUT_RESET~)	3.3 V	N/A
19		Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open.	3.3 V	N/A
20		Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open.	3.3 V	N/A

Table 4. GPSI-32 Signals (continued)

Pin #	Signal Name	Signal Function	Voltage Level	Direction (From SPIO-4)
21		Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open.	3.3 V	N/A
22		Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open.	3.3 V	N/A
23	SCS0_B~	Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open. If a second SPI bus is implemented, then use this pin as shown: Serial Bus B – Chip select for device 0.	3.3 V	N/A
24	SDRDY_B~	Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open. If a second SPI bus is implemented, then use this pin as shown: In certain SPI applications, if required, this pin serves as the DRDY~ signal from the DUT to the SPIO-4.	3.3 V	N/A
25	SCK_B	Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open. If a second SPI bus is implemented, then use this pin as shown: Serial Bus B – Serial clock from the master to the device.	3.3 V	N/A
26	SCS1_B~	Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open. If a second SPI bus is implemented, then use this pin as shown: Serial Bus B – Chip select for device 1.	3.3 V	N/A
27	SMISO_B	Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open. If a second SPI bus is implemented, then use this pin as shown: Serial Bus B – Data from the slave (device) to the master. The device may implement this as a tri-state signal that can be driven by multiple devices on Serial Bus B in a bussed fashion. The pullup resistor, if required, is on the DUT board.	3.3 V	N/A
28	SCS2_B~	Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open. If a second SPI bus is implemented, then use this pin as shown: Serial Bus B – Chip select for device 2.	3.3 V	N/A
29	SMOSI_B	Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open. If a second SPI bus is implemented, then use this pin as shown: Serial Bus B – Data from the master to the slave (device).	3.3 V	N/A
30	SCS3_B~	Available for implementation-specific use. Refer to the DUT board manual. If unused, leave it open. If a second SPI bus is implemented, then use this pin as shown: Serial Bus B – Chip Select for device 3.	3.3 V	N/A
31	Reserved	Reserved for future use. The DUT board leaves this pin open.	3.3 V	N/A
32	GND	Ground	N/A	N/A

2.6 Auxiliary Interface

The SPIO-4 board can be connected to auxiliary test equipment through debug connector J4 located on the board.

2.7 Computer Interface

The SPIO-4 board communicates with a PC via standard USB 2.0 at high-speed (up to a 480 Mbits/sec signaling rate). The board is fully backward-compatible with USB 1.1 devices and cables.

2.8 Memory

The SPIO-4 board comes with 8M × 16 bits of PSRAM for data storage. The memory is a single Micron MT45W8MW16BGX PSRAM configured for asynchronous accesses. In asynchronous configuration, the fastest access speed is 70 ns latency, or approximately 14.2 MHz per 16-bit transfer. Both the processor and the FPGA have read and write access to the PSRAM. The processor's static memory interface mastership is controlled by firmware within the processor because there is no hardware mechanism to share the bus.

2.9 Power Requirements

The SPIO-4 data capture board can be solely powered using the USB interface power, but can also be powered by an external power supply. The SPIO-4 data capture board consumes up to 500 mA of current depending on the DUT load. ADC evaluation boards differ widely in their power consumption; consult the manual that came with your evaluation board, and verify if an external supply is required for your DUT board. External power can be supplied via J10, and must be greater than 4.5 V and less than 6.0 V dc with a current rating of at least 1 A.

3 PCB Layout, Schematics, and Bill of Materials

The following section shows the printed circuit board (PCB) layout overview, the schematics, and the bill of materials (BOM).

3.1 PCB Layout Overview

Figure 4 shows the component side of the SPIO-4 board layout.

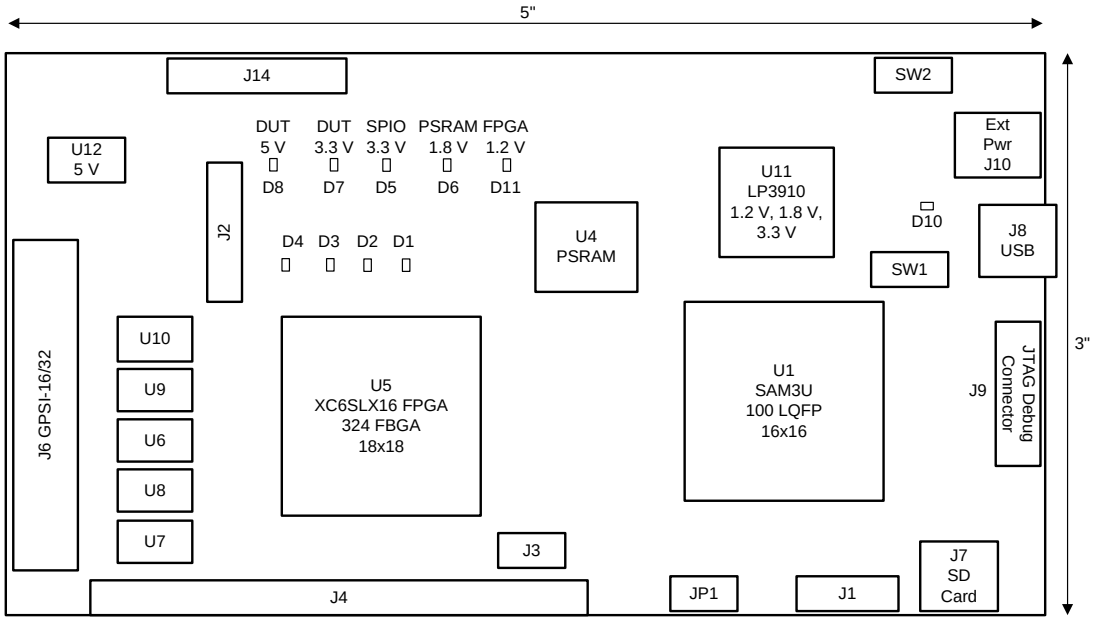

Figure 4. SPIO-4 Board Layout – Component Side

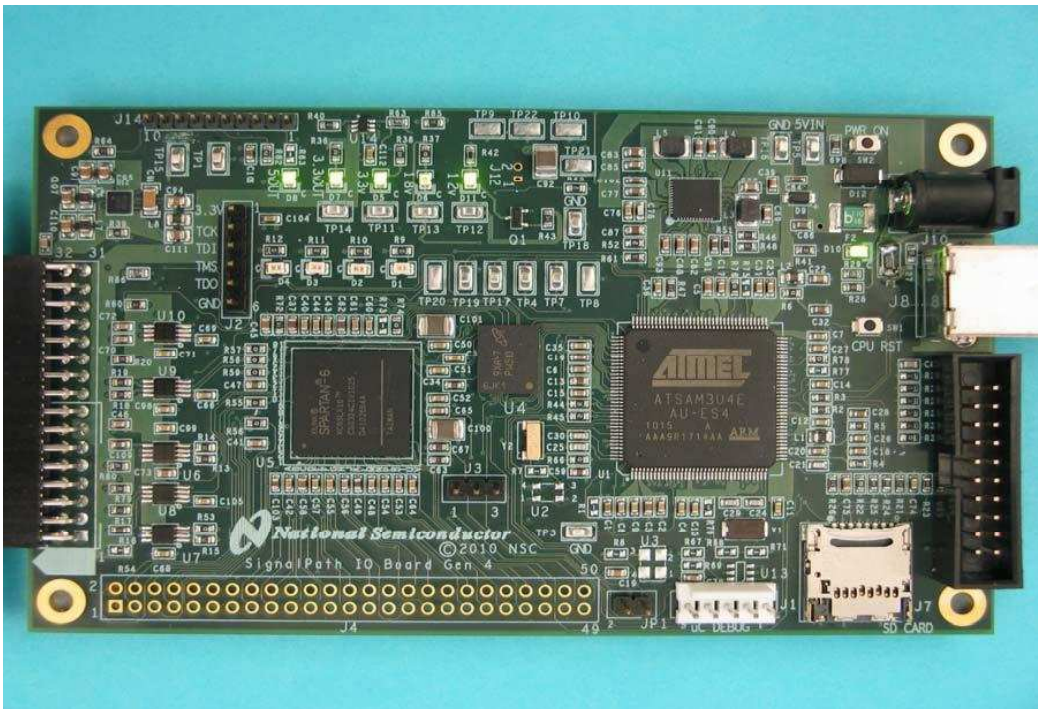

Figure 5. Board Photo Showing Respective Layout From Figure 4

3.2 Schematics

The following pages show the schematics of the board. These are provided for general information purposes only. TI reserves the right to make modifications to the board design at any time.

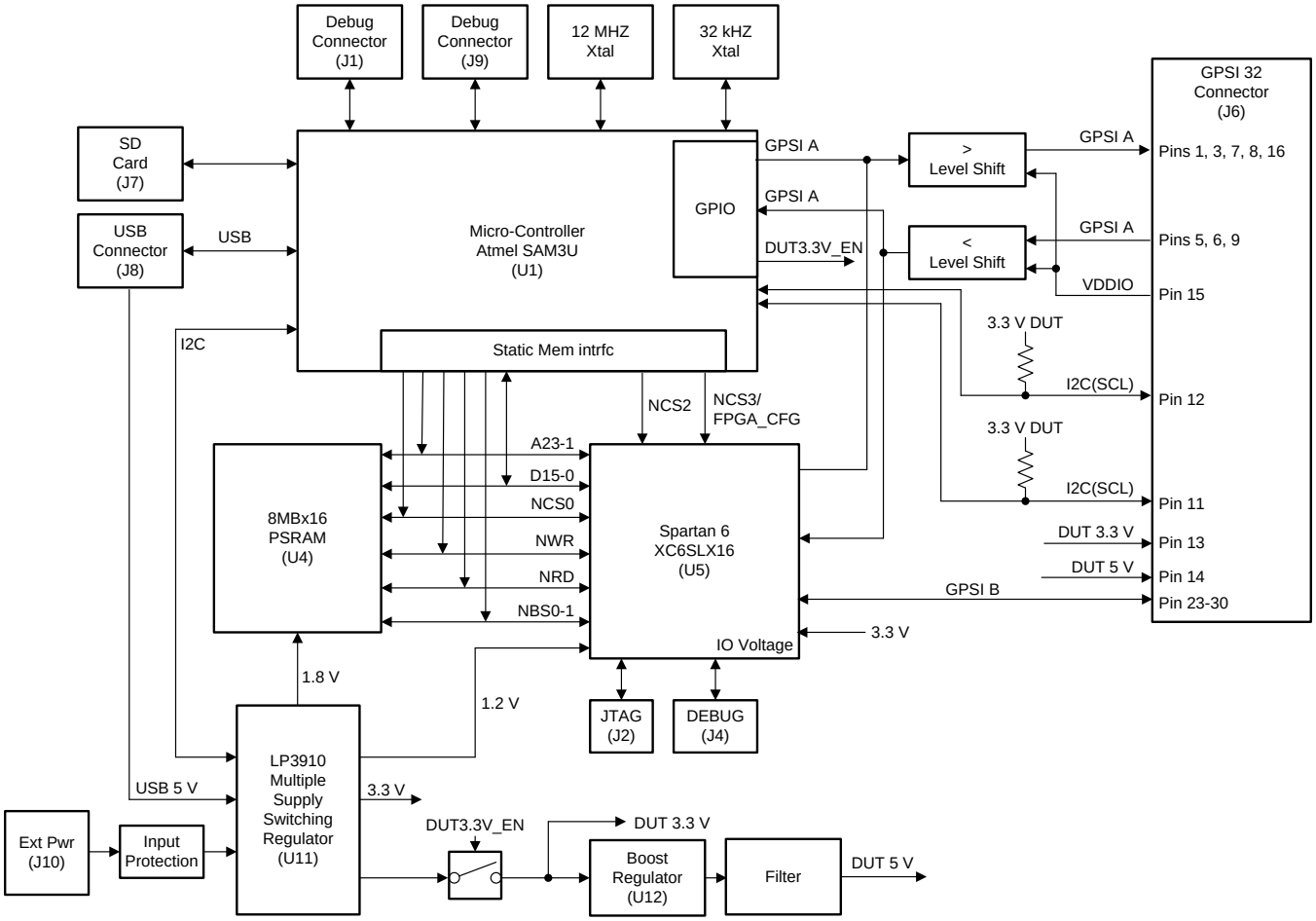

Figure 6. SPIO-4 Interface Board Block Diagram

Atmel ARM Microcontroller - Power, Debug, Analog

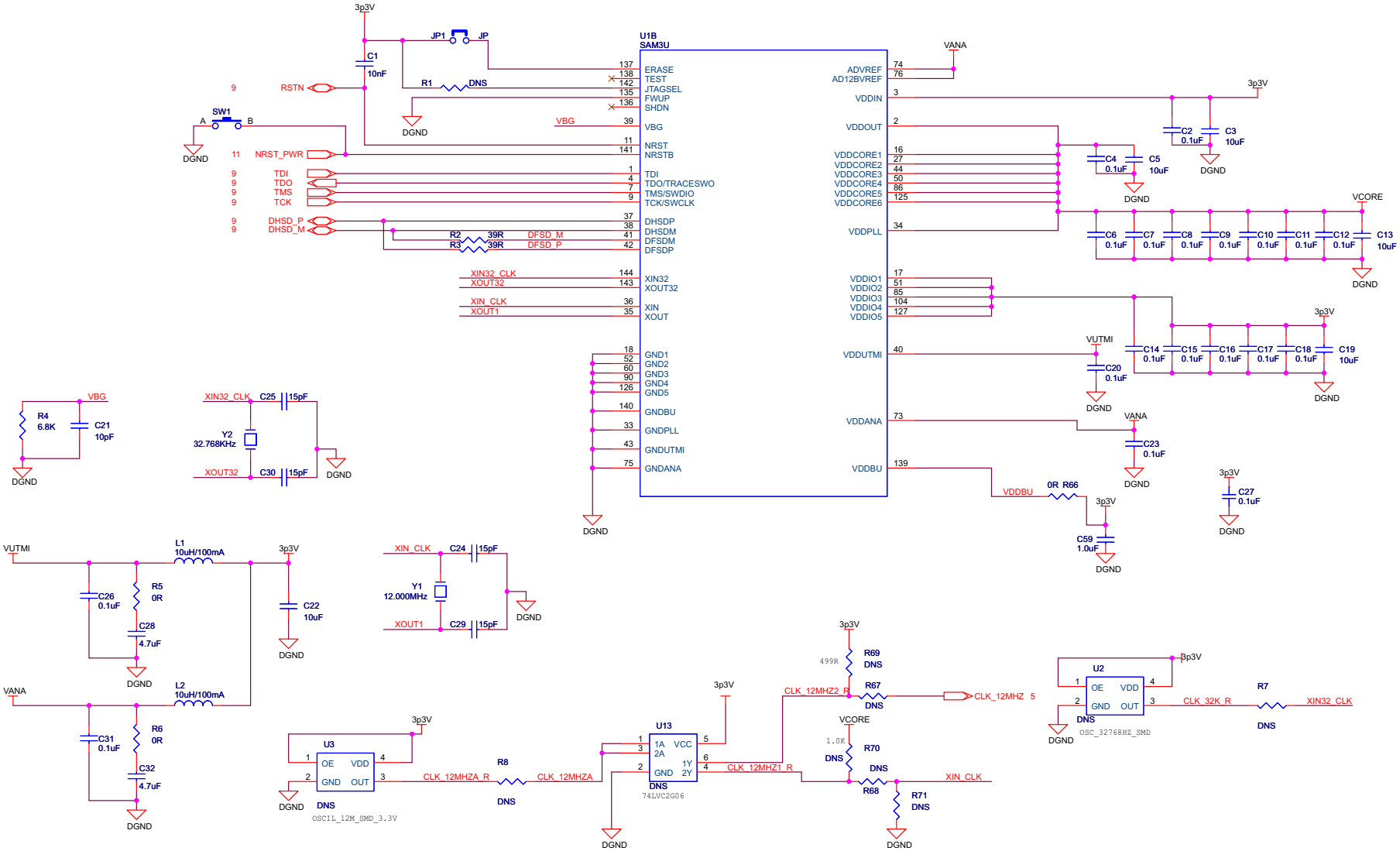

Figure 7. Atmel ARM Microcontroller: Power, Debug, and Analog

Atmel ARM Microcontroller, Port Connection

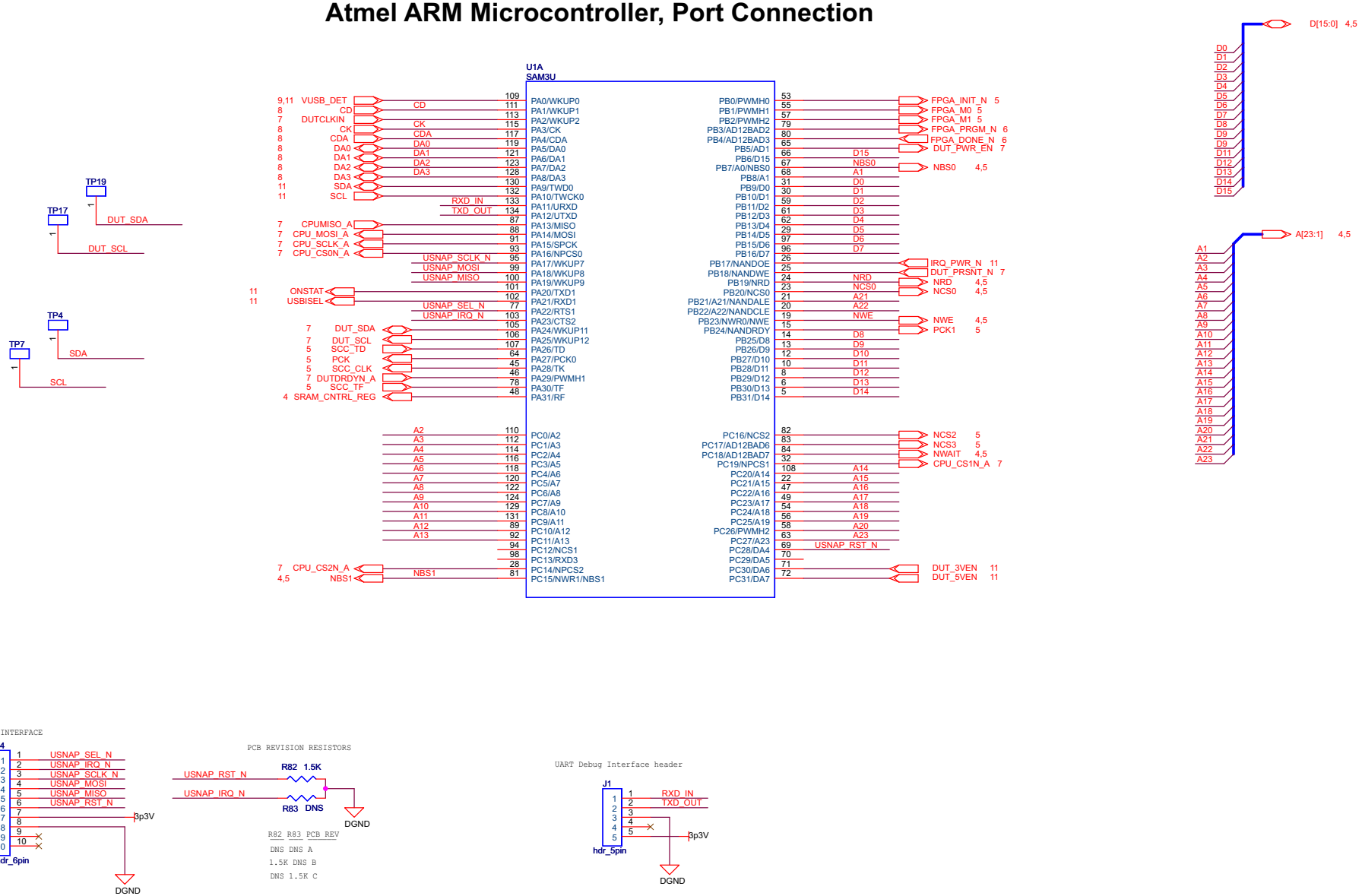

Figure 8. Atmel ARM Microcontroller and Port Connection

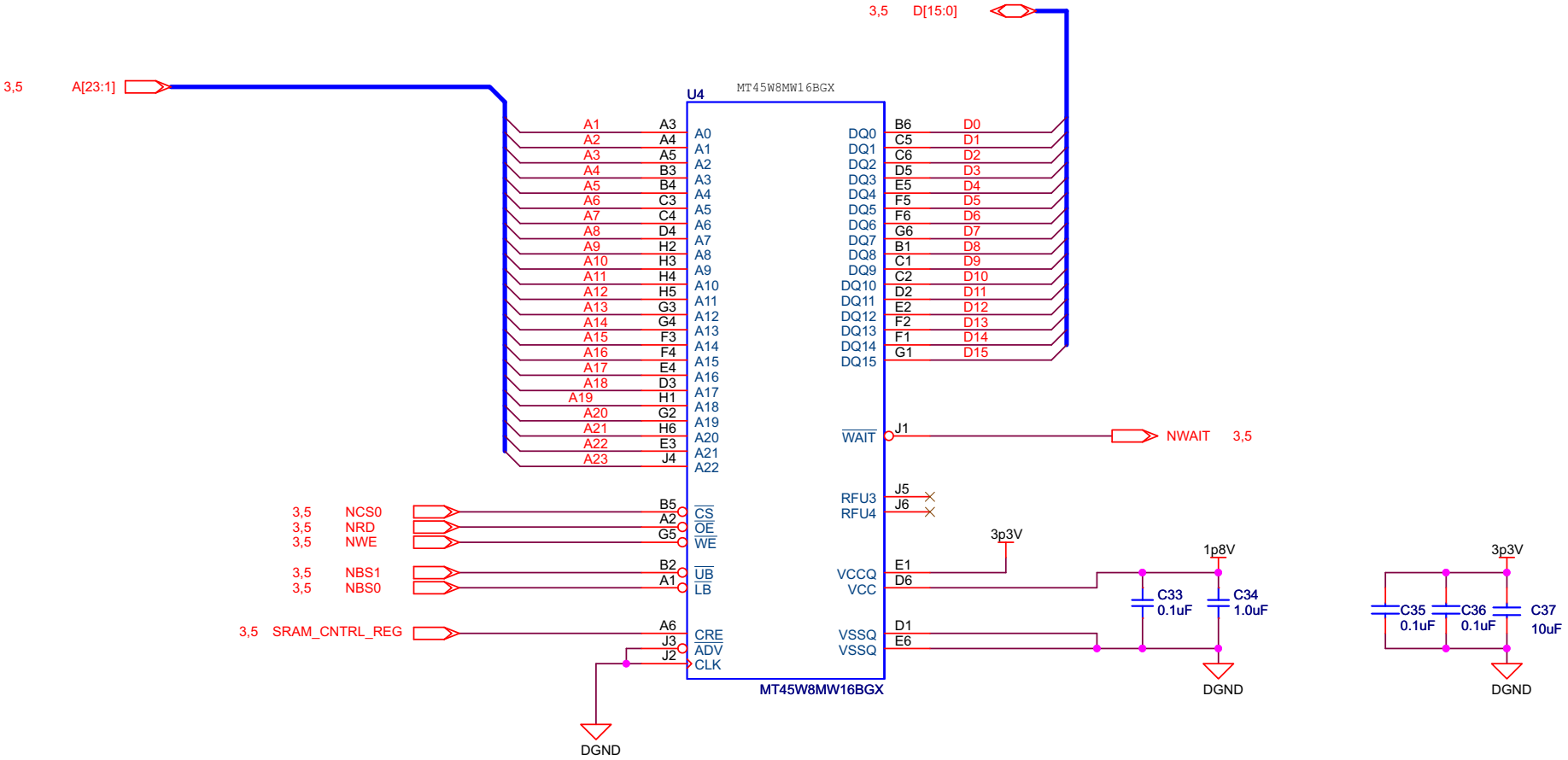

Figure 9. SPIO4 PSRAM

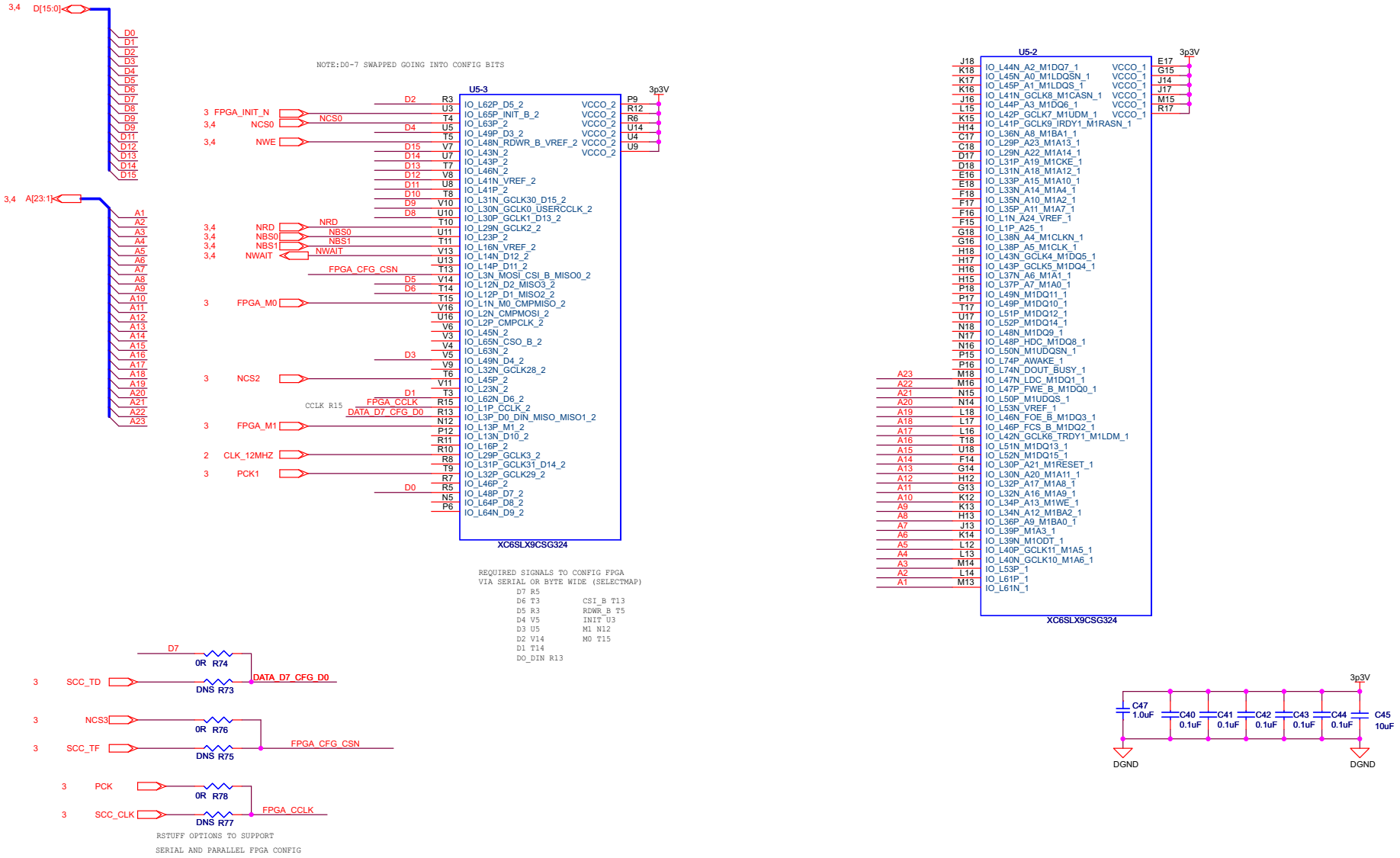

Figure 10. SPIO-4 FPGA SRAM and Configuration Interface

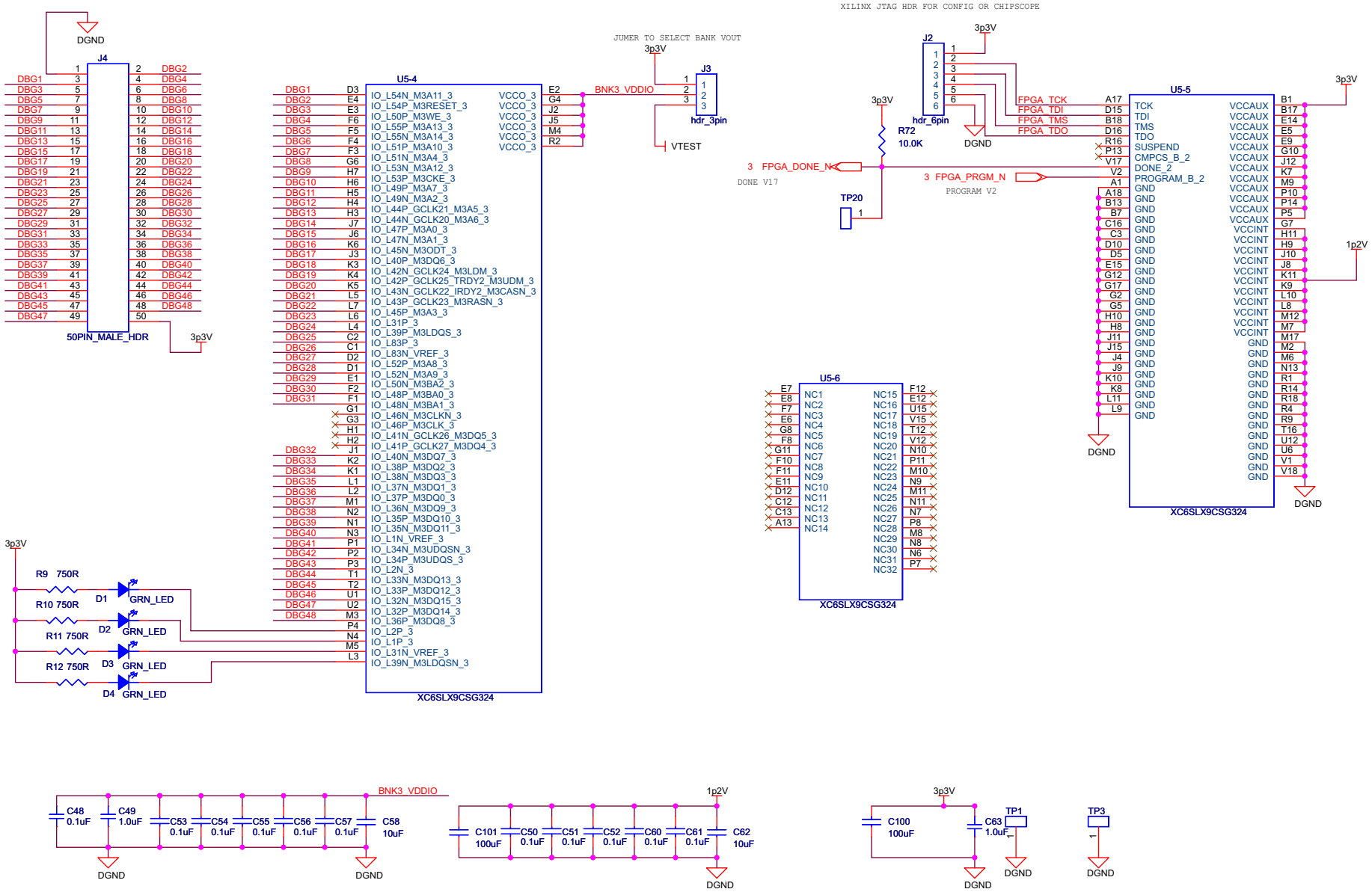

Figure 11. SPIO-4 FPGA DEBUG, JTAG Interfaces and Power

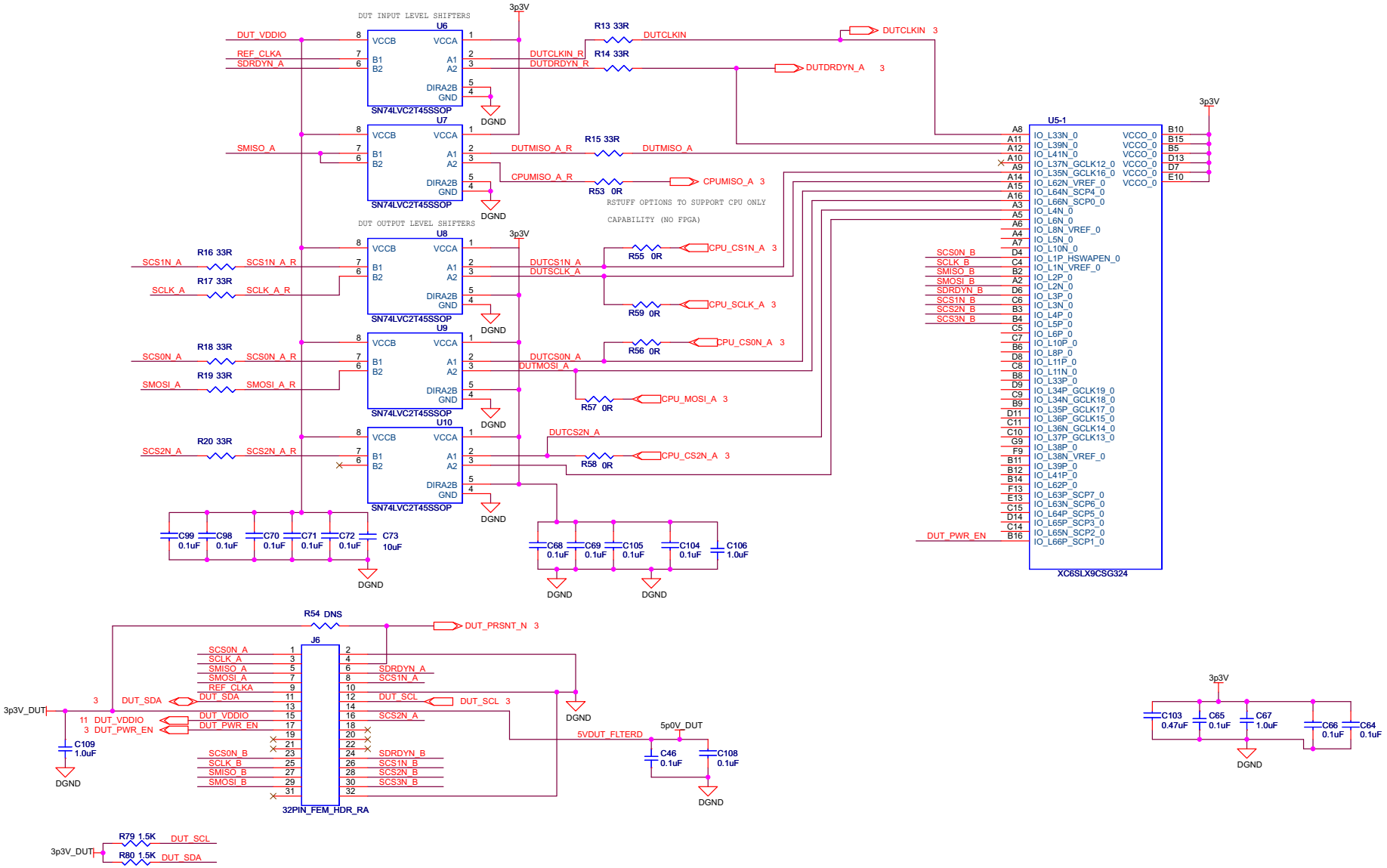

Figure 12. SPIO4 FPGA GPSI32 Interface

Micro SD Card

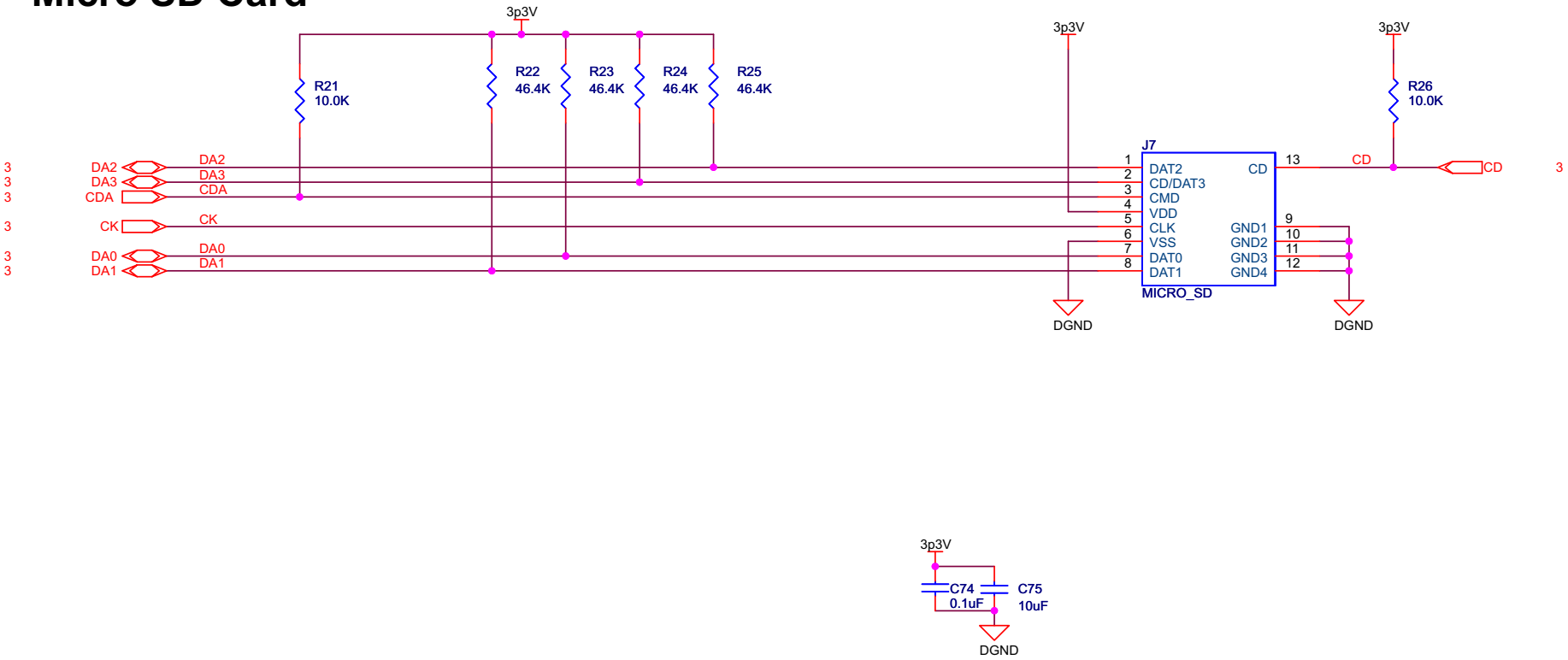

Figure 13. SPIO-4 Micro SD Card

USB, CPU JTAG

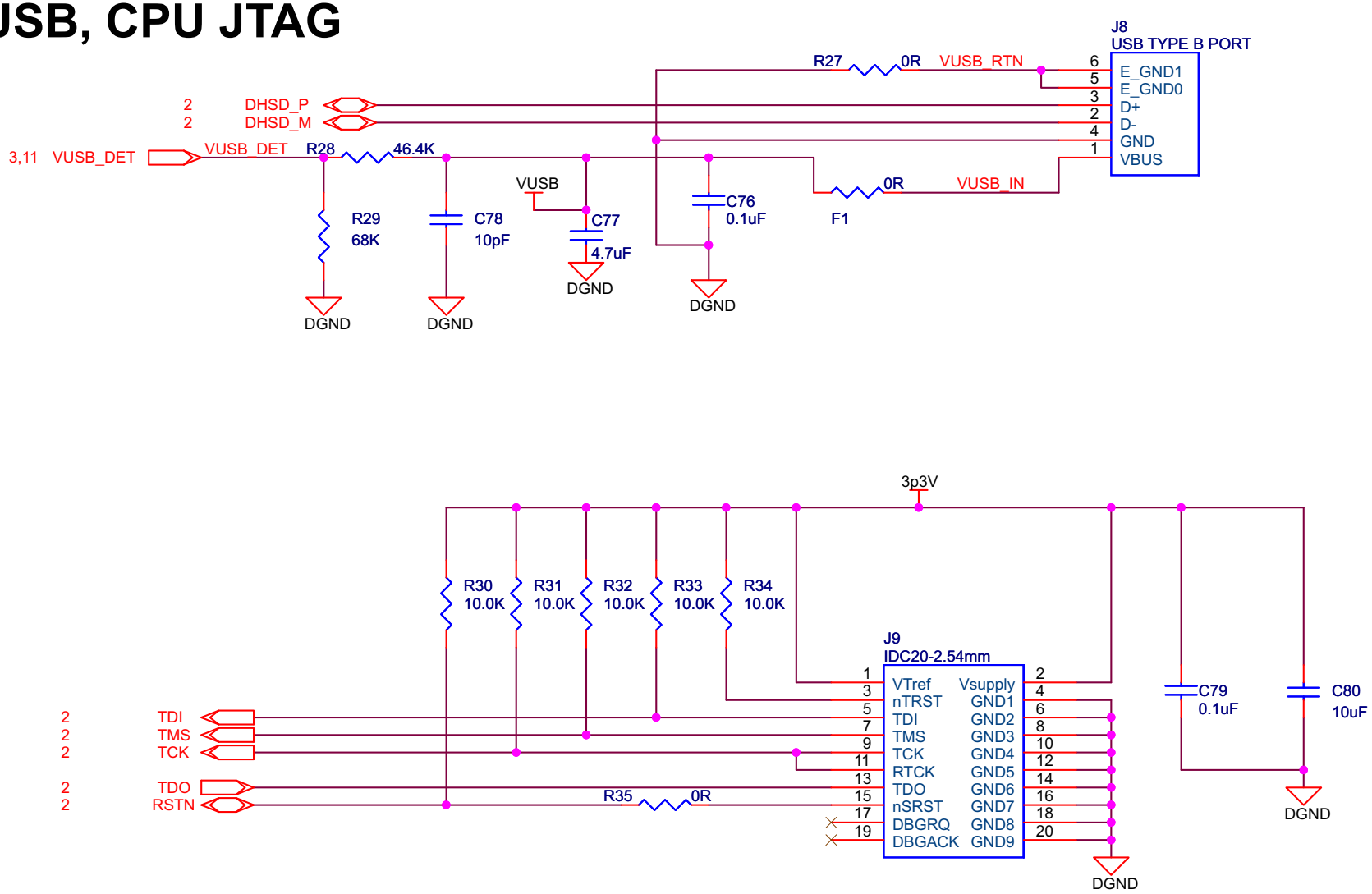

Figure 14. USB, CPU JTAG

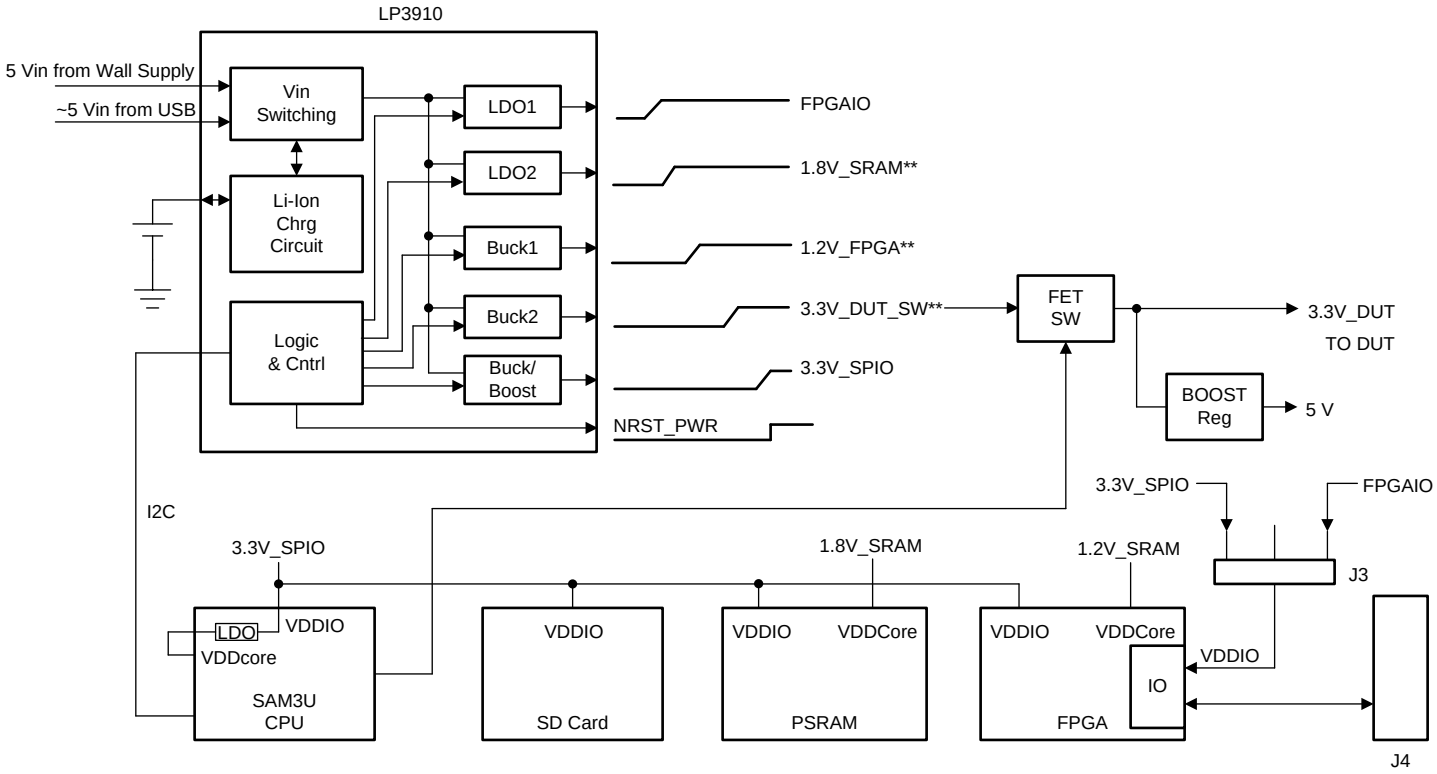

Figure 15. SPIO-4 Power Distribution

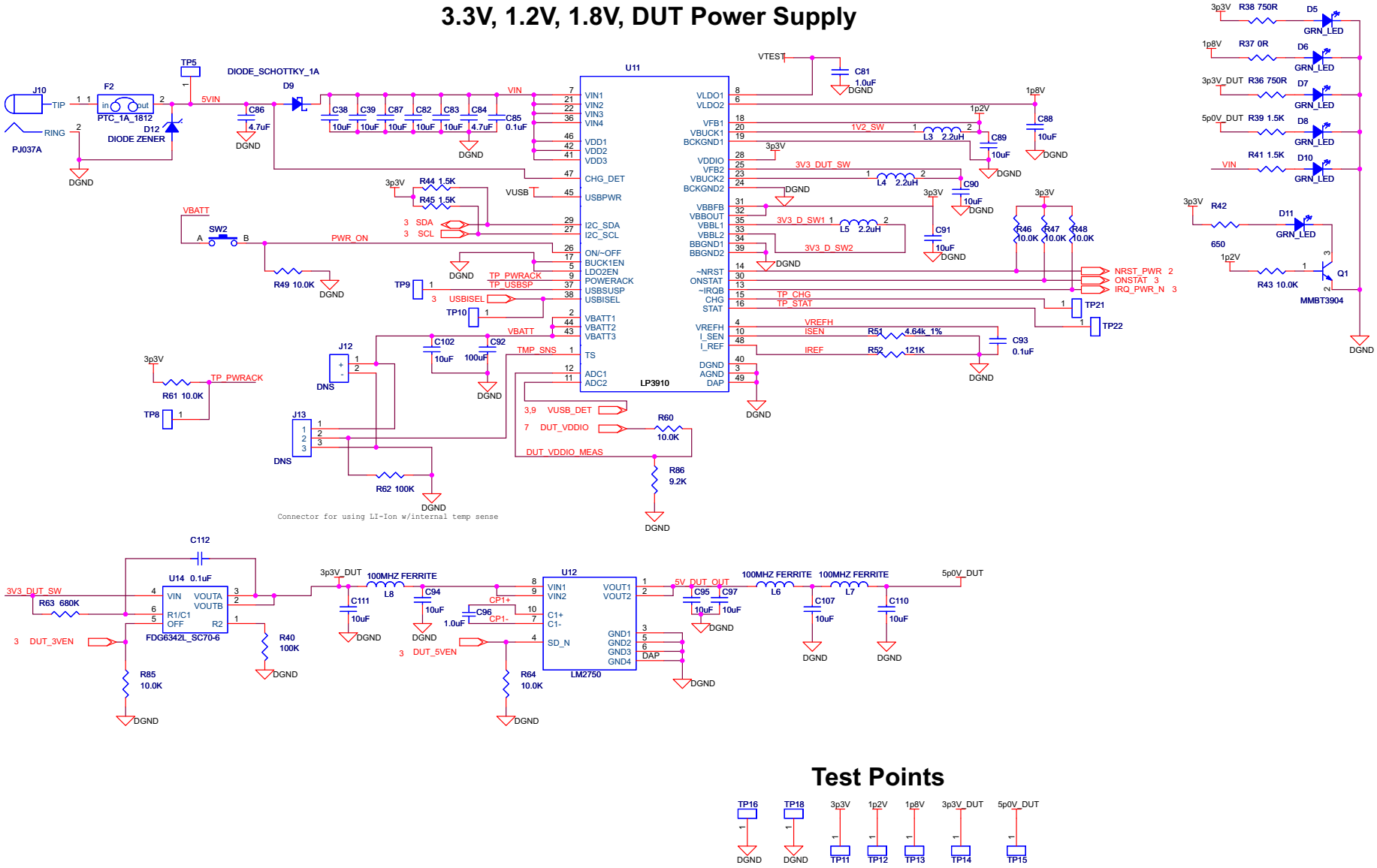

Figure 16. 3.3-V, 1.2-V, 1.8-V, and DUT Power Supplies

3.3 Bill of Materials (BOM)

Table 5 shows the bill of materials (BOM) for the SPIO-4 precision signal-path controller board.

Table 5. Bill of Materials

Item	Description	Qty	Reference	Manufacturer Name	Manufacturer No.
1	CAP CER 10000PF 25V Y5V 0603	1	C1	MURATA ELECTRONICS (VA)	GRM188F51E103ZA01D
2	CAP CER .47UF 10V X7R 0603	1	C103	TAIYO YUDEN (VA)	LMK107B7474KA-T
3	CAP .10UF 16V CERAMIC X7R 0603	58	C2,C4,C6,C7,C8,C9,C10,C11,C12,C14,C15,C16, C17,C18,C20,C23,C26,C27,C31,C33,C35,C36,C40, C41,C42,C43,C44,C46,C48,C50,C51,C52,C53,C54, C55,C56,C57,C60,C61,C64,C65,C66,C68,C69, C70,C71,C72,C74,C76,C79,C85,C93,C98,C99,C104, C105, C108,C112	YAGEO (VA)	CC0603KRX7R7BB104
4	CAP CERAMIC 10PF 50V NP0 0603	2	C21,C78	KEMET (VA)	C0603C100J5GACTU
5	CAP CER 15PF 50V C0G 5% 0603	4	C24,C25,C29,C30	TDK CORPORATION (VA)	C1608C0G1H150J
6	CAP CER 4.7UF 10V Y5V 0603	5	C28,C32,C77,C84,C86	MURATA ELECTRONICS (VA)	GRM188F51A475ZE20D
7	CAP CER 10UF 6.3V Y5V 0603	22	C3,C5,C13,C19,C22,C37,C38,C39,C45,C58,C62, C73,C75,C80,C82,C83,C87,C88,C89,C90,C91,C102	TDK CORPORATION (VA)	C1608Y5V0J106Z
8	CAP CER 1.0UF 10V X7R 0603	9	C34,C47,C49,C59,C63,C67,C81,C106,C109	TAIYO YUDEN (VA)	LMK107B7105KA-T
9	CAP CER 100UF 10V X5R 1210	3	C92,C100,C101	TAIYO YUDEN (VA)	LMK325BJ107MM-T
10	CAP CER 10UF 10V X5R 0805	6	C94,C95,C97,C107,C110,C111	JOHANSON DIELECTRICS INC (VA)	100R15X106KV4E
11	CAP CER 1.0UF 16V X7R 20% 1206	1	C96	TDK CORPORATION (VA)	C3216X7R1C105M/0.85
12	LED TOPLED 570NM GREEN CLR SMD	10	D1,D2,D3,D4,D5,D6,D7,D8,D10,D11	OSRAM OPTO SEMICONDUCTORS INC(VA)	LG M67K-G1J2-24-0-2-R18-Z
13	DIODE ZENER 6.2V 3W DO214AA	1	D12	MICRO COMMERCIAL CO (VA)	3SMBJ5920B-TP
14	DIODE SCHOTTKY 1A 20V SOD-123	1	D9	MICRO COMMERCIAL CO (VA)	MBRX120LF-TP
15	RES 0.0 OHM 1/2W 1210 SMD	1	F1	VISHAY/DALE (VA)	CRCW12100000Z0EA
16	PTC RESETTABLE 1.10A 16V 1812	1	F2	BOURNS INC (VA)	MF-MSMF110/16-2
17	CONN HEADER VERT 5POS .100 TIN	1	J1	TYCO ELECTRONICS AMP	640454-5
18	CON PWR JCK 2.0 X 6.5MM W/O SW	1	J10	CUI INC	PJ-037A
19	CONN HEADER 10POS 2MM VERT T/H	1	J14	3M	951110-8622-AR
20	CONN HEADER VERT SGL 6POS GOLD	1	J2	3M	961106-6404-AR
21	BERGSTIK II .100" SR STRAIGHT	1	J3	FCI	68000-203HLF
22	CONN FEMALE 32POS DL .1" R/A TIN	1	J6	SULLINS CONNECTOR SOLUTIONS	PPTC162LJBN-RC
23	CONN MICRO SD R/A HING TYPE SMD	1	J7	HIROSE ELECTRIC CO LTD (VA)	DM3C-SF
24	CONN RCPT USB TYPE B R/A PCB	1	J8	FCI	61729-0010BLF
25	CONN HEADER 2.54MM 20POS GOLD	1	J9	SULLINS CONNECTOR SOLUTIONS	SBH11-PBPC-D10-ST-BK
26	BERGSTIK II .100" SR STRAIGHT	1	JP1	FCI	68001-202HLF

Table 5. Bill of Materials (continued)

Item	Description	Qty	Reference	Manufacturer Name	Manufacturer No.
27	INDUCTOR 10UH 100MA 0805	2	L1,L2	MURATA ELECTRONICS (VA)	LQM21FN100M70L
28	INDUCTOR 2.2UH 1.20A 20% 1210	3	L3,L4,L5	TDK CORPORATION (VA)	NLCV32T-2R2M-PFR
29	FERRITE CHIP 2700 OHM 200MA 0805	3	L6,L7,L8	MURATA ELECTRONICS (VA)	BLM21BD272SN1L
30	TRANSISTOR NPN GP 40V SOT23	1	Q1	MICRO COMMERCIAL CO (VA)	MMBT3904-TP
31	RES 33.0 OHM 1/10W 1% 0603 SMD	8	R13,R14,R15,R16,R17,R18,R19,R20	YAGEO (VA)	RC0603FR-0733RL
32	RES 39 OHM 1/10W 5% 0603 SMD	2	R2,R3	PANASONIC - ECG (VA)	ERJ-3GEYJ390V
33	RES 10K OHM 1/10W 1% 0603 SMD	17	R21,R26,R30,R31,R32,R33,R34,R43,R46,R47,R48, R49,R60,R61, R64,R72,R85	STACKPOLE ELECTRONICS INC (VA)	RMCF0603FT10K0
34	RES 46.4K OHM 1/10W 1% 0603 SMD	5	R22,R23,R24,R25,R28	STACKPOLE ELECTRONICS INC (VA)	RMCF0603FT46K4
35	RES 68K OHM 1/10W 5% 0603 SMD	1	R29	PANASONIC - ECG (VA)	ERJ-3GEYJ683V
36	RES 1.5K OHM 1/10W 5% 0603 SMD	7	R39,R41,R44,R45,R79,R80,R82	STACKPOLE ELECTRONICS INC (VA)	RMCF0603JT1K50
37	RES 6.8K OHM 1/10W 1% 0603 SMD	1	R4	STACKPOLE ELECTRONICS INC (VA)	RMCF0603FT6K80
38	RES 100K OHM 1/10W 1% 0603 SMD	2	R40,R62	STACKPOLE ELECTRONICS INC (VA)	RMCF0603FT100K
39	RES 649 OHM 1/10W 1% 0603 SMD	1	R42	PANASONIC - ECG (VA)	ERJ-3EKF6490V
40	RES 0.0 OHM 1/10W 0603 SMD	15	R5,R6,R27,R35,R37,R53,R55,R56,R57,R58,R59, R66,R74,R76,R78	STACKPOLE ELECTRONICS INC (VA)	RMCF0603ZT0R00
41	RES 4.64K OHM 1/10W 1% 0603 SMD	1	R51	PANASONIC - ECG (VA)	ERJ-3EKF4641V
42	RES 121K OHM 1/10W 1% 0603 SMD	1	R52	STACKPOLE ELECTRONICS INC (VA)	RMCF0603FT121K
43	RES 680K OHM 1/10W 5% 0603 SMD	1	R63	PANASONIC - ECG (VA)	ERJ-3GEYJ684V
44	RES 9.1K OHM 1/10W 5% 0603 SMD	1	R86	PANASONIC - ECG (VA)	ERJ-3GEYJ912V
45	RES 750 OHM 1/10W 1% 0603 SMD	6	R9,R10,R11,R12,R36,R38	STACKPOLE ELECTRONICS INC (VA)	RMCF0603FT750R
46	SWITCH TACT SPST W/O GND SMD	2	SW1,SW2	OMRON ELECTRONICS INC-ECB DIV (VA)	B3U-1000P
47	PC TEST POINT MINIATURE SMT	14	TP1,TP3,TP4,TP5,TP7,TP11,TP12,TP13,TP14,TP15, TP16,TP17, TP18,TP19	KEYSTONE ELECTRONICS (VA)	5015
48	ATSAM3U4EA-AU-ND	1	U1		ATSAM3U4EA-AU-ND
49	LP3910SQ-AA	1	U11		LP3910SQ-AA
50	LM2750LD-5.0CT-ND	1	U12		LM2750LD-5.0CT-ND
51	IC LOAD SWITCH INTEGRATED SC70-6	1	U14	FAIRCHILD SEMICONDUCTOR (VA)	FDG6342L
52	IC PSRAM 128MBIT 70NS 54VFBGA	1	U4	MICRON TECHNOLOGY INC (VA)	MT45W8MW16BGX-701 IT TR
53	XC6SLX16-2CSG324C	1	U5		XC6SLX16-2CSG324C
54	IC BUS TRANSCVR 2BIT N-INV SM8	5	U6,U7,U8,U9,U10	TEXAS INSTRUMENTS (VA)	SN74LVC2T45DCTR
55	CRYSTAL 12.00 MHZ 8PF SMD	1	Y1	NDK (VA)	NX5032GA 12MHZ AT-W
56	CRYSTAL 32.768KHZ 12.5PF SMD	1	Y2	ABRACON CORPORATION (VA)	ABS10-32.768KHZ-T
57	PCB Fab	1	Fab	TEXAS INSTRUMENTS (VA)	551600474-001

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2010) to A Revision	Page
• Changed document to Texas Instruments format	1

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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