THE DATASHEET OF

SN65HVD257EVM

User's Guide
SLLU172–August 2012

SN65HVD257 CAN EVM: Functional Safety and Redundant CAN Network

This User Guide details the SN65HVD257 CAN EVM (Controller Area Network Evaluation Module) transceiver operation. It comes with two SN65HVD257 CAN transceivers factory installed, set up in a redundant (parallel) CAN bus configuration. The EVM may be reconfigured by a user for other CAN topologies. This User's Guide explains the EVM configurations for basic redundant CAN evaluation, and includes various load and termination settings.

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1 Introduction

1.1 Overview

Texas Instruments offers a broad portfolio of High Speed (HS) CAN transceivers compatible with the ISO11898-2 and ISO11898-5 High Speed CAN standards. These include 5V V_{CC} only, 3.3V V_{CC} only, 5V V_{CC} with IO level shifting and galvanic isolated CAN transceivers. These CAN transceiver families include product mixes with varying features such as low power standby modes with and without wake up, silent modes, loop back and diagnostic modes.

The Texas Instruments SN65HVD257 CAN EVM helps designers evaluate the operation and performance of the SN65HVD257 CAN transceiver. The SN65HVD257 includes many features for functional safety network implementation such as redundant CAN networks. The SN65HVD257 CAN EVM also provides PCB footprints for different bus terminations, bus filtering, and protection concepts. The EVM is provided with two SN65HVD257 devices installed. A separate EVM is available for the other CAN transceivers, SN65HVD255 CAN EVM, and another EVM uses the galvanic isolated CAN transceiver family (ISO1050).

The SN65HVD257 meets the ISO1189-2 High Speed CAN (Controller Area Network) Physical Layer standard (transceiver). It is designed as a next-generation CAN for the SN65HVD251 and ISO1050, but with added features for functional safety networks such as redundant networks. It has very fast loop times with a wide range of bus loading, allowing for data rates up to 1 megabit per second (Mbps) in long and highly loaded networks and higher data rates in small networks. The device includes many protection features to provide device and CAN network robustness. The device has two modes: normal mode and silent mode, selected on pin 8. The FAULT pin indicates TXD dominant time out, RXD dominant time out, thermal shut down and under voltage faults.

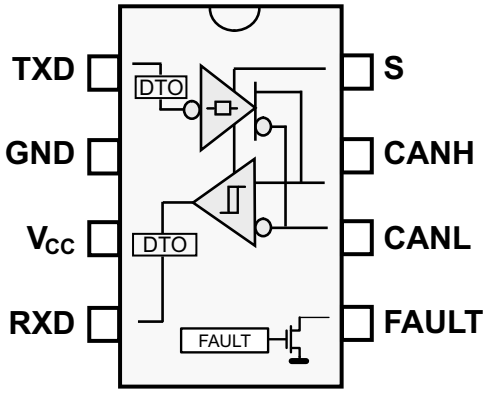

Figure 1. SN65HVD257 Basic Block Diagram and Pin Out

1.2 Example Using the SN65HVD257 in a Redundant Physical Layer CAN Network Topology

CAN is designed for standard linear bus topology using 120Ω twisted pair cabling. The SN65HVD257 CAN device includes several features that allow use of the CAN physical layer in nonstandard topologies with only one CAN link layer controller (µP) interface. The SN65HVD257 allows much greater flexibility in the physical topology of the bus while reducing the digital controller and software costs. The combination of RXD dominant time out and the FAULT output provides great flexibility, control and monitoring of these applications.

A simple example of this flexibility is to use two SN65HVD257 devices combined logically in parallel via an AND gate to build a redundant (parallel) physical layer (cabling and transceivers) CAN network. Adding a logic XOR with a filter adds automatic detection for a fault where one of the 2 networks goes open (recessive) in addition to the faults detected by the SN65HVD257.

To allow CAN's bit-wise arbitration to work, the RXD outputs of the transceivers must be connected via AND gate logic so that the link layer logic (µP) receives a dominant bit (low) from any of the branches; the transceivers appear to the link layer and above as a single physical network. The RXD dominant time out (DTO) feature prevents a bus stuck dominant fault in a single branch from taking down the entire network by returning the RXD pin for the transceivers on the branch with the fault to the recessive state (high) after

the t_{RXD_DTO} time. The remaining branch of the network continues to function. The FAULT pin of the transceivers on the branch with the fault shows this via the FAULT output to their host processors, which will diagnose the failure condition. The S-pin (silent mode pin) may be used to put a branch in silent mode to check each branch for other faults, including to look for bus open (recessive) faults. For automatic detection of a branch being open (recessive), an XOR gate may be used to combine the RXD outputs of both branches. During dominant bits (low), were the branches do not match the XOR, the circuit outputs a logic high. A small RC filter on the output eliminates false outputs due to small timing differences in the branches and transceivers. This XOR and the FAULT outputs of the transceivers could be connected to edge triggered interrupt pins on the host microprocessor to enter specialize software routines if there is an issue on the redundant network.

Thus it is possible build up a robust and redundant CAN network topology in a very simple and low cost manner. These concepts can be expanded into other more complicated and flexible CAN network topologies to solve various other system-level challenges with a networked infrastructure.

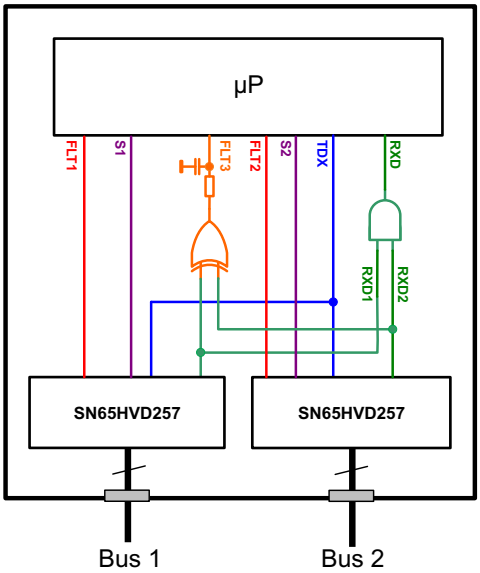

Figure 2. Typical SN65HVD257 Node To Build A Redundant Physical Layer Topology

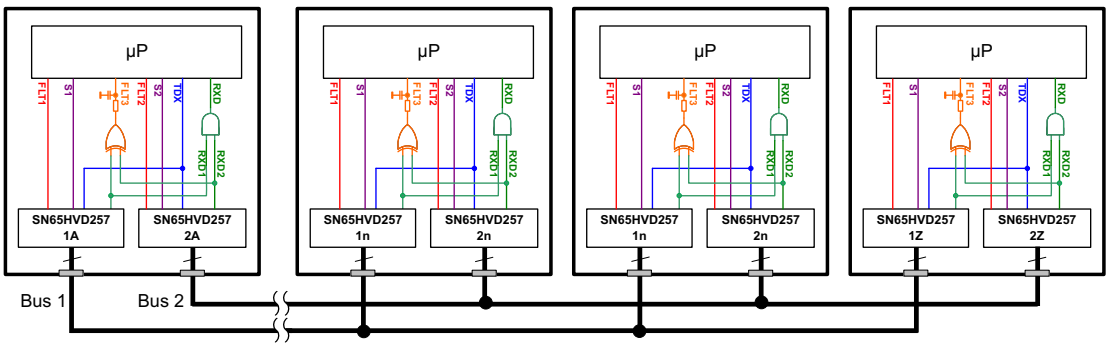

Figure 3. Typical Redundant Physical Layer Topology Using SN65HVD257

2 SN65HVD257 CAN EVM

The EVM consists of 2 CAN bus “nodes” and the necessary logic to build functional safety networks. It is pre-configured for redundant CAN network applications with the 2 CAN bus “nodes”, including the AND gate to combine the RXD output from both buses and the XOR gate and filter (50kHz) to detect a bus open fault. The EVM has simple connections to all necessary pins of the CAN transceiver devices and the necessary logic to create a redundant network. Jumpers are provided where necessary to provide flexibility for device pin and CAN bus configuration. There are test points (loops) for all main points where probing is necessary for evaluation such as GND, V_{CC}, TXD, RXD, CANH, CANL, S, FAULT. The EVM supports many options for CAN bus configuration. It is pre-configured with two 120Ω resistors that may be connected on the bus via jumpers; a single resistor is used with the EVM as a terminated line end (CAN is defined for 120Ω impedance twisted pair cable) or both resistors in parallel for electrical measurements representing the 60Ω load the transceiver “sees” in a properly terminated network (120Ω termination resistors at both ends of the cable). If the application requires “split” termination, TVS diodes for protection or Common Mode (CM) Choke the EVM has footprints available for these components via customer installation of the desired component(s).

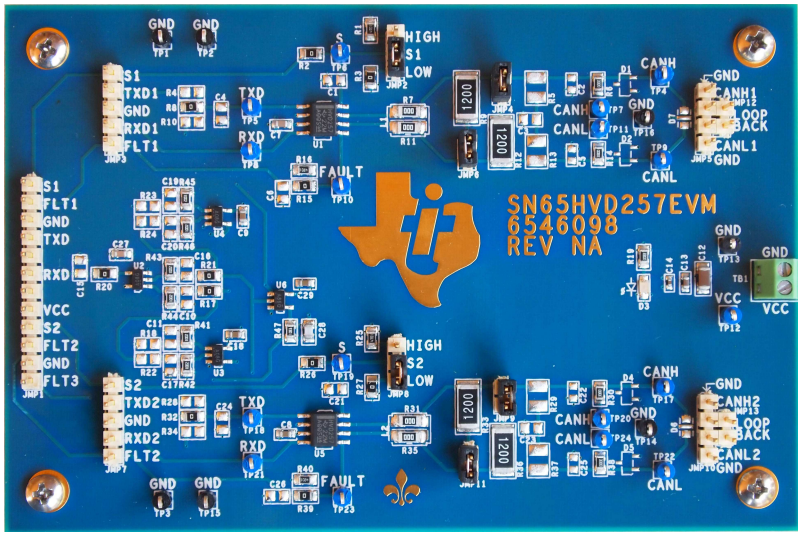

Figure 4. SN65HVD257 CAN EVM Top

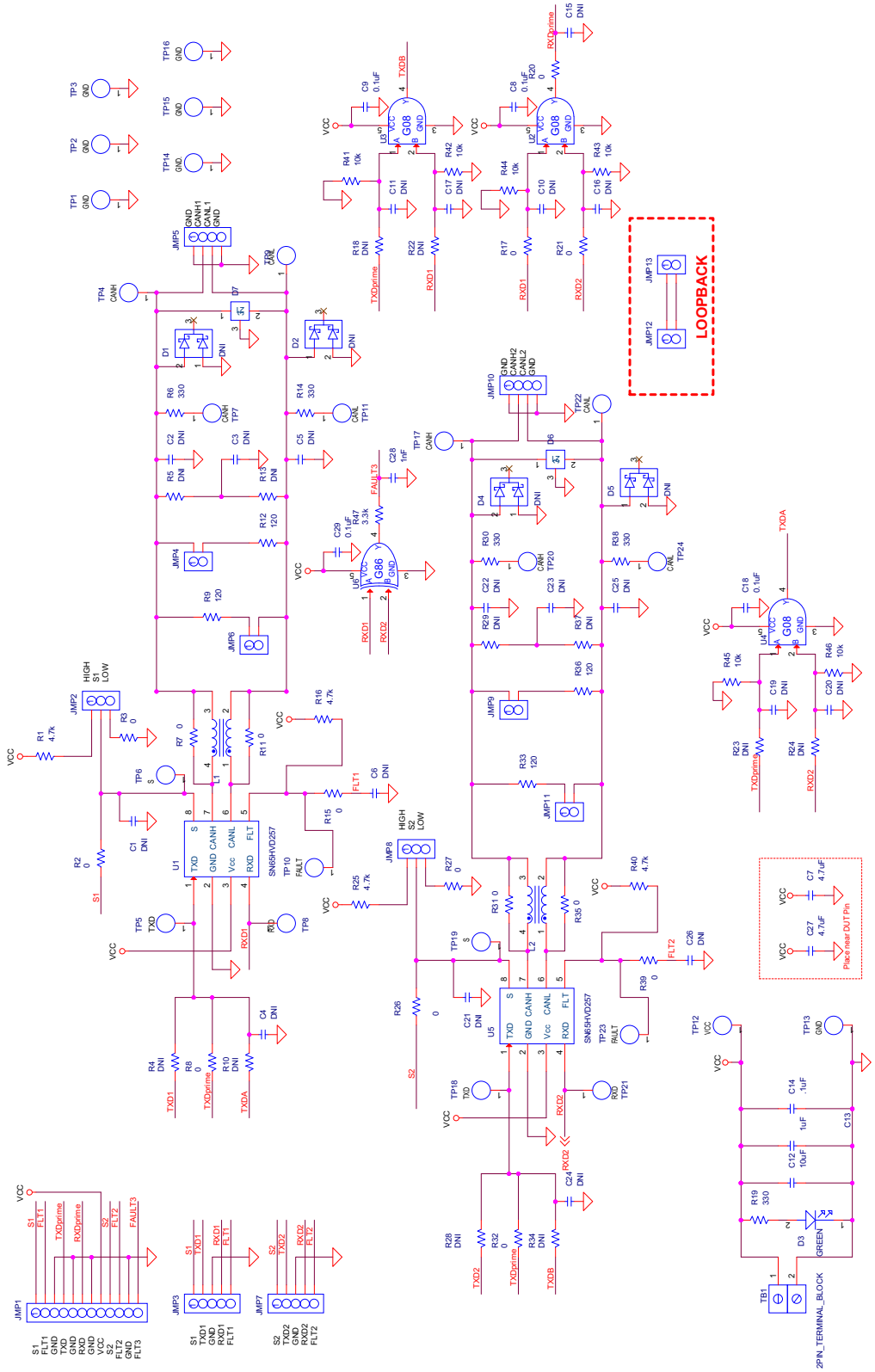

Figure 5. CAN EVM Schematic

Table 1. SN65HVD257 CAN EVM Connections

Connection	Type	Description
JMP1	12 pin header	Connection for access to all critical digital IO, supply and GND for driving the the CAN transceivers externally with test equipment or interfaced to a processor EVM
JMP2	3 pin jumper	S Mode Pin Control for transceiver 1
JMP3	5 pin header	Connection for access to all critical digital IO of the single transceiver 1 (bus) when EVM is used for 2 separate buses
JMP4	2 pin jumper	Connect 120Ω CAN termination to the bus. Used separately for a single termination if EVM is at end of the CAN bus and termination isn't in the cable. Used in combination with JMP6 to get to second CAN termination to represent the combined 60Ω load for CAN transceiver parametric measurement.
JMP5	4 pin header	Connection for access to transceiver 1 CAN bus output: CANH1, CANL1, GND, GND
JMP6	2 pin jumper	Connect 120Ω CAN termination to the bus. Used in combination with JMP4 to get to second CAN termination to represent the combined 60Ω load for CAN transceiver parametric measurement.
JMP7	5 pin header	Connection for access to all critical digital IO of the single transceiver 2 (bus) when EVM is used for 2 separate buses
JMP8	3 pin jumper	S Mode Pin Control for transceiver 2
JMP9	2 pin jumper	Connect 120Ω CAN termination to the bus. Used separately for a single termination if EVM is at end of the CAN bus and termination is not in the cable. Used in combination with JMP6 to get to second CAN termination to represent the combined 60Ω load for CAN transceiver parametric measurement.
JMP10	4 pin header	Connection for access to transceiver 2 CAN bus output: CANH2, CANL2, GND, GND.
JMP11	2 pin jumper	Connect 120Ω CAN termination to the bus. Used in combination with JMP4 to get to second CAN termination to represent the combined 60Ω load for CAN transceiver parametric measurement.
JMP12	2 pin jumper	Next to JMP5 to allow jumping CAN bus 1 to CAN bus 2
JMP13	2 pin jumper	Next to JMP10 to allow jumping CAN bus 1 to CAN bus 2
TB1	2 pin terminal block	V_{CC} supply and GND connection for the EVM
TP1	Test Point	GND test point
TP2	Test Point	GND test point
TP3	Test Point	GND test point
TP4	Test Point	CANH (bus 1) test point
TP5	Test Point	TXD, transceiver 1, test point
TP6	Test Point	S, transceiver 1, test point
TP7	Test Point	CANH (bus 1) via 330Ω serial resistor test point
TP8	Test Point	RXD, transceiver 1, test point
TP9	Test Point	CANL (bus 1) test point
TP10	Test Point	FAULT (transceiver 1) test point
TP7	Test Point	CANL (bus 1) via 330Ω serial resistor test point
TP12	Test Point	Vcc test point
TP13	Test Point	GND test point
TP14	Test Point	GND test point
TP15	Test Point	GND test point
TP16	Test Point	GND test point
TP17	Test Point	CANH (bus 2) test point
TP18	Test Point	TXD, transceiver 2, test point
TP19	Test Point	S, transceiver 2, test point
TP20	Test Point	CANH (bus 2) via 330Ω serial resistor test point
TP21	Test Point	RXD, transceiver 2, test point
TP22	Test Point	CANL (bus 2) test point
TP23	Test Point	FAULT (transceiver 2) test point
TP24	Test Point	CANL (bus 2) via 330Ω serial resistor test point

3 SN65HVD257 EVM Setup and Operation for Redundant (Parallel Networks)

This section describes the setup and operation of the EVM for parameter performance evaluation.

3.1 Overview and Basic Operation Settings

3.1.1 V_{CC} Power Supply (TB1 or TP12 or JMP1)

The basic setup of the EVM requires a single power supply to evaluate transceiver and network design performance. Supply V_{CC} on TB1, JMP1 header or via the V_{CC} and GND test point loops. The supplie powerd must meet the required specification of V_{CC} for the transceiver being tested. LED D3 indicates V_{CC}.

3.1.2 Main Supply and IO Header (JMP1)

All key IO and supply GND functions are brought to this header. It may be used to interface test equipment, or a short cable can be made to connect to an existing customer application board or MCU or DSP EVM board.

Table 2. Main Supply and IO Header (JMP1) Connections

Pin	Connection	Description
1	S1	Pin 5 of Transceiver 1. Used for Mode control.
2	FLT1	Pin 8 of Transceiver 1. Indicates fault with transceiver 1.
3	GND	GND
4	TXD	Pin 1 of Transceiver 1 and 2 (signal TXDprime). TXD (Transmit Data)
5	GND	GND
6	RXD	Pin 4 of Transceiver 1 and 2 combined via AND gate U2 (signal RXDprime). RXD (Receive Data)
7	GND	GND
8	VCC	Pin 3 of Transceiver. V_{CC}
9	S2	Pin 5 of Transceiver 2. Used for Mode control.
10	FLT2	Pin 8 of Transceiver 2. Indicates fault with transceiver 2.
11	GND	GND
12	FLT3	FAULT3: Open fault indicator. RXD (Pin 4) outputs of transceiver 1 and 2 combined via XOR gate U6 with filter (signal FAULT3). Indicates bus open faults.

3.1.3 TXD Input (JMP1)

The TXD input on JMP1 is connected via signal TXDprime to the TXD pin (pin 1) of both transceivers for redundant (parallel) transmission on both buses. Individually this signal may be observed at the transceiver pin via TP5 (transceiver 1) and TP18 (transceiver 2). The signal path TXDprime to the JMP1 header is pre-installed with a 0Ω series resistor, R10 and R34.

3.1.4 TXD Output (JMP1)

The RXD (combined) output of the transceivers via the AND gate for redundant (parallel) buses is JMP1. Individually the RXD signals may be seen at the transceiver pin via TP8 (transceiver 1) and TP21 (transceiver 2). The combined RXD (RXDprime) signal path to the JMP1 header is pre-installed with a 0Ω series resistor, R20 from the output of the AND gate U2.

3.1.5 S Pin (Mode Selection, pin 8) (JMP1, JMP2, JMP8, TP6 and TP19)

Pin 8 of the transceiver is the mode control pin of the device. Pin 8 of the devices is routed to JMP1, JMP2 and JMP8.

MODE SELECTION OPTIONS

JMP1 configuration:
Using header JMP1 (which assumes all the digital IO signals), V_{CC}, GND are routed to an external system. Ensure that the MODE (JMP2 and JMP8) jumper settings are not conflicting with signals to JMP1.

JMP2, transceiver 1 configuration (3 way jumper):
If using separate IO inputs, use JMP2 to configure the S pin (pin 8) of transceiver 1 to a pull up to V_{CC} (Silent Mode), or pull down to GND (Normal Mode).

JMP8, transceiver 2 configuration (3 way jumper):
If using separate IO inputs, use JMP8 to configure the S pin (pin 8) of transceiver 2 to a pull up to VCC (Silent Mode) or pull down to GND (Normal Mode).

TP6, transceiver 1 configuration:
This test point connects directly to the S pin (pin 8) of transceiver 1. Ensure that JMP1 and JMP2 are not configured to conflict if TP3 is used as the input connection.

TP19, transceiver 2 configuration:
This test point connects directly to the S pin (pin 8) of transceiver 2. Ensure that JMP1 and JMP8 are not configured to conflict if TP19 is used as the input connection.

3.1.6 FLT 1 (FAULT, pin 5, transceiver 1) (JMP1, TP10)

Pin 5 of transceiver 1 is the fault output of the transceiver. This output is routed to JMP1 and TP10. This output indicates a RXD DTO, TXD DTO, Thermal Shut Down or undervoltage fault with transceiver 1.

3.1.7 FLT 2 (FAULT, pin 5, transceiver 2) (JMP1, TP23)

Pin 5 of transceiver 2 is the fault output of the transceiver. This output is routed to JMP1 and TP23. This output indicates a RXD DTO, TXD DTO, Thermal Shut Down or undervoltage fault with transceiver 2.

3.1.8 FLT 3 (bus open fault) (JMP1)

FLT3 is the fault output of the filtered XOR combination of the two transceiver (bus) outputs. FLT3 will transition any time the two buses do not match, and thus indicate that one of the buses is open. The output filter of this logic is pre-installed with a cut off frequency of 50kHz to all for large deviations in timing between 2 parallel buses. This filter could be tuned by the user to match the filtering requirements of the target application with respect to bit timing and how much reaction time, or “missing” dominant bits the application requires, the XOR filter output to then show a transition to the monitoring processor.

3.1.9 JMP3 configuration (not used for Redundant Networks):

Using header JMP3 requires EVM reconfiguration for other applications.

3.1.10 JMP7 configuration (not used for Redundant Networks):

Using header JMP7 requires EVM reconfiguration for other applications.

3.2 Using CAN Bus Load and Termination Configuration

Each bus of the EVM is populated with two 120Ω power resistors selectable via jumpers between CANH and CANL. By using one of the resistors, the EVM may be used as a terminated end of a bus. For electrical measurements to represent the total loading of the bus, use both 120Ω resistors in parallel to give the standard 60Ω load for parametric measurement. The EVM also has footprints for customer installation of split termination if the application requires it. The table below summarizes how to use these termination options. If split termination is used, care must be taken to match the resistors. The common-mode filter frequency may be calculated by: $f_c = 1 / (2 \pi R C)$. Normally, the split capacitance is in the range of 4.7nF to 100nF. Keep in mind that this is the common-mode filter frequency, not a differential filter that will impact the differential CAN signal directly.

Table 3. CAN Bus Termination Configuration

"Termination Configuration Bus 1"	**120Ω Resistors**		**Split Termination Footprints**		**CM Stabilizing Capacitor**
	JMP4	**JMP6**	**R5**	**R13**	**C3**
Standard Termination (120Ω)	shorted	open	NA	NA	NA
60Ω load - Electrical Parameterics	shorted	shorted	NA	NA	NA
Split Termination (Common Mode Stabilization)	open	open	60Ω	60Ω	populated
"Termination Configuration Bus 2"	**120Ω Resistors**		**Split Termination Footprints**		**CM Stabilizing Capacitor**
	JMP9	JMP11	R29	R37	C23
Standard Termination (120Ω)	shorted	open	NA	NA	NA
60Ω load - Electrical Parameterics	shorted	shorted	NA	NA	NA
Split Termination (Common Mode Stabilization)	open	open	60Ω	60Ω	populated

3.3 Using CAN Bus Protection and Filtering Configuration

The EVM also has component footprints for various protection schemes to enhance robustness for extreme system-level EMC requirements. Table 4 summarizes these options. Typical examples of for these components are: CM choke (TDK ACT45B series and EPCOS B82789 series from 11µH to 100µH), bus filter capacitors are typically 100pF or less, TVS diodes from the MMBZ series 27V or lower, varistors such as the TDK AVR series).

Table 4. CAN Bus Protection and Filtering Configuration

Protection and Filtering Bus 1	Footprint Reference	Use Case	Population and Description
Series Resistors or Common Mode Choke	R7 and R11 or L1 (common footprint)	Direct CAN transceiver to bus connection	R7 and R11 populated with 0Ω (default population)
		Series resistance protection CAN transceiver to bus connection	R7 and R11 populated with MELF resistor as necessary for harsh EMC environment
		CM choke (bus filter)	L1 populated with CM choke to filter noise as necessary for harsh EMC environment
Bus Filtering Caps	C2 and C5	Bus filter	Filter noise as necessary for harsh EMC environment. Filter caps may be used in combination with L1 CM choke.
Transient Protection	D1 and D2, C2 and C7 or D7	Transient & ESD Protection	To add extra protection for system level transients and ESD protection, use the population option footprints D1 and D2 for TVS diodes, or C2 and C7 or D7 for varistors.
Protection and Filtering Bus 2	**Footprint Reference**	**Use Case**	**Population and Description**
Series Resistors or Common Mode Choke	R31 and R35 or L2 (common footprint)	Direct CAN transceiver to bus connection	R31 and R35 populated with 0Ω (default population)
		Series resistance protection CAN transceiver to bus connection	R31 and R35 populated with MELF resistor as necessary for harsh EMC environment
		CM choke (bus filter)	L2 populated with CM choke to filter noise as necessary for harsh EMC environment
Bus Filtering Caps	C22 and C25	Bus filter	Filter noise as necessary for harsh EMC environment. Filter caps may be used in combination with L2 CM choke.
Transient Protection	D4 and D5, C22 and C25 or D6	Transient & ESD Protection	To add extra protection for system level transients and ESD protection, use the population option footprints D4 and D5 for TVS diodes or C22 and C25 or D6 for varistors.

3.4 Using Customer Installable IO Options for Current Limiting, Pull up or down, Noise Filtering

The EVM has footprints on the PCB for the installation of various filtering and protection options to adapt the EVM to match CAN network topology requirements if the EVM is being used as a CAN node.

Each digital input or output pin has footprints to allow for series current limiting resistors (default populated with 0Ω), pull up or down resistors depending on pin use and a capacitor to GND which, configured with the serial resistor, implements RC filters (for noisy environments). The table below lists these features for each of the digital input and output pins of the EVM. Replace or populate the RC components as necessary for the application. The RC output filter pads for may be reused as a resistor divider network to level shift the outputs down to 3.3V levels. The SN65HVD257 already has 3.3V compatible inputs on TXD and S pins.

Table 5. EVM Digital IO Configuration

Signal		Jumper		Series R	Pull Up or Down	C to GND	Description
Description	Type	Pull Up	Pull Down				
TXD U1	Input	NA	NA	R8 (R4/R10)	NA	NA	TXD input from JMP1 to TXD U1
TXD U2	Input	NA	NA	R32 (R28/R34)	NA	NA	TXD input from JMP1 to TXD U2
RXD U1	Output	NA	NA	R17	R44 PD (10k)	C10	RXD U1 output to AND Gate for combined RXD redundant output
RXD U2	Output	NA	NA	R17	R43 PD (10k)	C16	RXD U1 output to AND Gate for combined RXD redundant output
RXDprime	Output	NA	NA	R20	NA	C15	RXDprime is the combined RXD output from the parallel CAN buses via AND gate U2 which is routed to JMP1 as RXD
S U1	Input	R1 (JMP2)	R3 (JMP2)	R2	NA	C1	S (Mode) pin input from JMP1 or PU or PD to S U1
S U2	Input	R25 (JMP2)	R27 (JMP2)	R26	NA	C21	S (Mode) pin input from JMP1 or PU or PD to S U2
FLT3	Output	NA	NA	R47 (3.3k)	NA	C28 (1nF)	FAULT3 is the combined RXD output from the parallel CAN buses via XOR gate U6 with the RC filter populated which is routed to JMP1 as FLT3.

3.5 Using customer installable IO options for 3.3V IO

The EVM may be configured to have a 3.3V level output through the repurposing of the RC output filter pads. These RC pads may be reused as a resistor divider network to level shift the outputs down to 3.3V levels. The SN65HVD257 already has 3.3V compatible inputs on the TXD and S pins. Table 6 shows some examples. For use in applications, calculations must be made to ensure the resistor divider network chosen adheres to the application requirement. Considerations should include: current biasing in the resistor network (loading, power), ensuring that the V_{OH} and V_{OL} of the divider will meet the V_{IH} and V_{IL} input threshold levels of the host processor, and that the output of the resistor divider will be below the absolute maximum rating of the host processor at the absolute maximum rating of the transceiver (or the worst case corner the application will provide).

Table 6. EVM Digital IO Configuration

Output	R1 Pad and Value	R2 Pad and Value	Description
RXDprime	R20 = 3.9 kΩ	C15 = 6.8 kΩ	C15 pad is repurposed as R2.
FLT1	R15 = 0 Ω R16 = 4.7k Ω	C6 = 8.2 kΩ	R1 is the pull up R16. C6 pad is repurposed as R2.
FLT2	"R39 = 0 Ω R40 = 4.7kΩ	C26 = 8.2 kΩ	R1 is the pull up R 40. C26 pad is repurposed as R2.
FLT3	R47 = 3.9 kΩ	C28 = 1nF and 6.8 kΩ	C28 pad is repurposed as R2 and filter C (stacked components).

4 SN65HVD257 EVM Configuration for Two Independent Networks

This section describes how to reconfigure the EVM into two independent networks. With this configuration, the EVM could be used to host two node physical layers. The sections of the EVM not specifically described below such as termination, filtering and protection are used in the same or similar fashion as when the EVM is configured for a redundant network.

4.1 Transceiver 1 Header (JMP3)

4.1.1 TXD1 Input (JMP3, TP5)

The TXD1 input on JMP3 connects to transceiver 1 (U1) and TP5. To reconfigure the EVM, R8 must be removed to disconnect TXDprime from U1, and R4 must be installed with a 0Ω resistor or current limiting serial resistor of choice for the application to route the TXD1 signal to U1.

4.1.2 RXD1 Output (JMP3, TP8)

The RXD1 output of transceiver 1 (U1) is routed to JMP3 and TP8. If no parasitic loading to the combining AND gate U2 is desired, then R17 may be removed.

4.1.3 S1 Input (Mode Selection,) (JMP3, JMP2 and TP6)

Pin 8 of the transceiver is the mode control pin of the device. Pin 8 of transceiver 1 is routed to JMP3, JMP2 and TP6.

MODE SELECTION OPTIONS

JMP3, transceiver 1 header configuration:
Header JMP3 handles all the digital IO signals for transceiver 1. JMP3 may be used to route these signals to an external host processor or test system. Make sure that the MODE (JMP2) jumper settings are not conflicting with signals to JMP3.

JMP2, transceiver 1 configuration (3 way jumper):
If the header is not used, then JMP2 may be used to configure the S pin (pin 8) of transceiver 1 to a pull up to V_{CC} (Silent Mode) or pull down to GND (Normal Mode).

TP6, transceiver 1 configuration:
This test point connects directly to the S pin (pin 8) of transceiver 1. Ensure that JMP3 and JMP2 are not configured to conflict if TP3 is used as the input connection.

4.1.4 FLT1 Output (JMP3, TP10)

Pin 5 of transceiver 1 is the fault output of the transceiver. This output routes to JMP3 and TP10. This output indicates a RXD DTO, TXD DTO, Thermal Shut Down or undervoltage fault with transceiver 1.

4.2 Transceiver 2 Header (JMP7)

4.2.1 TXD2 Input (JMP7, TP18)

The TXD2 input on JMP7 is connected to transceiver 2 (U5) and TP5. To reconfigure the EVM, R32 must be removed to disconnect TXDprime from U5, and R28 must be installed with a 0Ω resistor or current limiting serial resistor of choice for the application to route the TXD2 signal to U5.

4.2.2 RXD2 Output (JMP7, TP21)

The RXD2 output of transceiver 2 (U5) is routed to JMP7 and TP21. If no parasitic loading to the combining AND gate U2 is desired, then R21 may be removed.

4.2.3 S2 Input (Mode Selection,) (JMP7, JMP8 and TP19)

Pin 8 of the transceiver is the mode control pin of the device. Pin 8 of transceiver 2 is routed to JMP7, JMP8 and TP19.

MODE SELECTION OPTIONS

JMP7, transceiver 2 header configuration:
Header JMP7 handles all the digital IO signals for transceiver 2. JMP7 may be used to route the signals to an external host processor or test system. Ensure that the MODE (JMP8) jumper settings are not conflicting with signals to JMP7.

JMP8, transceiver 2 configuration (3 way jumper):
If the header is not used, then JMP8 may be used to configure S pin (pin 8) of transceiver 2 to a pull up to V_{CC} (Silent Mode) or pull down to GND (Normal Mode)

TP19, transceiver 2 configuration:
This test point connects directly to the S pin (pin 8) of transceiver 2. Ensure JMP7 and JMP8 are not configured to conflict if TP19 is used as the input connection.

4.2.4 FLT2 Output (JMP7, TP23)

Pin 5 of transceiver 2 is the fault output of the transceiver. This output routed to JMP7 and TP23. This output indicates a RXD DTO, TXD DTO, Thermal Shut Down or undervoltage fault with transceiver 2.

4.2.5 Loopback (single bus connection) of the Two Nodes (JMP12 and 13)

The EVM provides a path via JMP12 and JMP13 to connect to two nodes (transceivers) together on the board as a single CAN network. On node 1 (transceiver 1, U1) connect CANH1 and CANL1 across JMP5 and JMP12 as shown below. On node 2 (transceiver 2, U5) connect CANH2 and CANL2 across JMP10 and JMP13 as shown below. CANH1 is now connected to CANH2 and CANL1 is connected to CANL2 in one CAN network.

Figure 6. Loopback Node 1 (JMP5 to JMP12)

Figure 7. Loopback Node 2 (JMP10 to JMP13)

5 Bill of Material (BOM)

Item	QTY	Reference	Part	Footprint	Manufacturer
1	23	C1, C3, R4, C4, C6, R10, 10, C11, C15, C16, C17, C18, C19, C20, 21, R22, R23, C23, R24, C24, C26, R28, R34	DNI	805	ANY
2	4	C2, C5, C22, C25	DNI	603	ANY
3	2	C7, C27	4.7uF	603	ANY
4	4	C8, C9, C18, C29	0.1uF	603	ANY
5	1	C12	10uF	1206	ANY
6	1	C13	1uF	603	ANY
7	1	C14	0.1uF	402	ANY
8	1	C28	1nF	805	ANY
9	4	D1, D2, D4, D5	DNI	SOT_3DBZ	ANY
10	1	D3	GREEN	C170	ANY
11	2	D6, D7	DNI	CA05M2S10T100HG	TDK / EPCOS
12	1	JMP1	Header 1x12	HDR_THVT_1X12_100	ANY
13	2	JMP2, JMP8	Header 1x3	HDR_THVT_1X3_100	ANY
14	2	JMP3, JMP7	Header 1x5	HDR_THVT_1X5_100	ANY
15	6	JMP4, JMP6, JMP9, JMP11, JMP12, JMP13	Heder 1x2	HDR_THVT_1X2_100	ANY
16	2	JMP5, JMP10	Header 1x4	HDR_THVT_1X4_100	ANY
17	2	L1, L2	DNI	ACT45B or B82789 series CM choke	TDK / EPCOS
18	4	R1, R16, R25, R40	4.7k	805	ANY
19	11	R2, R3, R8, R15, R17, R20, R21, R26, R27, R32, R39	0	805	ANY
20	4	R3, R13, R29, R37	DNI	1210	ANY
21	5	R6, R14, 19, R30, R38	330	805	ANY
22	4	R7, R11, R31, R35	0	1206	ANY
23	4	R9, R12, R33, R36	120	2512	ANY
24	6	R41, R42, R43, R44, R45, R46	10k	805	ANY
25	1	R47	3.3k	805	ANY
26	1	TB1	2PIN_TERMINAL_BLOCK	TB_THRTSCR_1x2_100	ANY
27	18	TP4, TP5, TP6, TP7, TP8,TP9, TP10, TP11, TP12, TP13, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24	Test Point	HDR_THVT_1x1_100	ANY
28	6	TP1, TP2, TP3, TP14, TP15, TP16	Test Point	HDR_THVT_1x1_100	ANY
29	2	U1, U5	SN65HVD256D	SOIC_8D	TI
30	3	U2, U3, U4	SN74AHC1G86DBV	SOT_5DBV	TI
31	1	U6		SOT_5DBV	TI

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