



**THE DATASHEET OF
SD384EVK/NOPB**



SD384EVK LMH0384 Evaluation Board User Guide

National Semiconductor
EVK User Manual
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Overview

The SD384 Evaluation Kit (EVK) enables evaluation of the LMH0384 3G/HD/SD SDI Adaptive Cable Equalizer.

Evaluation Kit (SD384EVK) Contents

The EVK contains the following parts:

- SD384EVK board assembly with the LMH0384 cable equalizer
- SD384EVK User Guide

Evaluation Board Description

Figure 1 shows the SD384 evaluation board and highlights some of its features.

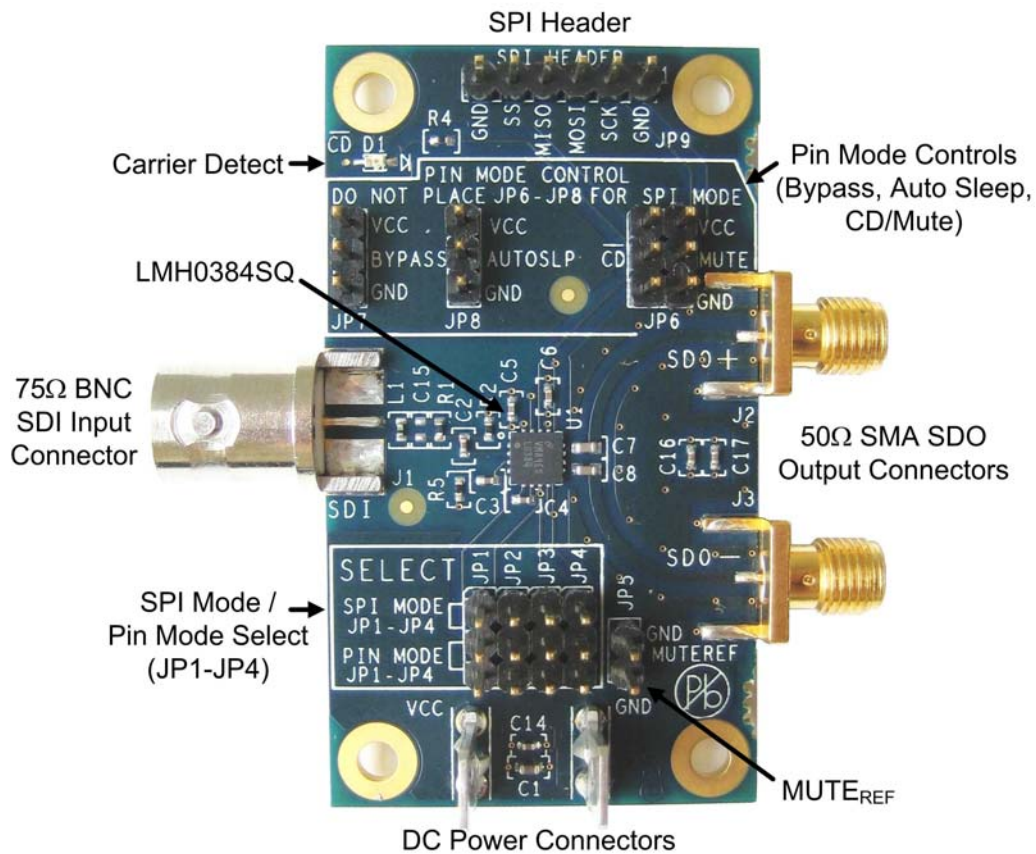


Figure 1. SD384 Evaluation Board

SDI Input and SDO Output

The SDI input connector (J1) is a 75Ω BNC connector. The SDI input should conform to the SMPTE 424M, SMPTE 292M, or SMPTE 259M standards.

The SDO output connectors (J2 and J3) are 50Ω SMA connectors. When using only one side of the output pair, the other side should be terminated with a 50Ω SMA termination. For example, when only using the SDO output, \overline{SDO} should be terminated with a 50Ω SMA termination.

DC Power Connectors

The VCC and GND power connectors should be powered with a DC input voltage of $3.3V \pm 5\%$ (3.6V maximum).

SPI Mode / Pin Mode Select (JP1 – JP4)

JP1, JP2, JP3, and JP4 are used to select between SPI Mode or Pin mode. To select Pin Mode, set four jumpers as shown in Figure 2, and to select SPI Mode, set four jumpers as shown in Figure 3. Either Pin Mode or SPI mode must be selected for proper operation; do not leave JP1-JP4 open.

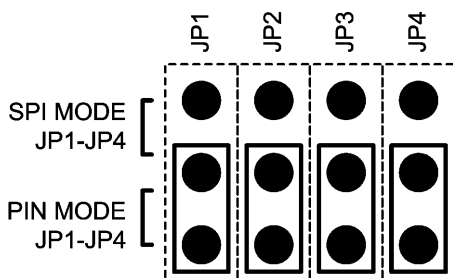


Figure 2. Pin Mode Select

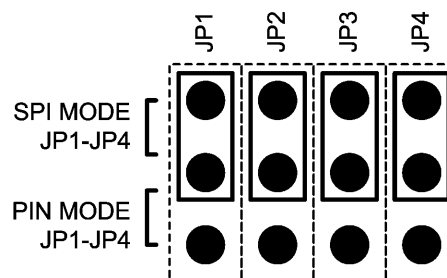


Figure 3. SPI Mode Select

MUTE_{REF} (JP5)

JP5 allows control of the MUTE_{REF} function and may be used in either Pin Mode or SPI Mode. MUTE_{REF} is an input voltage used to set the threshold for \overline{CD} . The MUTE_{REF} DC input voltage should be between 0V and 3.3V. Refer to the LMH0384 datasheet for details. Leave JP5 unconnected for normal operation.

Pin Mode Controls (JP6 – JP8)

JP6, JP7, and JP8 are used to control LMH0384 features while the device is configured for Pin Mode. **Jumpers should not be placed on JP6, JP7, or JP8 while the device is configured for SPI Mode.**

\overline{CD} and MUTE (JP6)

JP6 allows Carrier Detect (\overline{CD}) monitoring and MUTE control. \overline{CD} is high when no input signal is present. MUTE may be used to force the outputs on or off, or tied to \overline{CD} to allow automatic mute operation based on the input signal. To activate mute and force the outputs into a muted condition, set the jumper to pull MUTE to VCC. To turn off mute so that the outputs will never mute, set the jumper to tie MUTE to GND. For normal operation, set the jumper to tie \overline{CD} to MUTE for automatic mute control. The LMH0384 MUTE pin has an internal pulldown (to disable mute), so JP6 may be left unconnected and the LMH0384 will never mute.

BYPASS (JP7)

JP7 allows control of the equalization BYPASS function. To put the device into bypass mode, set the jumper to pull BYPASS to VCC. To turn off bypass (for normal operation) set the jumper to pull BYPASS to GND. The LMH0384 BYPASS pin has an internal pulldown (to disable bypass), so JP7 may be left unconnected for normal operation.

AUTO SLEEP (JP8)

JP8 allows control of the AUTO SLEEP function. To put the device into auto sleep mode in which it will power down when no input is detected, set the jumper to pull AUTO SLEEP to VCC. To turn off auto sleep and prevent the LMH0384 from automatically powering down, set the jumper to pull AUTO SLEEP to GND. The LMH0384 AUTO SLEEP pin has an internal pullup (to enable auto sleep), so JP8 may be left unconnected to enable auto sleep mode.

SPI Header (JP9)

JP9 is the SPI (Serial Peripheral Interface) header. It allows access to the SPI pins (\overline{SS} , MISO, MOSI, and SCK) while the LMH0384 is in SPI mode. These pins may be connected to a standard SPI controller to access the LMH0384 SPI registers. Refer to the LMH0384 datasheet for details.

Carrier Detect LED (D1)

D1 shows the status of Carrier Detect. This LED is GREEN when an input signal has been detected, and OFF when no input is detected. D1 shows the status of Carrier Detect while in Pin Mode or SPI Mode.

Typical Performance

Figures 4 and 5 show typical output waveforms of the SD384, with the 1m of Belden 1694A cable on the input and 110m of Belden 1694A cable on the input, respectively. The input signal is a 2.97 Gbps PRBS10, and the output signal is measured on the Agilent DCA-J 86100C Oscilloscope.

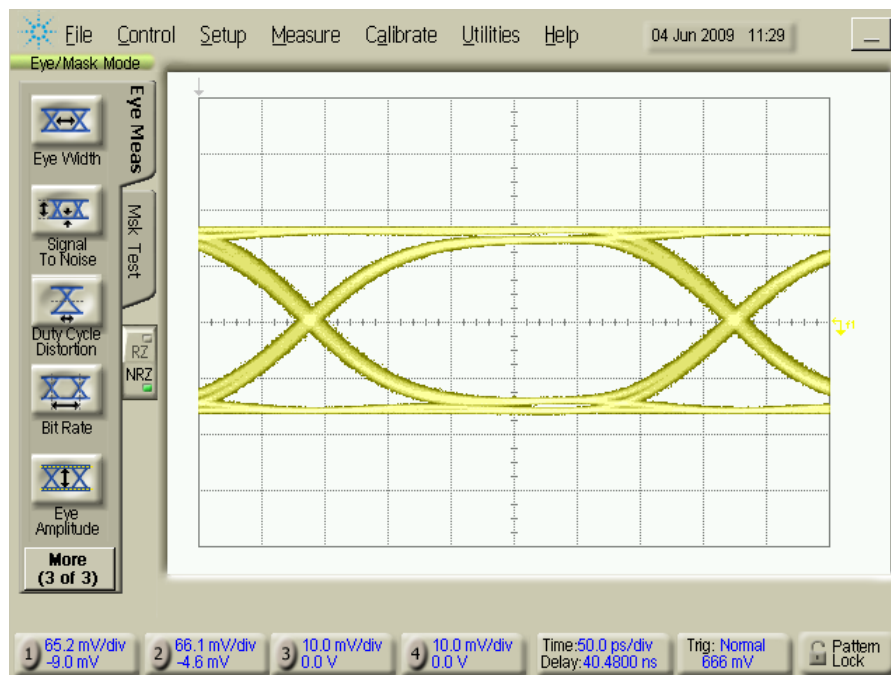


Figure 4. SD384 Output Waveform at 2.97 Gbps with 1m Belden 1694A Cable

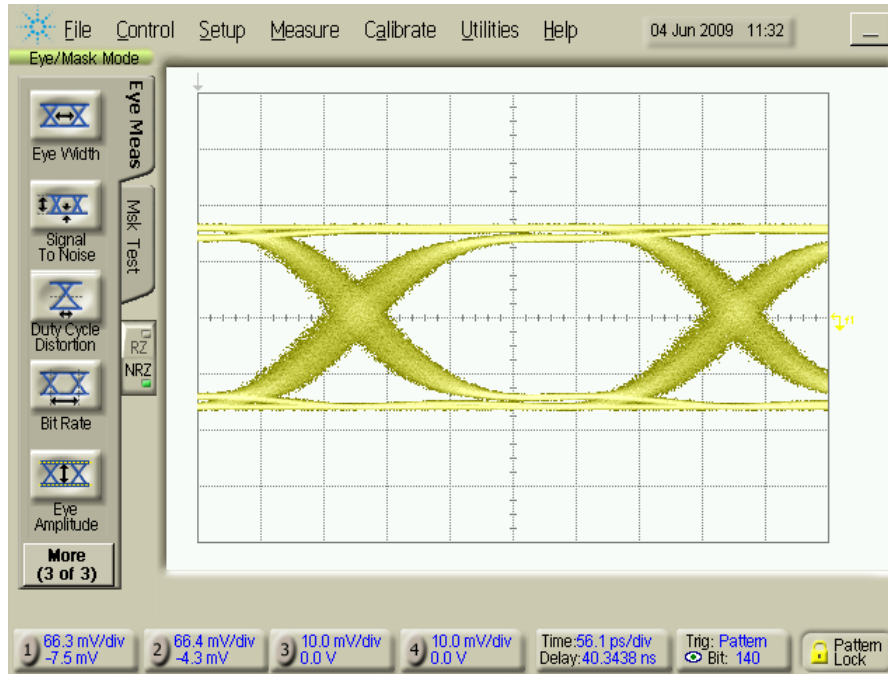
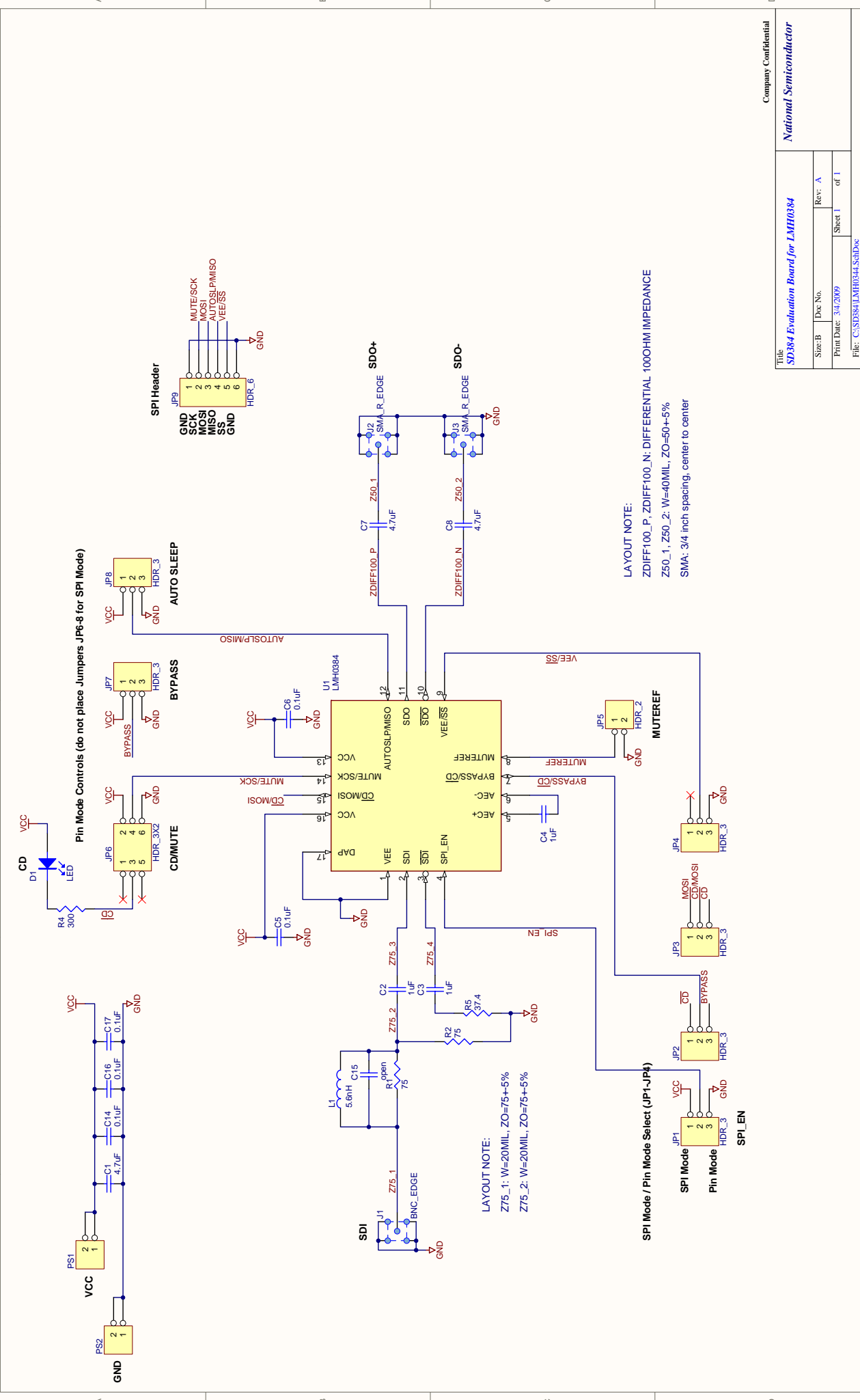


Figure 5. SD384 Output Waveform at 2.97 Gbps with 110m Belden 1694A Cable

Bill of Materials

Reference Designator	Qty	Description	Manufacturer	Manufacturer Part No.
C1, C7, C8	3	Capacitor, 4.7uF, 6.3V, X5R, 0603	Panasonic - ECG	ECJ-1VB0J475M
C2, C3, C4	3	Capacitor, 1uF, 6.3V, X5R, 0402	Panasonic - ECG	ECJ-0EB0J105M
C5, C6, C14, C16, C17	5	Capacitor, 0.1uF, 16V, X5R, 0402	Panasonic - ECG	ECJ-0EB1C104K
D1	1	LED, Green, 0603	Lite-On	LTST-C190GKT
J1	1	BNC, Amphenol, 75-ohm, edge launch	Amphenol	31-6009
J2, J3	2	SMA, 50-ohm, edge launch	Johnson Components	142-0701-851
JP1, JP2, JP3, JP4, JP7, JP8	6	Header, 3x1, 0.1"	3M/ESD	929834-02-36
JP5	1	Header, 2x1, 0.1"	3M/ESD	929834-02-36
JP6	1	Header, 3x2, 0.1"	3M/ESD	929836-02-36
JP9	1	Header, 6x1, 0.1"	3M/ESD	929834-02-36
L1	1	Inductor, 5.6nH, 0402	Murata	LQP15MN5N6B02D
PS1, PS2	2	PCB Quick-Fit Male Terminal, .052" diameter, .250" tab size	Keystone Electronics	1287-ST
R1, R2	2	Resistor, 75-ohm, 1/16W, 1%, 0402	Yageo	RC0402FR-0775RL
R5	1	Resistor, 37.4-ohm, 1/16W, 1%, 0402	Vishay/Dale	CRCW040237R4FKED
R4	1	Resistor, 300-ohm, 1/10W, 5%, 0402	Panasonic - ECG	ERJ-2GEJ301X
U1	1	LMH0384 Cable Equalizer, LLP-16	National Semiconductor	LMH0384SQ

Schematic



LAYOUT NOTE:
 ZDIFF100_P, ZDIFF100_N: DIFFERENTIAL 100OHM IMPEDANCE
 Z50_1, Z50_2: W=40MIL, ZO=50+5%
 SMA: 3/4 inch spacing, center to center

LAYOUT NOTE:
 Z75_1: W=20MIL, ZO=75+5%
 Z75_2: W=20MIL, ZO=75+5%

Title: SD384 Evaluation Board for LMH0384	
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Print Date: 3/4/2009	Sheet 1 of 1
File: C:\SD384\LMH0384.SchDoc	

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