THE DATASHEET OF

SI1024-868-A-DK

UDP UPPI CARD USER'S GUIDE

1. Introduction

The UPPI-series evaluation cards are the engine of an MCU-based system, containing an MCU, optional radio, and minimal support circuitry.

These cards are designed around either a C8051F96xMCU or a Si102x/3x Wireless MCU. Only placement-critical items, such as bypass capacitors, crystals, dc-dc inductor, and RF front end circuitry are included. All other circuits reside on the hosting platform.

These cards are compatible with Silicon Labs Unified Development Platform MCU cards (UDP-F960-MCU series). They may also be used as prototyping modules, as they fit on a 2 mm-center prototyping board.

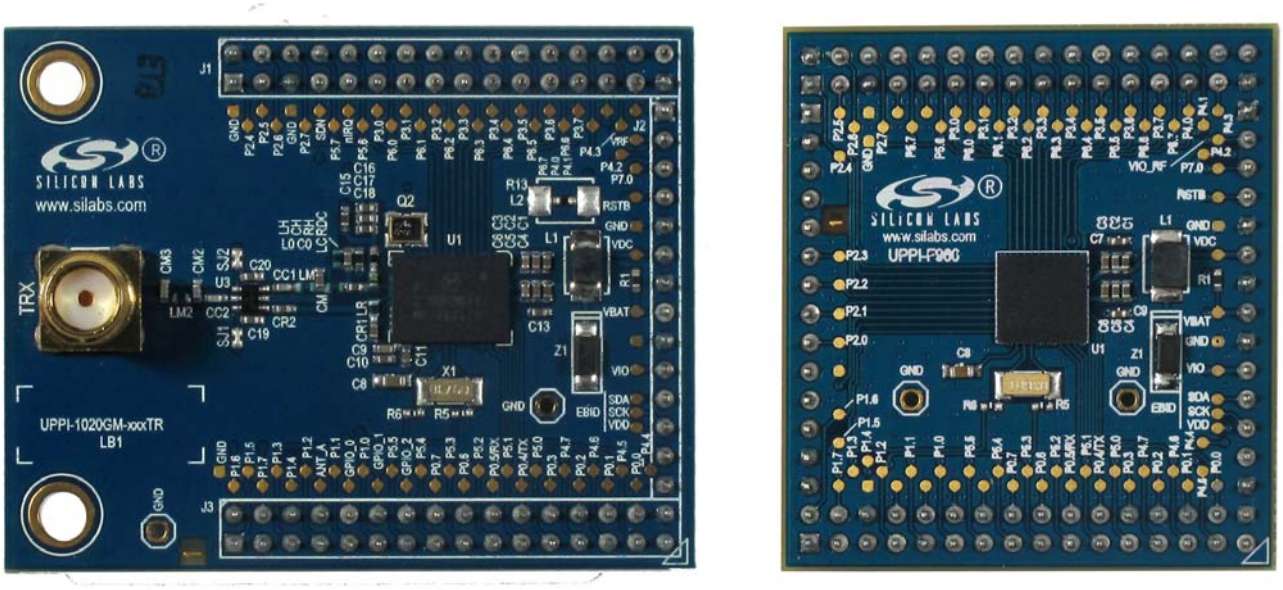


Figure 1. UPPI Cards with and without Radio

2. Description

The UPPI cards contain the MCU device and a minimal number of supporting components. Most of the core device pins are connected directly to headers, allowing signal mapping to be defined by the host board, typically a UDP MCU card. (See “2.3. Compatibility” for more information.)

Each board design varies in schematic and features. Refer to the board design files available from www.silabs.com for specifics.

2.1. Features

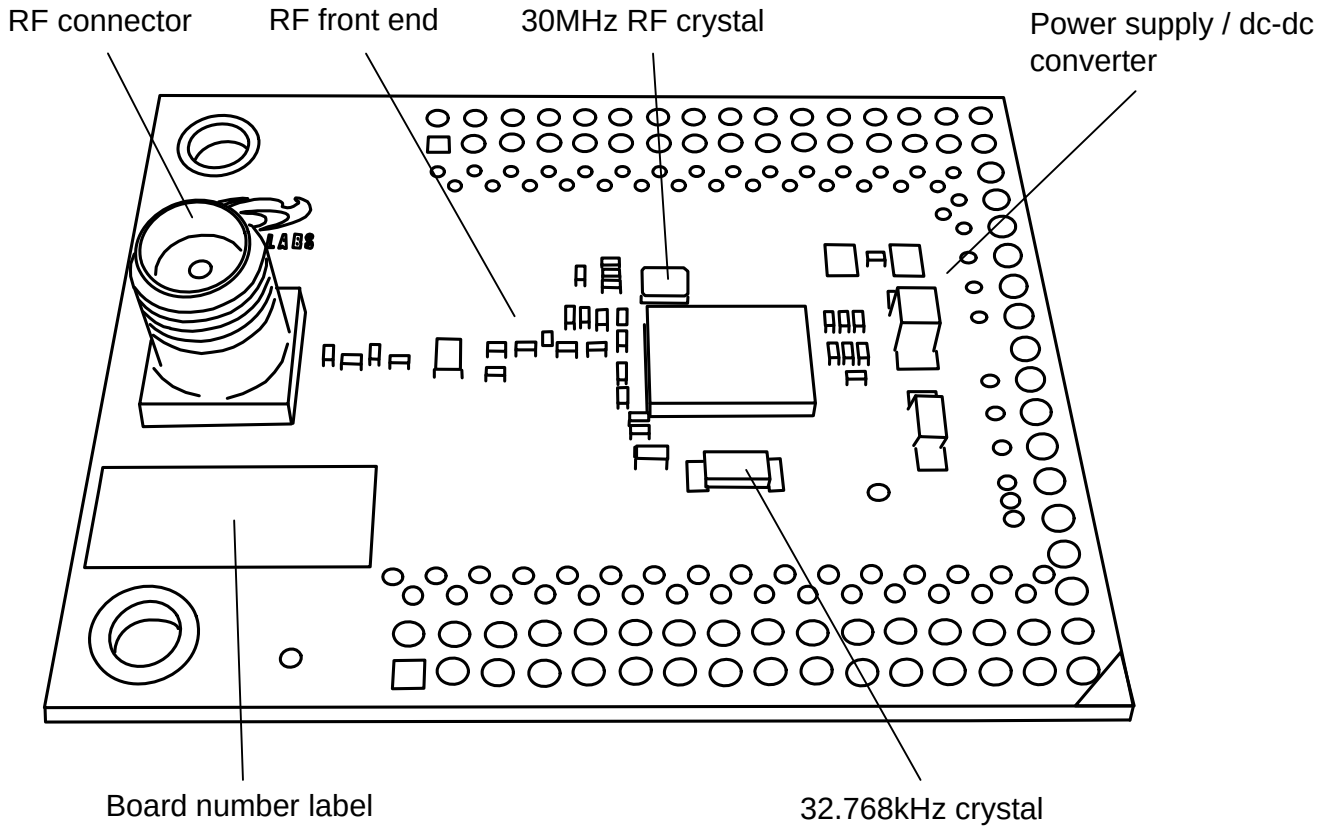


Figure 2. Top View: UPPI-10xx-fffTR and UPPI-10xx-fffDT Wireless MCU Boards

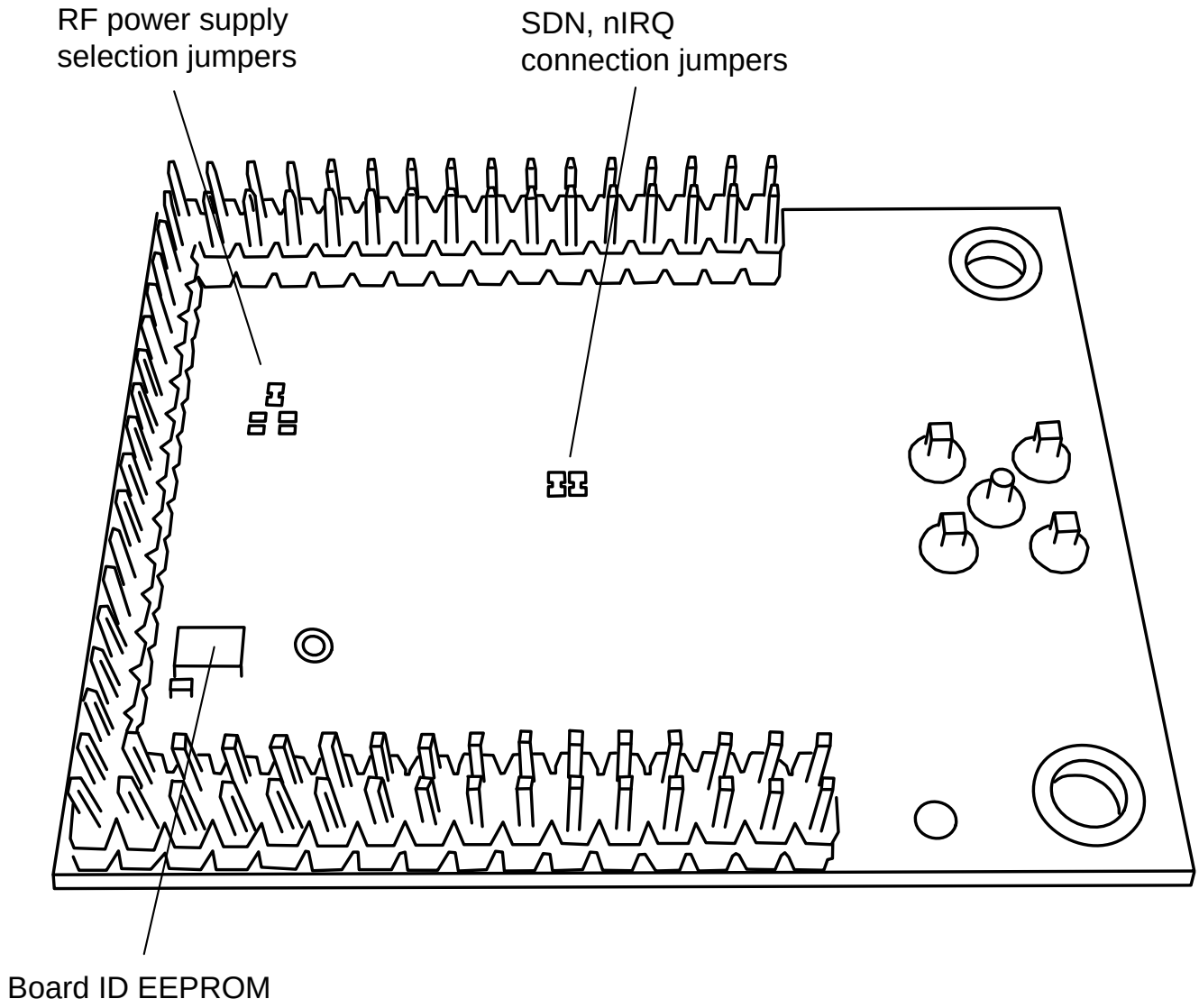


Figure 3. Bottom View: UPPI-10xx-fffTR and UPPI-10xx-fffDT Wireless MCU Boards

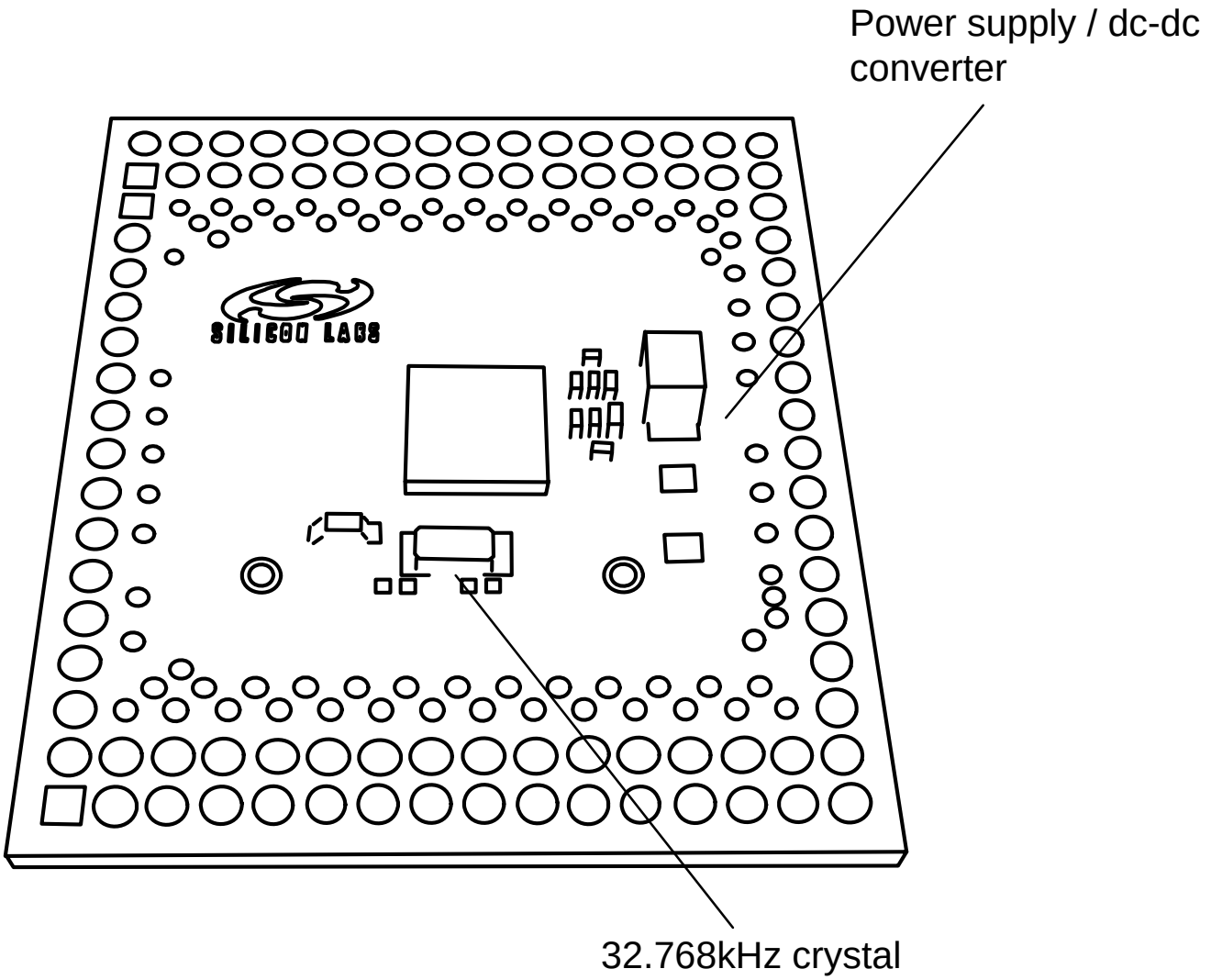


Figure 4. Top View: UPPI-F960

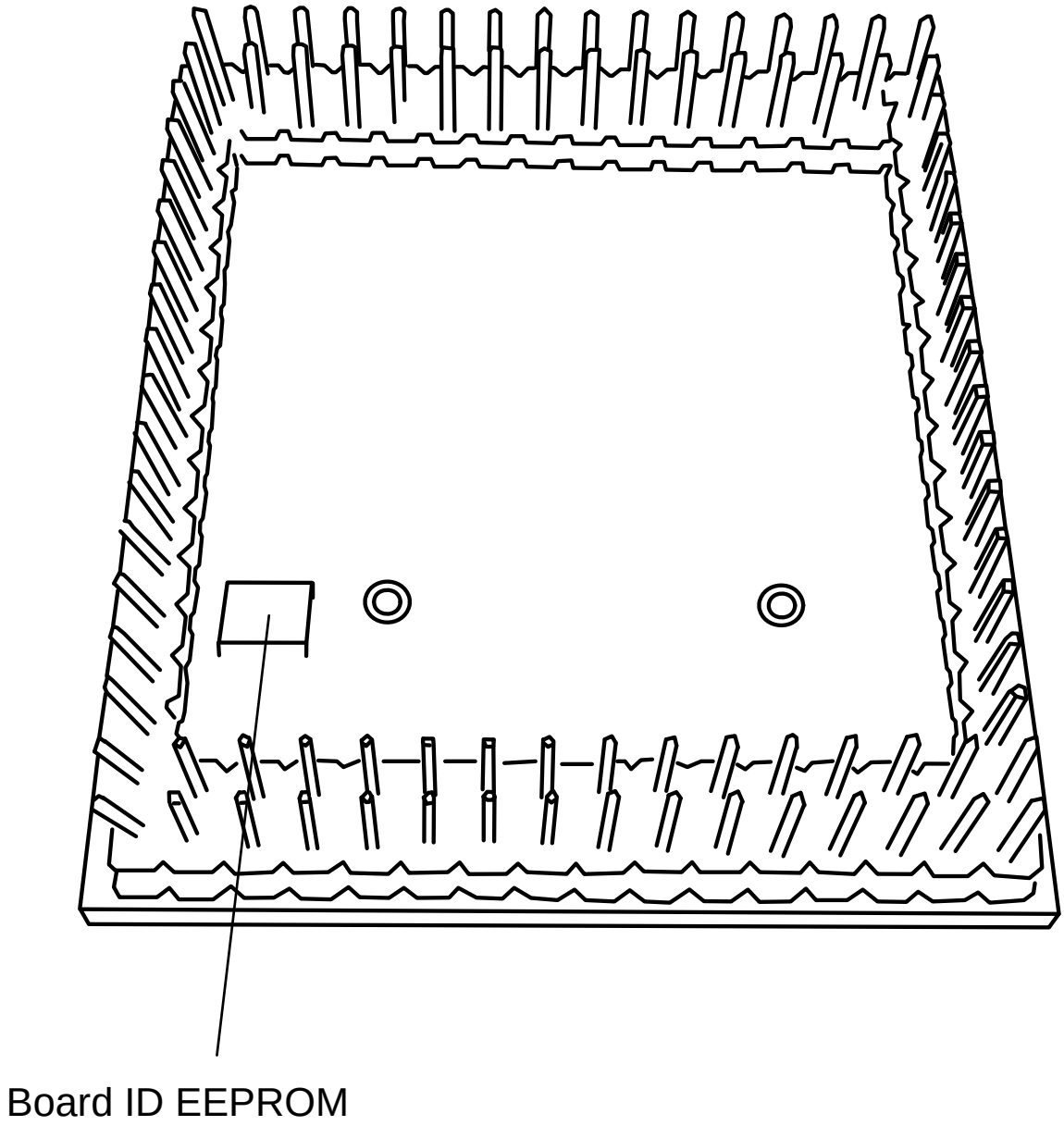


Figure 5. Bottom View: UPPI-F960

The UPPI cards contain the following functions:

- **Power Supply**
  The device's VBAT and VDC pins are connected to external pins. The dc-dc inductor, optional diode, and bypass capacitors are all included on the UPPI board as recommended in the data sheet.
  The VIO connection is routed to a pin and must be connected on the host board.
  The VIO_RF pin (if applicable) is connected to the VRF net and routed to a pin. This net supplies both the radio section power and the VIO_RF I/O voltage . The source is set on the host board, but may be optionally hard-wired via solder jumpers on the back of the board.
- **Crystal Oscillators**
  The MCU has a 32.768kHz crystal connected to the XTAL 3/4 pins. Devices with a radio have a 30 MHz crystal connected to the radio's XOUT/XIN pins. These nets are not connected to pins.
- **RF Front End**
  All RF matching circuitry is on-board. The transmitter and receiver pins are both matched to a 50 Ω SMA connector. This connector may be used with test equipment or an appropriate antenna.
  The matching is based on either a T/R switch or a Direct Tie topology. The T/R switch topology uses a TX/RX switch device to share the RF port between TX and RX paths. T/R is used with high power (+20dBm) devices. The Direct Tie topology passively sums TX and RX paths and is suitable for low-power (+13dBm) devices.
  Both matching topologies are discussed in detail in the following application notes:
  - AN427: EZRadioPRO™ Si433X & Si443X RX LNA Matching (+20dBm, T/R switch)
  - AN435: Si4032/4432 PA Matching (+20 dBm, T/R switch)
  - AN436: Si4030/4031/4430/4431 PA Matching (+13 dBm, Direct Tie)
- **RF GPIO Signals**
  The radio's GPIO_0 - GPIO_2 and ANT_A nets are connected to pins. GPIO_1 and GPIO_2 are also connected on-board to the RF transmit/receive switch on high power (“TR” version) boards.
- **RF to MCU Interface Signals**
  The radio and MCU are interconnected within the Si102x/3x device. Two external signals, shutdown (SDN) and the interrupt (nIRQ) are connected to MCU port pins on the board. These signals may be disconnected by cutting jumpers on the back of the board.
- **Port Pins**
  Most port pins are connected directly to the module's pins. Exceptions include
  - Pins dedicated to the on-board radio interface
  - P1.2 / P1.3, as these pins are used for the 32.768kHz crystal. These may be connected by adding 0-ohm resistors.
- **Programming/Debugging**
  C2CK/RSTB and C2D are connected to the module header. C2CK/RSTB has an on-board pullup resistor to VBAT.
- **Unified Development Platform Support**
  An EEPROM is included on the back side of the board to identify board information to the UDP system. This EEPROM is electrically isolated from the rest of the board except for a common ground.

The UPPI boards are based on 2mm-center headers. The footprint fits any C8051F96x- or Si102x/3x compatible Unified Development Platform MCU card. The UPPI boards may also be used for prototyping, using a 2mm-center perforated prototyping board.

The UPPI boards should be fastened to the base board using two 4-40 screws and 6.5mm standoffs to resist twisting moments from the antenna or RF cabling.

2.2. Ordering Information

A variety of UPPI boards are available, each tailored to a specific RF frequency band, transmitter power, and RF front end configuration. Refer to www.silabs.com for specific ordering information.

Table 1. Ordering Information

	Device	Description	Frequency	Tx Power (Max)	Rf Front End
MCU Only					
UPPI-F960	C8051F960	'F960 microcontroller only	—	—	—
Wireless MCU					
UPPI-1020-fffTR	Si1020	Si1020 Wireless MCU with T/R switch (+20 dBm)	fff MHz	+20 dBm max	T/R switch
UPPI-1024-fffDT	Si1024	Si1023 Wireless MCU with Direct Tie RF front end (+13 dBm)	fff MHz	+13 dBm max	Direct Tie
***Note:** refer to www.silabs.com for an up to date list of supported frequency variants					

2.3. Compatibility

These boards are compatible with the following UDP MCU cards:

- UDP F960 MCU card with Multiplexed LCD (UPMP-F960-MLCD)
- UDP F960 MCU card with EMIF (UPMP-F960-EMIF)

2.4. Schematics

These schematics show circuit topologies of the various cards. Refer to the latest schematics, available from www.silabs.com, for actual values.

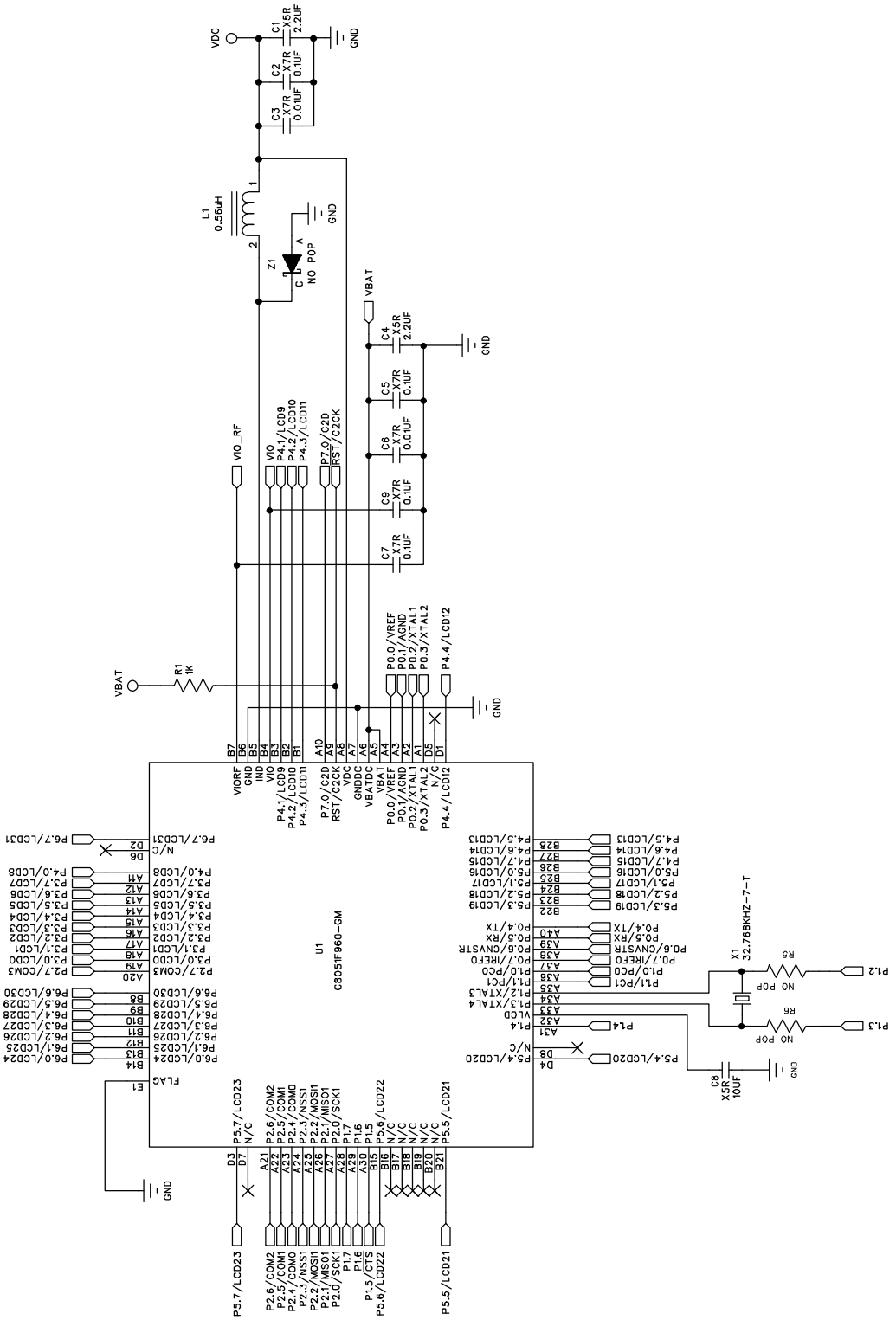


Figure 6. UPPI-F960 (1 of 2)

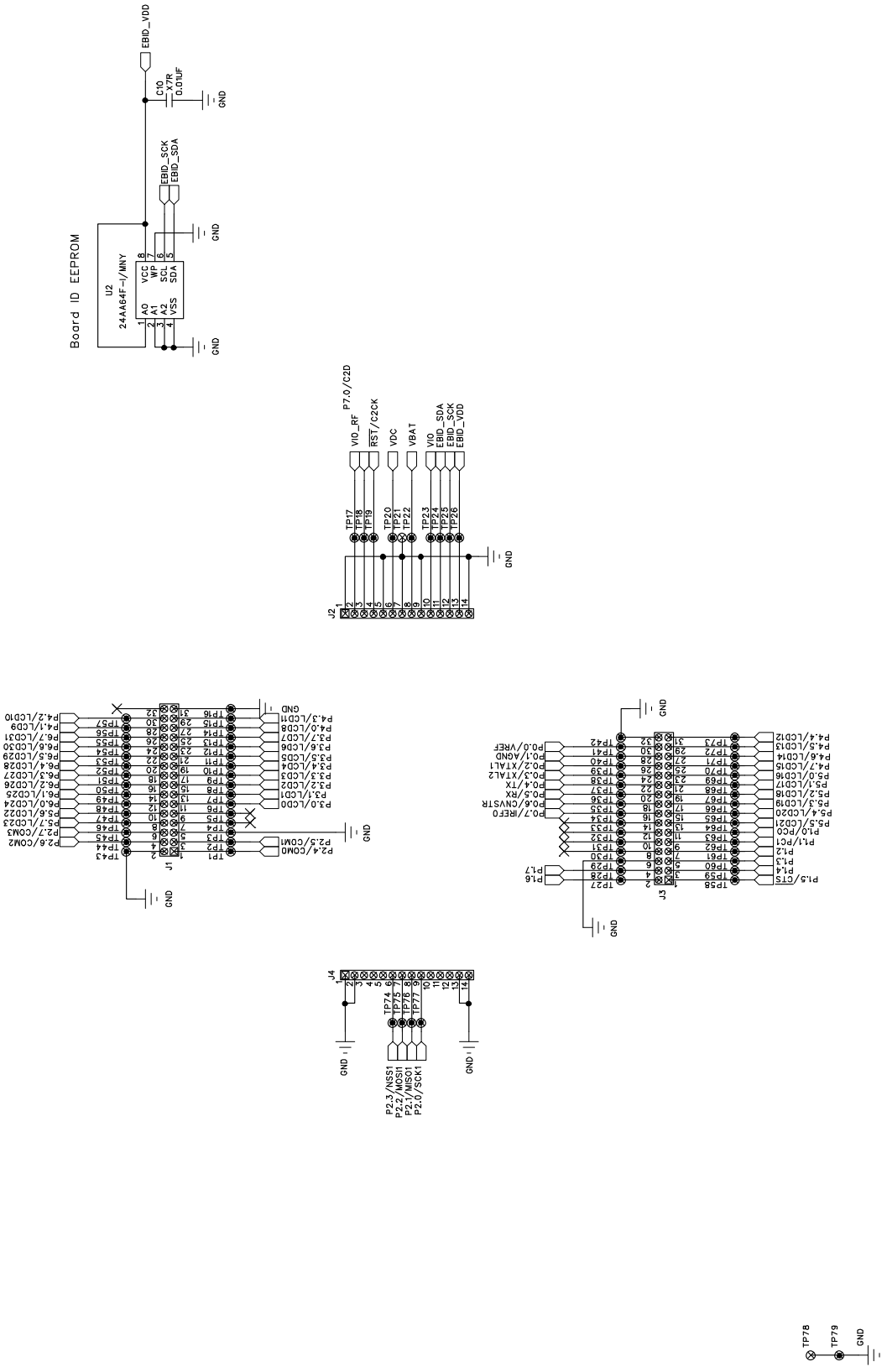


Figure 7. UPPI-F960 (2 of 2)

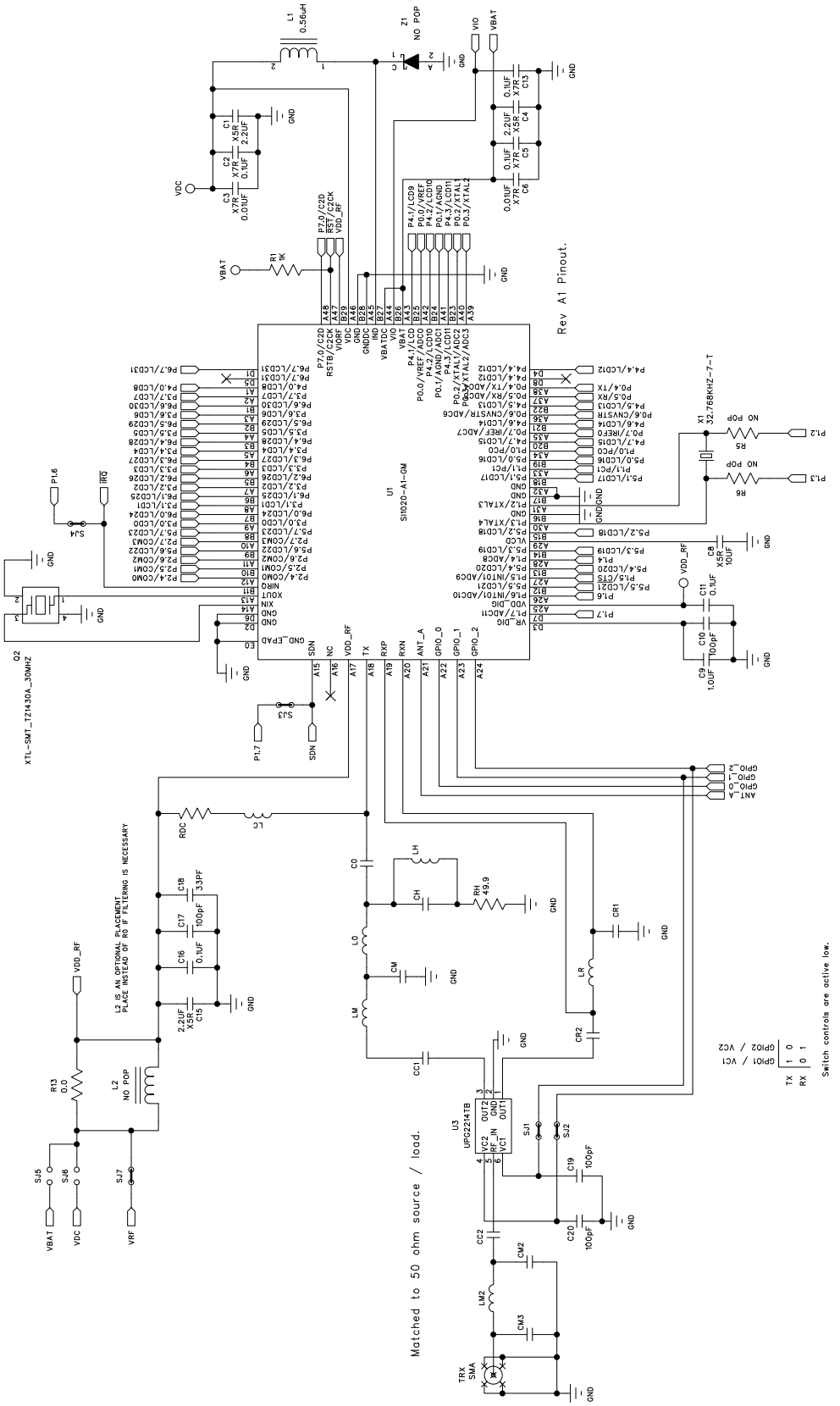


Figure 8. UPPI-1020-fffTR (1 of 2)

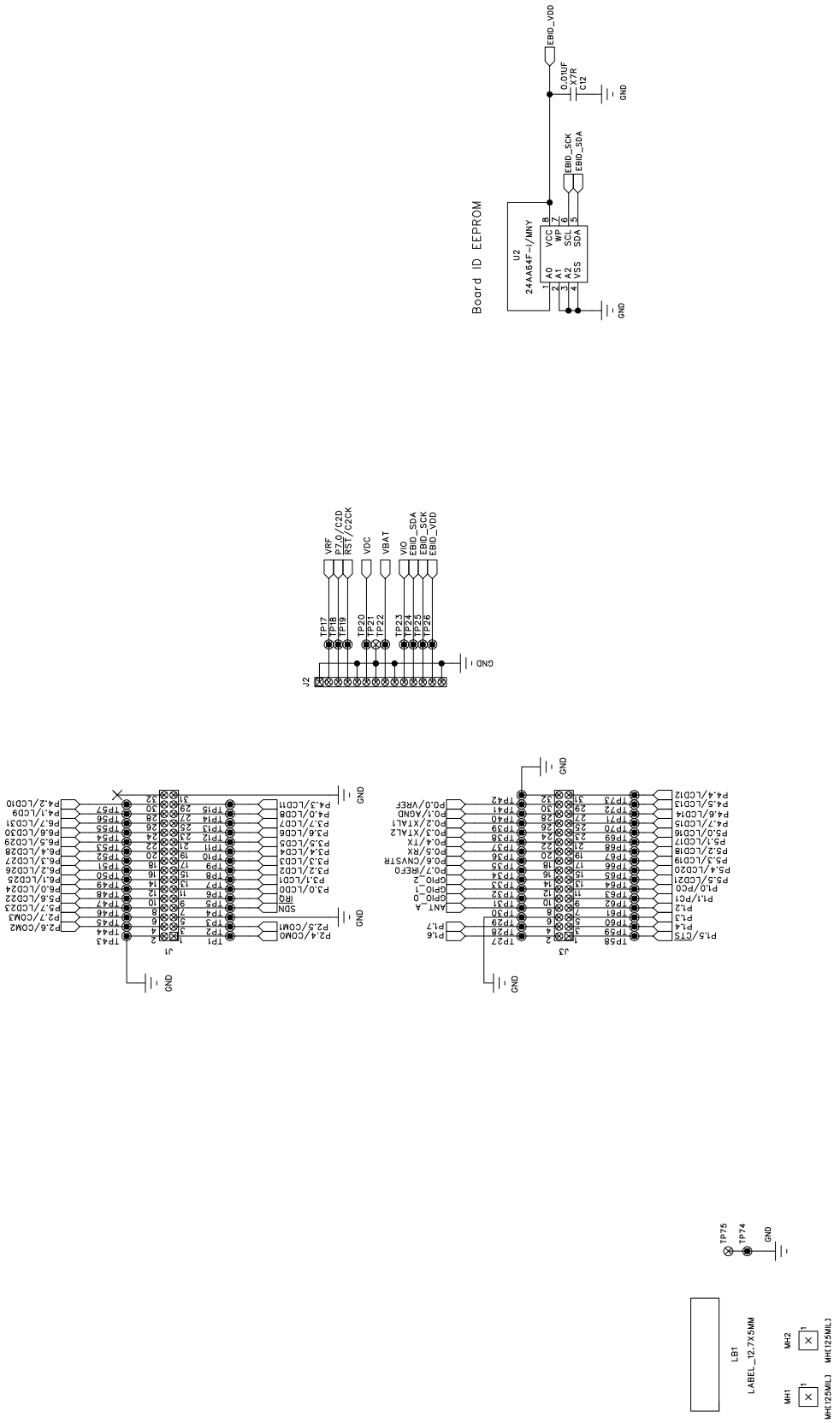


Figure 9. UPPI-1020-ffTR (2 of 2)

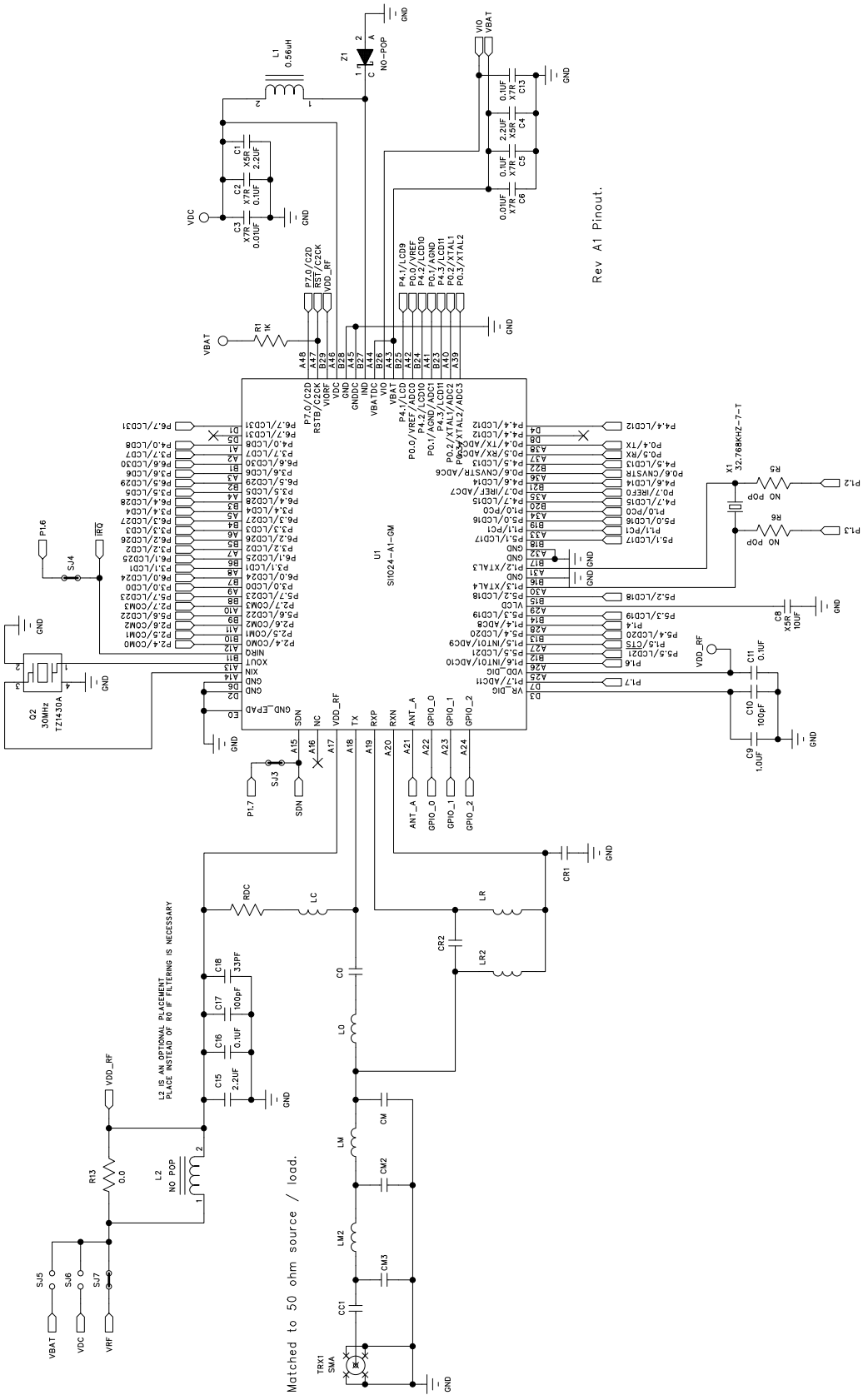


Figure 10. UPPI-1024-fffDT (1 of 2)

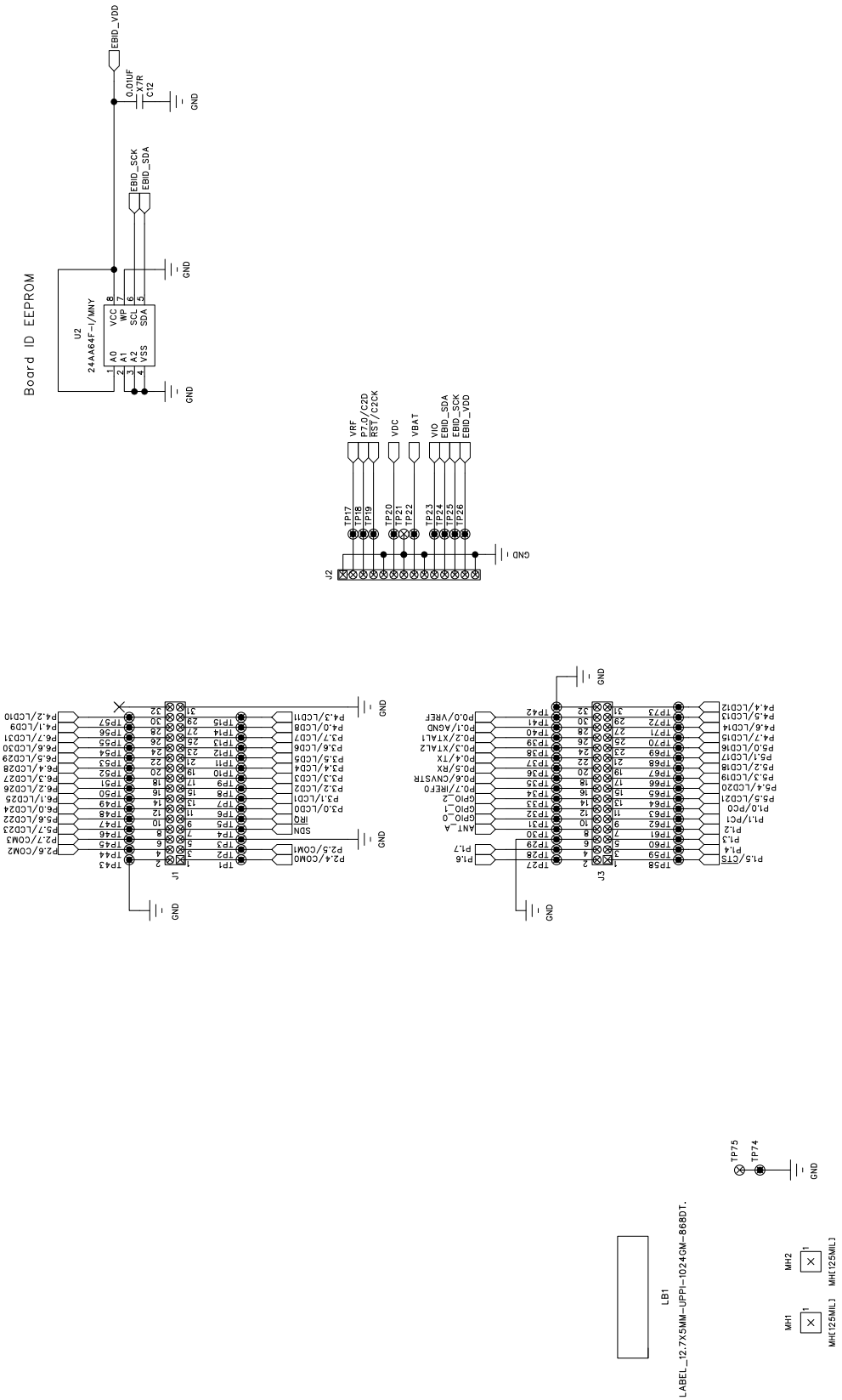


Figure 11. UPPI-1024-fffDT (2 of 2)

2.5. PCB Layouts

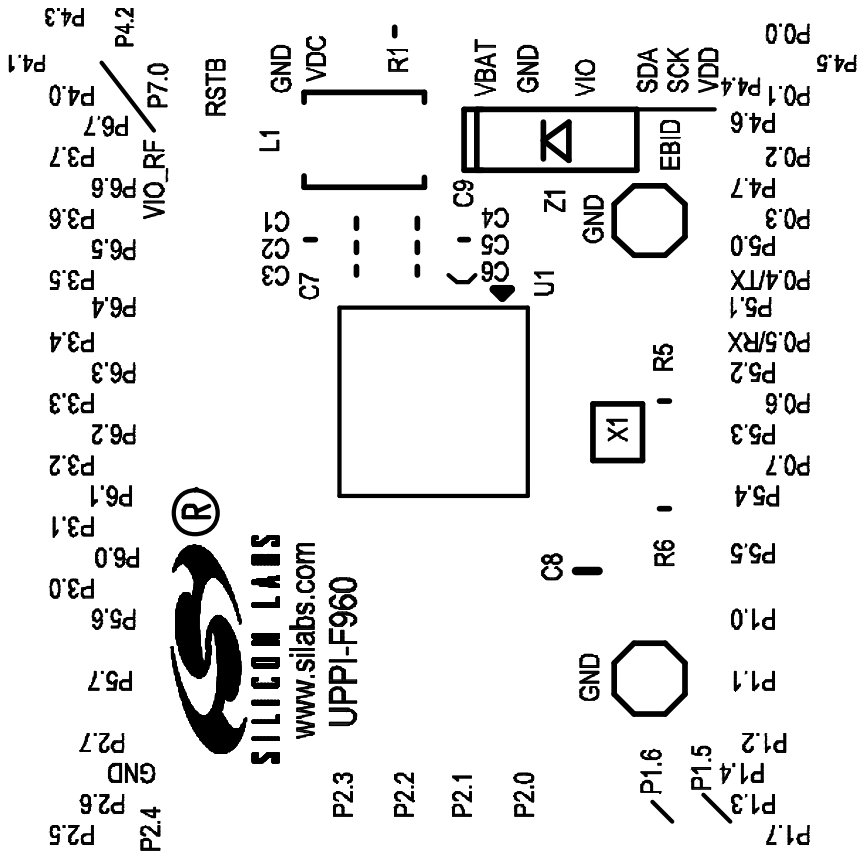


Figure 12. UPPI-F960 Silkscreen Top

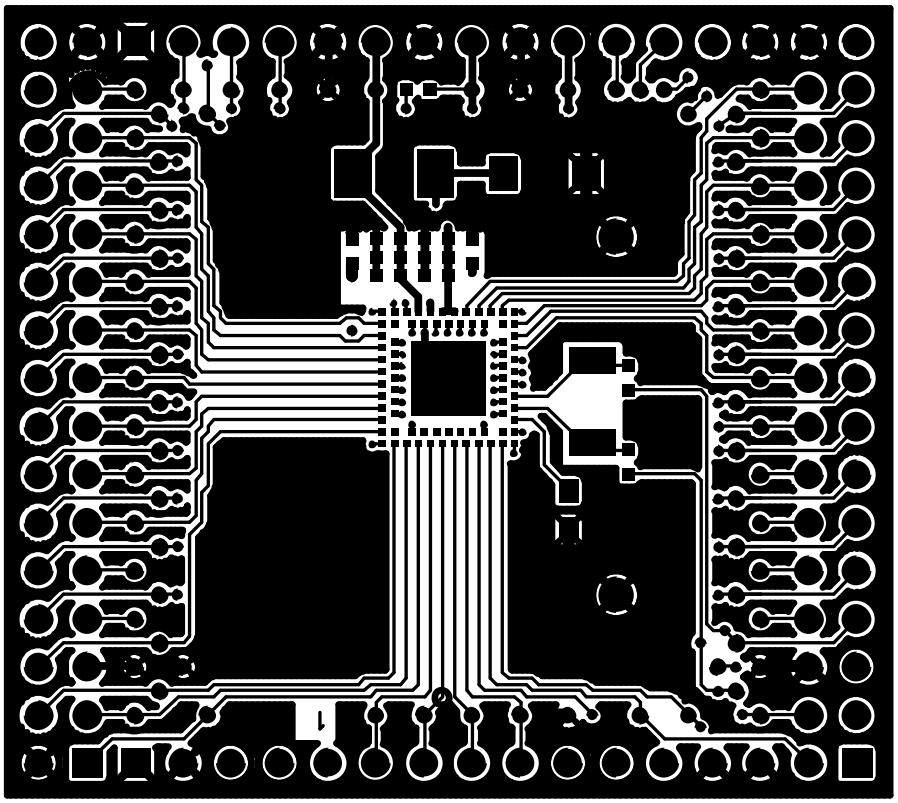


Figure 13. UPPI-F960 Top Side

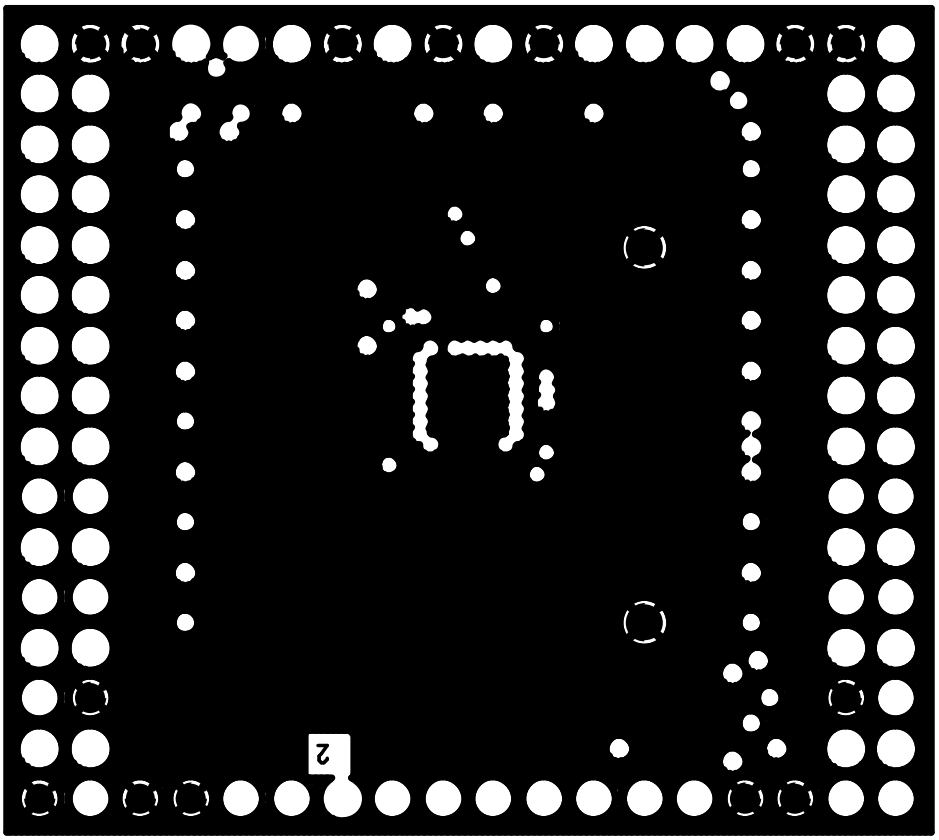


Figure 14. UPPI-F960 Layer 2

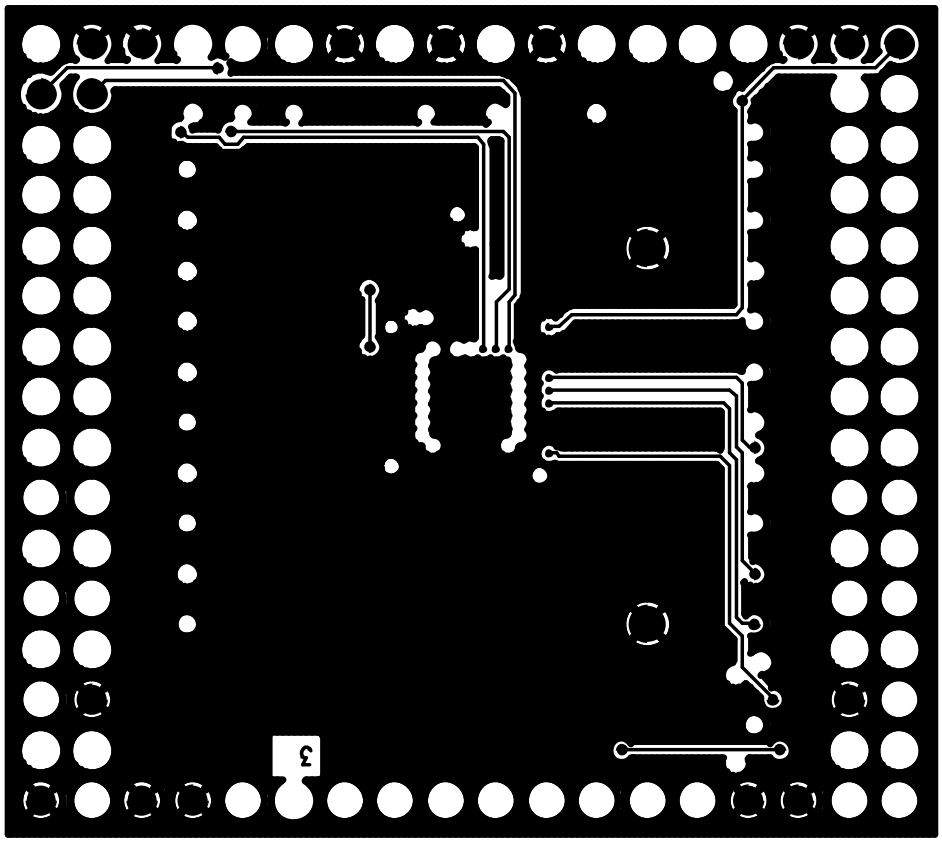


Figure 15. UPPI-F960 Layer 3

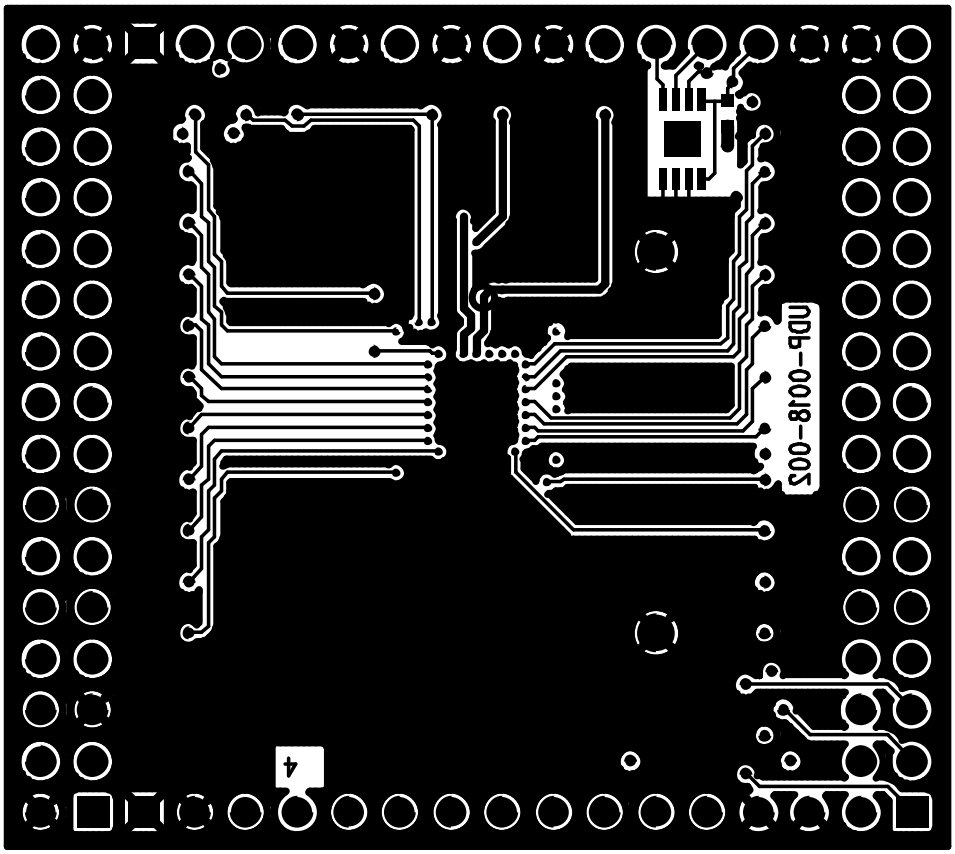
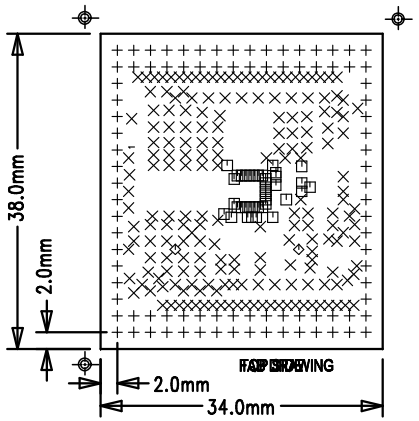


Figure 16. UPPI-F960 Bottom Side

NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345€C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING, UNLESS OTHERWISE SPECIFIED.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE +/- 0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" +/-10% ACROSS PADS.
10. WARP/TWIST SHALL NOT EXCEED 0.010 INCH PER INCH.
11. FINISH SHALL BE LPI, BLUE S.M.O.B.C., BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. NO VENDOR MARKINGS OR ALTERATIONS SHALL BE PERMITTED ON ANY METAL OR SILKSCREEN LAYERS.
14. BOARD STACKUP:
    TOP LAYER PLATED TO 1 OZ
    PREPREG FR4: 12 MILS +/- 1 MIL
    L2-GND 1 OZ Cu
    PREPREG FR4: 28 MILS
    L3-POWER 1 OZ Cu
    PREPREG FR4: 12 MILS +/- 1 MIL
    BOTTOM LAYER PLATED TO 1 OZ
15. PLATE IN ACCORDANCE WITH IPC-4552, 118-236uIN of NICKEL, WITH AN ADDITIONAL 2-6 uIN OF GOLD ON TOP.

SIZE	QTY	SYM	PLATED	TOL
30	92	+	YES	+/-0.003"
8	194	X	YES	+/-0.003"
6	39	⊡	YES	+/-0.003"
40	2	◇	YES	+/-0.003"



LAYER STACKUP	FILE NAMES
TOP SILKSCREEN	TOPSILK.TSP
TOP SOLDER MASK	SMASKTOP.SMT
TOP SIDE	TOP.TOP
L2	LAYER2.L2
L3	LAYER3.L3
BOTTOM SIDE	BOTTOM.BOT
BOTTOM SOLDER MASK	SMASKBOT.SMB
BOTTOM SILKSCREEN	BOTSILK.BSK

SCALE: NONE

Figure 17. UPPI-F960 Assembly Layer

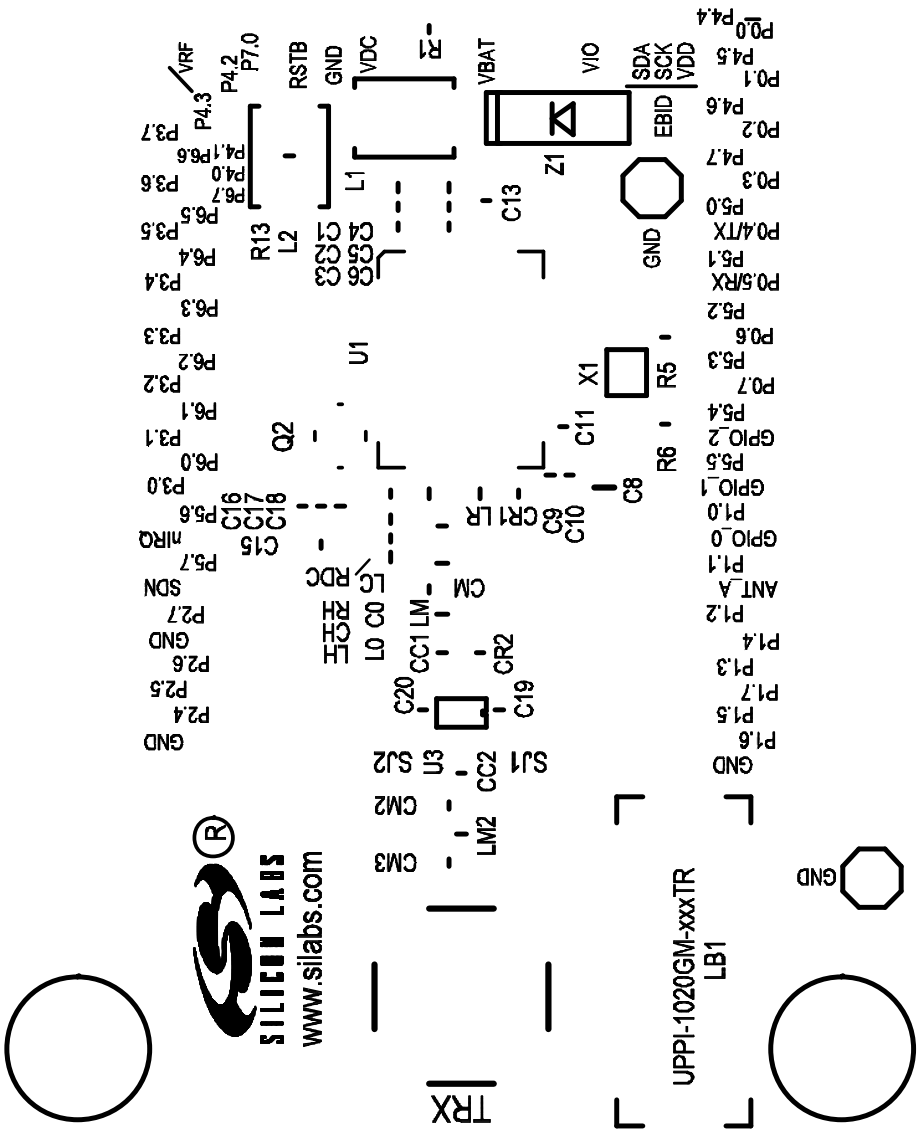


Figure 18. UPPI-1020-fffTR Silkscreen Top

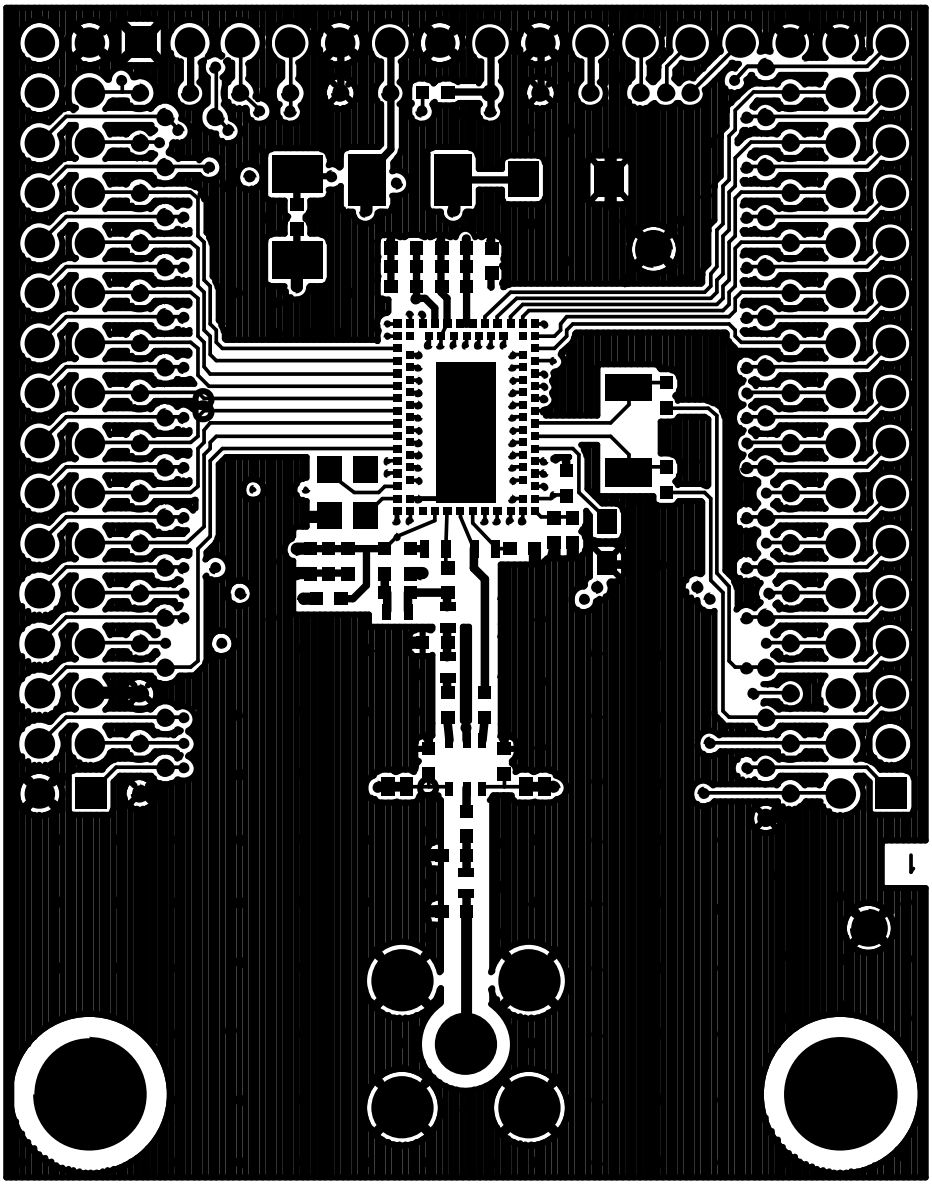


Figure 19. UPPI-1020-fffTR Top Side

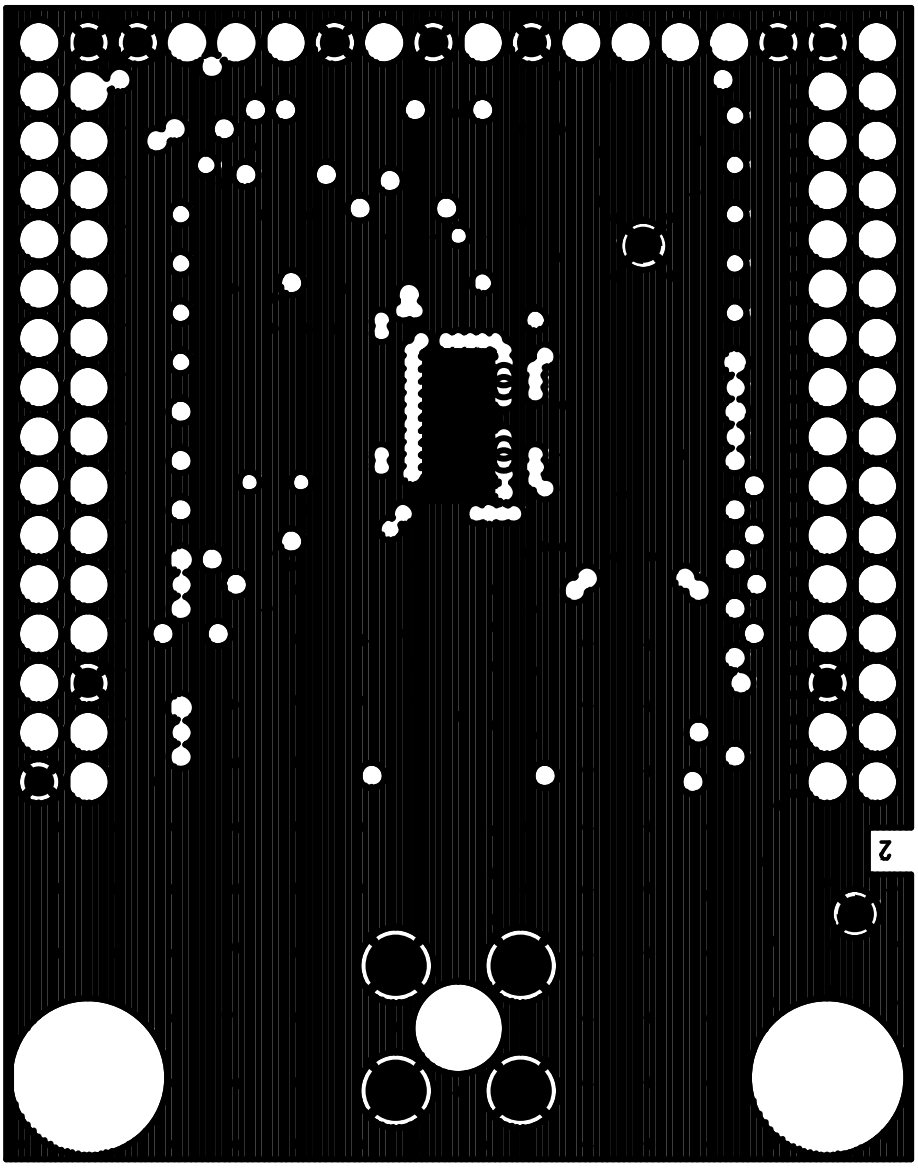


Figure 20. UPPI-1020-fffTR Layer 2

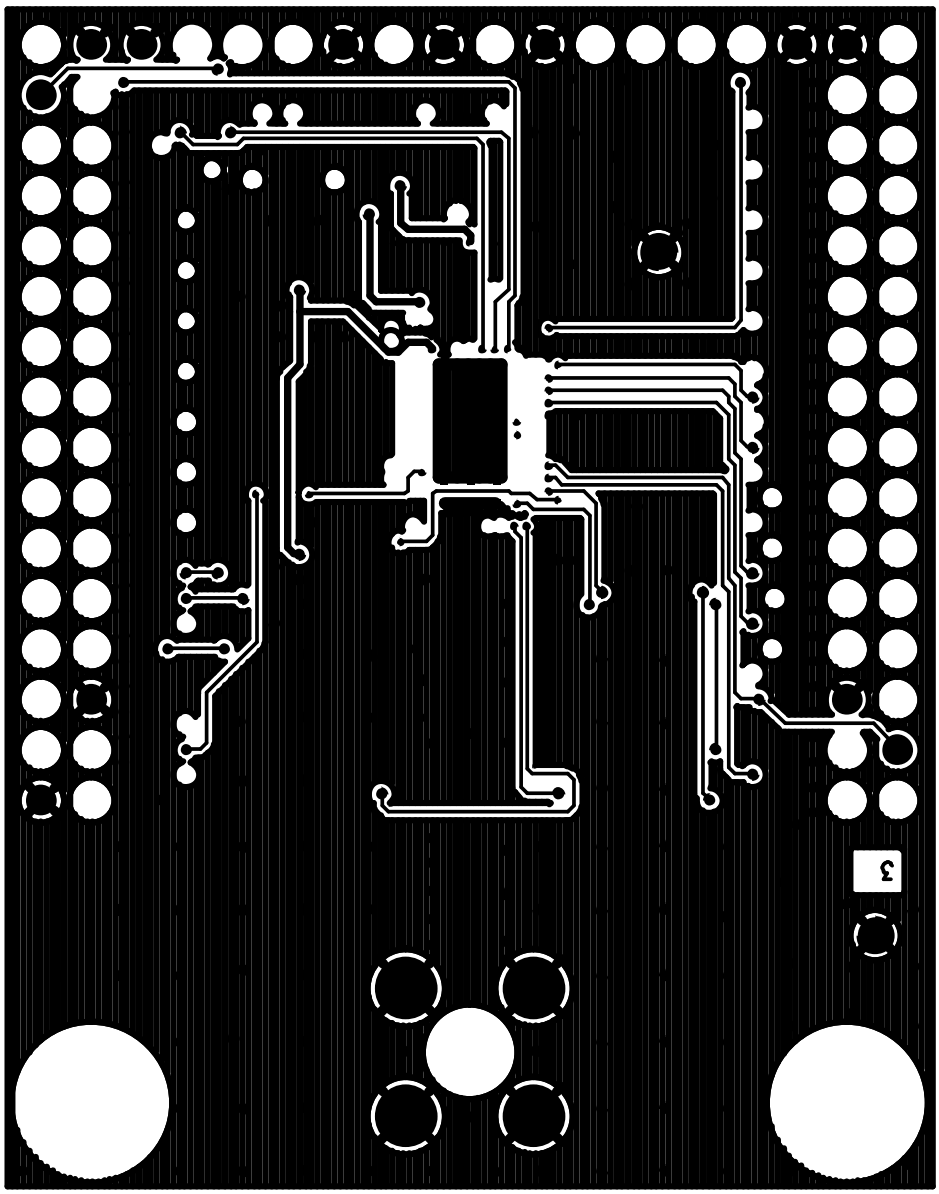


Figure 21. UPPI-1020-fffTR Layer 3

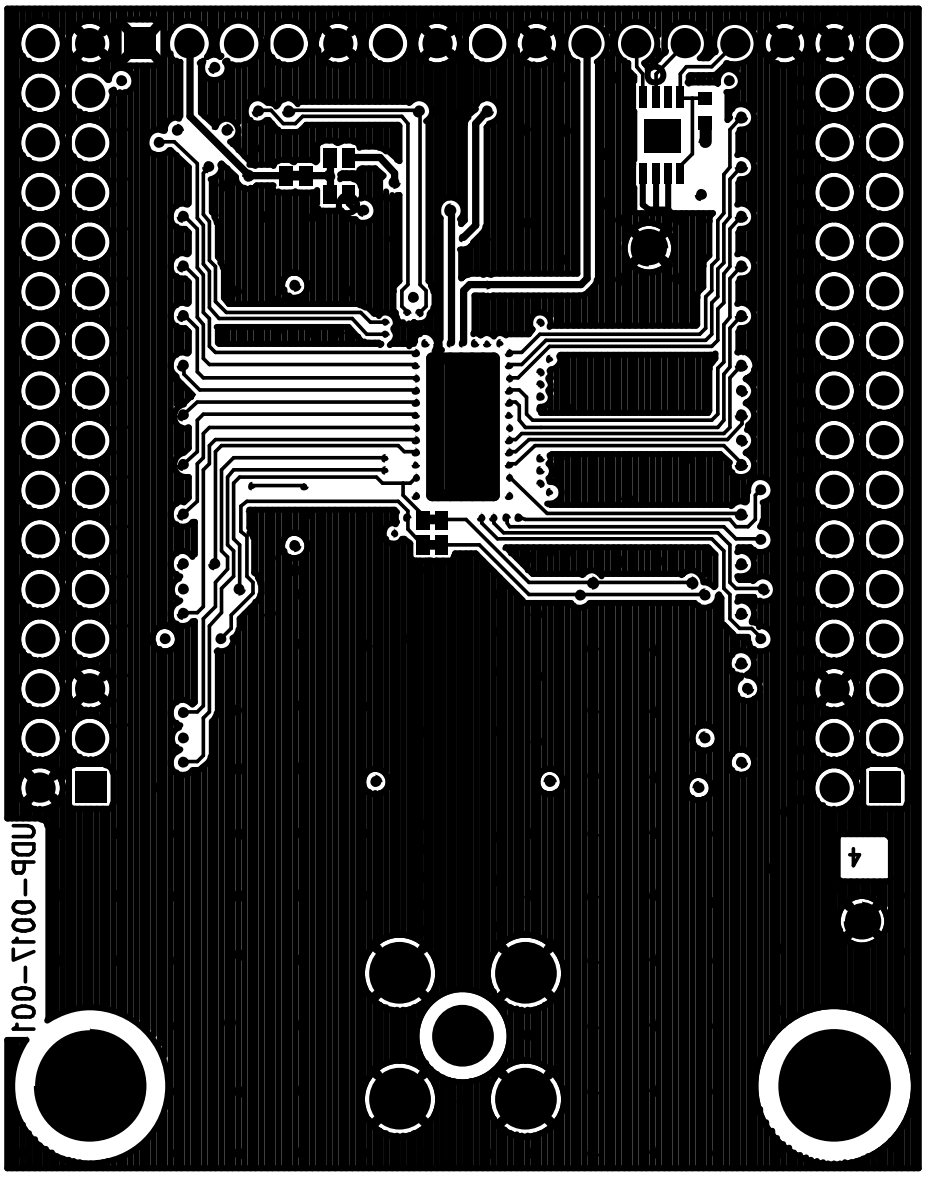
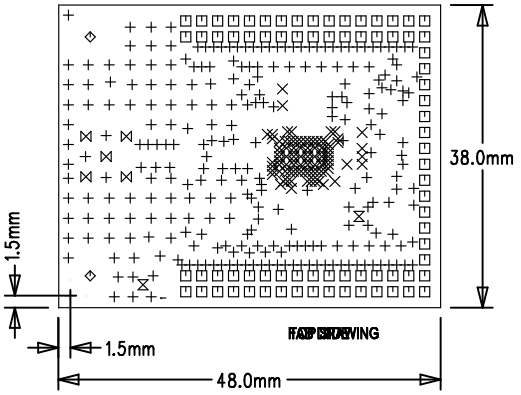


Figure 22. UPPI-1020-fffTR Bottom Side

NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345€C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING, UNLESS OTHERWISE SPECIFIED.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE +/- 0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" +/-10% ACROSS PADS.
10. WARP/TWIST SHALL NOT EXCEED 0.010 INCH PER INCH.
11. FINISH SHALL BE LPI, BLUE S.M.O.B.C., BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. NO VENDOR MARKINGS OR ALTERATIONS SHALL BE PERMITTED ON ANY METAL OR SILKSCREEN LAYERS.
14. BOARD STACKUP:
    TOP LAYER PLATED TO 1 OZ
    PREPREG FR4: 12 MILS +/- 1 MIL
    L2-GND 1 OZ Cu
    PREPREG FR4: 28 MILS
    L3-POWER 1 OZ Cu
    PREPREG FR4: 12 MILS +/- 1 MIL
    BOTTOM LAYER PLATED TO 1 OZ
15. PLATE IN ACCORDANCE WITH IPC-4552, 118-236uIN of NICKEL, WITH AN ADDITIONAL 2-6 uIN OF GOLD ON TOP.

SIZE	QTY	SYM	PLATED	TOL
0.008	261	+	YES	+/-0.003"
0.006	91	X	YES	+/-0.003"
0.03	78	◫	YES	+/-0.003"
0.125	2	◈	YES	+/-0.003"
0.04	2	⧖	YES	+/-0.003"
0.07	5	⋈	YES	+/-0.003"



SILICON LABS - UDP-0017-001 (UPPI-1020GM-915TR)

LAYER STACKUP	FILE NAMES
TOP SILKSCREEN	TOPSILK.TSP
TOP SOLDER MASK	SMASKTOP.SMT
TOP SIDE	TOP.TOP
L2	LAYER2.L2
L3	LAYER3.L3
BOTTOM SIDE	BOTTOM.BOT
BOTTOM SOLDER MASK	SMASKBOT.SMB
BOTTOM SILKSCREEN	BOTSILK.BSK

SCALE: NONE

Figure 23. UPPI-1020-fffTR Assembly Layer

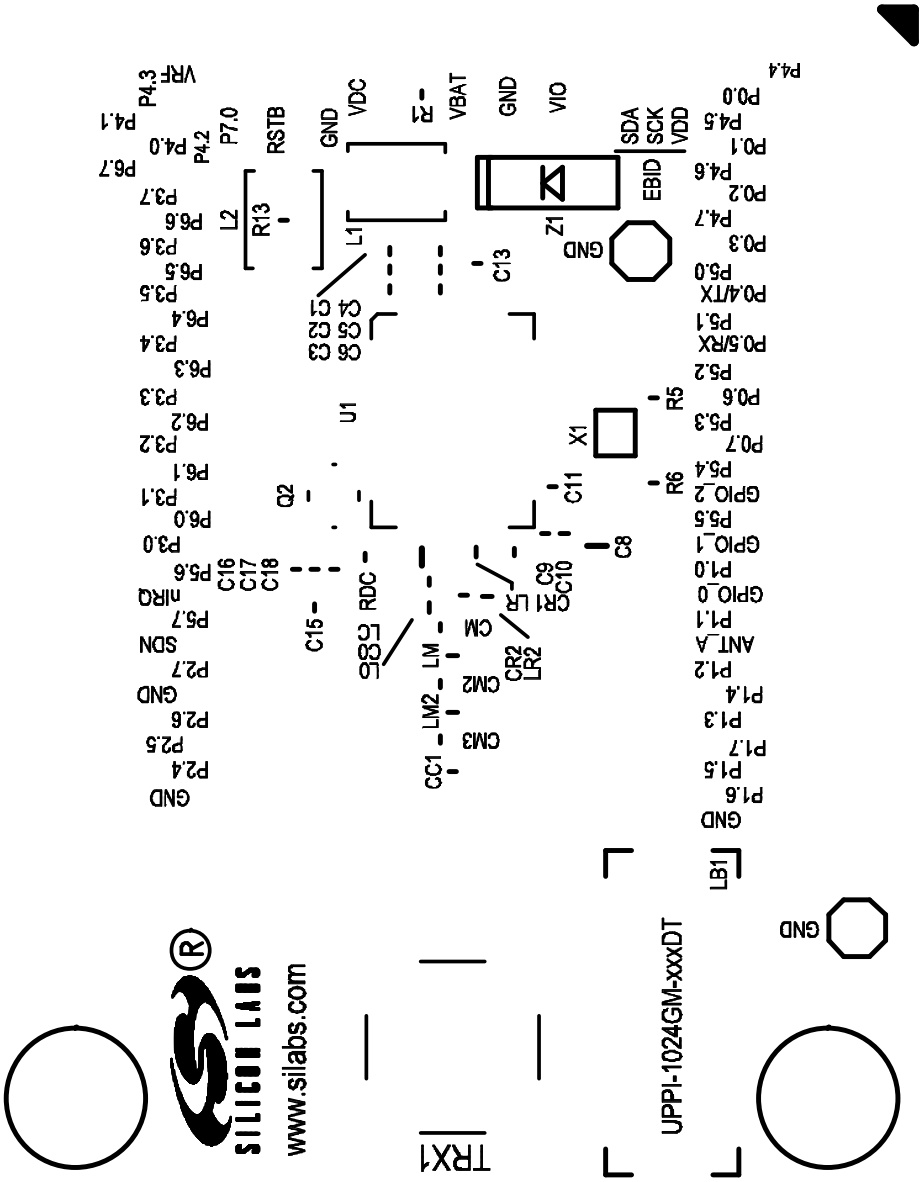


Figure 24. UPPI-1024-fffDT Silkscreen Top

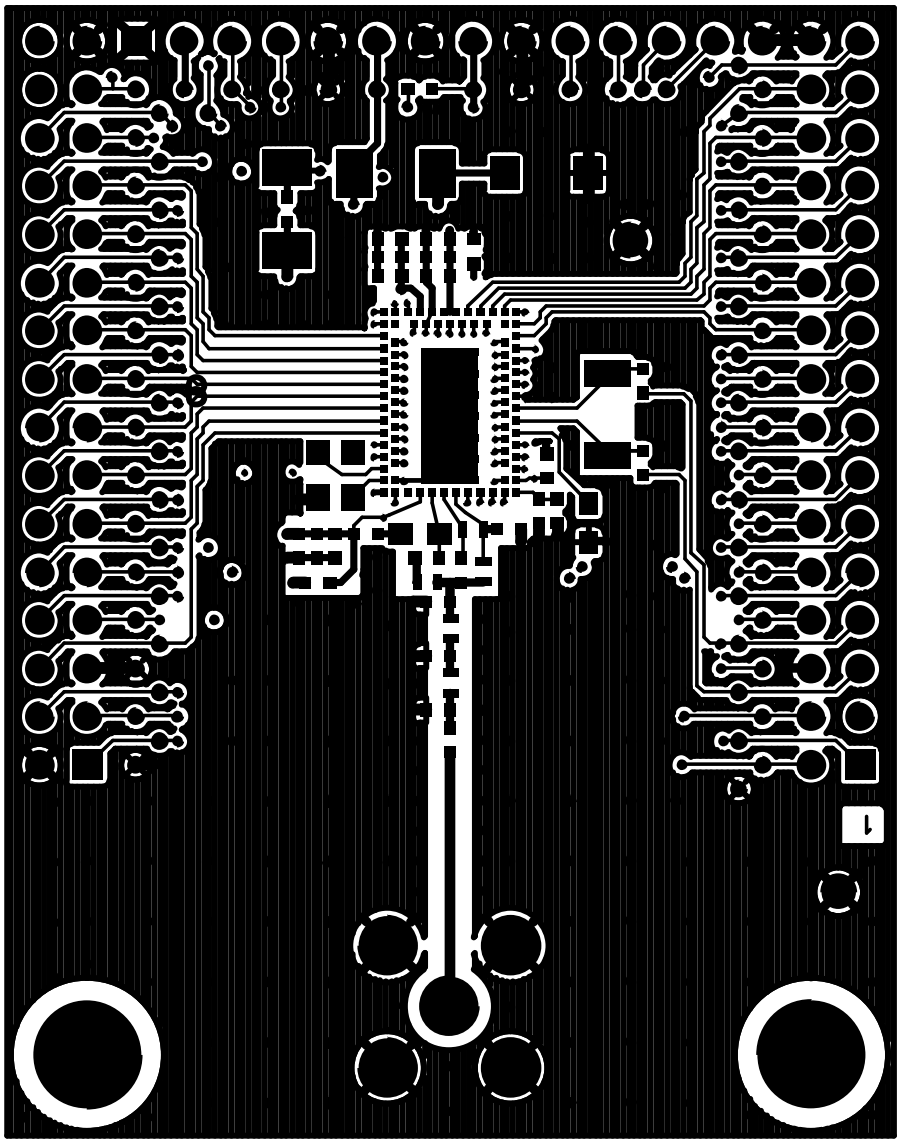


Figure 25. UPPI-1024-fffDT Top Side

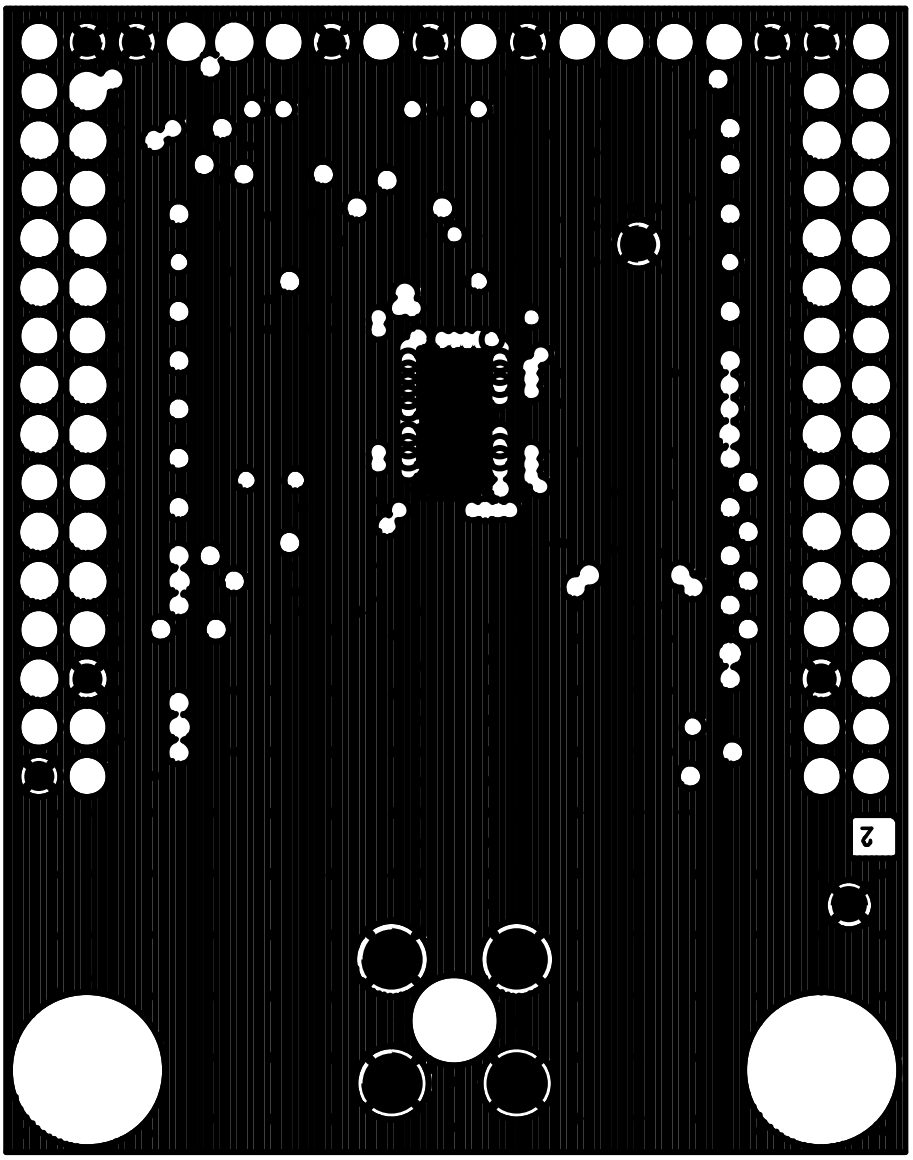


Figure 26. UPPI-1024-fffDT Layer 2

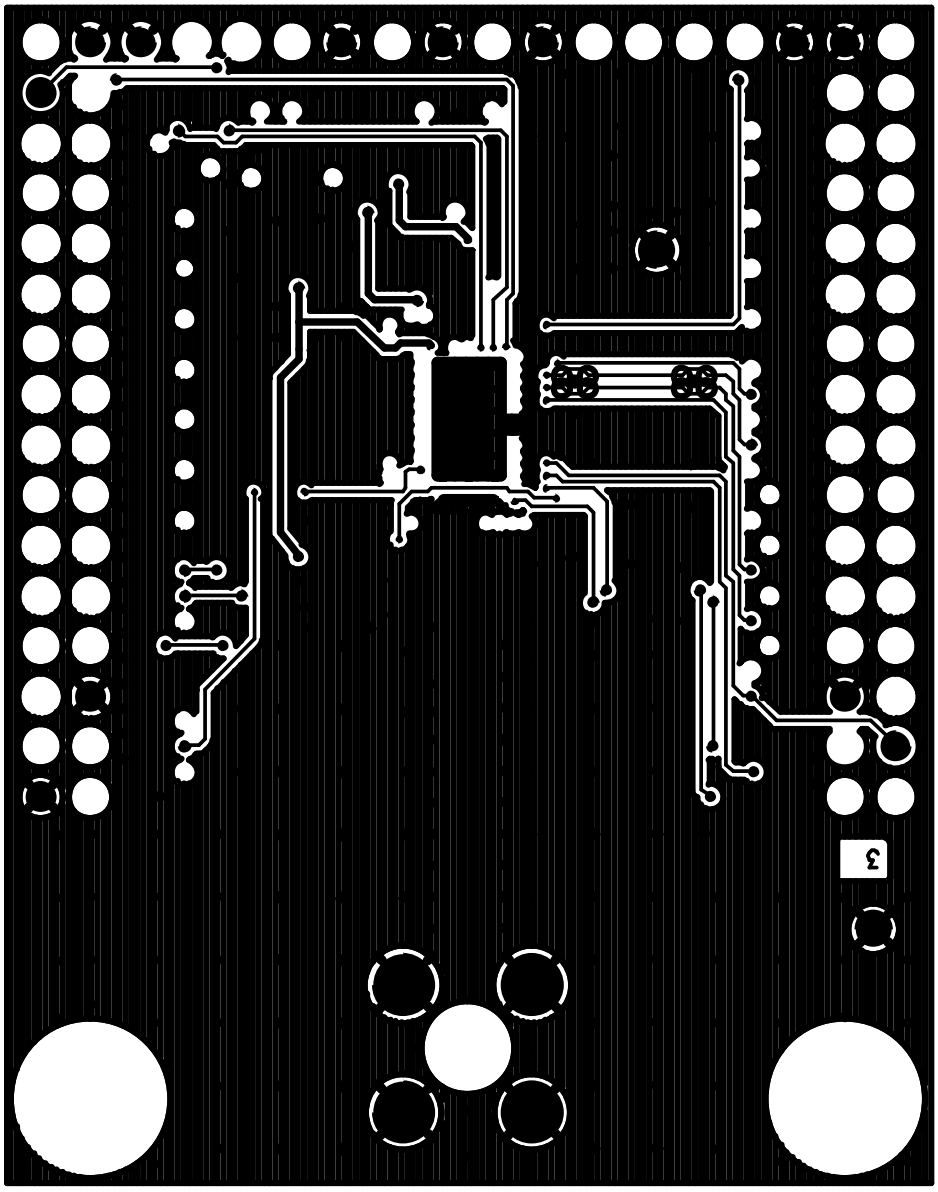


Figure 27. UPPI-1024-fffDT Layer 3

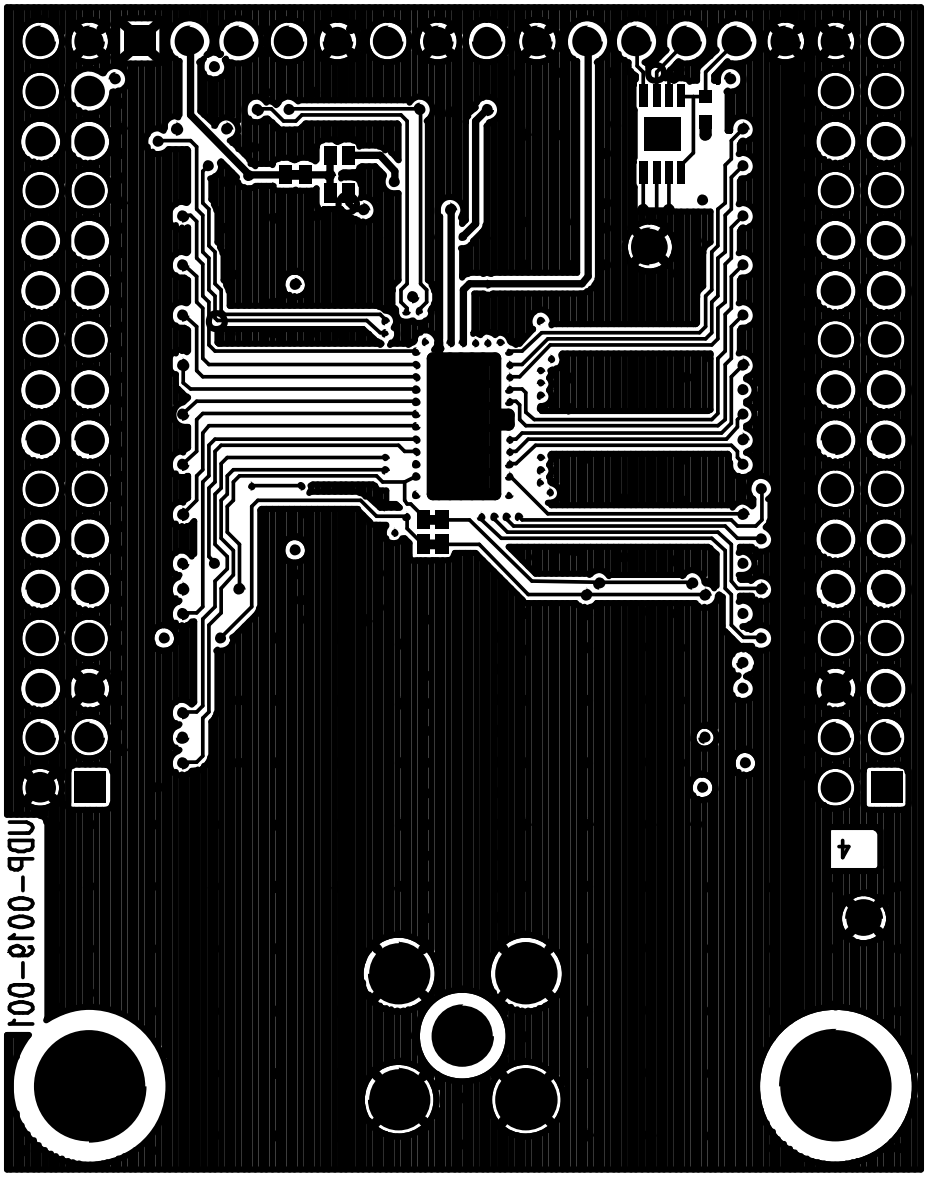


Figure 28. UPPI-1024-fffDT Bottom Side

NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345€C, COLOR, NATURAL.
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5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
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7. MINIMUM ANNULAR RING SHALL BE 0.001".
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11. FINISH SHALL BE LPI, BLUE S.M.O.B.C., BOTH SIDES.
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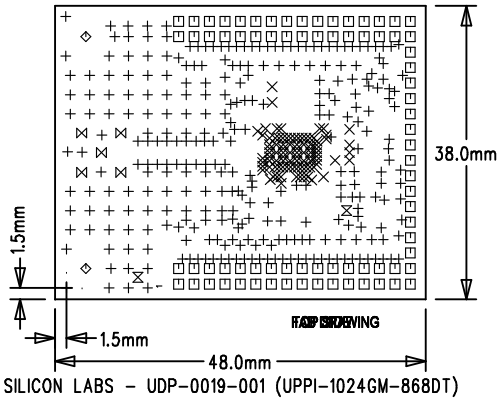
    L2-GND 1 OZ Cu
    PREPREG FR4: 28 MILS
    L3-POWER 1 OZ Cu
    PREPREG FR4: 12 MILS +/- 1 MIL
    BOTTOM LAYER PLATED TO 1 OZ
15. PLATE IN ACCORDANCE WITH IPC-4552, 118-236uIN of NICKEL, WITH AN ADDITIONAL 2-6 uIN OF GOLD ON TOP.

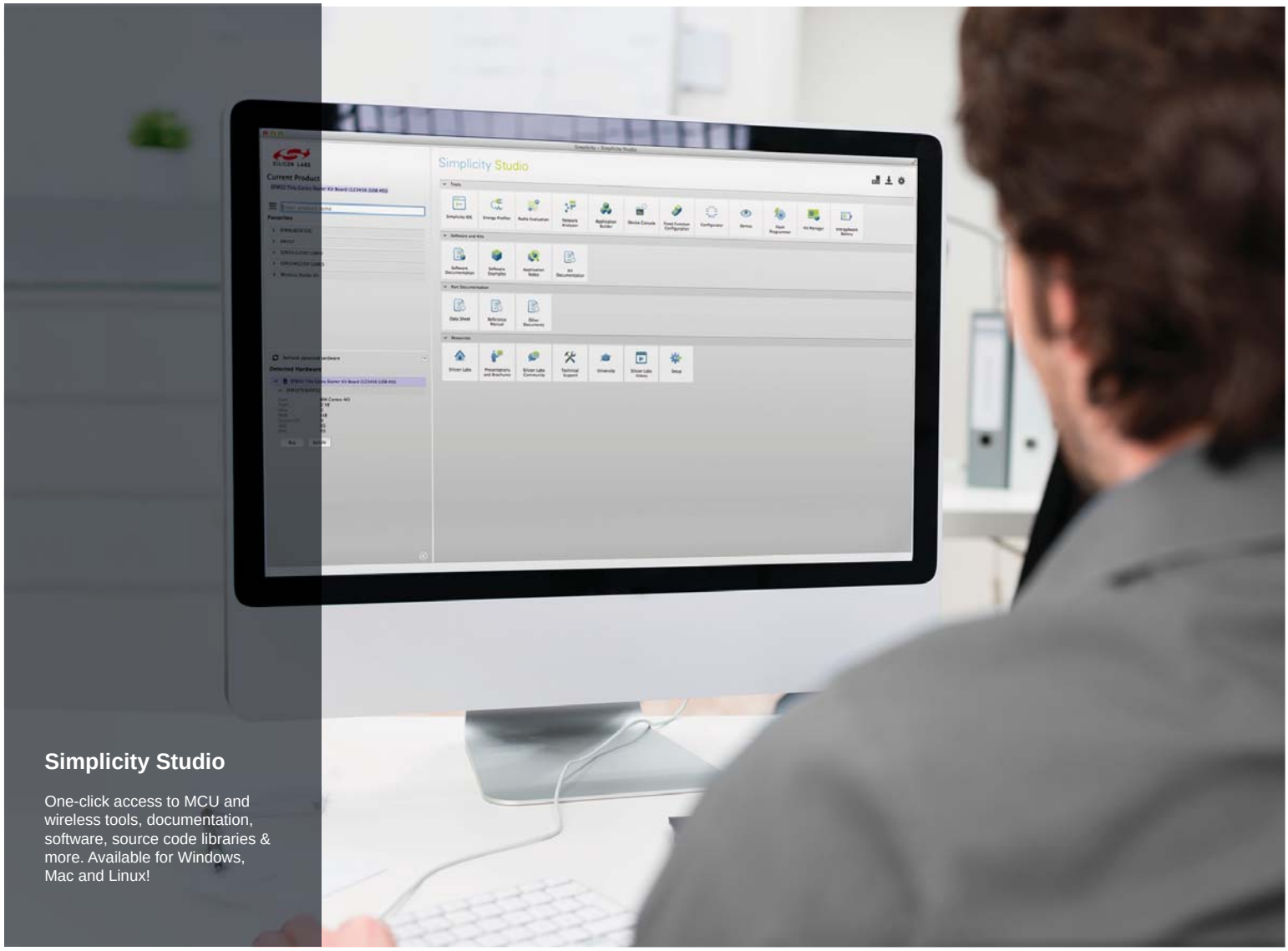
SIZE	QTY	SYM	PLATED	TOL
0.008	291	+	YES	+/-0.003"
0.006	91	X	YES	+/-0.003"
0.03	78	□	YES	+/-0.003"
0.125	2	◇	YES	+/-0.003"
0.04	2	⧖	YES	+/-0.003"
0.07	5	⋈	YES	+/-0.003"



LAYER STACKUP	FILE NAMES
TOP SILKSCREEN	TOPSILK.TSP
TOP SOLDER MASK	SMASKTOP.SMT
TOP SIDE	TOP.TOP
L2	LAYER2.L2
L3	LAYER3.L3
BOTTOM SIDE	BOTTOM.BOT
BOTTOM SOLDER MASK	SMASKBOT.SMB
BOTTOM SILKSCREEN	BOTSILK.BSK

SCALE: NONE

Figure 29. UPPI-1024-fffDT Assembly Layer



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