



**THE DATASHEET OF
SMBJ5358B/TR13**

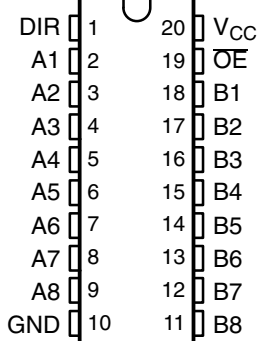


SN54ABT245A, SN74ABT245B OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

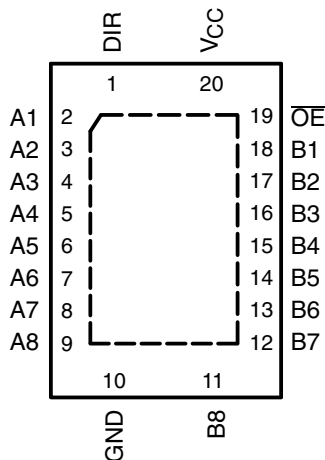
SCBS081L – JANUARY 1991 – REVISED APRIL 2005

- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

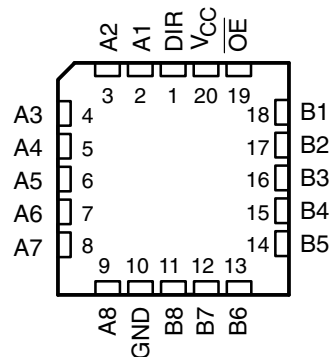
SN54ABT245A . . . J OR W PACKAGE
SN74ABT245B . . . DB, DGV, DW, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74ABT245B . . . RGY PACKAGE
(TOP VIEW)



SN54ABT245B . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ABT245BN	SN74ABT245BN
	QFN – RGY	Tape and reel	SN74ABT245BRGYR	AB245B
	SOIC – DW	Tube	SN74ABT245BDW	ABT245B
		Tape and reel	SN74ABT245BDWR	
	SOP – NS	Tape and reel	SN74ABT245BNSR	ABT245B
	SSOP – DB	Tape and reel	SN74ABT245BDBR	AB245B
	TSSOP – PW	Tube	SN74ABT245BPW	AB245B
		Tape and reel	SN74ABT245BPWR	
	TVSOP – DGV	Tape and reel	SN74ABT245BDGVR	AB245B
VFBGA – GQN	Tape and reel	SN74ABT245BGQNR	AB245B	
		SN74ABT245BZQNR		
-55°C to 125°C	CDIP – J	Tube	SNJ54ABT245AJ	SNJ54ABT245AJ
	CFP – W	Tube	SNJ54ABT245AW	SNJ54ABT245AW
	LCCC – FK	Tube	SNJ54ABT245AFK	SNJ54ABT245AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ABT245A, SN74ABT245B OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

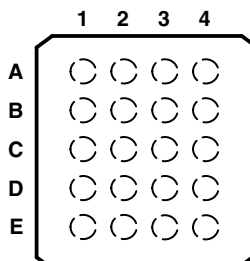
SCBS081L – JANUARY 1991 – REVISED APRIL 2005

description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

SN74ABT245B . . . GQN OR ZQN PACKAGE
(TOP VIEW)



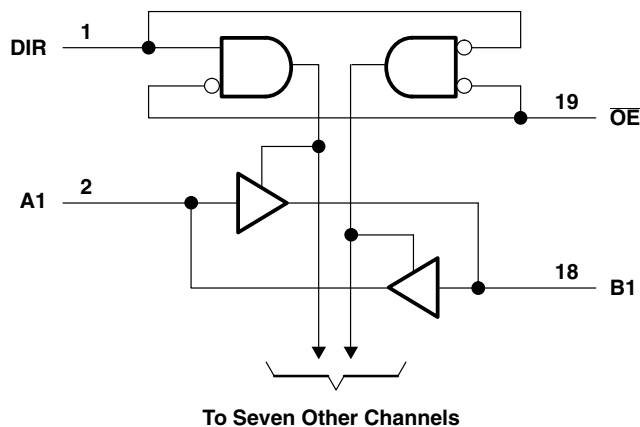
terminal assignments

	1	2	3	4
A	A1	DIR	V_{CC}	\overline{OE}
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.

SN54ABT245A, SN74ABT245B OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS081L – JANUARY 1991 – REVISED APRIL 2005

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT245A	96 mA
SN74ABT245B	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
(see Note 2): DGV package	92°C/W
(see Note 2): DW package	58°C/W
(see Note 2): GQN/ZQN package	78°C/W
(see Note 2): N package	69°C/W
(see Note 2): NS package	60°C/W
(see Note 2): PW package	83°C/W
(see Note 3): RGY package	37°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

	SN54ABT245A		SN74ABT245B		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–24		–32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate				200	μs/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT245A, SN74ABT245B OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS081L – JANUARY 1991 – REVISED APRIL 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT245A		SN74ABT245B		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5		2.5		2.5		V	
	V _{CC} = 5 V, I _{OH} = -3 mA		3		3		3			
	V _{CC} = 4.5 V	I _{OH} = -24 mA		2		2				
I _{OH} = -32 mA			2*				2			
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA			0.55		0.55		V	
		I _{OL} = 64 mA			0.55*			0.55		
V _{hys}			100						mV	
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND			±20		±100		±20	
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA	
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA	
I _{OZH} ‡	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2 V$			10		10		10	μA	
I _{OZL} ‡	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2 V$			-10		-10		-10	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 5.5 V			±100				±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V		-50	-140	-180	-50	-180	-50	-180	
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		5	250		250		250
			Outputs low		22	30		30		30
			Outputs disabled		1	250		250		250
ΔI _{CC} ¶	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled			1.5		1.5		1.5
			Outputs disabled			50		50		50
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	
C _i	Control inputs	V _I = 2.5 V or 0.5 V			4				pF	
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V			8				pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



**SN54ABT245A, SN74ABT245B
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

SCBS081L – JANUARY 1991 – REVISED APRIL 2005

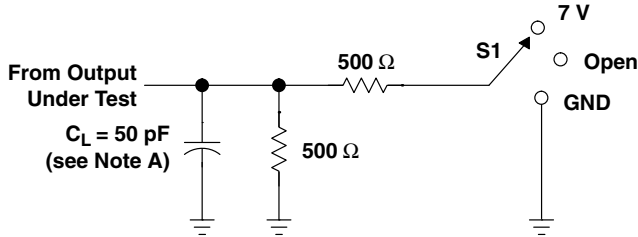
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT245A		SN74ABT245B		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2	3.2	0.8	3.8	1	3.6	ns
t_{PHL}			1	2.6	3.5	1	4.2	1	3.9	
t_{PZH}	\overline{OE}	A or B	2	3.5	4.5	1.2	6.2	2	5.6	ns
t_{PZL}			1.9	4	5.3	1.3	6.8	1.9	6.2	
t_{PHZ}	\overline{OE}	A or B	2.2	4.4	5.4	2.2	6.1	2.2	5.9	ns
t_{PLZ}			1.5	3	4	1.0	4.9	1.5	4.5	
$t_{sk(o)}$					0.5			0.5	ns	

SN54ABT245A, SN74ABT245B OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

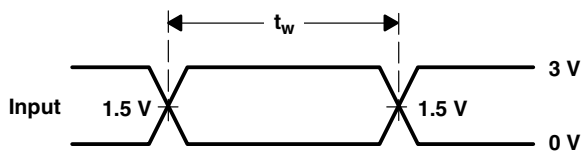
SCBS081L - JANUARY 1991 - REVISED APRIL 2005

PARAMETER MEASUREMENT INFORMATION

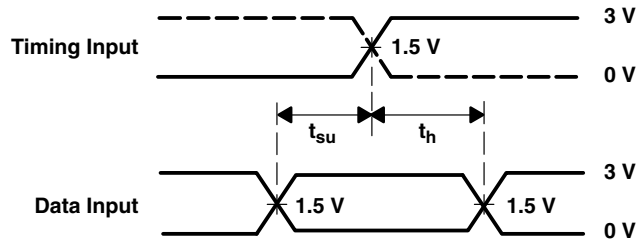


LOAD CIRCUIT

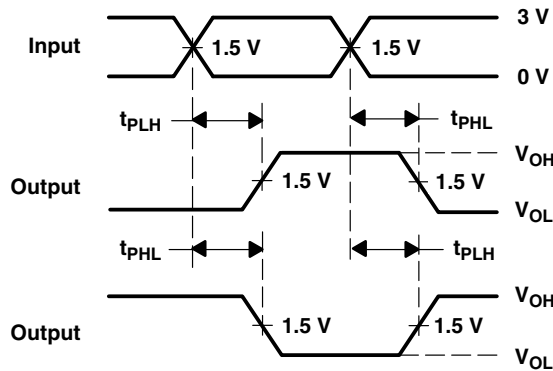
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



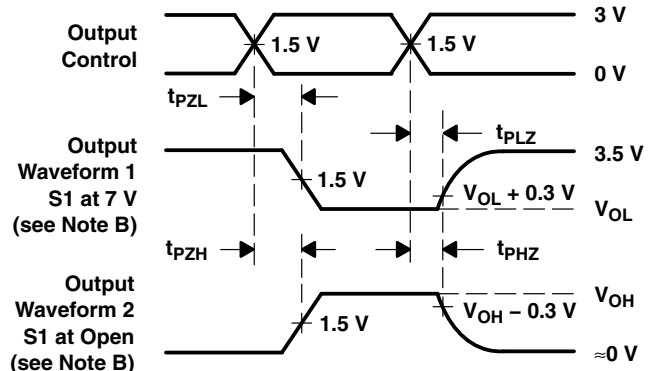
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9214802Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9214802Q2A SNJ54ABT 245AFK	Samples
5962-9214802QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9214802QR A SNJ54ABT245AJ	Samples
5962-9214802QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9214802QS A SNJ54ABT245AW	Samples
SN74ABT245BDBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BDBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT245B	Samples
SN74ABT245BDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT245B	Samples
SN74ABT245BDWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT245B	Samples
SN74ABT245BN	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT245BN	Samples
SN74ABT245BNE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT245BN	Samples
SN74ABT245BNSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT245B	Samples
SN74ABT245BPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BPWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BPWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BRGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AB245B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54ABT245AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9214802Q2A SNJ54ABT 245AFK	Samples
SNJ54ABT245AJ	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9214802QR A SNJ54ABT245AJ	Samples
SNJ54ABT245AW	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9214802QS A SNJ54ABT245AW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74ABT245B :

- Enhanced Product : [SN74ABT245B-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT245BDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT245BDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ABT245BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT245BNSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ABT245BPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74ABT245BRGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT245BDBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74ABT245BDGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74ABT245BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ABT245BNSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ABT245BPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74ABT245BRGYR	VQFN	RGY	20	3000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9214802Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9214802QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ABT245BDW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT245BN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT245BNE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT245BPW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74ABT245BPWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54ABT245AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ABT245AW	W	CFP	20	25	506.98	26.16	6220	NA

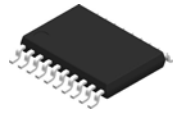
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

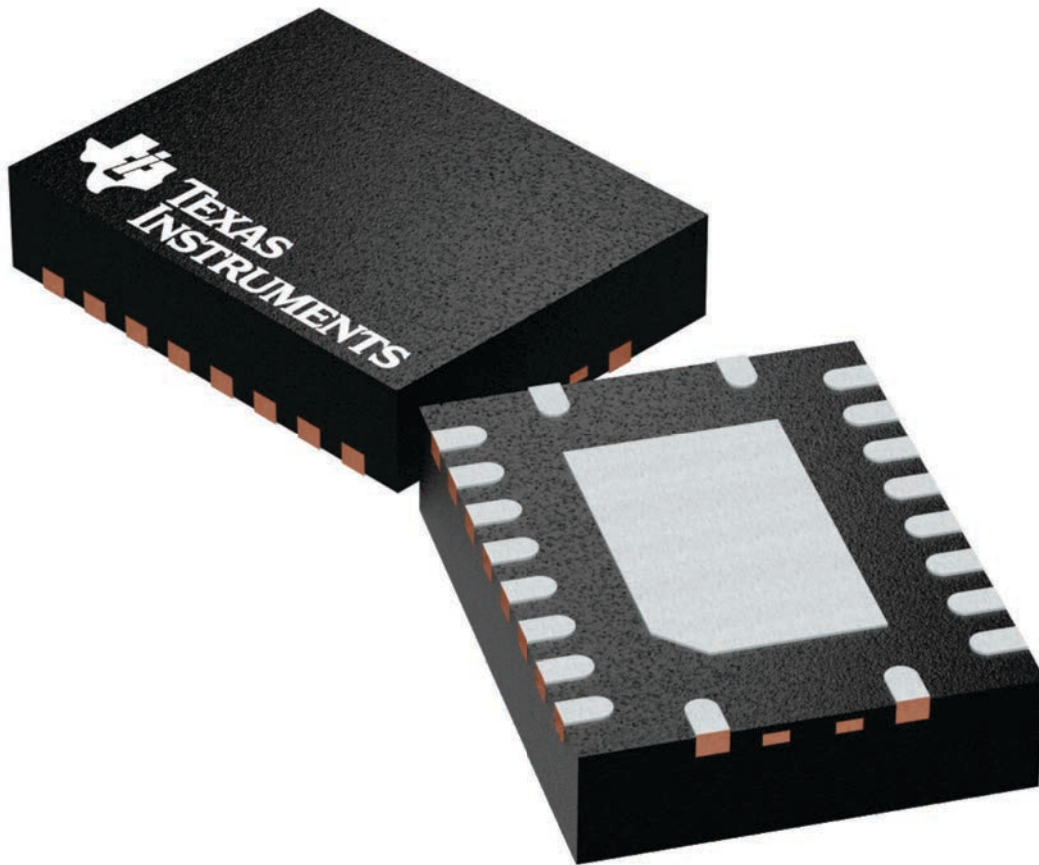
RGY 20

VQFN - 1 mm max height

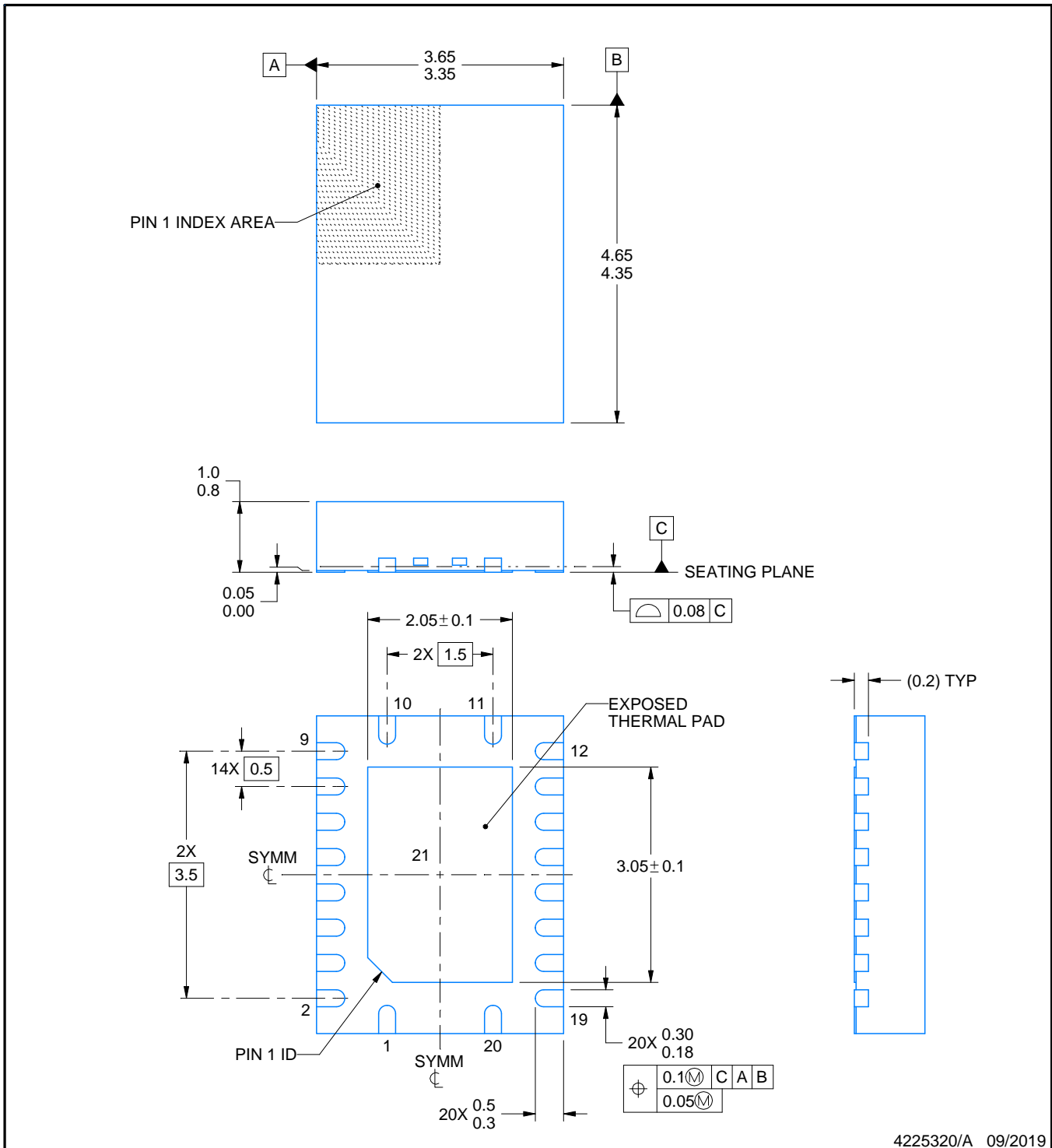
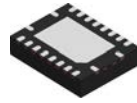
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

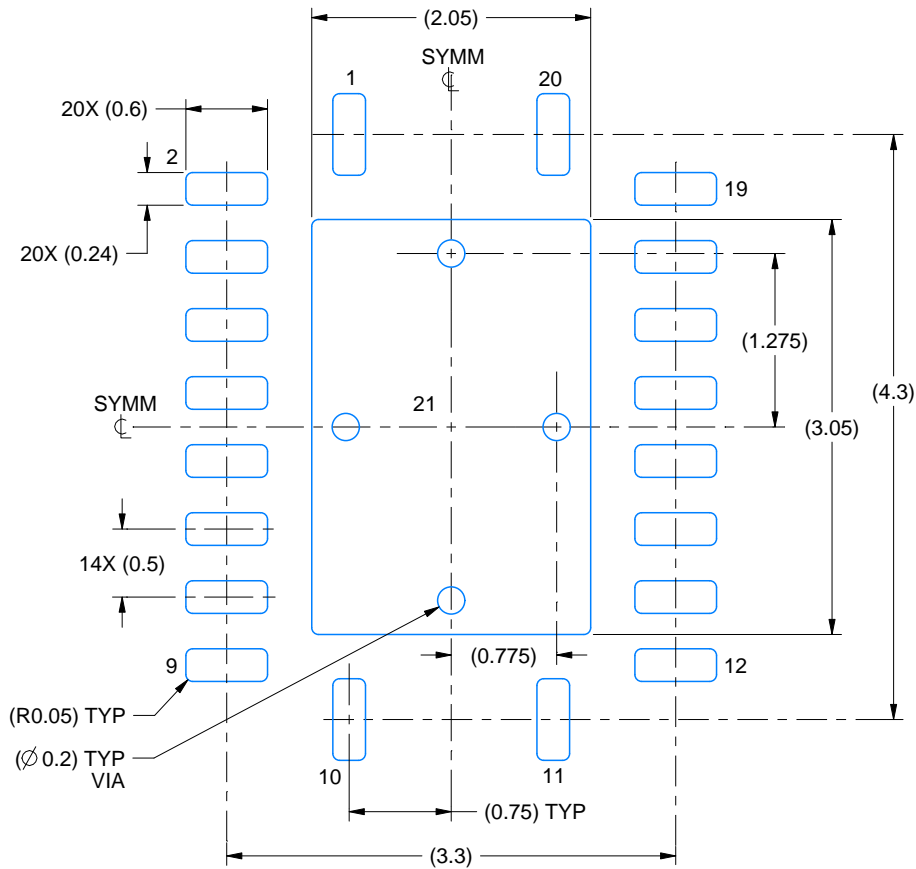
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

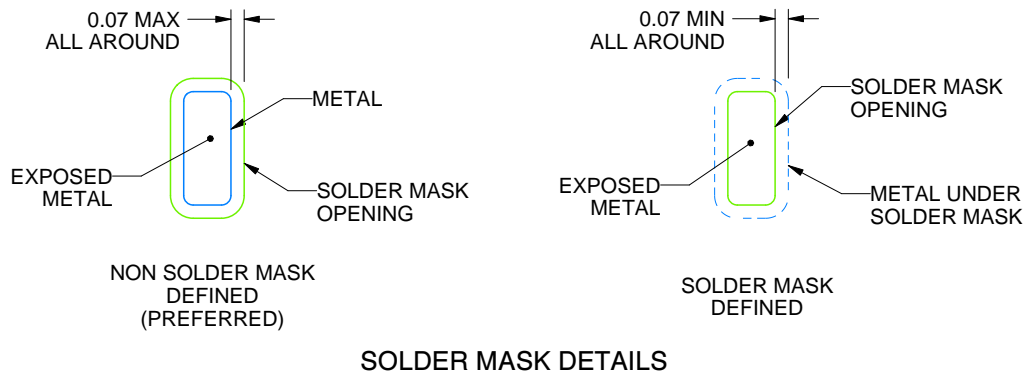
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

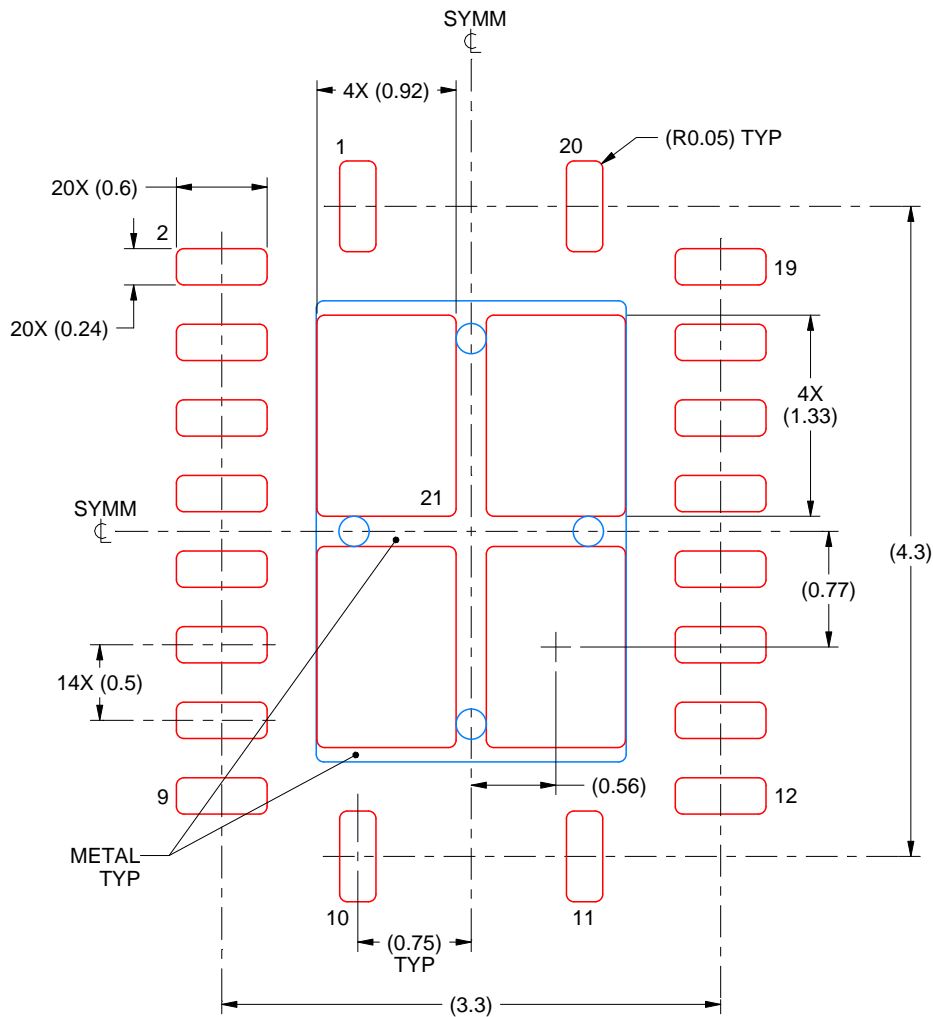
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

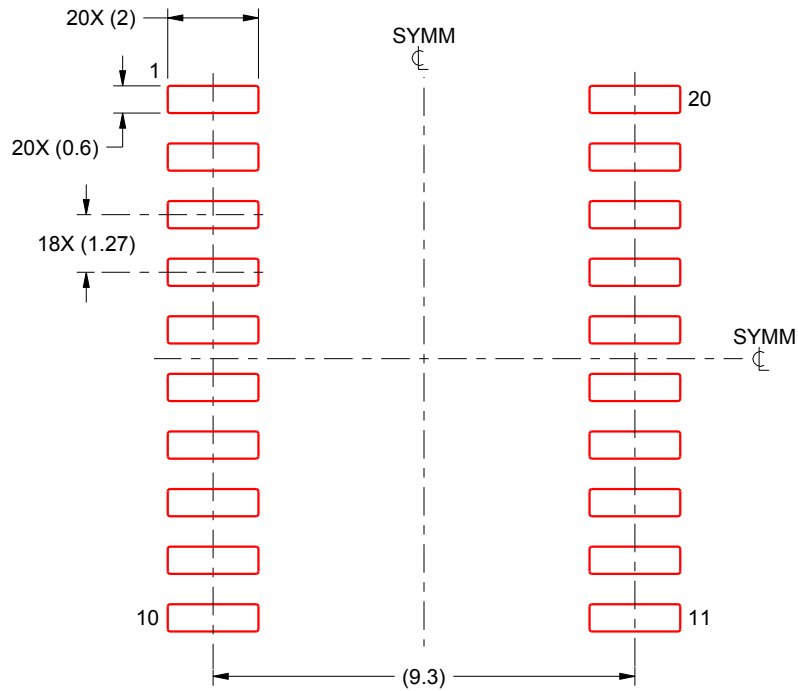
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View SMBJ5358B/TR13 on WIN SOURCE](#)
- ⊖ [Microchip Technology](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management