THE DATASHEET OF

SMBJ5935C/TR13

TPS929121-Q1 12-Channel Automotive 40-V High-Side LED Driver With FlexWire

1 Features

- AEC-Q100-qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- 12-channel precision high-side current output:
  - Supply voltage 4.5 V to 40 V
  - Up to 75-mA channel current set by resistor
  - 2-bit global, 6-bit independent current setting
  - High current accuracy < ±5% at 5 mA to 75 mA
  - High current accuracy < ±10% at 1 mA
  - Low voltage drop 500 mV at 50 mA
  - 12-bit independent PWM dimming
  - Programmable PWM frequency up to 20 kHz
  - Linear and exponential dimming method
- FlexWire control interface
  - Up to 1-MHz clock frequency
  - Maximum 16 devices on one FlexWire bus
  - Up to 8-bytes data transaction in one frame
  - 5-V LDO output to supply CAN transceiver
- Diagnostic and protection:
  - Programmable fail-safe state
  - LED open-circuit detection
  - LED short-circuit detection
  - Single-LED short-circuit diagnostic
  - Programmable low-supply detection
  - Open-drain $\overline{\text{ERR}}$ for fault indication
  - Watchdog and CRC for FlexWire interface
  - 8-Bit ADC for pin voltage measurement
  - Overtemperature protection

2 Applications

- Automotive exterior rear light
- Automotive exterior headlight
- Automotive interior ambient light
- Automotive cluster display

3 Description

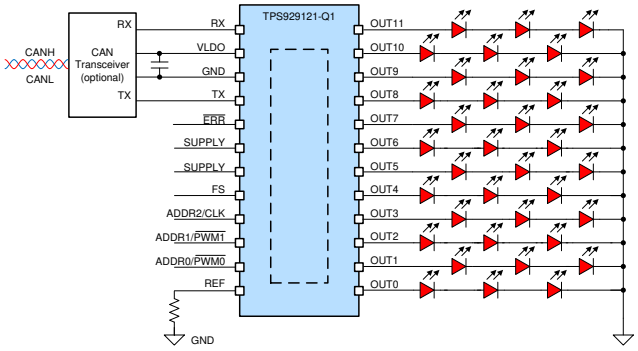
With increasing demand for animation in automotive lighting, LEDs must be controlled independently. Therefore, LED drivers with digital interfaces are essential to effectively drive pixel-controlled lighting applications. In exterior lighting, multiple lamp functions are typically located on different PCB boards with off-board wires connected to each other. It is difficult for a traditional single-ended interface to meet the strict EMC requirements. By using an industrial-standard CAN physical layer, the UART-based FlexWire interface of the TPS929121-Q1 easily accomplishes long distance off-board communication without impacting EMC.

The TPS929121-Q1 is a 12-channel, 40-V high-side LED driver that controls the 8-bit output current and 12-bit PWM duty cycles. The device meets multiple regulation requirements with LED open-circuit, short-to-ground, and single LED short-circuit diagnostics. A configurable watchdog also automatically sets fail-safe states when the MCU connection is lost, and, with programmable EEPROM, TPS929121-Q1 can flexibly be set for different application scenarios.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS929121-Q1	HTSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (February 2021)	Page
• Changed status from "Advance Information" to "Production Data"	1

5 Device Comparison Table

TPS929120QPWPRQ1	TPS929120AQPWPRQ1	TPS929121QPWPRQ1	TPS929121AQPWPRQ1
ADC coverage up to 20 V		ADC coverage up to 40 V	
$V_{(ADCLOWSUPTH)}$ = 5 V to 20 V		$V_{(ADCLOWSUPTH)}$ = 10 V to 40 V	
EEP_DEVADDR[3]=0 (default)	EEP_DEVADDR[3]=1 (default)	EEP_DEVADDR[3]=0 (default)	EEP_DEVADDR[3]=1 (default)

6 Pin Configuration and Functions

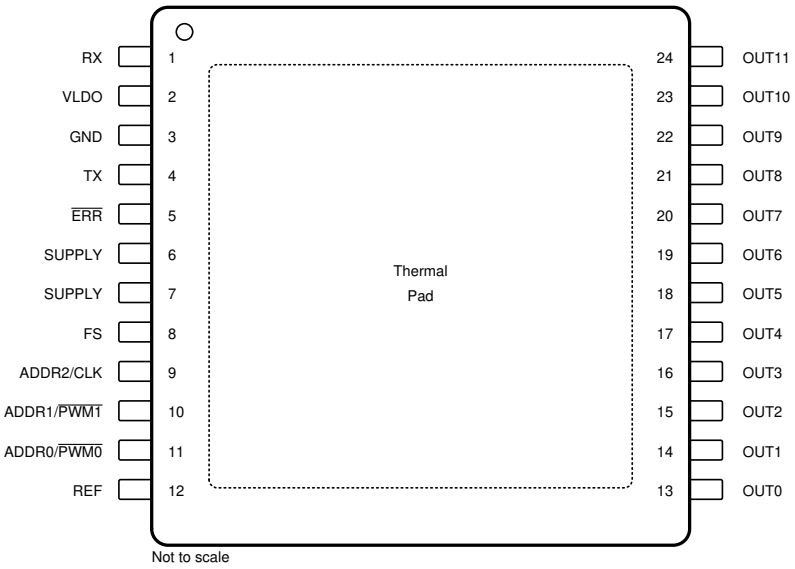


Figure 6-1. PWP Package 24-Pin HTSSOP With PowerPAD™ Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	RX	I	FlexWire RX.
2	VLDO	Power	5-V regulator output.
3	GND	GND	Device ground.
4	TX	O	FlexWire TX.
5	$\overline{\text{ERR}}$	I/O	Open-drain error output.
6, 7	SUPPLY	Power	Power supply.
8	FS	I	Fail-safe state selection. 0: Fail-safe state 0; 1: Fail-safe state 1.
9	ADDR2/CLK	I	Function as device address 2 in external address mode; Function as PWM clock input internal address mode when CONF_EXTCLK is 1.
10	ADDR1/ $\overline{\text{PWM1}}$	I	Function as device address 1 in external address mode; Function as PWM input channel for OUT6-11 in internal address mode.
11	ADDR0/ $\overline{\text{PWM0}}$	I	Function as device address 0 in external address mode; Function as PWM input channel for OUT0-5 in internal address mode.
12	REF	I/O	Device reference current setting, EEPROM programming chip-selection input.
13	OUT0	O	Output channel 0.
14	OUT1	O	Output channel 1.
15	OUT2	O	Output channel 2.
16	OUT3	O	Output channel 3.
17	OUT4	O	Output channel 4.
18	OUT5	O	Output channel 5.
19	OUT6	O	Output channel 6.
20	OUT7	O	Output channel 7.
21	OUT8	O	Output channel 8.
22	OUT9	O	Output channel 9.
23	OUT10	O	Output channel 10.
24	OUT11	O	Output channel 11.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
SUPPLY	Device supply voltage	–0.3	45	V
FS	High-voltage input	–0.3	$V_{(SUPPLY)}$ + 0.3	V
OUT0 - 11	High-voltage outputs	–0.3	$V_{(SUPPLY)}$ + 0.3	V
$\overline{ERR}$	High-voltage output	–0.3	22	V
ADDR2/CLK, ADDR1/$\overline{PWM1}$, ADDR0/$\overline{PWM0}$, REF, RX	Low-voltage input	–0.3	5.5	V
VLDO, TX	Low-voltage output	–0.3	5.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (RX, REF, OUT0, OUT11)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY	Device supply voltage	4.5		36	V
IOUT0-IOUT11	Channel output current	0.5		75	mA
FS	External fail-safe selection input	0		$V_{(SUPPLY)}$	V
TX	FlexWire TX output	0		5	V
RX	FlexWire RX input	0		5	V
VLDO	Internal 5V LDO output	0		5	V
$I_{(VLDO)}$	LDO external current load	0		80	mA
ADDR2/CLK, ADDR1/$\overline{PWM1}$, ADDR0/$\overline{PWM0}$	Device address selection and external CLK/PWM inputs	0		5	V
REF	Current reference setting	0		5	V
$\overline{ERR}$	Error feedback open-drain output	0		20	V
$t_{(r\_RX)}$	RX risetime			5%/f_{CLK}	
$t_{(f\_RX)}$	RX falltime			5%/f_{CLK}	
f_{CLK}	FlexWire frequency	10		1000	kHz
D_{SYNC}	Synchronization pulse dutycycle	45	50	55	%
T_A	Ambient temperature	–40		125	°C

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS929121-Q1 HTSSOP (PWP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

T_J = –40°C to 150°C, $V_{(SUPPLY)}$ = 5-40 V, For digital outputs, $C_{(LOAD)}$ = 20 pF, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS						
$V_{(SUPPLY)}$	Operating input voltage		4.5	12	40	V
$I_{Q(ON)}$	Quiescent current, all-channels-on	$V_{(SUPPLY)}$ = 12 V, $R_{(REF)}$ =31.6 kΩ, all-output ON			10	mA
$I_{Q(OFF)}$	Quiescent current, all-channels-off	$V_{(SUPPLY)}$ = 12 V, $R_{(REF)}$ = 31.6 kΩ, all-output OFF			3.5	mA
$I_{(FAULT)}$	Quiescent current, fail-safe state fault mode	$V_{(SUPPLY)}$ = 12 V, fail-safe state, all-output OFF, $\overline{ERR}$ = LOW		2.5	2.85	mA
$V_{(POR\_rising)}$	Power-on-reset rising threshold		4	4.2	4.4	V
$V_{(POR\_falling)}$	Power-on-reset falling threshold		3.8	4	4.2	V
$V_{(LDO)}$	LDO output voltage	$V_{(SUPPLY)}$ > 5.6 V, $I_{(LDO)}$ = 40 mA, CONF_LDO = 0b	4.75	5	5.25	V
		$V_{(SUPPLY)}$ > 5.6 V, $I_{(LDO)}$ = 40 mA, CONF_LDO = 1b	4.18	4.4	4.62	V
$I_{(LDO)}$	LDO output current capability				80	mA
$I_{(LDO\_LIMIT)}$	LDO output current limit		100			mA
$V_{(LDO\_DROP)}$	LDO maximum dropout voltage	$I_{(LDO)}$ = 80 mA		0.5	0.9	V
$V_{(LDO\_DROP)}$	LDO maximum dropout voltage	$I_{(LDO)}$ = 50 mA		0.3	0.6	V
$V_{(LDO\_POR\_rising)}$	LDO power-on-reset rising threshold		2.75	3	3.25	V
$V_{(LDO\_POR\_falling)}$	LDO power-on-reset falling threshold		2.5	2.75	3	V
$C_{(LDO)}$	Supported LDO loading capacitance range		1		10	µF
$f_{(OSC)}$	Internal oscillator frequency		-2.5%	32.15	+2.5%	MHz
ERR						
$V_{IL(\overline{ERR})}$	Input logic low voltage, $\overline{ERR}$				0.7	V
$V_{IH(\overline{ERR})}$	Input logic high voltage, $\overline{ERR}$		2			V
$I_{(pd\_\overline{ERR})}$	$\overline{ERR}$ pull-down current capability	$V_{(\overline{ERR})}$ = 0.4 V	3	6	9	mA

7.5 Electrical Characteristics (continued)

T_J = –40°C to 150°C, $V_{(SUPPLY)}$ = 5-40 V, For digital outputs, $C_{(LOAD)}$ = 20 pF, (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{lkg(\overline{ERR})}$	$\overline{ERR}$ leakage current				1	µA
FLEXWIRE INTERFACE						
$V_{IL(RX)}$	Input logic low voltage, RX				0.7	V
$V_{IH(RX)}$	Input logic high voltage, RX		2			V
$V_{OL(TX)}$	Low-level output voltage TX,	I_{sink} = 5 mA,	0		0.3	V
$V_{OH(TX)}$	High-level output voltage TX,	I_{source} = 5 mA, $V_{pull-up}$ = 5 V	4.7		5	V
I_{lkg}	TX, RX		–1		1	µA
ADDRESS, FS						
$V_{IL(IO)}$	Input logic low voltage, ADDR2/CLK, ADDR1/$\overline{PWM1}$, ADDR0/$\overline{PWM0}$, FS				0.7	V
$V_{IH(IO)}$	Input logic high voltage, ADDR2/CLK, ADDR1/$\overline{PWM1}$, ADDR0/$\overline{PWM0}$, FS		2			V
$R_{(PD\_ADDR)}$	Internal pull down resistance, ADDR2/CLK, ADDR1/$\overline{PWM1}$, ADDR0/$\overline{PWM0}$			100		kΩ
$R_{(PD\_FS)}$	Internal pull down resistance, FS			100		kΩ
ADC						
DNL	Differential nonlinearity		–1[1]		1[1]	LSB
INL	Integral nonlinearity		–2[1]		2[1]	LSB
OUTPUT DRIVERS						
$f_{(PWM\_200)}$		200-Hz selection		200		Hz
$f_{(PWM\_1000)}$		1-kHz selection		1000		Hz
$\Delta I_{(OUT\_d2d)}$	Device-to-device accuracy $\Delta I_{(OUT\_d2d)}$ = 1- $I_{avg(OUT)}$ / $I_{ideal(OUT)}$	$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 11b, DC=63	–5	0	5	%
		$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 10b, DC=63	–5	0	5	
		$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 01b, DC=63	–5	0	5	
		$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 00b, DC=63	–5	0	5	
$\Delta I_{(OUT\_c2c)}$	Channel-to-channel accuracy $\Delta I_{(OUT\_c2c)}$ = 1- $I_{(OUTx)}$ / $I_{avg(OUT)}$	$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 11b, DC=63	–3	0	3	%
		$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 10b, DC=31	–3	0	3	
		$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 01b, DC=15	–5	0	5	
		$R_{(REF)}$ = 31.6 kOhm, CONF_REFRANGE = 01b, DC=12	–7	0	7	
$I_{(OUT\_75mA)}$		$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 11b, DC=63		75		mA
$I_{(OUT\_50mA)}$		$R_{(REF)}$ = 12.7 kOhm, CONF_REFRANGE = 11b, DC=63		50		mA
$I_{(OUT\_20mA)}$		$R_{(REF)}$ = 31.6 kOhm, CONF_REFRANGE = 11b, DC=63		20		mA
$I_{(OUT\_1mA)}$		$R_{(REF)}$ = 31.6 kOhm, CONF_REFRANGE = 01b, DC = 12		1		mA
$V_{(OUT\_drop)}$	output dropout voltage	$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 11b, DC=38, $I_{(OUTx)}$ = 45 mA		400	700	mV

7.5 Electrical Characteristics (continued)

T_J = –40°C to 150°C, $V_{(SUPPLY)}$ = 5-40 V, For digital outputs, $C_{(LOAD)}$ = 20 pF, (unless otherwise noted).

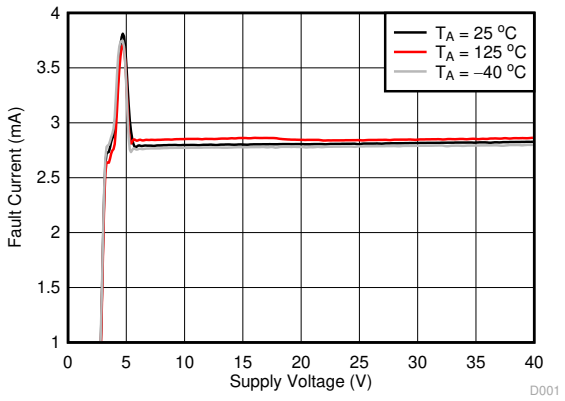
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OUT\_drop)}$	output dropout voltage	$R_{(REF)}$ = 8.45 kOhm, CONF_REFRANGE = 11b, DC=63, $I_{(OUTx)}$ = 75 mA		600	1000	mV
$R_{(REF)}$			1		50	kΩ
$C_{(REF)}$			0		4.7	nF
$V_{(REF)}$				1.235		V
$K_{(REF\_11)}$		CONF_REFRANGE = 11b		512		
$K_{(REF\_10)}$		CONF_REFRANGE = 10b		256		
$K_{(REF\_01)}$		CONF_REFRANGE = 01b		128		
$K_{(REF\_00)}$		CONF_REFRANGE = 00b		64		
$I_{(REF\_OPEN\_th)}$				10		µA
$V_{(REF\_SHORT\_th)}$				0.6		V
DIAGNOSTICS						
$V_{(OPEN\_th\_rising)}$	LED open rising threshold	$V_{(SUPPLY)}$ - $V_{(OUTx)}$	200	400	600	mV
$V_{(OPEN\_th\_falling)}$	LED open falling threshold	$V_{(SUPPLY)}$ - $V_{(OUTx)}$	300	500	700	mV
$V_{(OPEN\_th\_hyst)}$				100		mV
$V_{(SG\_th\_rising)}$	Short-to-ground rising threshold		0.8	0.9	1	V
$V_{(SG\_th\_falling)}$	Short-to-ground falling threshold		1.1	1.2	1.3	V
$V_{(SG\_th\_hyst)}$	Short-to-ground hysteresis			0.3		V
EEPROM						
$N_{(EEP)}$	Number of programming cycles.	$V_{(SUPPLY)}$ = 12 V	1000			
MISC						
$T_{(PRETSD)}$	Pre-thermal warning threshold			135		°C
$T_{(PRETSD\_HYS)}$	Pre-thermal warning hysteresis			5		°C
$T_{(TSD)}$	Over-temperature protection threshold		160	175	190	°C
$T_{(TSD\_HYS)}$	Over-temperature protection hysteresis			15		°C

(1) Guaranteed by design only

7.6 Timing Requirements

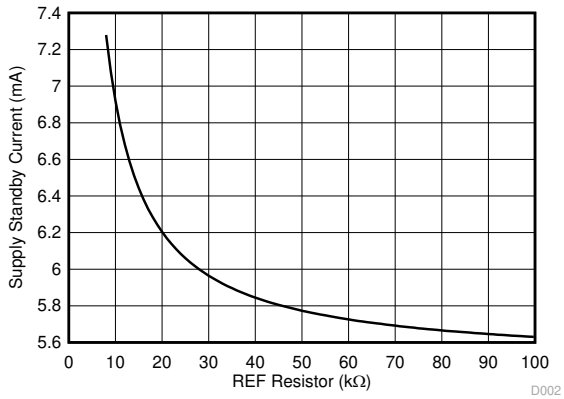
		MIN	NOM	MAX	UNIT
$t_{(ODPW)}$	Diagnostics pulse-width, CONF_ODPW = 0h		100		µs
$t_{(CONV)}$	time needed to complete one AD conversion		57		µs
$t_{(OPEN\_deg)}$	Open-circuit deglitch timer		5		µs
$t_{(SHORT\_deg)}$	Short-circuit deglitch timer		5		µs
$t_{(retry)}$	Fault retry timer		10		ms

7.7 Typical Characteristics



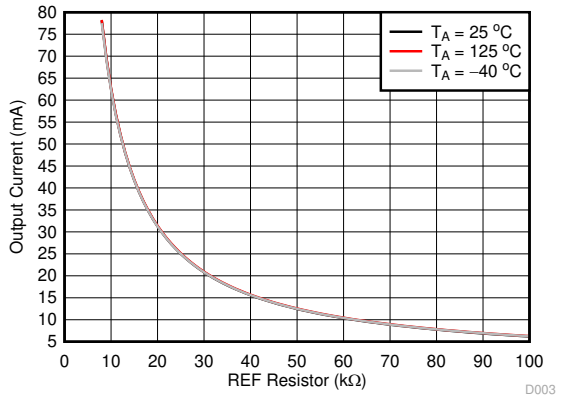
$R_{(REF)}$ = 8.35 kΩ
CONF_REFRANGE[1:0] = 3h

Figure 7-1. Fault Current vs Supply Voltage



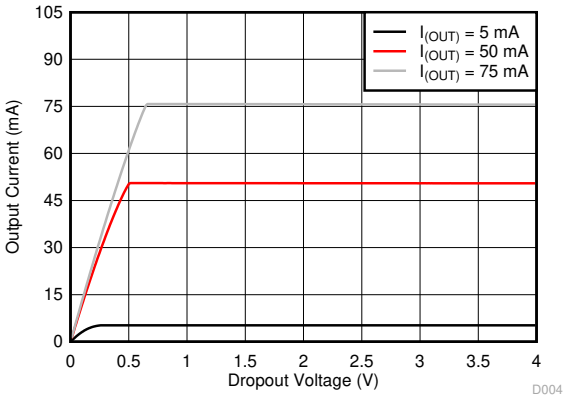
CONF_REFRANGE[1:0] = 3h

Figure 7-2. Standby Current vs REF Resistor



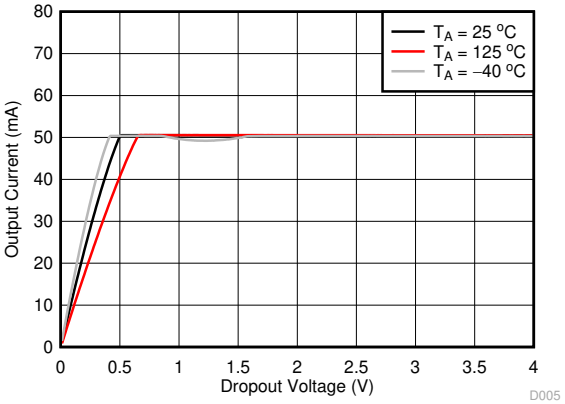
CONF_IOUTx[5:0] = 3Fh
CONF_REFRANGE[1:0] = 3h

Figure 7-3. Output Full-range Current vs REF Resistor



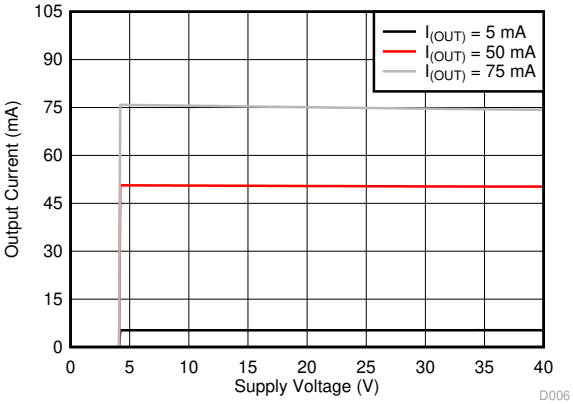
CONF_REFRANGE[1:0] = 3h

Figure 7-4. Output Current vs Dropout Voltage



$R_{(REF)}$ = 12.6 kΩ
CONF_IOUTx[5:0] = 3Fh

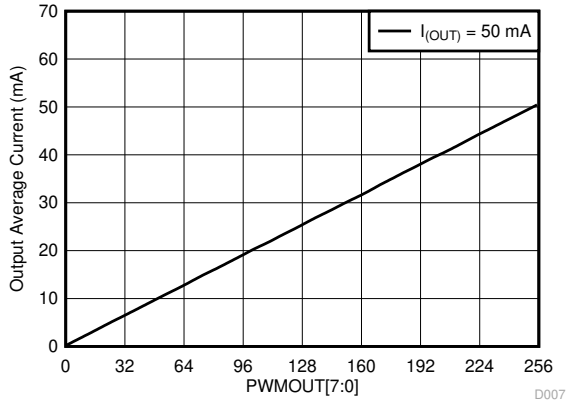
Figure 7-5. Output Current vs Dropout Voltage



CONF_REFRANGE[1:0] = 3h

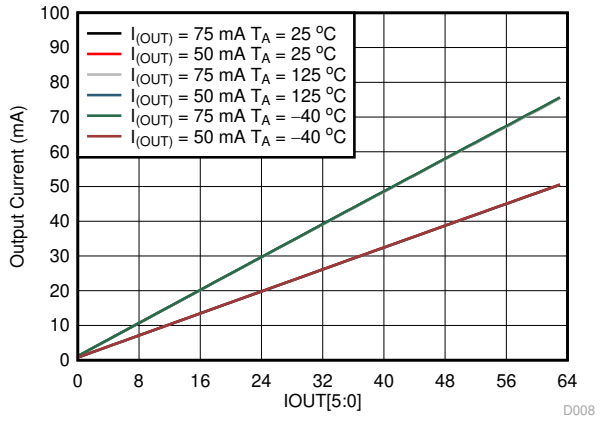
Figure 7-6. Output Current vs Supply Voltage

7.7 Typical Characteristics



$R_{(REF)}$ = 12.6 kΩ
CONF_IOUTx[5:0] = 3Fh

Figure 7-7. Average Current vs PWMOUT[7:0]



$R_{(REF)}$ = 8.35 kΩ & 12.6 kΩ
CONF_REFRANGE[1:0] = 3h

Figure 7-8. Output DC Current vs IOUT[5:0]

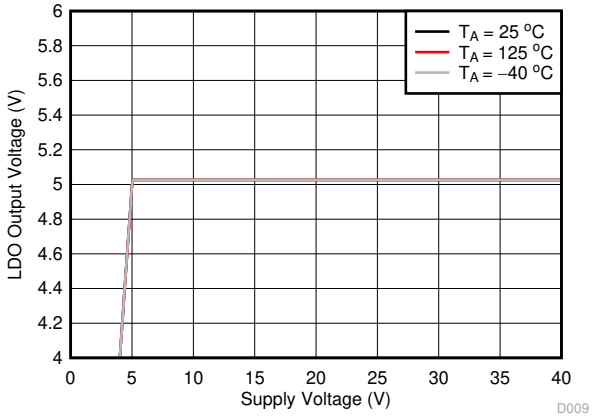


Figure 7-9. LDO Output Line Regulation

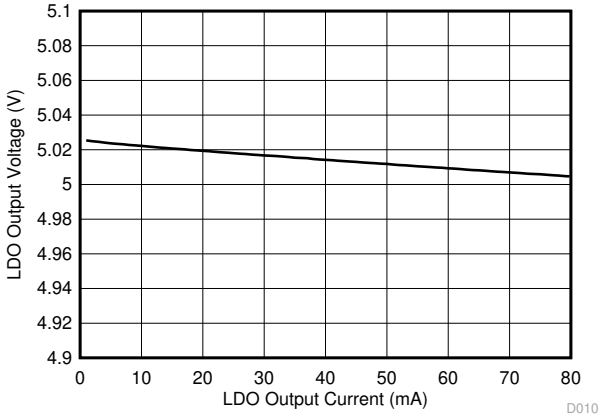
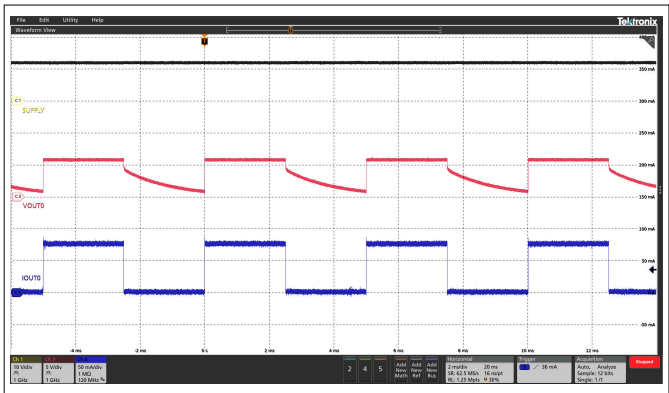
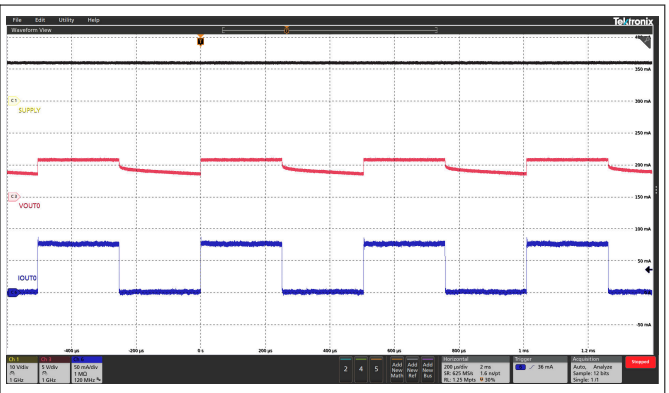


Figure 7-10. LDO Output Load Regulation



Ch1 = $V_{(SUPPLY)}$ Ch3 = $V_{(OUT0)}$ Ch6 = $I_{(OUT0)}$

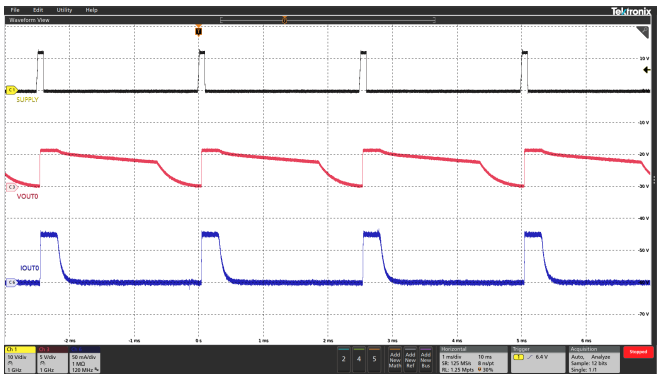
Figure 7-11. PWM Dimming at 200 Hz



Ch1 = $V_{(SUPPLY)}$ Ch3 = $V_{(OUT0)}$ Ch6 = $I_{(OUT0)}$

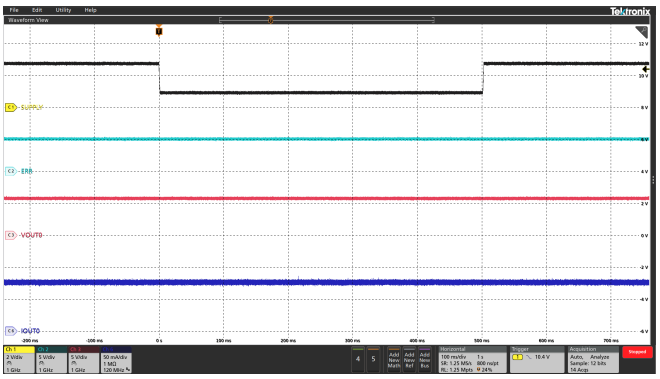
Figure 7-12. PWM Dimming at 2000 Hz

7.7 Typical Characteristics (continued)



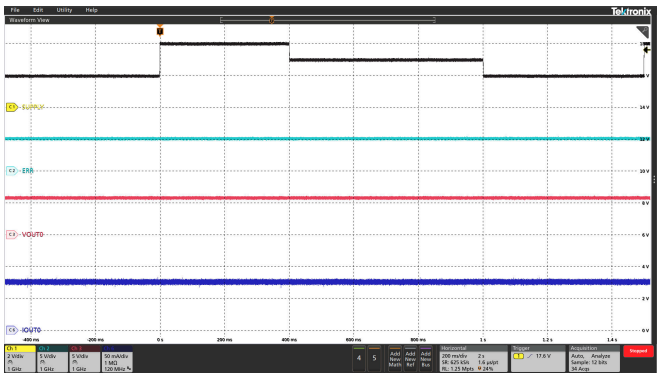
Ch1 = $V_{(SUPPLY)}$ Ch3 = $V_{(OUT0)}$ Ch6 = $I_{(OUT0)}$

Figure 7-13. Supply Dimming In Fail-Safe Mode



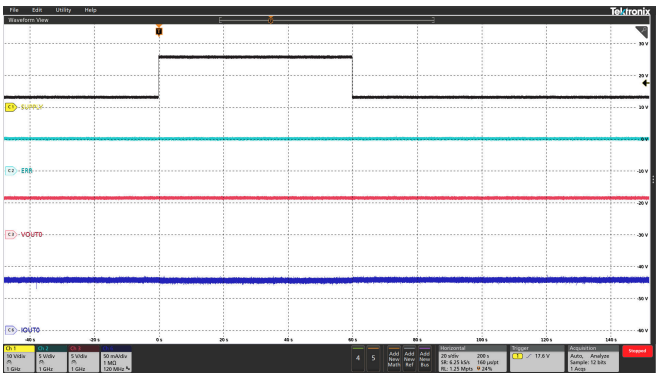
Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT0)}$
Ch6 = $I_{(OUT0)}$

Figure 7-14. Transient Undervoltage



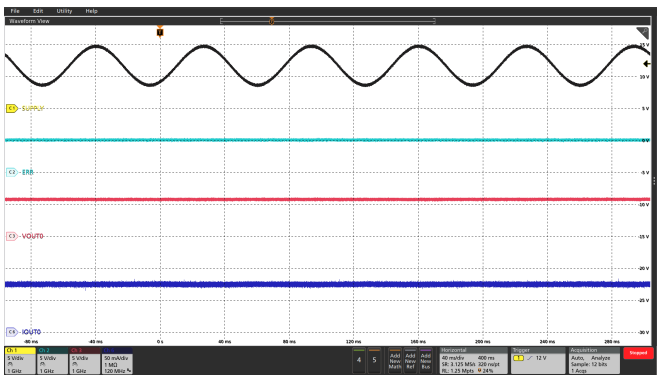
Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT0)}$
Ch6 = $I_{(OUT0)}$

Figure 7-15. Transient Overvoltage



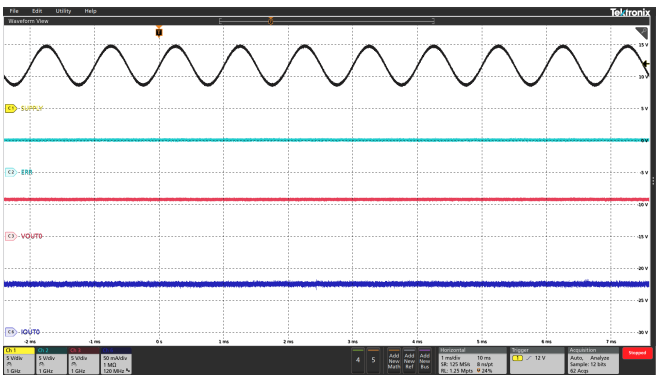
Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT0)}$
Ch6 = $I_{(OUT0)}$

Figure 7-16. Jump Start



Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT0)}$
Ch6 = $I_{(OUT0)}$

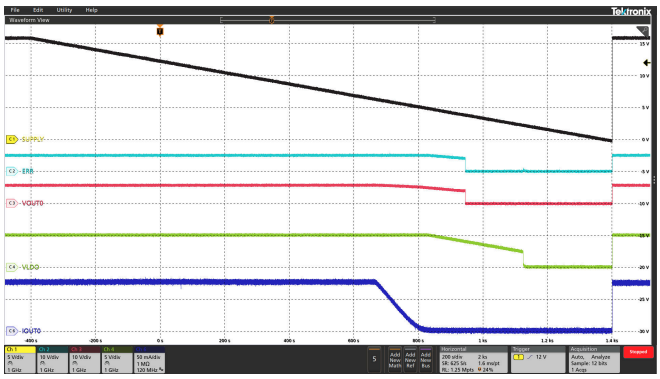
Figure 7-17. Superimposed Alternating Voltage 15 Hz



Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT0)}$
Ch6 = $I_{(OUT0)}$

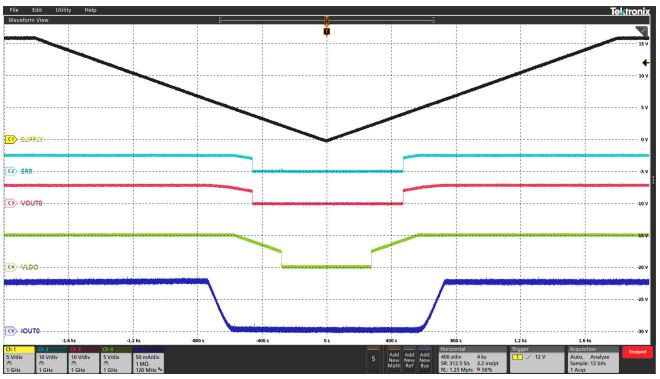
Figure 7-18. Superimposed Alternating Voltage 1 kHz

7.7 Typical Characteristics (continued)



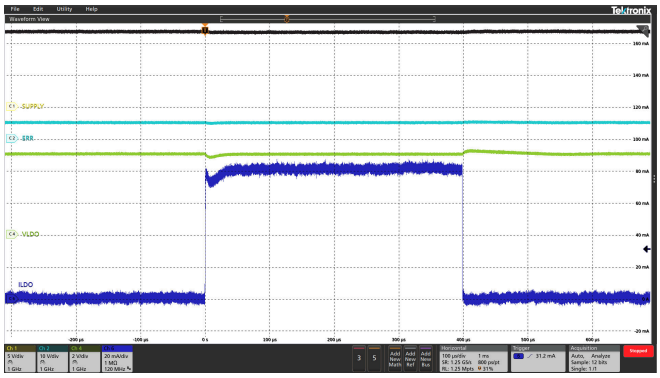
Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT0)}$
Ch4 = $V_{(LDO)}$ Ch6 = $I_{(OUT0)}$

Figure 7-19. Slow Decrease and Quick Increase of Supply Voltage



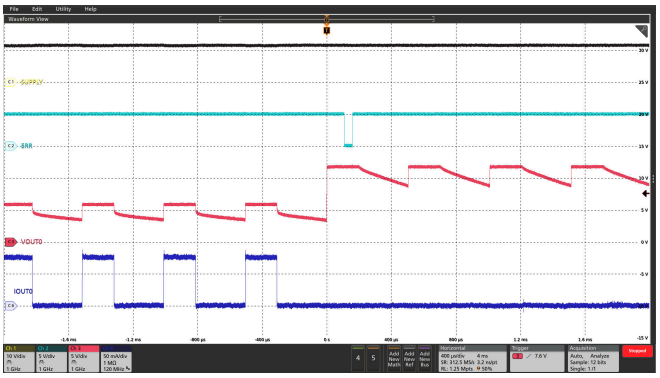
Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT0)}$
Ch4 = $V_{(LDO)}$ Ch6 = $I_{(OUT0)}$

Figure 7-20. Slow Decrease and Slow Increase of Supply Voltage



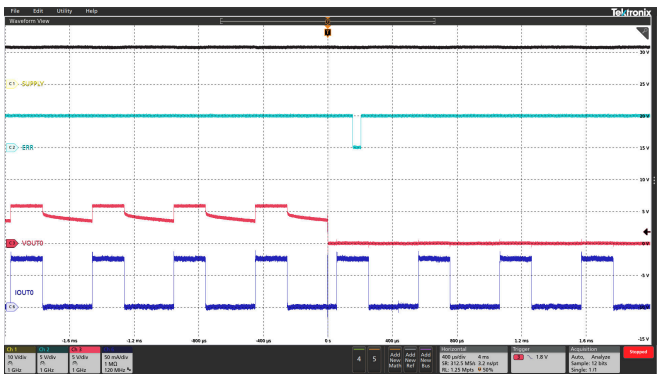
Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch4 = $V_{(LDO)}$
Ch6 = $I_{(LDO)}$ 0 to 80 mA

Figure 7-21. LDO Output Load Transient



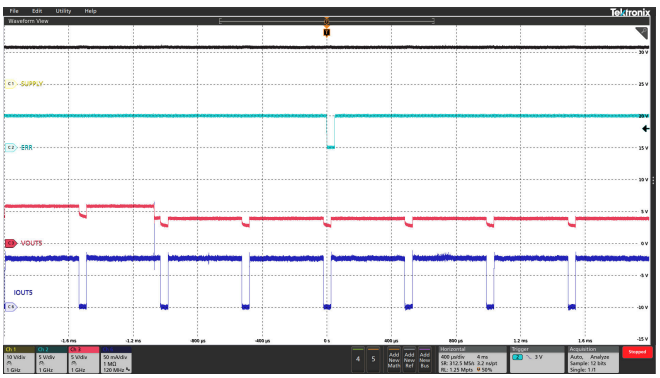
Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT0)}$
Ch6 = $I_{(OUT0)}$ $T_{(ODPW)}$ = 100 µs $F_{(PWM)}$ = 2 kHz

Figure 7-22. LED Open-Circuit Detection In Normal Mode



Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT0)}$
Ch6 = $I_{(OUT0)}$ $T_{(ODPW)}$ = 100 µs $F_{(PWM)}$ = 2 kHz

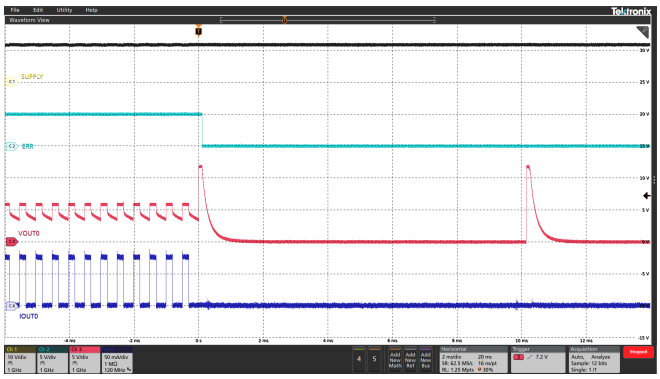
Figure 7-23. LED Short-Circuit Detection In Normal Mode



Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT5)}$
Ch6 = $I_{(OUT5)}$ $T_{(ODPW)}$ = 100 µs $F_{(PWM)}$ = 2 kHz
$V_{(ADCSHORTTH)}$ = 4 V

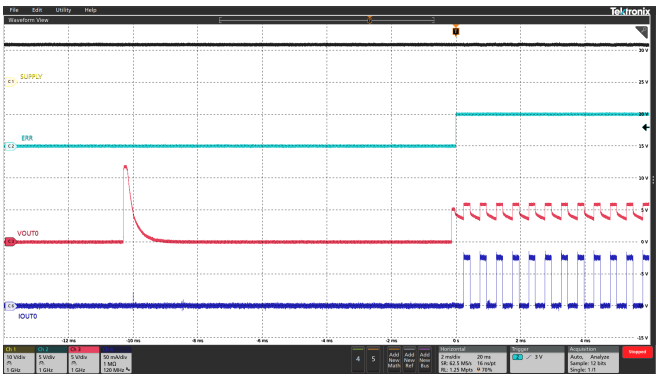
Figure 7-24. Single-LED Short-Circuit Detection In Normal Mode

7.7 Typical Characteristics (continued)



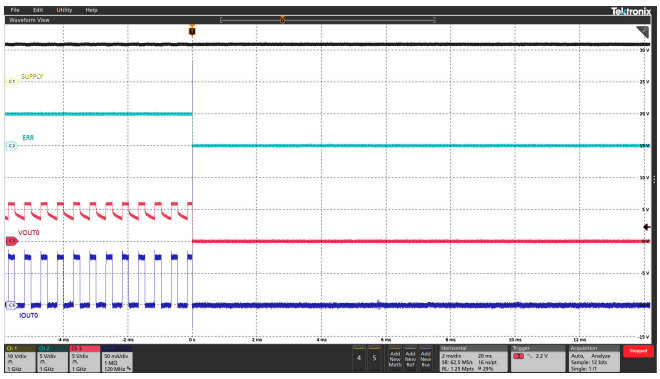
Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT5)}$
Ch6 = $I_{(OUT0)}$ $T_{(ODPW)}$ = 100 µs $F_{(PWM)}$ = 2 kHz

Figure 7-25. LED Open-Circuit Detection In FS Mode



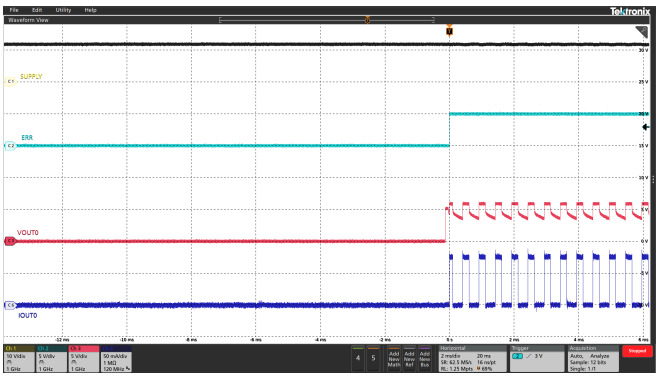
Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT5)}$
Ch6 = $I_{(OUT0)}$ $T_{(ODPW)}$ = 100 µs $F_{(PWM)}$ = 2 kHz

Figure 7-26. LED Open-Circuit Recovery In FS Mode



Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT5)}$
Ch6 = $I_{(OUT0)}$ $T_{(ODPW)}$ = 100 µs $F_{(PWM)}$ = 2 kHz

Figure 7-27. LED Short-Circuit Detection In Fail-Safe Mode



Ch1 = $V_{(SUPPLY)}$ Ch2 = $\overline{ERR}$ Ch3 = $V_{(OUT5)}$
Ch6 = $I_{(OUT0)}$ $T_{(ODPW)}$ = 100 µs $F_{(PWM)}$ = 2 kHz

Figure 7-28. LED Short-Circuit Recovery In Fail-Safe Mode

8 Detailed Description

8.1 Overview

TPS929121-Q1 is an automotive 12-channel LED driver with FlexWire interface to address increasing requirements for individual control of each LED string. Each of its channel can support both analog dimming and pulse-width-modulation (PWM) dimming, configured through its FlexWire serial interface. The internal electrically erasable programmable read-only memory (EEPROM) allows users to configure device in the scenario of communication loss to fulfill system level safety requirements.

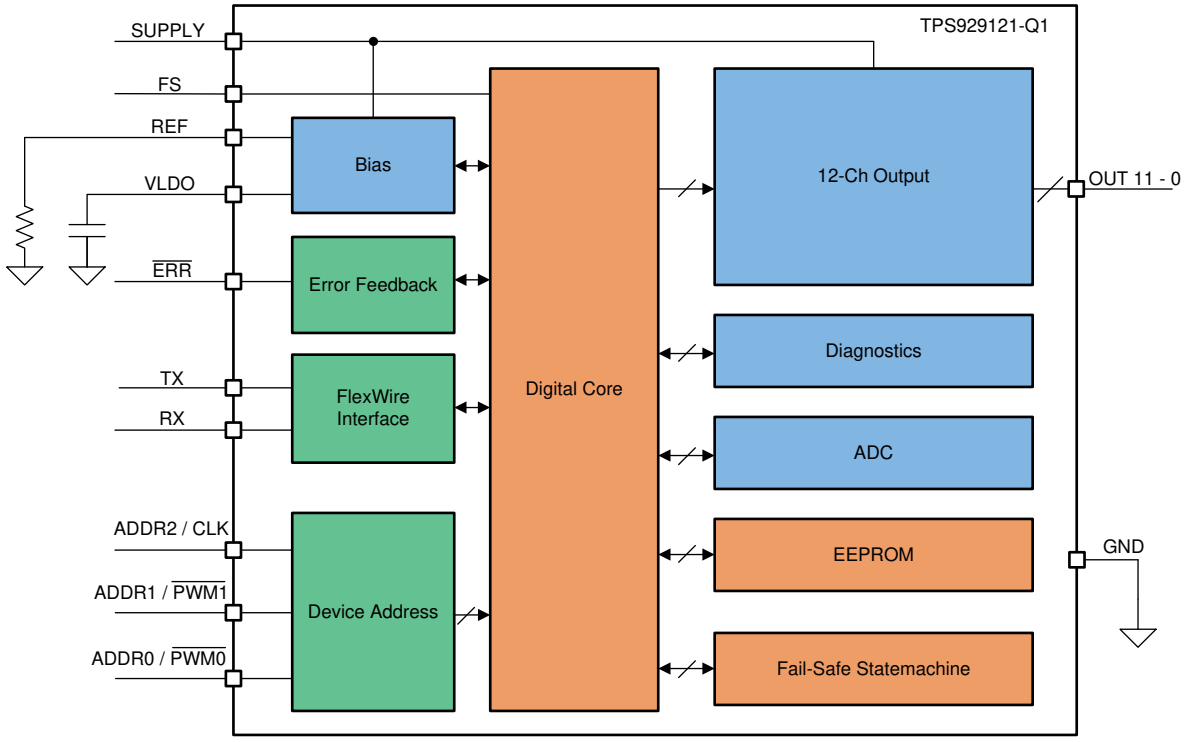
The FlexWire interface is a robust address-based master-slave interface with flexible baud rate. The interface is based on multi-frame universal asynchronous receiver-transmitter (UART) protocol. The unique synchronization frame of FlexWire reduces system cost by saving external crystal oscillators. It also supports various physical layer with the help of external physical layer transceiver such as CAN or LIN transceivers. The embedded CRC correction is able to ensure robust communication in automotive environments. The FlexWire interface is easily supported by most MCUs in the markets.

Each output is a constant current source with individually programmable current output and PWM duty cycle. Each channel features various diagnostics including LED open-circuit, short-circuit and single-LED short-circuit detection. The on-chip analog-digital convertor (ADC) allows controller to real-time monitor loading conditions.

To further increase robustness, the unique fail-safe of the device state machine allows automatic switching to fail-safe states in the case of communication loss, for example, MCU failure. The device supports programming fail-safe settings with user-programmable EEPROM. In fail-safe states, the device supports different configurations if output fails, such as one-fails-all-fail or one-fails-others-on. Each channel can be independently programmed as on or off in fail-safe states. The fail-safe state machine also allows the system to function with pre-programmed EEPROM settings without presence of any controller in the system, also known as stand-alone operation.

The microcontroller can access each of the device through the FlexWire interface. By setting and reading back the registers, the master, which is the microcontroller, has full control over the device and LEDs. All EEPROMs are pre-programmed to default values. TI recommends that users program the EEPROM at the end-of-line for application-specific settings and fail-safe configurations.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Device Bias and Power

8.3.1.1 Power Supply (SUPPLY)

The TPS929121-Q1 is AECQ-100 qualified for automotive applications. The power input to the device through SUPPLY pin can be low to 4.5 V and up to 40 V for automotive battery directly powered systems.

8.3.1.2 5-V Low-Drop-Out Linear Regulator (VLDO)

The TPS929121-Q1 has an integrated low-drop-out linear regulator to provide power supply to external CAN transceivers, such as TCAN1042. The internal LDO powered by supply voltage $V_{(SUPPLY)}$ provides a stable 5-V output with up to 80-mA constant current capability. TI recommends a ceramic capacitor from 1 µF to 10 µF on the VLDO pin. The LDO has an internal current limit $I_{(LDO\_LIMIT)}$ for protection and soft start. The capacitor charging time must be considered to total start-up time period, because the device is held in POR state if the capacitor voltage is not charged to above UVLO threshold.

8.3.1.3 Undervoltage Lockout (UVLO) and Power-On-Reset (POR)

In order to ensure clean start-up, the TPS929121-Q1 uses UVLO and POR circuitry to clear its internal registers upon power-up and to reset registers with its default values.

The TPS929121-Q1 has internal UVLO circuits so that when either power supply voltage $V_{(SUPPLY)}$ or LDO output voltage $V_{(LDO)}$ is lower than its UVLO threshold, POR is triggered. In POR state, the device resets digital core and all registers to default value. FLAG_POR register is set to 1 for each POR cycle to indicate the POR history.

Before both powers are above UVLO thresholds, the TPS929121-Q1 stays in POR state with all outputs off and $\overline{ERR}$ pulled down. Once both power supplies are above UVLO threshold, the device enters INIT mode for initialization releasing $\overline{ERR}$ pulldown. A programmable timer starts counting in INIT state, the timer length can be set by EEPROM register EEP_INITTIMER. When the timer is completed, the device switches to normal state. In INIT state, setting CLR_POR to 1 clears FLAG_POR, disables the timer, and sets the device to normal state.

Upon powering up, the TPS929121-Q1 automatically loads all settings stored in EEPROM to correlated registers and sets the other registers to default value which don't have correlated EEPROM. All channels are powered up in off-state by default to avoid unwanted blinking.

Writing 1 to CLR_REG manually loads EEPROM setting to the correlated registers and set the other registers to default value. After CLR_REG is set, the FLAG_POR is set 1 to indicate registers clear to default values. Writing 1 to CLR_POR resets the FLAG_POR register to 0. TI recommends settting CLR_REG to 1 to clear the internal registers every time after POR. The CLR_REG automatically resets to 0.

8.3.1.4 Programmable Low Supply Warning

The TPS929121-Q1 uses its internal ADC to monitor supply voltage $V_{(SUPPLY)}$. If the supply is below allowable working threshold, the output voltage may not be sufficient to keep the LED operating with desired brightness output as expected. The ADC output is automatically compared with threshold set by register CONF_ADCLOWSUPTH as described in *Register Maps*. When the supply voltage is below threshold, the device sets warning flag register FLAG_ADCLOWSUP to 1 in the status register. CLR_FAULT is able to clear the FLAG_ADCLOWSUP as well as other fault registers. In addition, the LED open-circuit and single LED short-circuit detection is disabled if the supply voltage is below threshold to avoid LED open circuit and to prevent the single LED short-circuit fault from being mis-triggered. The 4-bit register CONF_ADCLOWSUPTH has total 15 options covering from 5 V to 20 V.

8.3.2 Constant Current Output

8.3.2.1 Reference Current With External Resistor (REF)

The TPS929121-Q1 must have an external resistor $R_{(REF)}$ to set the internal current reference $I_{(REF)}$ as shown in Figure 8-1.

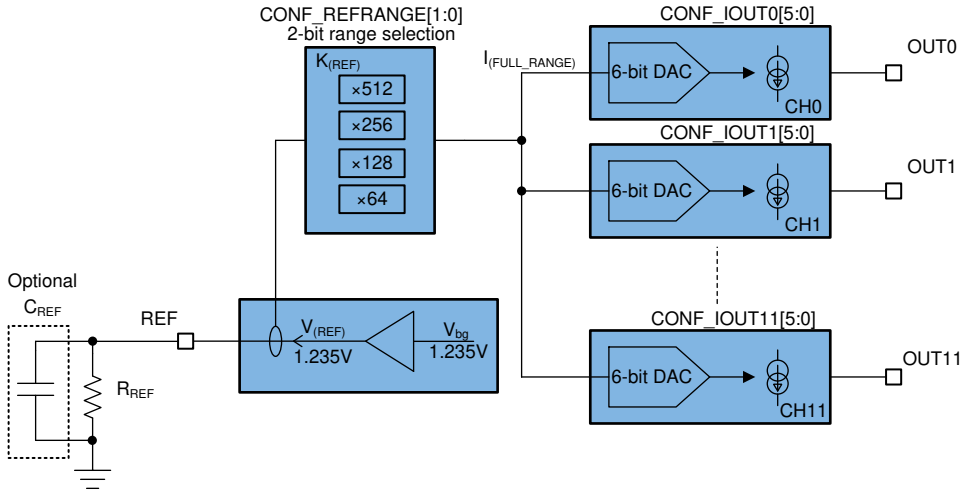


Figure 8-1. Output Current Setting

The internal current reference $I_{(FULL\_RANGE)}$ is generated based on the $I_{(REF)}$ multiplied by factor $K_{(REF)}$ to provide the full range current reference for each OUTx channel. The $K_{(REF)}$ is programmable by 2-bit register CONF_REFRANGE with 4 different options. The $I_{(FULL\_RANGE)}$ can be calculated with Equation 1.

$$I_{(FULL\_RANGE)} = \frac{V_{(REF)}}{R_{(REF)}} \times K_{(REF)} \quad (1)$$

where

- $V_{(REF)}$ = 1.235 V typically
- $K_{(REF)}$ = 64, 128, 256, or 512 (default)

The recommended resistor values of $R_{(REF)}$ and amplifier ratios of $K_{(REF)}$ are listed in Table 8-1.

Table 8-1. Reference Current Range Setting

CONF_REFRANGE	$K_{(REF)}$	FULL RANGE CURRENT (mA)		
		$R_{(REF)}$ = 8.45 kΩ	$R_{(REF)}$ = 12.7 kΩ	$R_{(REF)}$ = 31.6 kΩ
11b	512	75	50	20
10b	256	37.5	25	10
01b	128	18.75	12.5	5
00b	64	9.375	6.25	2.5

Place the $R_{(REF)}$ resistor as close as possible to the REF pin with an up to 2.2-nF ceramic capacitor in parallel to improve the noise immunity. The off-board $R_{(REF)}$ setup is not allowed due to the concern of instability reference current. TI recommends a 1-nF ceramic capacitor in parallel with $R_{(REF)}$.

8.3.2.2 64-Step Programmable High-Side Constant-Current Output

TPS929121-Q1 has 12 channels of high-side current sources. Each channel has its own enable configuration register CONF_ENCHx. Setting CONF_ENCHx to 1 enables the channel output; clearing the register to 0 disables the channel output. To completely turn off the channel current, user can clear channel enable bit CONF_ENCHx to 0. Upon power up, CONF_ENCHx is automatically reset to 0 to avoid unwanted blinking.

Each OUTx channel supports individual 64-step programmable current setting, also known as dot correction (DC). The DC feature can be used to set binning values for output LEDs or to calibrate the LEDs to achieve high brightness homogeneity based on external visual system to further save binning cost. The 6-bit register CONF_IOUTx sets the current independently, where x is the channel number from 0 to 11. The OUTx current can be calculated with Equation 2.

$$I_{(OUTx)} = \frac{(CONF\_IOUTx + 1)}{64} \times I_{(FULL\_RANGE)} \quad (2)$$

where

- CONF_IOUTx is programmable from 0 to 63.
- x is from 0 to 11 for different output channel.
- $I_{(FULL\_RANGE)}$ can be calculated with Equation 1.

8.3.3 PWM Dimming

TPS929121-Q1 integrates independent 12-bit PWM generators for each OUTx channel. The current output for each OUTx channel is turned on and off controlled by the integrated PWM generator. The average current of each OUTx can be adjusted by PWM duty cycle independently, therefore, to control the brightness for LEDs in each channel.

8.3.3.1 PWM Dimming Frequency

The frequency for PWM dimming is programmable by 4-bit register CONF_PWMFREQ with 16 options covering from 200 Hz to 20.8 kHz. Select the frequency for PWM dimming based on the minimum brightness requirement in application. TPS929121-Q1 supports down to 1-µs minimum pulse current for all 12-channel outputs.

8.3.3.2 PWM Generator

The 12-bit PWM generator constructs the cyclical PWM output based on a 12-bit digital binary input to control the output current ON and OFF. Basically the PWM generator counts 256 pulses at base high frequency for PWM output cycle period and counts number of pulses determined by MSB 8 bits of 12-bit binary input at the same frequency for PWM ON period. The LSB 4 bits of 12-bit binary input is used to set up the dithering to realize total 12-bit resolution. The base high frequency is generated by internal oscillator, which is 256 times of the frequency programmable by CONF_PWMFREQ. Figure 8-2 is the signal path diagram for PWM generator.

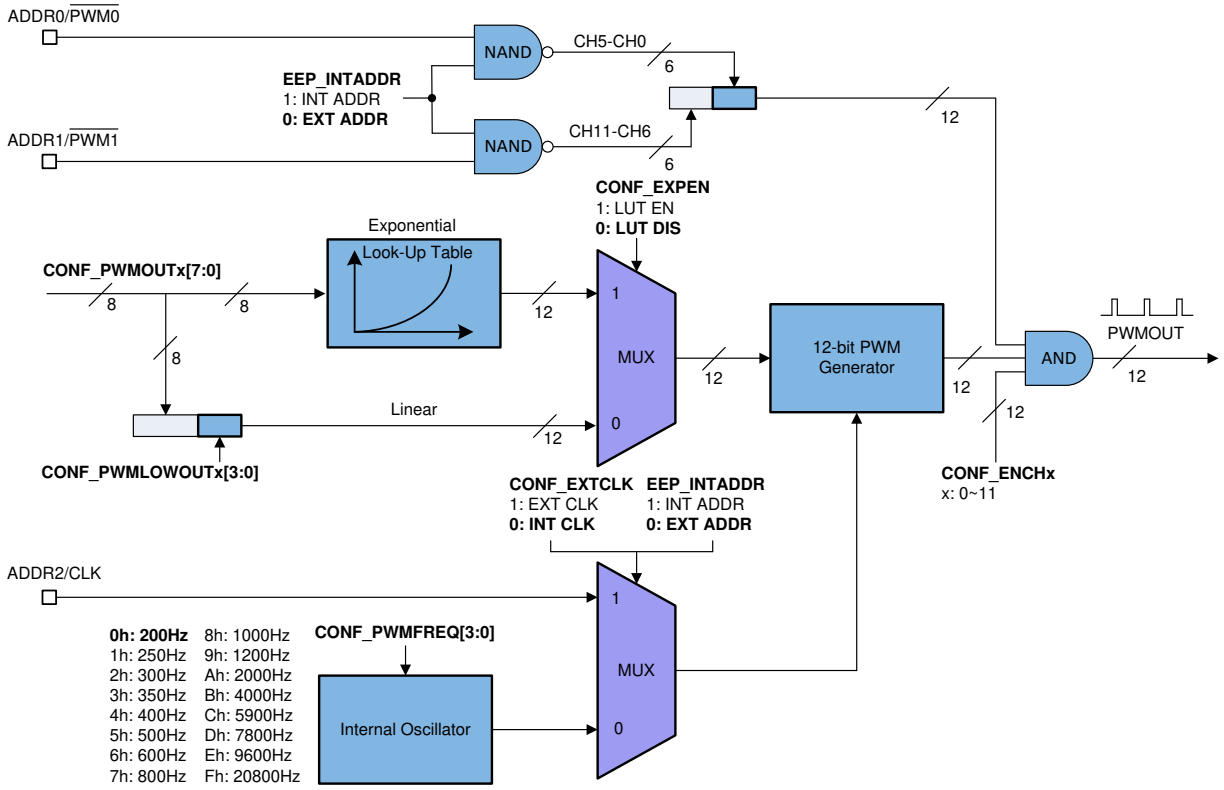


Figure 8-2. PWM Generator Path Diagram

8.3.3.3 Linear Brightness Control

When register CONF_EXPEN is set to 0, the MSB 8 bits of 12-bit binary input to PWM generator is directly copied from 8-bit register CONF_PWMOUTx, and the LSB 4 bits is directly copied from 4-bit register CONF_PWMLOWOUTx. The PWM output duty cycle can be calculated with Equation 3. Because the 4 LSB bits inputs are used to control the dithering, setting CONF_PWMLOWOUTx to Fh disables the dithering if it is not needed. The PWM output duty cycle is linearly controlled by the register CONF_PWMOUTx and CONFPWMLOWOUTx, which provides the linearly brightness control to each channel output.

$$D_{(OUTx)} = \frac{(16 \times CONF\_PWMOUTx + CONF\_PWMLOWOUTx + 1)}{4096} \times 100\% \quad (3)$$

where

- CONF_PWWOUTx is decimal number from 0 to 255.
- CONF_PWMLOWOUTx is decimal number from 0 to 15.
- x is from 0 to 11 for different output channel.

If using the dithering feature to realize the 12-bit dimming resolution, set the PWM frequency higher than 2 kHz through setting register CONF_PWMFREQ to avoid visible brightness flicker when the value of CONF_PWMLOWOUTx is less than Fh. Higher PWM frequency can also prevent the visible LED flash in video display due to the low beat frequency between digital camera shutter frequency and PWM frequency for LED dimming.

Because the 12-bit PWM duty cycles require 2 bytes of write operation to update the completed data, the output PWM duty cycle is not changed in between of the two bytes data transmission. TPS929121-Q1 only updates PWM duty cycle of any output when its high 8-bit CONF_PWMOUTx is written. When very fast brightness change is needed, for example, fade-in and fade-out effects, simultaneous PWM duty cycle change of all

channels is required. Setting CONF_SHAREPWM to 1 enables all channels using the PWM dutycycle setting of channel 0 to save communication latency.

8.3.3.4 Exponential Brightness Control

The TPS929121-Q1 can also generate PWM duty-cycle output following exponential curve. The integrated look-up table provides a one-to-one conversion from 8-bit register CONF_PWMOUTx to 12-bit binary code following exponential increment when register CONF_EXPEN is set to 1 as Figure 8-3 illustrated. When exponential control path is selected, the CONF_PWMLOWOUTx data is neglected. By using the exponential brightness control, LED brightness change by one LSB is invisible to human eyes especially at low brightness range.

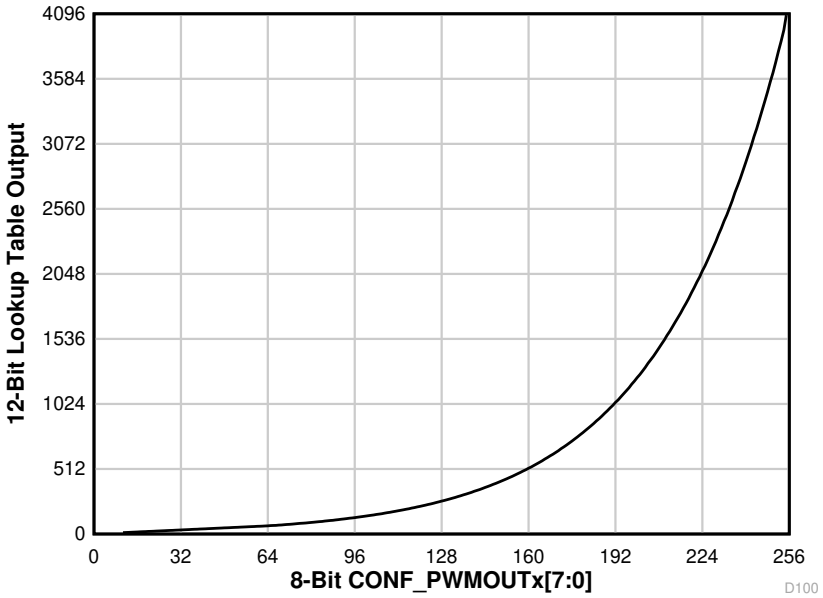


Figure 8-3. PWM Duty Cycle vs 8-bit Code for Exponential Dimming

CONF_EXPEN bit selects the dimming method between linear or exponential. Setting the bit CONF_EXPEN to 1 enables the look-up table for exponential dimming curve. In exponential PWM dimming mode, 8-bit register CONF_PWMOUTx is converted to 12-bit PWM dutycycle by look-up table automatically. Clear the bit CONF_EXPEN to 0 disables the look-up table. In this case, users must provide 12-bit PWM duty cycle. CONF_PWMOUTx stores the high 8-bit of 12-bit PWM duty-cycle information. CONF_PWMLOWOUTx stores the low 4-bit.

To avoid visible brightness flicker for exponential dimming, choose PWM frequency higher than 2 kHz through setting register CONF_PWMFREQ. Higher PWM frequency can also avoid the visible LED flash in video display due to the low beat frequency between digital camera shutter frequency and PWM frequency for LED dimming.

During power-up or in fail-safe state, the registers CONF_EXPEN, CONF_PWMOUTx, CONF_PWMFREQ are automatically reset to their default values stored in EEPROM register EEP_EXPEN, EEP_PWMOUTx, EEP_PWMFREQ. CONF_PWMLOWOUTx is reset to Fh as default value.

In fail-safe state, PWM generator only uses 8-bit EEPROM data from EEP_PWMOUTx to build PWM dutycycle output and ignores the low 4-bit. The PWM duty-cycle calculation is as shown in Equation 4.

$$D_{(OUTx)} = \frac{(EEP\_PWMOUTx+1)}{256} \times 100\% \quad (4)$$

where

- EEP_PWMOUTx is decimal number from 0 to 255.
- x is from 0 to 11 for different output channel.

8.3.3.5 External Clock Input for PWM Generator (CLK)

The TPS929121-Q1 has internal precision oscillator for PWM generators. In addition, the device also supports an external clock for the PWM generator source with ADDR2/CLK input considering the synchronization requirement.

Then external clock inputs through ADDR2/CLK pin is a multi-function pin not only for external clock input but also for device slave address selection. The device slave address stored in EEPROM must be enabled by burning EEP_INTADDR to 1 to release ADDR2/CLK pin for external clock input. In addition, register CONF_EXTCLK can be used to choose the PWM generator between external input or an internal oscillator. Writing CONF_EXTCLK to 1 enables the external clock source. The external clock frequency must be 256 times of desired PWM dimming frequency. The external clock source is only used in PWM generation. TI recommends that the external clock frequency be less than 1 MHz. The internal clock is recommended when high dimming frequency is required.

8.3.3.6 External PWM Input ($\overline{PWM0}$ and $\overline{PWM1}$)

The TPS929121-Q1 has two PWM inputs that can be used to directly control OUT0-11. The both ADDR1/ $\overline{PWM1}$ and ADDR0/ $\overline{PWM0}$ pins are multi-function pins for not only external PWM input signal but also device slave address selection pins. The register EEP_INTADDR must be written to 1 to release both twos for external PWM input. When the EEP_INTADDR is 1, the ADDR0/ $\overline{PWM0}$ is functional as external active low PWM control input for OUT0-5 and the ADDR1/ $\overline{PWM1}$ is functional as external active low PWM control input for OUT6-11, as shown in Figure 8-2. Setting the register CONF_PWMOUTx to 0xFF and the register CONF_PWMLOWOUTx to 0xF is recommended when external PWM input is used. In case external PWM is not used, ADDR0/ $\overline{PWM0}$ and ADDR1/ $\overline{PWM1}$ must be tied to GND when EEP_INTADDR is set to 1.

8.3.4 On-chip 8-bit Analog-to-Digital Converter (ADC)

The TPS929121-Q1 has integrated a successive-approximation-register (SAR) ADC for diagnostics. It routinely monitors supply voltage if the ADC is idle and stores SUPPLY conversion results into ADC_SUPPLY.

To manually read the voltage of an ADC channel as listed in Table 8-2, user must write the 5-bit register CONF_ADCCH to select channel. Once CONF_ADCCH register is written, the one time ADC conversion starts and clears FLAG_ADCDONE register. As long as the ADC conversion is completed, the ADC result is available in 8-bit register ADC_OUT and sets FLAG_ADCDONE to 1. Reading the ADC_OUT register also clears FLAG_ADCDONE, and the FLAG_ADCDONE is set to 0 after reading completion.

Because the TPS929121-Q1 supports PWM control for adjusting LED brightness, the voltage on OUT0 to OUT11 is like a pulse waveform. When the current output is enabled by setting CONF_ENCHx to 1, the ADC measures the voltage on assigned OUTx after the channel is turned on with $t_{(diag\_pulse)}$ delay time, which is programmable by 4-bit register CONF_ODPW. When the channel is disabled by setting CONF_ENCHx to 0, the ADC samples the voltage on assigned OUTx at off state.

The analog value can be calculated based on the read back binary code with Equation 5 and Table 8-2.

$$\text{Analog Value} = a + k \times (\text{ADC\_OUT}) \tag{5}$$

where

- ADC_OUT is decimal number from 0 to 255.

Table 8-2. ADC Channel

CHANNEL NO.	CONF_ADCCH	NAME	ADC CALCULATION PARAMETER (a)	ADC CALCULATION PARAMETER (k)	COMMENT
0	00h	REF	0.007 V	0.0101 V/LSB	Reference voltage
1	01h	SUPPLY	0.2878 V	0.1583 V/LSB	Supply voltage
2	02h	VLDO	0.0465 V	0.022 V/LSB	5-V LDO output voltage
3	03h	TEMPSNS	–304.7 °C	2.463°C/LSB	Internal temperature sensor
4	04h	IREF	0.7592 µA	0.7461 µA/LSB	Reference current
5	05h	MAXOUT	0.2878 V	0.1583 V/LSB	Maximum channel output voltage
6-15	06h - 0Fh	RESERVED	RESERVED	RESERVED	RESERVED
16	10h	OUT0	0.2878 V	0.1583 V/LSB	Output voltage channel 0
17	11h	OUT1			Output voltage channel 1
18	12h	OUT2			Output voltage channel 2
19	13h	OUT3			Output voltage channel 3
20	14h	OUT4			Output voltage channel 4
21	15h	OUT5			Output voltage channel 5
22	16h	OUT6			Output voltage channel 6
23	17h	OUT7			Output voltage channel 7
24	18h	OUT8			Output voltage channel 8
25	19h	OUT9			Output voltage channel 9
26	1Ah	OUT10			Output voltage channel 10
27	1Bh	OUT11			Output voltage channel 11
28	1Ch	RESERVED	RESERVED	RESERVED	RESERVED
29	1Dh	RESERVED	RESERVED	RESERVED	RESERVED
30	1Eh	RESERVED	RESERVED	RESERVED	RESERVED
31	1Fh	RESERVED	RESERVED	RESERVED	RESERVED

The TPS929121-Q1 also provides ADC auto-scan mode for single-led short-circuit diagnostics. The detail description for auto-scan mode can be found in *On-Demand Off-State Single-LED Short-Circuit (SS) Diagnostics*.

In ADC auto-scan mode, If MAXOUT channel is selected by writing 05h to CONF_ADCCH, the maximum voltage of OUT0 to OUT11 is recorded into ADC_OUT register. The maximum channel output voltage is available after at least one output PWM cycle is completed. Based on the measured maximum output voltage and supply voltage, microcontroller is able to regulate supply voltage from previous power stage to minimize the power consumption on the TPS929121-Q1. Basically microcontroller needs to program the output voltage of previous power stage to be just higher than the measured maximum channel output voltage plus the required dropout voltage $V_{(OUT\_drop)}$ of the TPS929121-Q1. In this way, the TPS929121-Q1 takes minimum power consumption, and overall power efficiency is optimized.

8.3.5 Diagnostic and Protection in Normal State

The TPS929121-Q1 has full-diagnostics coverage for supply voltage, current output, and junction temperature.

In normal state, the device detects all failures and reports the status out through the $\overline{ERR}$ or FLAG registers, without any actions taken by the device except UVLO and overtemperature protection. The master controller must handle all fault actions, for example, retry several times and shut down the outputs if the error still exists. The fault behavior in normal state can be found in Table 8-3.

8.3.5.1 Fault Masking

The TPS929121-Q1 provides fault masking capability using masking registers. The device is capable of masking faults by channels or by fault types. The fault masking does not disable diagnostics features but only prevents fault reporting to FLAG_OUT register, FLAG_ERR register, and $\overline{ERR}$ output.

To disable diagnostics on a single channel, setting CONF_DIAGENCHx registers to 0 disables diagnostics of channel x and thus no fault of this channel is reported to FLAG_OUT or FLAG_ERR registers, or to the $\overline{ERR}$ output.

CONF_MASKREF prevents the reference fault being reported to FLAG_ERR and $\overline{ERR}$ output.

CONF_MASKOPEN prevents the output open-circuit fault being reported to FLAG_OUT, FLAG_ERR and $\overline{ERR}$ output.

CONF_MASKSHORT prevents the output short-circuit fault being reported to FLAG_OUT, FLAG_ERR and $\overline{ERR}$ output.

CONF_MASKTSD prevents the overtemperature shutdown fault being reported to FLAG_ERR and $\overline{ERR}$ output.

CONF_MASKCRC prevents the CRC fault being reported to FLAG_ERR and $\overline{ERR}$ output.

8.3.5.2 Supply Undervoltage Lockout Diagnostics in Normal State

When SUPPLY or VLDO voltage drops below its UVLO threshold, the device enters POR state. Upon voltage recovery, the device automatically switches to INIT state with FLAG_POR and FLAG_ERR set to 1.

8.3.5.3 Low-Supply Warning Diagnostics in Normal State

The internal AD converter of TPS92910-Q1 continuously monitors the supply voltage and compares the results with internal threshold $V_{(ADCLOWSUPTH)}$ set by CONF_ADCLOWSUPTH as described in *Register Maps*. If the supply voltage is lower than threshold, the device pulls $\overline{ERR}$ pin down with one pulsed current sink for 50 µs to report the fault and set flag registers including FLAG_ADCLOWSUP to 1. The master controller can write register CLR_FAULT to 1 to reset this flag, and the CLR_FAULT bit automatically returns to 0. The internal ADC monitors supply voltage and converters to 8-bit binary code in every conversion cycle $T_{(CONV)}$ when it is in idle. After each AD conversion-cycle time on supply, the ADC_SUPPLY is automatically updated with the latest result.

The low-supply warning is also used to disable the LED open-circuit detection and single-LED short-circuit detection. When the voltage applied on SUPPLY pin is higher than the threshold $V_{(ADCLOWSUPTH)}$, the TPS929121-Q1 enables LED open-circuit and single-LED short-circuit diagnosis. When $V_{(SUPPLY)}$ is lower than the threshold $V_{(ADCLOWSUPTH)}$, the device disables LED-open-circuit detection and single-LED short-circuit diagnosis. Because when $V_{(SUPPLY)}$ drops below the maximum total LED forward voltage plus required $V_{(DROPOUT)}$ at required current, the TPS929121-Q1 is not able to deliver sufficient current output to pull the voltage of each output channel as close as possible to the $V_{(SUPPLY)}$. In this condition, the LED open-circuit fault or single-LED short-circuit fault might be detected and reported by mistake. Setting the low-supply warning threshold high enough can avoid the LED open-circuit and single LED short-circuit fault being detected when $V_{(SUPPLY)}$ drops to low. The $V_{(ADCLOWSUPTH)}$ is programmable from 5 V to 20 V.

8.3.5.4 Reference Diagnostics in Normal State

The TPS929121-Q1 integrates diagnostics for REF resistor open/short fault. If the current output from REF pin $I_{(REF)}$ is lower than $I_{(REF\_OPEN\_th)}$, the reference resistor open-circuit fault is reported. The reference resistor short-circuit fault is reported if the voltage of REF pin $V_{(REF)}$ is lower than $V_{(REF\_SHORT\_th)}$. The device pulls the

$\overline{ERR}$ pin down with constant current sink and set flag registers including FLAG_REF and FLAG_ERR to 1. The master controller must send CLR_FAULT to clear fault flag registers after fault removal.

In normal state, the device does not perform any actions automatically when reference resistor fault is detected. However, the output may not work properly and the output current may be operating at high current level. It is recommended for master controller to shut down the device outputs and report error to upper level control system such as body control module (BCM).

The TPS929121-Q1 monitors the reference current $I_{(REF)}$ set by external resistor $R_{(REF)}$. The $I_{(REF)}$ can be calculated with Equation 6.

$$I_{(REF)} = \frac{V_{(REF)}}{R_{(REF)}} \tag{6}$$

where

- $V_{(REF)}$ = 1.235 V typically

8.3.5.5 Pre-Thermal Warning and Overtemperature Protection in Normal State

The TPS929121-Q1 has pre-thermal warning at typical 135°C and overtemperature shutdown at typical 175°C.

When the junction temperature $T_{(J)}$ of TPS929121-Q1 rises above pre-thermal warning threshold, the device reports pre-thermal warning, pull $\overline{ERR}$ pin with pulsed current sink for 50 µs and sets the flag registers including FLAG_PRETSD to 1. The master controller must write 1 to CLR_FAULT register to clear FLAG_PRETSD.

When device junction temperature $T_{(J)}$ further rises above overtemperature protection threshold, the device shuts down all output drivers, pulls the $\overline{ERR}$ pin low with constant current sink, and sets the flag registers including FLAG_TSD and FLAG_ERR to 1. When junction temperature falls below $T_{(TSD)} - T_{(TSD\_HYS)}$, the device resumes all outputs and releases $\overline{ERR}$ pin pulldown. The FLAG_TSD still must be cleared by writing CLR_FAULT to 1.

If the $T_{(J)}$ rises too high above 180ºC typically, the TPS929121-Q1 turns off the internal linear regulator to shutdown all the analog and digital circuit. When the $T_{(J)}$ drops below $T_{(TSD)} - T_{(TSD\_HYS)}$, the TPS929121-Q1 restarts from POR state with all the registers cleared to default value.

When more accurate thermal measurement on LED unit is required, one current output channel can be sacrificed to provide current bias to external thermal resistor such as PTC or NTC. The voltage of external thermal resistor can be measured by integrated ADC to acquire the temperature information of thermal resistor located area. The master controller can determine actions based on the acquired temperature information to turn off or reduce current output.

8.3.5.6 Communication Loss Diagnostic in Normal State

The TPS929121-Q1 monitors the FlexWire interface for the communication with an internal watchdog timer. Any successful non-broadcast communication with correct CRC and address matching target device automatically resets the timer . If the watchdog timer overflows, device automatically switches to fail-safe state as indicated by external FS input. If FS = 0, the device switches to fail-safe state 0, If FS = 1, the device switches to fail-safe state 1.

The watchdog timer is programmable by 4-bit register CONF_WDTIMER. The TPS929121-Q1 can directly enter fail-safe states from normal mode by burning EEP_WDTIMER to 0xFh. Disabling the watchdog timer by setting CONF_WDTIMER to 0x0h prevents the device from getting into fail-safe state.

8.3.5.7 LED Open-Circuit Diagnostics in Normal State

The TPS929121-Q1 integrates LED open-circuit diagnostics to allow users to monitor LED status real time. The device monitors voltage difference between SUPPLY and OUTx to judge if there is any open-circuit failure. The SUPPLY voltage is also monitored by on-chip ADC with programmable threshold to determine if supply voltage is high enough for open-circuit diagnostics.

The open-circuit monitor is only enabled during PWM-ON state with programmable minimal pulse width greater than $T_{(ODPW)}$ + $T_{(OPEN\_deg)}$. The $T_{(ODPW)}$ is programmed by register CONF_ODPW. If PWM on-time is less than $T_{(ODPW)}$ + $T_{(OPEN\_deg)}$, the device does not report any open-circuit fault.

When the voltage difference $V_{(SUPPLY)}$ – $V_{(OUTx)}$ is below threshold $V_{(OPEN\_th\_rising)}$ with duration longer than $T_{(ODPW)}$ + $T_{(OPEN\_deg)}$, and the device supply voltage $V_{(SUPPLY)}$ is above the threshold $V_{(ADCLOWSUPTH)}$ set by register CONF_ADCLOWSUPTH, the TPS929121-Q1 pulls the $\overline{ERR}$ pin down with one pulsed current sink for 50 µs to report fault and set flag registers including FLAG_OPENCHx, FLAG_OUT and FLAG_ERR to 1. If the device supply voltage $V_{(SUPPLY)}$ is below the threshold $V_{(ADCLOWSUPTH)}$ set by register CONF_ADCLOWSUPTH, open-circuit fault is not detected nor reported.

Once the open-circuit failure is removed, the master controller must write 1 to CLR_FAULT to reset fault flags.

8.3.5.8 LED Short-Circuit Diagnostics in Normal State

The TPS929121-Q1 has internal analog comparators to monitor all channel outputs with respect to a fixed threshold. If the device has detected channel voltage below threshold, it sets FLAG_SHORTCHx accordingly. The FLAG_OUT and FLAG_ERR are set as well. Writing 1 to CLR_FAULT register is able to clear the fault flag registers.

The short-circuit detection is only enabled during PWM-ON state with programmable minimal pulse width of $T_{(ODPW)}$ + $T_{(SHORT\_deg)}$. The $T_{(ODPW)}$ is programmable by register CONF_ODPW. If PWM on-time is less than $T_{(ODPW)}$ + $T_{(SHORT\_deg)}$, the device can not report any short-circuit fault. When the voltage $V_{(OUTx)}$ is below threshold $V_{(SG\_th\_rising)}$ with duration longer than deglitch timer length of $T_{(ODPW)}$ + $T_{(SHORT\_deg)}$, the device pulls $\overline{ERR}$ pin down with pulsed current sink for 50 µs to report fault and set flag registers including FLAG_SHORTCHx, FLAG_OUT and FLAG_ERR. In normal state, the device does not take any actions in response the LED short-circuit fault and waits for the master controller to detect need for protection behavior. The fault is latched in flag registers. The master controller must write 1 to register CLR_FAULT to reset fault flags if the LED short-circuit fault is removed.

Possible user case:

1. Supply voltage dip below threshold, triggering false single led short-circuit fault
2. LED short to ground and recover
3. LED single LED short and recover
4. Dutycycle too short to detect
5. Extra capacitance caused false short-circuit

8.3.5.9 On-Demand Off-State Invisible Diagnostics

It is commonly required to ensure there is no fault on each LED load before lighting them up, especially for LED animation. Otherwise, the LED fault is detected in the middle of the admiration pattern, which results a random and uncertain failure animation pattern. The TPS929121-Q1 provides a solution to diagnose the LED open-circuit or LED short-circuit fault without lighting up the LEDs. With this feature, the master controller can initiate the on-demand invisible diagnostics before commencing the animation sequence. If one of the channel fails, the device is able to detect it immediately instead of only when the fault channel is turned on in traditional diagnostics mode. To initiate the on-demand invisible diagnostics, the master controller writes register CONF_INVDIAGSTART to 1. The register CONF_INVDIAGSTART returns to 0 automatically in the next clock cycle. Once the diagnostics started, the on-demand diagnostics ready flag FLAG_ODREADY is cleared to 0. Once the diagnostics finished, the FLAG_ODREADY is set to 1. If any channel has output failures, its on-demand diagnostic flag FLAG_ODDIAGCHx is set 1.

To ensure the invisibility of the diagnostics, the TPS929121-Q1 outputs only a small DC current in short period to each output channel and detects if there is any LED open-circuit or LED short-circuit failures. The output DC current $I_{(ODIOUT)}$ can be adjusted to a proper value by setting the DC current CONF_ODIOUT and ignoring the DC current setup by register CONF_IOUTx. The pulse-width $T_{(ODPW)}$ of output DC current can be programmable by CONF_ODPW and neglecting duty cycle configuration by register CONF_PWMOUTx. At the end of the current output pulse, if there is any LED open-circuit fault as *LED Open-Circuit Diagnostics in Normal State* described, the TPS929121-Q1 pulls the $\overline{ERR}$ pin down with one pulsed current sink for 50 µs to report fault and set flag registers including FLAG_OPENCHx, FLAG_OUT and FLAG_ERR to 1. If there is any LED short-circuit

fault as *LED Short-Circuit Diagnostics in Normal State* described, the TPS929121-Q1 pulls the $\overline{ERR}$ pin down with one pulsed current sink for 50 µs to report fault and set flag registers including FLAG_SHORTCHx, FLAG_OUT and FLAG_ERR to 1. The master controller must write 1 to CLR_FAULT register to clear fault flags after the fault removal is verified by another on-demand off-state invisible diagnostics. TI recommends turning off all output channels by set CONF_ENCHx to 0 before invisible diagnostics.

For invisible diagnostics mode, it is required to have a short-pulse and low output current to avoid lighting up LEDs. However, the diagnostics are strongly affected by large loading capacitance. If the invisible diagnostics pulse failed to charge output capacitance above short-circuit threshold, the device reports a false short-circuit failure. If pulse failed to charge output above open-circuit threshold at maximum supply voltage, the device does not report open-circuit fault correctly. Thus, the DC current and period of the detection pulse must be carefully selected based on the capacitance value at output in real application.

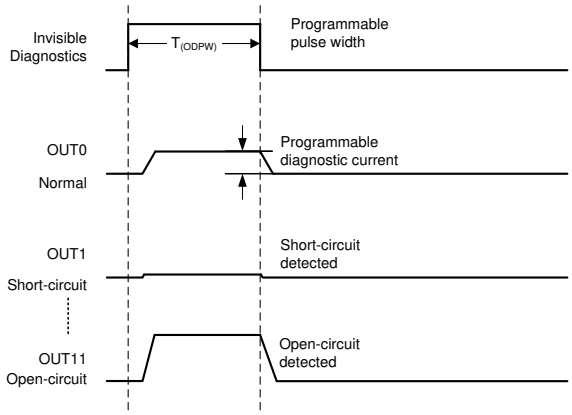


Figure 8-4. Programmable Invisible Diagnostics Timing Sequence

8.3.5.10 On-Demand Off-State Single-LED Short-Circuit (SS) Diagnostics

To provide single-LED short-circuit diagnostics, the TPS929121-Q1 uses internal ADC to compare the output channel voltage with respect to pre-set threshold $V_{(ADCSHORTTH)}$.

Setting the register CONF_SSSTART to 1 starts the diagnostics immediately. The CONF_SSSTART returns to 0 in the next clock cycle. Once the diagnostics starts, the on-demand diagnostics ready flag FLAG_ODREADY are cleared to 0. Once the diagnostics finished, the FLAG_ODREADY are set to 1.

In off-state single-LED short-circuit diagnostics, once the master controller initiates single-LED short-circuit diagnostics by setting the register CONF_SSSTART, the device sequentially turns on all outputs starting from OUT0 with DC current $I_{(ODIOUT)}$ programed by register CONF_ODIOUT and pulse width $T_{(ODPW)}$ programmable by CONF_ODPW. At the end of pulse, the device initiates an AD conversion. As long as the completion of ADC conversion, the result are compared with pre-set threshold $V_{(ADCSHORTTH)}$ and start the diagnostics for the next channel. After all channels have been checked, the TPS929121-Q1 also checks if the supply voltage is over $V_{(ADCLOWSUPTH)}$ to make sure the device is not in low-dropout conditions. If the supply voltage is truly lower than $V_{(ADCLOWSUPTH)}$, the single-LED short-circuit fault cannot be detected and reported. If the supply voltage is high enough, and any one channel output voltage is less than pre-set threshold $V_{(ADCSHORTTH)}$, the TPS92910-Q1 pulls the $\overline{ERR}$ pin down with pulsed current sink for 50 µs to report fault and set the flag register including FLAG_ODDIAGCHx, FLAG_OUT and FLAG_ERR to 1. The master controller must write 1 to CLR_FAULT register to clear the fault flags after fault removal is verified by another on-demand off-state single-LED short-circuit diagnostic.

The configurable DC current $I_{(ODIOUT)}$ and pulse width $T_{(ODPW)}$ can be used to minimize the optical impact during on-demand diagnostics. TI recommends using the normal current setting and short pulse-width to avoid visible pulse; however, the parasitic capacitance impact at each output must taken care of to leave enough charging time and avoid false alarm. Low DC current setting also reduces LED forward voltage, which also affects the integrity of the detection. Thus the threshold set by CONF_ADCSHORTTH must be selected carefully. Setting CONF_ODIOUT to 0xFh uses the channel current setting by register CONF_IOUTx as on-demand pulse current.

The V(ADCSHORTTH) can be calculated with Equation 7.

$$V_{(ADCSHORTTH)} = a + k \times (CONF\_ADCSHORTTH) \quad (7)$$

where

- a = 0.2878 V.
- k = 0.1583 V/LSB.
- CONF_ADCSHORTTH is decimal number from 0 to 255.

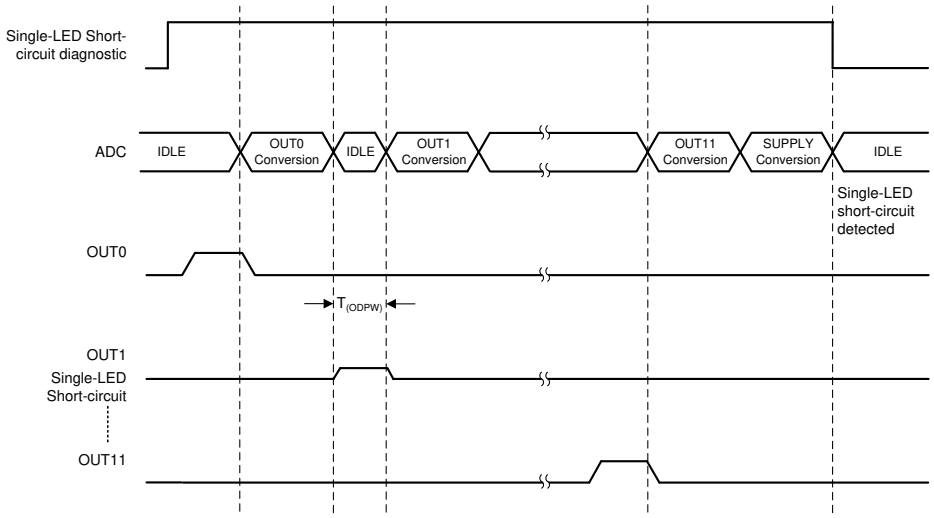


Figure 8-5. Single-LED Short-Circuit Off-state Timing Sequence

8.3.5.11 Automatic Single-LED Short-Circuit (AutoSS) Detection in Normal State

In order to check LED single-LED short-circuit issue during lighting up, the TPS929121-Q1 also provides automatically single-LED short-circuit (AutoSS) diagnostic. Setting the register CONF_AUTOSS to 1 enables the scanning of each current out channel at the beginning of every PWM cycle. The AutoSS detection takes two PWM cycles to complete scanning. The channel OUT0 to OUT5 are scanned in first cycle and the OUT6 to OUT11 are scanned in second cycle as depicted in Figure 8-6.

On PWM rising edge, the device waits for a programmable delay $T_{(ODPW)}$ programmable by CONF_ODPW to allow output voltage settle and start AD conversion. The minimal pulse width of PWM must be longer than programmable delay $T_{(ODPW)}$ plus 6 times AD conversion time $T_{(CONV)}$ to make sure 6 output channels can be scanned in one PWM cycle. The TPS929121-Q1 checks low-supply warning to avoid reporting the single-LED short-circuit fault by mistake in low-dropout mode. If the supply voltage is truly lower than $V_{(ADCLOWSUPTH)}$, the single-LED short-circuit fault cannot be detected and reported. If the supply voltage is high enough, and any one channel output voltage is less than pre-set threshold $V_{(ADCSHORTTH)}$, the TPS92910-Q1 pulls $\overline{ERR}$ pin down with pulsed current sink for 50 µs to report fault and set the flag register including FLAG_ODDIAGCHx, FLAG_OUT and FLAG_ERR to 1. The master controller must write 1 to CLR_FAULT register to clear the fault flags. The single-LED short circuit threshold $V_{(ADCSHORTTH)}$ is programmable by CONF_ADCSHORTTH. If any channel is disabled by CONF_ENCHx to 0, the AutoSS diagnostics skips the channel.

During the single-led short-circuit diagnostics, the ADC keeps the on-demand ADC conversion request pending until single-led short-circuit diagnostics finished. TI does not recommend using external PWM inputs when AutoSS is required to avoid false diagnostics.

When CONF_AUTOSS is set to 1, selecting MAXOUT by writing 05h to CONF_ADCCH automatically outputs the ADC conversion result to register ADC_OUT for the output channel with the highest voltage in all scanned channels. The master controller can adjust the previous power stage output voltage based on the voltage difference read back from register ADC_SUPPLY and ADC_OUT to minimize the voltage drop on the

TPS929121-Q1 as well as temperature rising if the output voltage of previous power stage is programmable by digital interface.

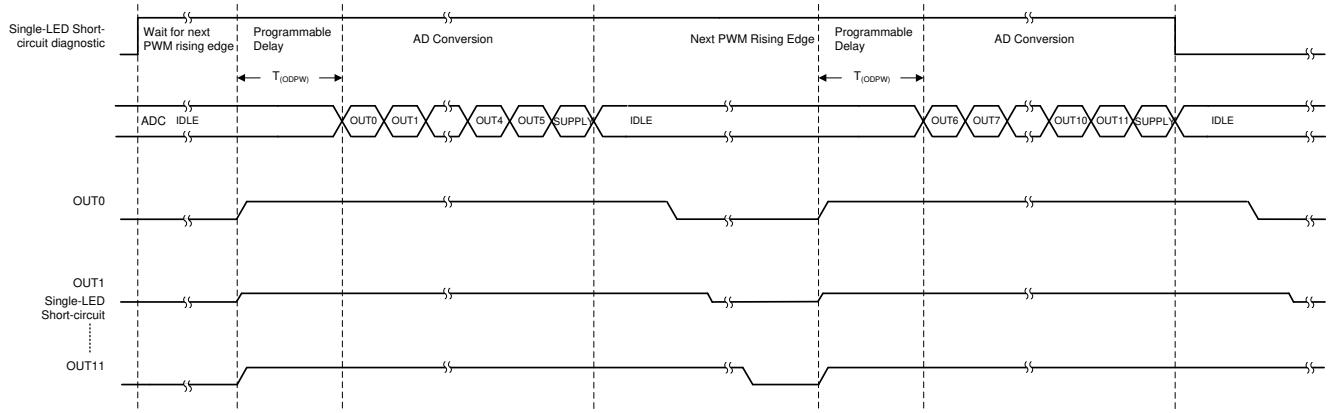


Figure 8-6. Single-LED Short-Circuit On-state Diagnostics Timing Sequence

8.3.5.12 EEPROM CRC Error in Normal State

The TPS929121-Q1 implements a EEPROM CRC check after loading the EEPROM code to configuration register in normal state. The calculated CRC result is sent to register CALC_EEPCRC and compared to the data in EEPROM register EEP_CRC, which stores the CRC code for all EEPROM registers. If the code in register CALC_EEPCRC is not matched to the code in register EEP_CRC, the TPS929121-Q1 pulls the $\overline{ERR}$ pin down with pulsed current sink for 50 µs to report the fault and set the registers including FLAG_EEPCRC and FLAG_ERR to 1. The master controller must write CLR_FAULT to 1 to clear the fault flags. The CRC code for all the EEPROM registers must be burnt into EEPROM register EEP_CRC in the end of production line. The CRC code algorithm for multiple bytes of binary data is based on the polynomial, $X^8 + X^5 + X^4 + 1$. The CRC code contain 8 bits binary code, and the initial value is FFh. As described in Figure 8-7, all bits code shift to MSB direction for 1 bit with three exclusive-OR calculation. A new CRC code for one byte input could be generated after repeating the 1-bit shift and three exclusive-OR calculation for 8 times. Based on this logic, the CRC code can be calculated for all the EEPROM register byte. When the EEPROM design for production is finalized, the corresponding CRC code based on the calculation must be burnt to EEPROM register EEP_CRC together with other EEPROM registers in the end of production line. If the DC current for each output channel needs to be calibrated in the end of production for different LED brightness bin, the CRC code for each production devices must be calculated independent and burnt during the calibration. The CRC algorithm must be implemented into the LED calibration system in the end of production line.

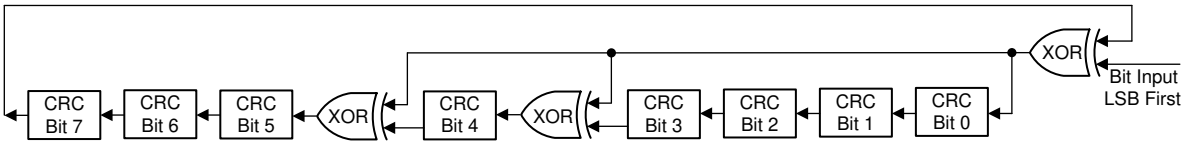


Figure 8-7. CRC Algorithm Diagram

Table 8-3. Diagnostics Table in Normal State

FAULT TYPE	DETECTION CRITERIA	CONDITIONS	FAULT ACTIONS	FAULT OUTPUT	$\overline{\text{ERR}}$ PIN	RECOVERY
Supply UVLO	$V_{(SUPPLY)} < V_{(POR\_falling)}$ or $V_{(LDO)} < V_{(LDO\_POR\_falling)}$		Device switch to POR state	FLAG_POR FLAG_ERR	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLR_POR
Low-supply warning	$V_{(SUPPLY)} < V_{(ADCLOWSUPTH)}$		Disable fault type *	FLAG_ADCLOWSUP FLAG_ERR	One pulse pulled down for 50µs	Clear fault flag with CLR_FAULT
Reference fault	$V_{(REF)} < V_{(REF\_SHORT\_th)}$ or $I_{(REF)} < I_{(REF\_OPEN\_th)}$		No action	FLAG_REF FLAG_ERR (Maskable)	Constant pulled down (maskable)	Clear fault flag with CLR_FAULT
Pre-thermal warning	$T_{(J)} > T_{(PRETSD)}$		No action	FLAG_PRETSD	One pulse pulled down for 50µs	Clear fault flag with CLR_FAULT
Overtemperature protection	$T_{(J)} > T_{(TSD)}$		Turn off all channels	FLAG_TSD FLAG_ERR (Maskable)	Constant pulled down (maskable)	Automatically recover upon junction temperature falling below threshold with hysteresis. Clear fault flag with CLR_FAULT
Communication loss fault	$T_{(WDTIMER)}$ overflows		Enter fail-safe states	FLAG_FS	No action	Set CLR_FS to 1 to set the device to normal state
LED open-circuit fault *	$V_{(SUPPLY)} - V_{(OUTx)} < V_{(OPEN\_th\_rising)}$ and $V_{(SUPPLY)} > V_{(ADCLOWSUPTH)}$	PWM pulse width greater than $T_{(ODPW)} + T_{(OPEN\_deg)}$ CONF_ENCHx = 1 CONF_DIAGENCHx = 1	No action	FLAG_OPENCHx FLAG_OUT (Maskable) FLAG_ERR (Maskable)	One pulse pulled down for 50 µs (maskable)	Clear fault flag with CLR_FAULT
LED short-circuit fault	$V_{(OUTx)} < V_{(SG\_th\_rising)}$	PWM pulse width greater than $T_{(ODPW)} + T_{(SHORT\_deg)}$ CONF_ENCHx = 1 CONF_DIAGENCHx = 1	No action	FLAG_SHORTCHx FLAG_OUT (Maskable) FLAG_ERR (Maskable)	One pulse pulled down for 50 µs (maskable)	Clear fault flag with CLR_FAULT
On-demand off-state invisible diagnostic	LED Open-circuit or LED Short-circuit fault	Pulse Width: $T_{(ODPW)}$ Current: $I_{(ODIOUT)}$ CONF_ENCHx = 0 CONF_DIAGENCHx = 1 CONF_INVDIAGSTART = 1	No action	FLAG_ODREADY FLAG_ODDIAGCHx FLAG_OUT FLAG_ERR	One pulse pulled down for 50 µs	Clear fault flag with CLR_FAULT
On-demand off-state single-LED Short-circuit *	$V_{(OUTx)} < V_{(ADCSHORTTH)}$ and $V_{(SUPPLY)} > V_{(ADCLOWSUPTH)}$	Pulse Width: $T_{(ODPW)}$ Current: $I_{(ODIOUT)}$ CONF_ENCHx = 0 CONF_DIAGENCHx = 1 CONF_SSSTART = 1	No action	FLAG_ODREADY FLAG_ODDIAGCHx FLAG_OUT FLAG_ERR	One pulse pulled down for 50 µs	Clear fault flag with CLR_FAULT
Auto single-LED short circuit *	$V_{(OUTx)} < V_{(ADCSHORTTH)}$ and $V_{(SUPPLY)} > V_{(ADCLOWSUPTH)}$	PWM pulse width greater than $T_{(ODPW)} + 6*T_{(CONV)}$ CONF_ENCHx = 1 CONF_DIAGENCHx = 1 CONF_AUTOSS = 1	No action	FLAG_ODDIAGCHx FLAG_OUT FLAG_ERR	One pulse pulled down for 50 µs	Clear fault flag with CLR_FAULT
EEPROM CRC error	CALC_EEPCRC is different EEP_CRC		No action	FLAG_EEPCRC FLAG_ERR (Maskable)	One pulse pulled down for 50 µs (maskable)	Clear fault flag with CLR_FAULT

8.3.6 Diagnostic and Protection in Fail-Safe States

In fail-safe state, the TPS929121-Q1 also detects all failures and reports the status out by $\overline{ERR}$ or FLAG registers. The summary of the fault detection criteria and the device behavior after fault detected is listed in Table 8-4. Basically the TPS929121-Q1 actively takes the action to turn off the failed output channels, retry on the failed channels, or restart the device to keep device operating without controlled by master. The EEPROM register EEP_OFAF can be used to set the fault behavior for LED short-circuit and LED open-circuit. The one-fails-all-fail behavior is selected when the register EEP_OFAF is burnt to 1; otherwise the one-fails-others-on behavior is chosen. The TPS929121-Q1 turns off all output channels when any one type of LED fault is detected on any one of output channels for one-fails-all-fail behavior. On the other hand, the TPS929121-Q1 only turns off the failed channel and keep all other normal channels on.

In fail-safe state, the fault flag registers of TPS929121-Q1 still can be accessed through FlexWire interface for master controller to identify the fault.

8.3.6.1 Fault Masking

The TPS929121-Q1 provides fault masking capability by masking registers. The device is capable of masking faults by channels or by fault types. The fault masking doe not disable diagnostics features but only prevents fault reporting to FLAG_OUT register, FLAG_ERR register, and $\overline{ERR}$ output.

To disable diagnostics on a single channel, setting CONF_DIAGENCHx registers to 0 disables diagnostics of channel x and thus no fault of this channel is reported to FLAG_OUT, FLAG_ERR registers, and $\overline{ERR}$ output.

CONF_MASKREF prevents the reference fault being reported to FLAG_ERR and $\overline{ERR}$ output.

CONF_MASKOPEN prevents the output open-circuit fault being reported to FLAG_OUT, FLAG_ERR and $\overline{ERR}$ output.

CONF_MASKSHORT prevents the output short-circuit fault being reported to FLAG_OUT, FLAG_ERR and $\overline{ERR}$ output.

CONF_MASKTSD prevents the overtemperature shutdown fault being reported to FLAG_ERR and $\overline{ERR}$ output.

CONF_MASKCRC prevents the CRC fault being reported to FLAG_ERR and $\overline{ERR}$ output.

8.3.6.2 Supply UVLO Diagnostics in Fail-Safe States

When SUPPLY or VLDO voltage drops below its UVLO threshold, the device enter into POR state. Upon voltage recovery, the device automatically switches to INIT state with FLAG_POR and FLAG_ERR set to 1.

8.3.6.3 Low-supply Warning Diagnostics in Fail-Safe states

The internal ADC of TPS92910-Q1 continuously monitors supply voltage and compares the results with internal threshold $V_{(ADCLOWSUPTH)}$ set by CONF_ADCLOWSUPTH as described in *Register Maps*. If the supply voltage is lower than threshold, the device sets flag registers including FLAG_ADCLOWSUP and FLAG_ERR to 1. Master controller can write register CLR_FAULT to 1 to reset this flag, and the CLR_FAULT bit automatically returns to 0. The internal ADC monitors supply voltage and converters to 8-bit binary code in every conversion cycle $T_{(CONV)}$ when it is in idle.

After each AD conversion cycle time on supply, the ADC_SUPPLY is automatically updated with the latest result.

8.3.6.4 Reference Diagnostics at Fail-Safe States

The TPS929121-Q1 integrates diagnostics for REF resistor open/short fault. If the current output from REF pin $I_{(REF)}$ is lower than $I_{(REF\_OPEN\_th)}$, the reference resistor open-circuit fault is reported. Or the reference resistor short-circuit fault is reported if the voltage of REF pin $V_{(REF)}$ is lower than $V_{(REF\_SHORT\_th)}$. The device pulls $\overline{ERR}$ pin down with constant current sink and set flag registers including FLAG_REF and FLAG_ERR to 1.

In fail-safe state, the device turns off all output channels if reference fault is detected. The device automatically recovers and turns on all used channel after fault removal. The master controller need send CLR_FAULT to clear the flag register after fault removal.

The TPS929121-Q1 monitors the reference current $I_{(REF)}$ set by external resistor $R_{(REF)}$. The $I_{(REF)}$ can be calculated with Equation 6.

8.3.6.5 Overtemperature Protection in Fail-Safe State

When the junction temperature $T_{(J)}$ of TPS929121-Q1 rises above overtemperature protection threshold, the device shuts down all output drivers, pulls $\overline{ERR}$ pin low with constant current sink, and sets flag register including FLAG_TSD and FLAG_ERR to 1. When junction temperature falls below $T_{(TSD)}$ - $T_{(TSD\_HYS)}$, the device resumes all outputs and releases $\overline{ERR}$ pin pulldown. The FLAG_TSD still can be cleared by writing CLR_FAULT to 1.

If the $T_{(J)}$ rises too high above 180ºC typically, the TPS929121-Q1 turns off the internal linear regulator to shutdown all the analog and digital circuit. When the $T_{(J)}$ drops below $T_{(TSD)}$ - $T_{(TSD\_HYS)}$, the TPS929121-Q1 restarts from POR state with all the registers cleared to default value.

8.3.6.6 LED Open-circuit Diagnostics in Fail-Safe State

The TPS929121-Q1 integrates LED open-circuit diagnostics to allow users to monitor LED status in real time. The device monitors voltage difference between SUPPLY and OUTx to detect if there is any open-circuit failure. The SUPPLY voltage is also monitored by on-chip ADC with programmable threshold to detect if supply voltage is high enough for open-circuit diagnostics.

The open-circuit monitor is only enabled during PWM-ON state with minimal pulse width greater than $T_{(ODPW)}$ + $T_{(OPEN\_deg)}$. If PWM on-time is less than $T_{(ODPW)}$ + $T_{(OPEN\_deg)}$, the device does not report any open-circuit fault. $T_{(ODPW)}$ is programmable by register CONF_ODPW.

When the voltage difference $V_{(SUPPLY)}$ – $V_{(OUTx)}$ is below threshold $V_{(OPEN\_th\_rising)}$ with duration longer than $T_{(ODPW)}$ + $T_{(OPEN\_deg)}$ and the device supply voltage $V_{(SUPPLY)}$ is above the threshold $V_{(ADCLOWSUPTH)}$ set by register CONF_ADCLOWSUPTH, the TPS929121-Q1 turns off the current output on the open-circuit channel, pulls $\overline{ERR}$ pin down with constant current sink to report fault and sets the flag registers including FLAG_OPENCHx, FLAG_OUT and FLAG_ERR to 1. If the device supply voltage $V_{(SUPPLY)}$ is below the threshold $V_{(ADCLOWSUPTH)}$ set by register CONF_ADCLOWSUPTH, open-circuit fault are not detected and reported. If any channel is disabled by CONF_ENCHx to 0, the LED open-circuit diagnostics skip the channel. If one-fails-all-fail protection is enabled by setting EEPROM register EEP_OFAF to 1, all the used output channels are turned off even though the LED open-circuit is only detected on one channel. If one-fails-all-fail protection is disabled by setting EEPROM register EEP_OFAF to 0, only failed channels are turned off.

In fail-safe states, the TPS929121-Q1 retries the failed channel with low-current retry pulses every 10 ms. The pulse width $T_{(ODPW)}$ is programmable by CONF_ODPW, and the retry current is set by CONF_ODIOUT. If the retry is succeed, the device automatically releases the $\overline{ERR}$ pin and clear the flag registers. If the CONF_DIAGENCHx is set to 0, the open-circuit fault is ignored.

Possible user case:

1. Supply voltage dip below threshold, triggering false open-circuit fault
2. Real LED open-circuit and recover
3. Extra capacitance caused false open-circuit
4. Dutycycle too short to detect
5. Sequential Turn Error Detection. Only on-time diagnostics only
6. Off-state diagnostics?

8.3.6.7 LED Short-circuit Diagnostics in Fail-Safe State

The TPS929121-Q1 has internal analog comparators to monitor all channel outputs with respect to a fixed threshold. If the device has detected channel voltage below threshold, it sets FLAG_SHORTCHx accordingly. The FLAG_OUT and FLAG_ERR are set as well.

The short-circuit detection is only enabled during PWM-ON state with programmable minimal pulse width of $T_{(ODPW)}$ + $T_{(SHORT\_deg)}$. The $T_{(ODPW)}$ is programmable by register CONF_ODPW. If PWM on-time is less than $T_{(ODPW)}$ + $T_{(SHORT\_deg)}$, the device cannot report any short-circuit fault. When the voltage $V_{(OUTx)}$ is below threshold $V_{(SG\_th\_rising)}$ with duration longer than deglitch timer length of $T_{(ODPW)}$ + $T_{(SHORT\_deg)}$, the device turns off the current output on the LED short-circuit channels, pulls the $\overline{ERR}$ pin down with constant current sink to

report fault, and sets flag registers including FLAG_SHORTCHx, FLAG_OUT and FLAG_ERR. If any channel is disabled by CONF_ENCHx to 0, the LED short-circuit diagnostics skip the channel. If one-fails-all-fail protection is enabled by setting EEPROM register EEP_OFAF to 1, all the used output channels are turned off even though the LED short-circuit is only detected on one channel. If one-fails-all-fail protection is disabled by setting EEPROM register EEP_OFAF to 0, only failed channels are turned off.

In fail-safe states, the TPS929121-Q1 retries the failed channel with a low-current retry pulses in every 10 ms. The pulse width $T_{(ODPW)}$ is programmable by CONF_ODPW, and the retry current is set by CONF_ODIOUT. If the retry is succeed, the device turns on the channel current, automatically release the $\overline{ERR}$ pin and clears the flag registers. If the CONF_DIAGENCHx is set to 0, the short-circuit fault is ignored.

Possible user case:

1. Supply voltage dip below threshold, triggering false single led short-circuit fault
2. LED short to ground and recover
3. LED single LED short and recover
4. Dutycycle too short to detect
5. Extra capacitance caused false short-circuit

8.3.6.8 EEPROM CRC Error in Fail-safe State

The TPS929121-Q1 automatically reloads all EEPROM code into the corresponding configuration registers every time after entering the fail-safe state. The TPS929121-Q1 implements a EEPROM CRC check after loading the EEPROM code to configuration register in fail-safe state. The calculated CRC result are sent to register CALC_EEPCRC and compared to the data in EEPROM register EEP_CRC, which stores the CRC code for all EEPROM registers. If the code in register CALC_EEPCRC is not matched to the code in register EEP_CRC, the TPS929121-Q1 turns off all channels output, pulls the $\overline{ERR}$ pin down with constant current sink to report the fault, and sets the registers including FLAG_EEPCRC and FLAG_ERR to 1. The CRC code for all the EEPROM registers must be burnt into EEPROM register EEP_CRC in the end of production line. The CRC code algorithm is described in *EEPROM CRC Error in Normal State*.

Table 8-4. Diagnostics Table in Fail-Safe State

FAULT TYPE	DETECTION CRITERIA	CONDITIONS	FAULT ACTIONS	FAULT OUTPUT	$\overline{ERR}$ PIN	RECOVERY
Supply UVLO	$V_{(SUPPLY)} < V_{(POR\_falling)}$ or $V_{(LDO)} < V_{(LDO\_POR\_falling)}$		Device switch to POR state	FLAG_POR FLAG_ERR Automatically clears flag register and recover upon fault removal.	Constant pulled down	Device switch to INIT state when all voltage rails are good. Clear fault flag with CLR_POR.
Low-supply warning	$V_{(SUPPLY)} < V_{(ADCLOWSUPTH)}$		Disable fault type *	FLAG_ADCLOWSUP FLAG_ERR	No action	Automatically clear fault flags when supply voltage is above threshold.
Reference fault	$V_{(REF)} < V_{(REF\_SHORT\_th)}$ or $I_{(REF)} < I_{(REF\_OPEN\_th)}$		Turn off all channels	FLAG_REF FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover, release $\overline{ERR}$ and clear fault flags upon fault removal.
Overtemperature protection	$T_{(J)} > T_{(TSD)}$		Turn off all channels	FLAG_TSD FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover, release $\overline{ERR}$ and clear fault flags upon fault removal.
LED open-circuit fault *	$V_{(SUPPLY)} - V_{(OUTx)} < V_{(OPEN\_th\_rising)}$ and $V_{(SUPPLY)} > V_{(ADCLOWSUPTH)}$	PWM pulse width greater than $T_{(ODPW)} + T_{(OPEN\_deg)}$ CONF_ENCHx = 1 CONF_DIAGENCHx = 1	Turn off the failed channels and retries every 10 ms	FLAG_OPENCHx FLAG_OUT (maskable) FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover, release $\overline{ERR}$ and clear fault flags upon fault removal.
LED short-circuit fault	$V_{(OUTx)} < V_{(SG\_th\_rising)}$	PWM pulse width greater than $T_{(ODPW)} + T_{(SHORT\_deg)}$ CONF_ENCHx = 1 CONF_DIAGENCHx = 1	Turn off the failed channels and retries every 10 ms	FLAG_SHORTCHx FLAG_ERR (maskable) FLAG_OUT (maskable)	Constant pulled down (maskable)	Automatically recover, release $\overline{ERR}$ and clear fault flags upon fault removal.
EEPROM CRC error	CALC_EEPCRC is different EEP_CRC		Turn off all channels	FLAG_EEPCRC FLAG_ERR (maskable)	Constant pulled down (maskable)	Automatically recover, release $\overline{ERR}$ and clear fault flags upon fault removal.

8.4 Device Functional Modes

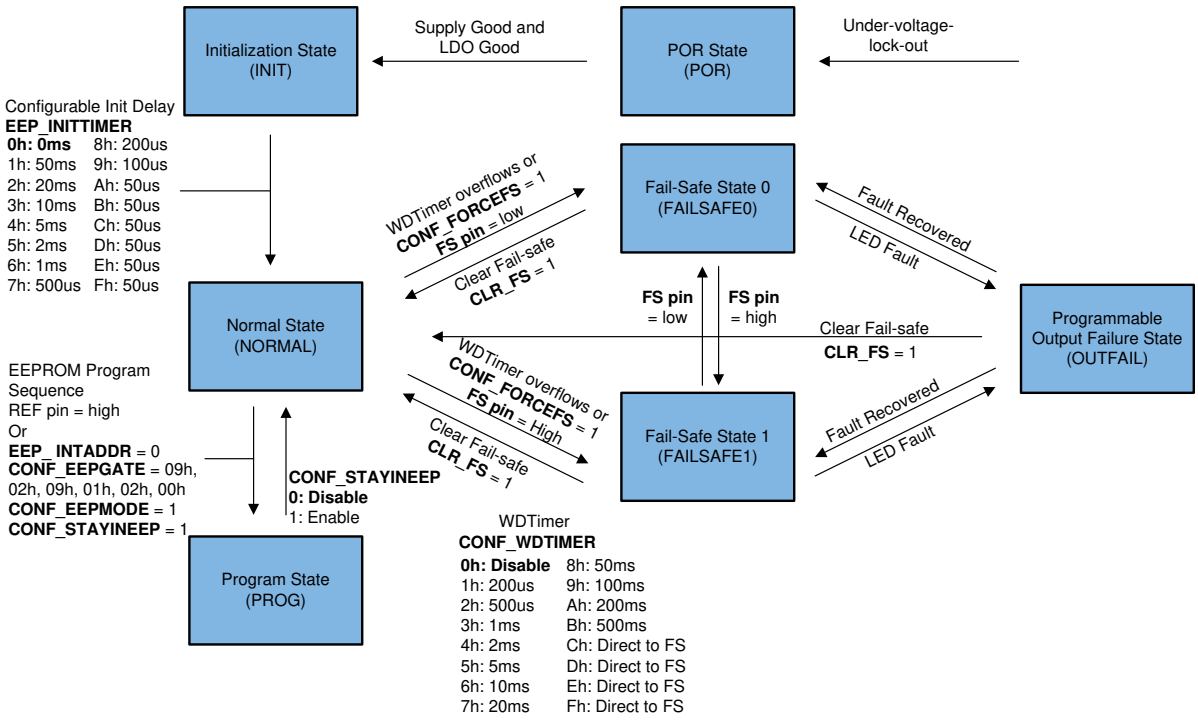


Figure 8-8. Device Functional Mode Statemachine

8.4.1 POR State

Upon power up, the TPS929121-Q1 enters power-on-reset (POR) state. In this mode, registers are cleared, outputs are disabled, and the device cannot be accessed through the FlexWire interface.

Once both the supply and LDO are above their UVLO threshold, the device switches to Initialization state (INIT). If any of the supply fails below UVLO threshold in other states, the device immediately switches to POR state.

8.4.2 Initialization State

The initialization state is designed to allow master controller to have enough time to power up before the device automatically gets into fail-safe states. INIT mode has a configurable delay programmed by 4-bit E^2PROM register EEP_INITTIMER. Once the delay counter is reached, the device changes to normal state. In INIT state, the communication between master controller and the TPS929121-Q1 is enabled through FlexWIre interface. If the master controller sets CLR_POR to 1, the device immediately switches to normal state. In Initialization state, device automatically load register map default values, which can be programmed by E^2PROM. The channel enable register CONF_ENCHx are all 0 to avoid unwanted blinking.

8.4.3 Normal State

Once the TPS929121-Q1 is in normal state, the device operates under master control for LED animation and diagnostics using a FlexWire interface. The TPS929121-Q1 integrates a watchdog timer to monitor the communication on FlexWire. The watchdog timer is programable by a 4-bit register CONF_WDTIMER for 13 options. The timer in TPS929121-Q1 starts to count when there is no instruction received from master controller. The TPS929121-Q1 enters fail-safe states when the timer overflows. The device can be also forced into fail-safe states anytime in normal state by setting CONF_FORCEFS to 1.

8.4.4 Fail-Safe States

When the TPS929121-Q1 is entering fail-safe states from normal state, all the registers are set to default value or reloaded from EEPROM. The TPS929121-Q1 provides two sets of channel enable configuration in fail-safe states, programmable by EEP_FS0CHx and EEP_FS1CHx. In fail-safe state 0, the channel-enable register

CONF_ENCHx automatically loads code from EEP_FS0CHx; in fail-safe state 1, the channel-enable register CONF_ENCHx automatically loads code from EEP_FS1CHx. The fail-safe state is selective by FS pin voltage. The fail-safe state 1 is selected by pulling the FS pin to high, otherwise the fail-safe state 0 is selected. The flag register FLAG_EXTFS shows the FS input level at real-time. If FS pin input voltage is logic high, the FLAG_EXTFS is set to 1.The device does not reset diagnostics status or FLAG registers when switching between two fail-safe states.

Setting CONF_FORCEFS to 1 forces the device into fail-safe state from normal state. The TPS929121-Q1 can quit from fail-safe state to normal state by setting CLR_FS to 1 with FLAG registers cleared. The CONF_CLRLOCK register is automatically set to 1 when the TPS929121-Q1 goes into the fail-safe state to prevent the modification of configuration register by mistake. To get out of fail-safe states to normal state, CONF_CLRLOCK register must be cleared to 0 before setting CLR_FS to 1.

The fail-safe states also allows the TPS929121-Q1 operating as standalone device without master controlling in the system. The $\overline{\text{ERR}}$ pin is used as fault indicator to achieve one-fails-all-fail or one-fails-others-on diagnostics requirement. When low quiescent current in fault mode is required, all channels must be set as one-fails-all-fail. In this case, if fault is triggered, the device goes into low current fault mode and disables FlexWire interface to save quiescent current.

8.4.5 Program State

The TPS929121-Q1 can enter EEPROM program state by pulling up the REF pin voltage to 5 V or writing multiple configuration registers to enter EEPROM program state. The TPS929121-Q1 ignores diagnostics and fault input except supply or LDO UVLO and overtemperature protection in EEPROM program state. Refer to *EEPROM Programming* for details of getting into program state.

8.4.6 Programmable Output Failure State

The TPS929121-Q1 has a unique programmable output failure state. If there is a failure detected in fail-safe states, the TPS929121-Q1 automatically goes into OUTFAIL state. The EEPROM register EEP_OFAF determines whether the result behavior of output failure is one-fails-all-fail or one-fails-others-on.

As different channels may serve different functions, diagnostics requirements are different as well. CONF_DIAGENCHx is able to control diagnostics for every channel. For channels that requires one-fails-all-fail with $\overline{\text{ERR}}$ pin as the fault bus, the fault enable register CONF_DIAGENCHx must be set to 1 and EEP_OFAF to 1. For channels that requires one-fails-others-on in fail-safe states, the fault enable register CONF_DIAGENCHx must be set 1 and EEP_OFAF to 0. In case the channel diagnostics is not needed, set the CONF_DIAGENCHx to 0. Details as described in Table 8-5. The register CONF_DIAGENCHx automatically loads the code from EEPROM register EEP_DIAGENCHx as well as other configuration registers every time entering fail-safe state.

8.4.7 $\overline{\text{ERR}}$ Output

The $\overline{\text{ERR}}$ pin is a programmable fault indicator pin. It can be used as an interrupt output to master controller in case there is any fault in normal mode. In fail-safe states, the $\overline{\text{ERR}}$ pin can be used as an output to other $\overline{\text{ERR}}$ pin of other TPS929121-Q1 to realize one-fails-all-fail at system level. The $\overline{\text{ERR}}$ pin is a open-drain output with current limit up to $I_{(pd\_\overline{ERR})}$. TI recommends a <10-kΩ external pullup resistor from the $\overline{\text{ERR}}$ pin to the same IO voltage of master controller.

In normal state, when a fault is triggered, depending on the fault type, the $\overline{\text{ERR}}$ pin is either pulled down constantly or pulled down for a single pulse. Once an $\overline{\text{ERR}}$ output is triggered, the master controller must take action to deal with the failure and reset the fault flag. Otherwise the $\overline{\text{ERR}}$ pin cannot be pulled down again. For non-critical faults, the TPS929121-Q1 pulls down the $\overline{\text{ERR}}$ pin with a duration of 50 µs and release; for critical faults, device constantly pulls down $\overline{\text{ERR}}$ as described in Table 8-3. In normal state, basically the TPS929121-Q1 only reports the faults to the master controller for most of the failure and takes no actions except supply or LDO UVLO and overtemperature. The master controller determine what action to take according to the type of the failure.

The TPS929121-Q1 provides a forced-error feature to validate the error feedback-loop integrity in normal state. In normal state, if microcontroller sets CONF_FORCEERR to 1, the FLAG_ERR is set 1 and pulls down $\overline{\text{ERR}}$ output with a pulse of 50 µs accordingly. The CONF_FORCEERR automatically returns to 0.

In fail-safe states, the $\overline{ERR}$ pin is used as fault bus. When there is any output failure reported, the $\overline{ERR}$ is pulled down by internal current sink $I_{(pd\_\overline{ERR})}$. The TPS929121-Q1 monitors the voltage of the $\overline{ERR}$ pin. If the one-fails-all-fail diagnostics is enabled by setting register EEP_OFAF to 1, all current output channels are turned off, as well as diagnostics, when the $\overline{ERR}$ pin voltage is low. If register EEP_OFAF is 0, the device only turns off the failed channel with alive channels diagnostics enabled.

Table 8-5. One-Fails-All-Fail Feature in Fail-safe States

	EEP_OFAF = 1	EEP_OFAF = 0
$\overline{ERR}$ = 0	All OUT channel OFF if any one OUT failure is detected	Only detected failed OUT OFF
$\overline{ERR}$ = 1	Only failed OUT OFF	Only detected failed OUT OFF

If multiple TPS929121-Q1 devices are used in one application, tying the $\overline{ERR}$ pins together achieves the one-fails-all-fail behavior in fail-safe states without master controlling. Any one of TPS929121-Q1 reports fault by pulling the $\overline{ERR}$ pin to low, and the low voltage on $\overline{ERR}$ bus is detected by other TPS929121-Q1 as Figure 8-9 illustrated. If the register EEP_OFAF is set to 1 for all TPS929121-Q1 devices having the $\overline{ERR}$ pins tied together, all TPS929121-Q1 devices turn off current for all output channels.

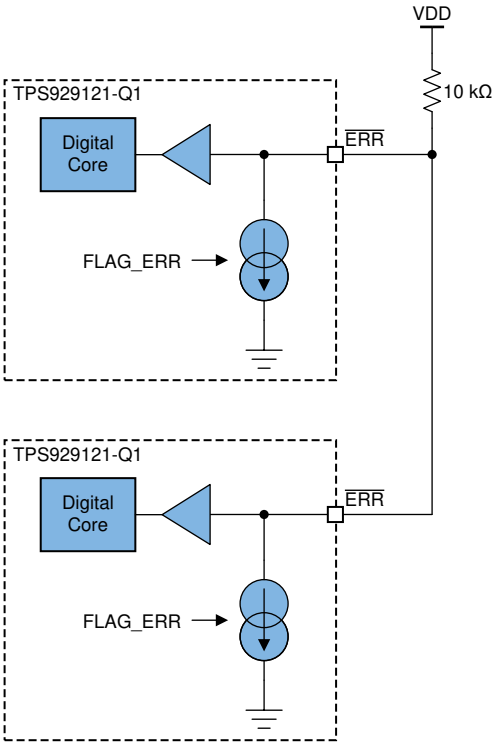


Figure 8-9. $\overline{ERR}$ Internal Block Diagram

8.4.8 Register Default Data

The TPS929121-Q1 has two types of configuration registers. The registers address between 00h to 0Bh, 20h to 2Bh and 50h to 5Bh, have the almost same set of EEPROM mirror registers from 80h to 8Bh, A0h to ABh and C0h to CBh. These registers load the code from the corresponding EEPROM registers by the following operations:

- The TPS929121-Q1 starts from POR.
- The TPS929121-Q1 restarts from supply or LDO UVLO triggered.
- The TPS929121-Q1 enters fail-safe mode by watchdog timer timeout.
- Writing CONF_FORCEFS to 1 to force TPS929121-Q1 into fail-safe mode.
- Writing CLR_REG to 1 to reset all registers to default code.

- Writing CONF_EEPREADBACK to 1 to reload all registers from corresponding EEPROM.

For other configuration registers without corresponding EEPROM are cleared to default values by following operations:

- The TPS929121-Q1 starts from POR.
- The TPS929121-Q1 restarts from supply or LDO UVLO triggered.
- The TPS929121-Q1 enters fail-safe mode by watchdog-timer timeout.
- Writing CONF_FORCEFS to 1 to force TPS929121-Q1 into fail-safe mode.
- Writing CLR_REG to 1 to reset all registers to default code.

8.5 Programming

8.5.1 FlexWire Protocol

8.5.1.1 Protocol Overview

The FlexWire is a UART-based protocol supported by most microcontroller units (MCU), Each frame contains multiple bytes started with a synchronization byte. The synchronization byte allow LED drivers to synchronize with master MCU frequency, therefore saving the extra cost on high precision oscillators that are commonly used in UART / CAN interfaces. Each byte has 1 start bit, 8 data bits, 1 stop bit, no parity check. The LSB data follows the start bit as Figure 8-10 described. The FlexWire supports adaptive communication frequency ranging from 10kHz to 1MHz. The protocol supports master-slave with star-connected topology.

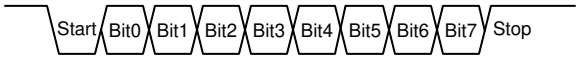


Figure 8-10. One Byte Data Structure

The FlexWire is designed robust for automotive environment. Once the slave device receives a communication frame, it firstly verifies its CRC byte. Only when CRC is verified, the slave device sends out response frame and clears the watchdog timer. In addition, if one communication frame is interrupted in the middle without any bus toggling for a period longer than timeout timer $T_{(FLTIMEOUT)}$, the TPS929121-Q1 resets the communication and wait for next communication starting from synchronization byte. It is also required for idle period between bytes within $T_{(FLTIMEOUT)}$. The timeout timer $T_{(FLTIMEOUT)}$ is programmable by configuration register CONF_FLTIMEOUT. TI recommends using a longer timeout setting for low baud rate communication to avoid unintended timeout and using a shorter timeout setting for high baud rate communication.

If communication CRC check fails, the TPS929121-Q1 ignores the message without sending the feedback. The master does not receive any feedback if the communication is unsuccessful. In this case, the communication can be reset by keeping communication bus idle for $T_{(FLTIMEOUT)}$, which forces the TPS929121-Q1 to clear its cache and be ready for new communication.

FlexWire supports both write and readback. Both write or readback communication supports burst mode for high throughput and single-byte mode. Figure 8-11 describes the frame structure of a typical single-byte write action. The master frame consists of SYNC, DEV_ADDR, REG_ADDR, DATA and CRC bytes. Once CRC is verified, the slave immediately feeds back ACK byte. Figure 8-12 describes the frame structure of a typical single-byte readback action. The master frame consists of SYNC, DEV_ADDR, REG_ADDR, and CRC bytes. Once CRC is verified, the slave immediately feeds back DATA and ACK bytes.

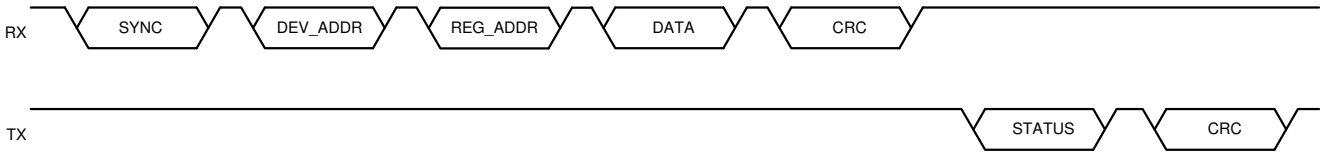


Figure 8-11. Single-Byte Write Command With Status Feedback

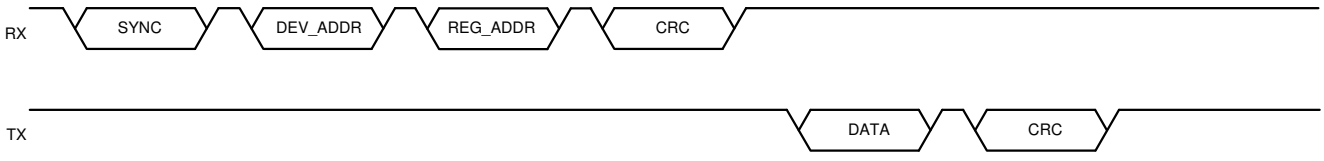


Figure 8-12. Single-Byte Readback Command

Table 8-6. Frame-Byte Description

BYTE NAME	LENGTH (byte)	DESCRIPTION
SYNC	1	Synchronization byte from master
DEV_ADDR	1	Device address bit, r/w, broadcast, burst mode
REG_ADDR	1	Register address

Table 8-6. Frame-Byte Description (continued)

BYTE NAME	LENGTH (byte)	DESCRIPTION
DATA_N	Variable (1, 2, 4, 8)	N-th byte data content
CRC	1	Cyclic redundancy check (CRC) for DEV_ADDR, REG_ADDR and all DATA bytes
STATUS	1	Acknowledgment (Return FLAG0 register value)

8.5.1.2 UART Interface Address Setting

Each FlexWire bus supports maximum 16 slave devices. The TPS929121-Q1 has 3 pinouts including ADDR2, ADDR1, and ADDR0 for slave address configuration. There are additional 4-bit EEPROM register to program the slave address of the TPS929121-Q1. The EEPROM register EEP_INTADDR sets the device slave address by either address pins setup or internal EEPROM register code.

If EEP_INTADDR is 1, the device uses the binary code burnt in EEPROM register EEP_DEVADDR as slave address as shown in Table 8-7 . In this conditions, the ADDR2 pin is used for external clock input for internal PWM generator as described in *External Clock Input for PWM Generator (CLK)*, however ADDR1 and ADDR0 pins are used for external PWM inputs to directly control the current output as described in *External PWM Input $\overline{PWM0}$ and $\overline{PWM1}$*.

If EEP_INTADDR is 0, the device uses EEP_DEVADDR[3] code together with external inputs on ADDR2, ADDR1 and ADDR0 as shown in Table 8-7 and ignore EEP_DEVADDR[2:0] code.

The address 0h to Fh can be used as slave address for up to 16 pieces of TPS929121-Q1 in same FlexWire bus. In broadcast mode, 0h must be used for all slave devices address. It is not allowed to have two TPS929121-Q1 sharing the same slave address either setting by internal EEPROM register EEP_DEVADDR or address pins configuration on ADDR2, ADDR1 and ADDR0.

Table 8-7. Device Address Setting

Address(HEX)	INTERNAL ADDRESS SETTING				EXTERNAL ADDRESS SETTING			
	BIT3	BIT2	BIT1	BIT0	BIT3	BIT2	BIT1	BIT0
	EEP_DEVADDR[3]	EEP_DEVADDR[2]	EEP_DEVADDR[1]	EEP_DEVADDR[0]	EEP_DEVADDR[3]	ADDR2	ADDR1	ADDR0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	0	0	1
A	1	0	1	0	1	0	1	0
B	1	0	1	1	1	0	1	1
C	1	1	0	0	1	1	0	0
D	1	1	0	1	1	1	0	1
E	1	1	1	0	1	1	1	0
F	1	1	1	1	1	1	1	1

The TPS929121-Q1 has EEP_DEVADDR[3] bit set to 0 as default, however TPS929121A version has EEP_DEVADDR[3] bit set to 1 as default. It allows up to 16 pieces of TPS929121-Q1 on same FlexWire bus accessible through external configuration on ADDR2, ADDR1 and ADDR0 without burning the EEP_DEVADDR registers.

8.5.1.3 Status Response

When the TPS929121-Q1 as a slave device receives a non-broadcast frame, it first verifies the CRC byte. Once CRC check is succeed, the TPS929121-Q1 sends out the device status of FLAG0 register byte followed by CRC byte.

Every communication requires CRC verification to make sure the integrity for the data transaction. In broadcast mode, TPS929121-Q1 does not send out acknowledge response.

8.5.1.4 Synchronization Byte

The first byte data sent from master controller to TPS929121-Q1 is synchronization frame (SYNC). The master controller sends the clock signal to TPS929121-Q1 through outputting 01010101 binary code in first frame. The TPS929121-Q1 adaptively uses the same clock to communicate with master by synchronization of internal high frequency clock. To avoid clock drift over time, the synchronization byte is always required for each new instruction transaction on FlexWire interface. With this approach, the communication reliability is improved, and the cost for external crystal oscillator is saved. Figure 8-13 is the timing diagram for synchronization frame and device address frame.

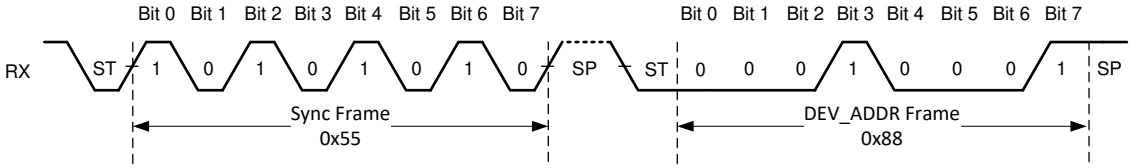


Figure 8-13. Synchronization Byte

8.5.1.5 Device Address Byte

The device address byte, DEV_ADDR frame follows the SYNC frame. There are total 8 bits binary code in device address byte. The detail definition for each bit function is described in Table 8-8. The DEVICE_ADDR register is required to set to 0000b for broadcast mode, otherwise the broadcast mode can not be enabled.

Table 8-8. DEV_ADDR Byte

BIT	FIELD	DESCRIPTION
3-0	DEVICE_ADDR	Target device address.
5-4	DATA_LENGTH	00b: Single-byte mode with 1 byte of data; 01b: Bust mode with 2 bytes of data; 10b: Burst mode with 4 bytes of data; 11b: Burst mode with 8 bytes of data
6	BROADCAST	Broadcast mode. 1: Broadcast (DEVICE_ADDR =0000b); 0: Single-device only
7	READ/WRITE	Read / Write mode. 1: Write mode; 0: Read mode

8.5.1.6 Register Address Byte

The register address byte, REG_ADDR frame follows the device address frame. There are total 8 bits binary code in register address byte. The maximum allowed register address is 255. Figure 8-14 is the timing diagram for register address frame and data frame.

Table 8-9. REG_ADDR Byte

BIT	FIELD	DESCRIPTION
0 - 7	REG_ADDR	Register address.

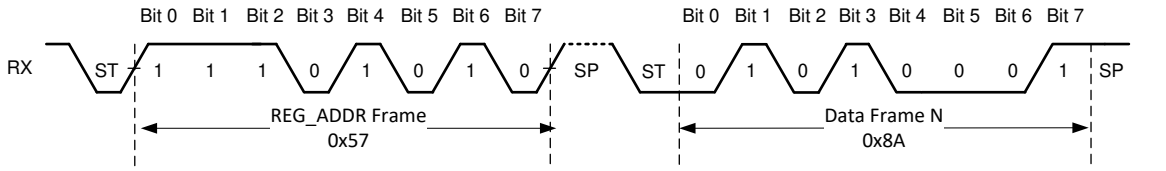


Figure 8-14. Address and Data Bytes

8.5.1.7 Data Frame

The data bytes, data frame follows the register address byte. The TPS929121-Q1 supports single-data-byte, or multiple-data-byte writing in one time data transaction. The number of data byte is defined in the device address byte as introduced in Table 8-8. There are total 4 options including 1 data byte, 2, 4, or 8 data bytes.

Table 8-10. DATA Byte

BIT	FIELD	DESCRIPTION
0 - 7	DATA	Data

8.5.1.8 CRC Frame

The CRC data byte follows the data byte as the final byte in the end of one data transaction to ensure the TPS929121-Q1 correctly receiving all the data bytes from master controller. The master controller must calculate the CRC value for all bytes binary code including device address byte, register address byte, data bytes and send it to TPS929121-Q1 to end the one time communication. The TPS929121-Q1 receives all bytes data, calculates the CRC and compares the calculated CRC code with received CRC code. If two CRC codes do not match each other, the TPS929121-Q1 ignores the data transaction and wait for next data transaction without reset FlexWire watchdog timer, WDTIMER. The CRC algorithm is same to the EEPROM CRC diagnostics as described in *EEPROM CRC Error in Normal State*. The initial code for CRC is FFh as well.

Table 8-11. CRC Byte

BIT	FIELD	DESCRIPTION
0 - 7	CRC	CRC Residual

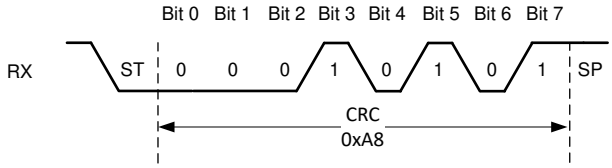


Figure 8-15. CRC Byte

8.5.1.9 Burst Mode

The TPS929121-Q1 with FlexWire protocol supports burst mode for multiple data bytes writing and reading in one data transaction cycle to accelerate the communication between the master controller and slaves. Figure 8-16 shows the data format for multiple data bytes write, and Figure 8-17 shows the data format for multiple data bytes read. The DATA_1 is written to the register in REG_ADDR address, and the following DATA_2 to DATA_N are written to the registers in REG_ADDR+1 to REG_ADDR+N address sequentially for multiple bytes write. For multiple data read, the DATA_1 is read from the register in REG_ADDR address, and the following DATA_2 to DATA_N are read from the registers in REG_ADDR+1 to REG_ADDR+N address sequentially.

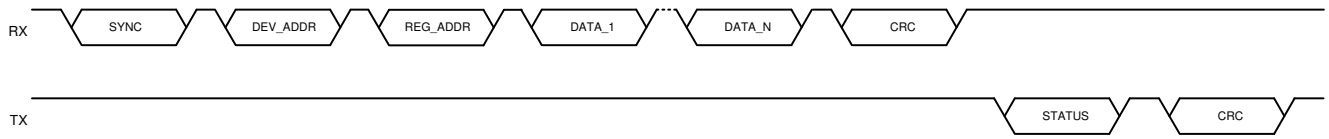


Figure 8-16. Multiple Data Bytes Write in Burst Mode

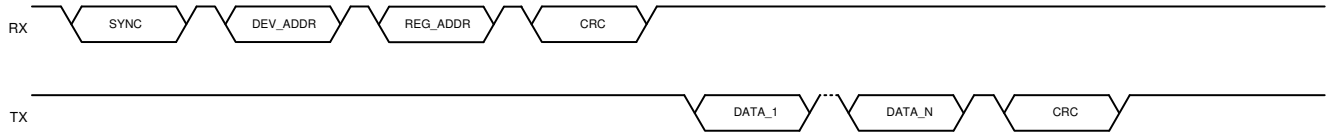


Figure 8-17. Multiple Data Bytes Read in Burst Mode

8.5.2 Registers Lock

The TPS929121-Q1 provides registers content lock feature to prevent unintended modification of registers. There are 4 register lock bits for different type of registers covering all registers. The 4-lock register bits is set to 1 as default, which means the master controller must the set lock bit to 0 before write operation to the corresponding registers. TI recommends locking the register after register writing operations.

- Setting CONF_IOUTLOCK to 1 disables write operation to IOUTx registers.
- Setting CONF_PWMLOCK to 1 disables write operation to PWMx and PWMLx registers.
- Setting CONF_CONFLOCK to 1 disables write operation to CONFx registers.
- Setting CONF_CLRLOCK to 1 disables write operation to CLRx registers.

8.5.3 All Registers CRC Check

The TPS929121-Q1 has a 8-bit register CALC_CONFCRC to store the calculated CRC result for all registers listed in Table 8-12. The master controller can read back the data in CALC_CONFCRC to quickly check any untended change of registers without reading back all configuration registers. The CRC algorithm is same to the EEPROM CRC diagnostics as described in *EEPROM CRC Error in Normal State*. The initial code for CRC is FFh as well.

8.5.4 EEPROM Programming

The TPS929121-Q1 has a user-programmable EEPROM with high reliability for automotive applications. All the EEPROM registers have internal shadow registers used as buffer for programming only. The TPS929121-Q1 supports two solutions for individual chip selection through pulling REF pin high or through device address configuration by address pin.

8.5.4.1 Chip Selection by Pulling REF Pin High

The TPS929121-Q1 supports using REF pin as chip-select during EEPROM programming. Considering multiple TPS929121-Q1 devices connected on one FlexWire bus before burning EEPROM, the slave address for all TPS929121-Q1 are all same before programming in case internal EEPROM register EEP_DEVADDR is used for slave address setup. The EEPROM burning instruction can be sent to target TPS929121-Q1 by pulling the REF pin of the target TPS929121-Q1 to 5 V. Once the REF pin is pulled up to 5 V, the TPS929121-Q1 ignores the device address set up by ADDR2/ADDR1/ADDR0 pins or EEPROM programmed device address in EEP_DEVADDR. The master controller must send out data to target TPS929121-Q1 with device address as 0h and not in broadcast mode (Write 0 to bit 6 in device address byte).

8.5.4.2 Chip Selection by ADDR Pins configuration

The TPS929121-Q1 also supports using configuration on ADDR2/ADDR1/ADDR0 pins to determine the slave address for TPS929121-Q1 if multiple TPS929121-Q1 devices are connected on same FlexWire interface. It is recommended to use this approach for applications with eight or less than eight of TPS929121-Q1 in same FlexWire interface. The master controller can send out register data to target TPS929121-Q1 with device address matched to the ADDR2/ADDR1/ADDR0 pins configuration and not in broadcast mode (Write 0 to bit 6 in device address byte).

8.5.4.3 EEPROM Register Access and Burn

After selecting the target TPS929121-Q1 for EEPROM burning, the master controller must send a serial data bytes to register CONF_EEPGATE, set 1 to CONF_EEPMODE and set 1 to register CONF_STAYINEEP one by one in below sequency to finally enable the EEPROM register access. Each data written must be a single-byte operation instead of burst-mode operation.

Chip is selected by pulling REF pin high, below instruction is required to access the EEPROM register.

- Write 09h, 02h, 09h, 01h, 02h, 00h to 8-bit register CONF_EEPGATE one-byte by one-byte sequentially.
- Write 1 to 1-bit register CONF_EEPMODE.
- Write 1 to 1-bit register CONF_STAYINEEP.

Chip is selected by ADDR pins configuration, below instruction is required to access the EEPROM register.

- Write 00h, 02h, 01h, 09h, 02h, 09h to 8-bit register CONF_EEPGATE one-byte by one-byte sequentially.
- Write 1 to 1-bit register CONF_EEPMODE.
- Write 1 to 1-bit register CONF_STAYINEEP.

The EEPROM registers of the TPS929121-Q1 can be overwritten after the access enabled. Then master controller can set CONF_EEPPROG to 1 to start the burning of all the EEPROM register. The data for EEPROM register is only stored in EEPROM shadow register without burning into true EEPROM cell before setting CONF_EEPPROG to 1. The data is lost after POR cycle if it is not burnt to EEPROM cell. All EEPROM shadow registers need to be written to target value before burning. The CONF_EEPPROG automatically returns to 0 at the next clock cycle. The programming takes around 200 ms and flag register FLAG_PROGREADY is 0 during programming. It is important to keep device power supply stable for at least 200 ms after writing 1 to CONF_EEPPROG to make sure solid and robust burning. After programming is done, the FLAG_PROGREADY is automatically set to 1. The detail flow chart is described in Figure 8-18.

The EEPROM cells for TPS929121-Q1 can be overwritten and burnt for up to 1000 times. The one time EEPROM burning is counted once the register CONF_EEPPROG is set to 1 even though the EEPROM data is not changed at all.

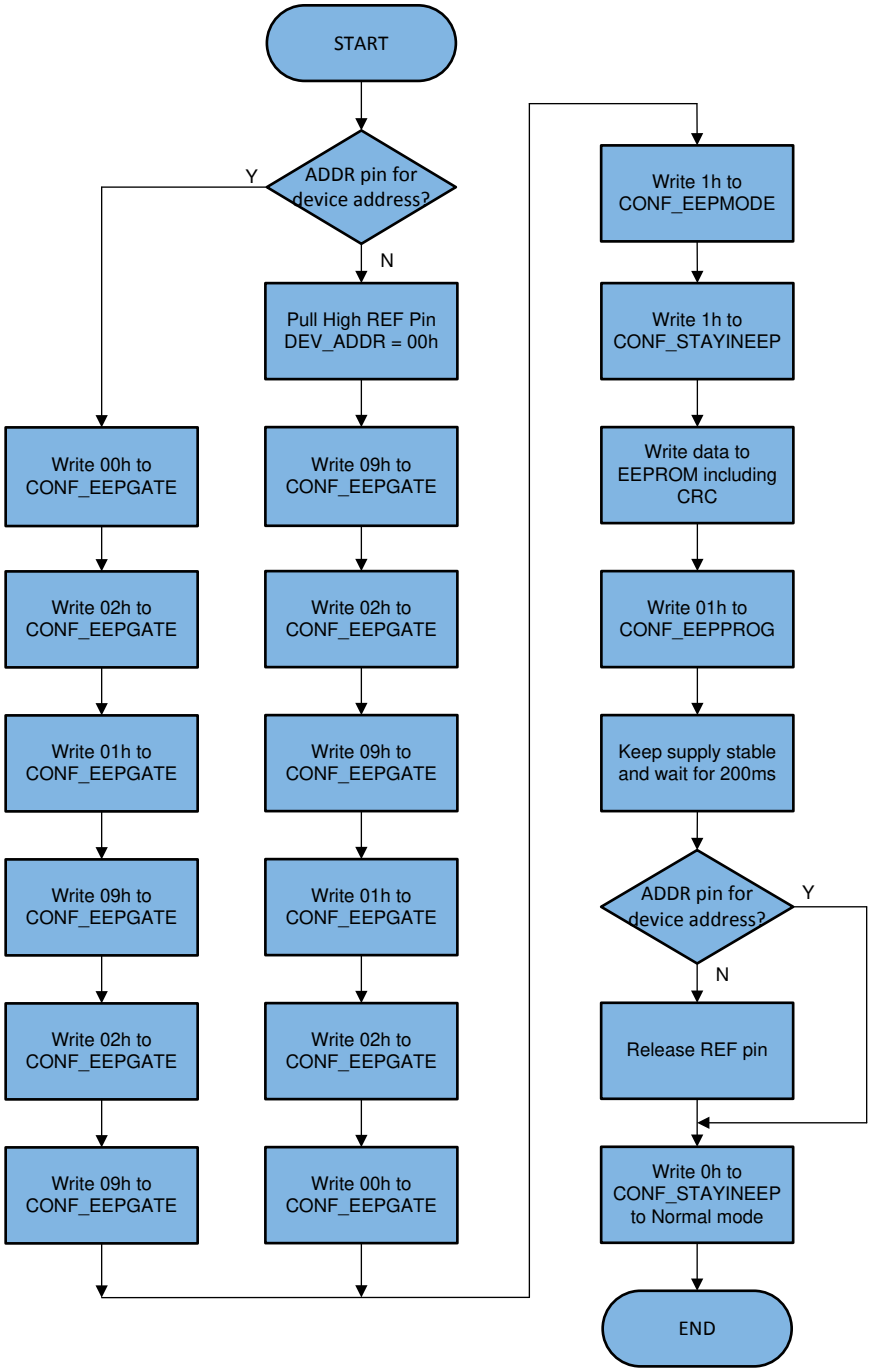


Figure 8-18. Programming Sequence

8.5.4.4 EEPROM Program State Exit

The REF pin can be released after EEPROM burning if it is pulled high to 5 V for chip selection. The REF pin must be kept high during all EEPROM program state.

The TPS929121-Q1 can quit the EEPROM program state to normal state after burning by writing 0 to register CONF_STAYINEEP. TI recommends reloading the EEPROM data to the registers after EEPROM burning by set 1 to CLR_REG.

8.5.4.5 Reading Back EEPROM

The TPS929121-Q1 supports EEPROM data reading back for both shadow registers and EEPROM cells. When the register CONF_READSHADOW is set to 1, reading back for certain EEPROM registers address returns shadow registers content. When the register CONF_READSHADOW is set to 0, reading back for certain EEPROM registers address returns content in EEPROM cell.

8.6 Register Maps

CAUTION

All the RESERVED bits in register and EEPROM are set to 0b in TI manufacture. All the RESERVED bits in both register and EEPROM must be written to 0b in case of unavoidable register and EEPROM writing.

Table 8-12. Register Map

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT
00h	IOUT0	RESERVED	RESERVED	CONF_IOUT0						EEPI0
01h	IOUT1	RESERVED	RESERVED	CONF_IOUT1						EEPI1
02h	IOUT2	RESERVED	RESERVED	CONF_IOUT2						EEPI2
03h	IOUT3	RESERVED	RESERVED	CONF_IOUT3						EEPI3
04h	IOUT4	RESERVED	RESERVED	CONF_IOUT4						EEPI4
05h	IOUT5	RESERVED	RESERVED	CONF_IOUT5						EEPI5
06h	IOUT6	RESERVED	RESERVED	CONF_IOUT6						EEPI6
07h	IOUT7	RESERVED	RESERVED	CONF_IOUT7						EEPI7
08h	IOUT8	RESERVED	RESERVED	CONF_IOUT8						EEPI8
09h	IOUT9	RESERVED	RESERVED	CONF_IOUT9						EEPI9
0Ah	IOUT10	RESERVED	RESERVED	CONF_IOUT10						EEPI10
0Bh	IOUT11	RESERVED	RESERVED	CONF_IOUT11						EEPI11
20h	PWM0	CONF_PWMOUT0								EEPP0
21h	PWM1	CONF_PWMOUT1								EEPP1
22h	PWM2	CONF_PWMOUT2								EEPP2
23h	PWM3	CONF_PWMOUT3								EEPP3
24h	PWM4	CONF_PWMOUT4								EEPP4
25h	PWM5	CONF_PWMOUT5								EEPP5
26h	PWM6	CONF_PWMOUT6								EEPP6
27h	PWM7	CONF_PWMOUT7								EEPP7
28h	PWM8	CONF_PWMOUT8								EEPP8
29h	PWM9	CONF_PWMOUT9								EEPP9
2Ah	PWM10	CONF_PWMOUT10								EEPP10
2Bh	PWM11	CONF_PWMOUT11								EEPP11
40h	PWML0	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT0				0Fh
41h	PWML1	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT1				0Fh

Table 8-12. Register Map (continued)

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT
42h	PWML2	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT2				0Fh
43h	PWML3	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT3				0Fh
44h	PWML4	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT4				0Fh
45h	PWML5	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT5				0Fh
46h	PWML6	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT6				0Fh
47h	PWML7	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT7				0Fh
48h	PWML8	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT8				0Fh
49h	PWML9	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT9				0Fh
4Ah	PWML10	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT10				0Fh
4Bh	PWML11	RESERVED	RESERVED	RESERVED	RESERVED	CONF_PWMLOWOUT11				0Fh
50h	CONF_EN0	CONF_ENCH7	CONF_ENCH6	CONF_ENCH5	CONF_ENCH4	CONF_ENCH3	CONF_ENCH2	CONF_ENCH1	CONF_ENCH0	00h
51h	CONF_EN1	RESERVED	RESERVED	RESERVED	RESERVED	CONF_ENCH11	CONF_ENCH10	CONF_ENCH9	CONF_ENCH8	00h
54h	CONF_DIAGEN0	CONF_DIAGEN CH7	CONF_DIAGEN CH6	CONF_DIAGEN CH5	CONF_DIAGEN CH4	CONF_DIAGEN CH3	CONF_DIAGEN CH2	CONF_DIAGEN CH1	CONF_DIAGEN CH0	EEPM4
55h	CONF_DIAGEN1	RESERVED	RESERVED	RESERVED	RESERVED	CONF_DIAGEN CH11	CONF_DIAGEN CH10	CONF_DIAGEN CH9	CONF_DIAGEN CH8	EEPM5
56h	CONF_MISC0	CONF_AUTOSS	CONF_LDO	RESERVED	CONF_EXPEN	RESERVED	RESERVED	RESERVED	RESERVED	EEPM6
57h	CONF_MISC1	CONF_PWMFREQ				RESERVED	RESERVED	CONF_REFRANGE		EEPM7
58h	CONF_MISC2	RESERVED	CONF_FLTIMEOUT			CONF_ADCLOWSUPTH				EEPM8
59h	CONF_MISC3	CONF_ODIOUT				CONF_ODPW				EEPM9
5Ah	CONF_MISC4	CONF_WDTIMER				RESERVED	RESERVED	RESERVED	RESERVED	EEPM10
5Bh	CONF_MISC5	CONF_ADCSHORTTH								EEPM11
60h	CLR	RESERVED	RESERVED	CONF_FORCEFS	CLR_REG	CONF_FORCEERR	CLR_FS	CLR_FAULT	CLR_POR	00h
61h	CONF_LOCK	RESERVED	RESERVED	RESERVED	RESERVED	CONF_CLRLOCK	CONF_CONFLOCK	CONF_IOUTLOCK	CONF_PWMLOCK	0Fh
62h	CONF_MISC6	CONF_STAYINEEP	CONF_EEPREADBACK	RESERVED	CONF_ADCCH					00h
63h	CONF_MISC7			CONF_EXTCLK	CONF_SHAREPWM			CONF_READSHADOW	CONF_EEPMODE	00h
64h	CONF_MISC8	CONF_MASKREF	CONF_MASKCRC	CONF_MASKOPEN	CONF_MASKSHORT	CONF_MASKTSD	CONF_EEPPROG	CONF_SSSTART	CONF_INVDIAGSTART	00h
65h	CONF_MISC9	CONF_EEPGATE								00h
70h	FLAG0	RESERVED	FLAG_REF	FLAG_FS	FLAG_OUT	FLAG_PRETSD	FLAG_TSD	FLAG_POR	FLAG_ERR	03h

Table 8-12. Register Map (continued)

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT
71h	FLAG1	RESERVED	RESERVED	FLAG_EXTFS	FLAG_PROGREADY	FLAG_ADCLOWSUP	FLAG_ADCDONE	FLAG_ODREADY	FLAG_EEPCRC	X
72h	FLAG2	ADC_SUPPLY								X
73h	FLAG3	ADC_OUT								00h
74h	FLAG4	FLAG_ODDIAGCH7	FLAG_ODDIAGCH6	FLAG_ODDIAGCH5	FLAG_ODDIAGCH4	FLAG_ODDIAGCH3	FLAG_ODDIAGCH2	FLAG_ODDIAGCH1	FLAG_ODDIAGCH0	00h
75h	FLAG5	RESERVED	RESERVED	RESERVED	RESERVED	FLAG_ODDIAGCH11	FLAG_ODDIAGCH10	FLAG_ODDIAGCH9	FLAG_ODDIAGCH8	00h
77h	FLAG7	CALC_EEPCRC								B3h(1)
78h	FLAG8	CALC_CONFCRC								X
7Bh	FLAG11	FLAG_OPENCH7	FLAG_OPENCH6	FLAG_OPENCH5	FLAG_OPENCH4	FLAG_OPENCH3	FLAG_OPENCH2	FLAG_OPENCH1	FLAG_OPENCH0	00h
7Ch	FLAG12	RESERVED	RESERVED	RESERVED	RESERVED	FLAG_OPENCH11	FLAG_OPENCH10	FLAG_OPENCH9	FLAG_OPENCH8	00h
7Dh	FLAG13	FLAG_SHORTCH7	FLAG_SHORTCH6	FLAG_SHORTCH5	FLAG_SHORTCH4	FLAG_SHORTCH3	FLAG_SHORTCH2	FLAG_SHORTCH1	FLAG_SHORTCH0	00h
7Eh	FLAG14	RESERVED	RESERVED	RESERVED	RESERVED	FLAG_SHORTCH11	FLAG_SHORTCH10	FLAG_SHORTCH9	FLAG_SHORTCH8	00h

(1) For TPS929121A version, the default value of register FLAG7 is 09h.

Table 8-13. EEPROM Map

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT
80h	EEPI0	RESERVED	RESERVED	EEP_IOUT0						3Fh
81h	EEPI1	RESERVED	RESERVED	EEP_IOUT1						3Fh
82h	EEPI2	RESERVED	RESERVED	EEP_IOUT2						3Fh
83h	EEPI3	RESERVED	RESERVED	EEP_IOUT3						3Fh
84h	EEPI4	RESERVED	RESERVED	EEP_IOUT4						3Fh
85h	EEPI5	RESERVED	RESERVED	EEP_IOUT5						3Fh
86h	EEPI6	RESERVED	RESERVED	EEP_IOUT6						3Fh
87h	EEPI7	RESERVED	RESERVED	EEP_IOUT7						3Fh
88h	EEPI8	RESERVED	RESERVED	EEP_IOUT8						3Fh
89h	EEPI9	RESERVED	RESERVED	EEP_IOUT9						3Fh
8Ah	EEPI10	RESERVED	RESERVED	EEP_IOUT10						3Fh
8Bh	EEPI11	RESERVED	RESERVED	EEP_IOUT11						3Fh
A0h	EEPP0	EEP_PWMOUT0								FFh
A1h	EEPP1	EEP_PWMOUT1								FFh
A2h	EEPP2	EEP_PWMOUT2								FFh
A3h	EEPP3	EEP_PWMOUT3								FFh
A4h	EEPP4	EEP_PWMOUT4								FFh
A5h	EEPP5	EEP_PWMOUT5								FFh
A6h	EEPP6	EEP_PWMOUT6								FFh
A7h	EEPP7	EEP_PWMOUT7								FFh
A8h	EEPP8	EEP_PWMOUT8								FFh
A9h	EEPP9	EEP_PWMOUT9								FFh
AAh	EEPP10	EEP_PWMOUT10								FFh
ABh	EEPP11	EEP_PWMOUT11								FFh
C0h	EEPM0	EEP_FS0CH7	EEP_FS0CH6	EEP_FS0CH5	EEP_FS0CH4	EEP_FS0CH3	EEP_FS0CH2	EEP_FS0CH1	EEP_FS0CH0	00h
C1h	EEPM1	RESERVED	RESERVED	RESERVED	RESERVED	EEP_FS0CH11	EEP_FS0CH10	EEP_FS0CH9	EEP_FS0CH8	00h
C2h	EEPM2	EEP_FS1CH7	EEP_FS1CH6	EEP_FS1CH5	EEP_FS1CH4	EEP_FS1CH3	EEP_FS1CH2	EEP_FS1CH1	EEP_FS1CH0	FFh
C3h	EEPM3	RESERVED	RESERVED	RESERVED	RESERVED	EEP_FS1CH11	EEP_FS1CH10	EEP_FS1CH9	EEP_FS1CH8	0Fh
C4h	EEPM4	EEP_DIAGENCH7	EEP_DIAGENCH6	EEP_DIAGENCH5	EEP_DIAGENCH4	EEP_DIAGENCH3	EEP_DIAGENCH2	EEP_DIAGENCH1	EEP_DIAGENCH0	FFh
C5h	EEPM5	RESERVED	RESERVED	RESERVED	RESERVED	EEP_DIAGENCH11	EEP_DIAGENCH10	EEP_DIAGENCH9	EEP_DIAGENCH8	0Fh

Table 8-13. EEPROM Map (continued)

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT
C6h	EEPM6	RESERVED	EEP_LDO	RESERVED	EEP_EXPEN	EEP_DEVADDR				00h(1)
C7h	EEPM7	EEP_PWMFREQ				EEP_INTADDR	EEP_OFAF	EEP_REFRANGE		A7h
C8h	EEPM8	RESERVED	EEP_FLTIMEOUT			EEP_ADCLOWSUPTH				03h
C9h	EEPM9	EEP_ODIOUT				EEP_ODPW				00h
CAh	EEPM10	EEP_WDTIMER				EEP_INITTIMER				00h
CBh	EEPM11	EEP_ADCSHORTTH								00h
CCh	EEPM12	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	00h
CDh	EEMP13	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	00h
CEh	EEMP14	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	00h
CFh	EEPM15	EEP_CRC								B3h(2)

(1) For TPS929121A version, the default value of EEPROM register EEPM6 is 08h.
(2) For TPS929121A version, the default value of EEPROM register EEPM15 is 09h.

8.6.1 FullMap Registers

Table 8-14 lists the FullMap registers. All register offset addresses not listed in Table 8-14 should be considered as reserved locations and the register contents should not be modified.

Table 8-14. FULLMAP Registers

Offset	Acronym	Register Name	Section
0h	IOUT0	Output Current Setting for CH0	Go
1h	IOUT1	Output Current Setting for CH1	Go
2h	IOUT2	Output Current Setting for CH2	Go
3h	IOUT3	Output Current Setting for CH3	Go
4h	IOUT4	Output Current Setting for CH4	Go
5h	IOUT5	Output Current Setting for CH5	Go
6h	IOUT6	Output Current Setting for CH6	Go
7h	IOUT7	Output Current Setting for CH7	Go
8h	IOUT8	Output Current Setting for CH8	Go
9h	IOUT9	Output Current Setting for CH9	Go
Ah	IOUT10	Output Current Setting for CH10	Go
Bh	IOUT11	Output Current Setting for CH11	Go
20h	PWM0	Output PWM Duty-cycle Setting for CH0	Go
21h	PWM1	Output PWM Duty-cycle Setting for CH1	Go
22h	PWM2	Output PWM Duty-cycle Setting for CH2	Go
23h	PWM3	Output PWM Duty-cycle Setting for CH3	Go
24h	PWM4	Output PWM Duty-cycle Setting for CH4	Go
25h	PWM5	Output PWM Duty-cycle Setting for CH5	Go
26h	PWM6	Output PWM Duty-cycle Setting for CH6	Go
27h	PWM7	Output PWM Duty-cycle Setting for CH7	Go
28h	PWM8	Output PWM Duty-cycle Setting for CH8	Go
29h	PWM9	Output PWM Duty-cycle Setting for CH9	Go
2Ah	PWM10	Output PWM Duty-cycle Setting for CH10	Go
2Bh	PWM11	Output PWM Duty-cycle Setting for CH11	Go
40h	PWML0	Output PWM Duty-cycle Setting Lower bits for CH0	Go
41h	PWML1	Output PWM Duty-cycle Setting Lower bits for CH1	Go
42h	PWML2	Output PWM Duty-cycle Setting Lower bits for CH2	Go
43h	PWML3	Output PWM Duty-cycle Setting Lower bits for CH3	Go
44h	PWML4	Output PWM Duty-cycle Setting Lower bits for CH4	Go
45h	PWML5	Output PWM Duty-cycle Setting Lower bits for CH5	Go
46h	PWML6	Output PWM Duty-cycle Setting Lower bits for CH6	Go
47h	PWML7	Output PWM Duty-cycle Setting Lower bits for CH7	Go
48h	PWML8	Output PWM Duty-cycle Setting Lower bits for CH8	Go
49h	PWML9	Output PWM Duty-cycle Setting Lower bits for CH9	Go
4Ah	PWML10	Output PWM Duty-cycle Setting Lower bits for CH10	Go
4Bh	PWML11	Output PWM Duty-cycle Setting Lower bits for CH11	Go
50h	CONF_EN0	Channel Enable Register 0	Go
51h	CONF_EN1	Channel Enable Register 1	Go
54h	CONF_DIAGEN0	Diagnostics Enable Register 0	Go
55h	CONF_DIAGEN1	Diagnostics Enable Register 1	Go
56h	CONF_MISC0	Miscellanous Register 0	Go
57h	CONF_MISC1	Miscellanous Register 1	Go

Table 8-14. FULLMAP Registers (continued)

Offset	Acronym	Register Name	Section
58h	CONF_MISC2	Miscellanous Register 2	Go
59h	CONF_MISC3	Miscellanous Register 3	Go
5Ah	CONF_MISC4	Miscellanous Register 4	Go
5Bh	CONF_MISC5	Miscellanous Register 5	Go
60h	CLR	Configuration Register for Clear	Go
61h	CONF_LOCK	Configuration Register for LOCK	Go
62h	CONF_MISC6	Miscellanous Register 6	Go
63h	CONF_MISC7	Miscellanous Register 7	Go
64h	CONF_MISC8	Miscellanous Register 8	Go
65h	CONF_MISC9	Miscellanous Register 9	Go
70h	FLAG0	Device status flag register 0	Go
71h	FLAG1	Device status flag register 1	Go
72h	FLAG2	Device status flag register 2	Go
73h	FLAG3	Device status flag register 3	Go
74h	FLAG4	Device status flag register 4	Go
75h	FLAG5	Device status flag register 5	Go
77h	FLAG7	Device status flag register 7	Go
78h	FLAG8	Device status flag register 8	Go
7Bh	FLAG11	Device status flag register 11	Go
7Ch	FLAG12	Device status flag register 12	Go
7Dh	FLAG13	Device status flag register 13	Go
7Eh	FLAG14	Device status flag register 14	Go
80h	EEPI0	EEPROM Output Current Setting for CH0	Go
81h	EEPI1	EEPROM Output Current Setting for CH1	Go
82h	EEPI2	EEPROM Output Current Setting for CH2	Go
83h	EEPI3	EEPROM Output Current Setting for CH3	Go
84h	EEPI4	EEPROM Output Current Setting for CH4	Go
85h	EEPI5	EEPROM Output Current Setting for CH5	Go
86h	EEPI6	EEPROM Output Current Setting for CH6	Go
87h	EEPI7	EEPROM Output Current Setting for CH7	Go
88h	EEPI8	EEPROM Output Current Setting for CH8	Go
89h	EEPI9	EEPROM Output Current Setting for CH9	Go
8Ah	EEPI10	EEPROM Output Current Setting for CH10	Go
8Bh	EEPI11	EEPROM Output Current Setting for CH11	Go
A0h	EEPP0	EEPROM Output PWM Duty-cycle Setting for CH0	Go
A1h	EEPP1	EEPROM Output PWM Duty-cycle Setting for CH1	Go
A2h	EEPP2	EEPROM Output PWM Duty-cycle Setting for CH2	Go
A3h	EEPP3	EEPROM Output PWM Duty-cycle Setting for CH3	Go
A4h	EEPP4	EEPROM Output PWM Duty-cycle Setting for CH4	Go
A5h	EEPP5	EEPROM Output PWM Duty-cycle Setting for CH5	Go
A6h	EEPP6	EEPROM Output PWM Duty-cycle Setting for CH6	Go
A7h	EEPP7	EEPROM Output PWM Duty-cycle Setting for CH7	Go
A8h	EEPP8	EEPROM Output PWM Duty-cycle Setting for CH8	Go
A9h	EEPP9	EEPROM Output PWM Duty-cycle Setting for CH9	Go
AAh	EEPP10	EEPROM Output PWM Duty-cycle Setting for CH10	Go

Table 8-14. FULLMAP Registers (continued)

Offset	Acronym	Register Name	Section
ABh	EEPP11	EEPROM Output PWM Duty-cycle Setting for CH11	Go
C0h	EEPM0	EEPROM Miscellaneous registers 0	Go
C1h	EEPM1	EEPROM Miscellaneous registers 1	Go
C2h	EEPM2	EEPROM Miscellaneous registers 2	Go
C3h	EEPM3	EEPROM Miscellaneous registers 3	Go
C4h	EEPM4	EEPROM Miscellaneous registers 4	Go
C5h	EEPM5	EEPROM Miscellaneous registers 5	Go
C6h	EEPM6	EEPROM Miscellaneous registers 6	Go
C7h	EEPM7	EEPROM Miscellaneous registers 7	Go
C8h	EEPM8	EEPROM Miscellaneous registers 8	Go
C9h	EEPM9	EEPROM Miscellaneous registers 9	Go
CAh	EEPM10	EEPROM Miscellaneous registers 10	Go
CBh	EEPM11	EEPROM Miscellaneous registers 11	Go
CFh	EEPM15	EEPROM CRC Check Value Registers	Go

Complex bit access types are encoded to fit into small table cells. Table 8-15 shows the codes that are used for access types in this section.

Table 8-15. FullMap Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 IOUT0 Register (Offset = 0h) [reset = X]

IOUT0 is shown in Figure 8-19 and described in Table 8-16.

Return to the Summary Table.

Figure 8-19. IOUT0 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT0					
R-0h		R/W-X					

Table 8-16. IOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT0	R/W	X	Output current setting for OUT0 Load EEPI0 data when reset

8.6.1.2 IOUT1 Register (Offset = 1h) [reset = X]

IOUT1 is shown in Figure 8-20 and described in Table 8-17.

Return to the Summary Table.

Figure 8-20. IOUT1 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT1					
R-0h		R/W-X					

Table 8-17. IOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT1	R/W	X	Output current setting for OUT1 Load EEPI1 data when reset

8.6.1.3 IOUT2 Register (Offset = 2h) [reset = X]

IOUT2 is shown in Figure 8-21 and described in Table 8-18.

Return to the Summary Table.

Figure 8-21. IOUT2 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT2					
R-0h		R/W-X					

Table 8-18. IOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT2	R/W	X	Output current setting for OUT2 Load EEPI2 data when reset

8.6.1.4 IOUT3 Register (Offset = 3h) [reset = X]

IOUT3 is shown in Figure 8-22 and described in Table 8-19.

Return to the Summary Table.

Figure 8-22. IOUT3 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT3					
R-0h		R/W-X					

Table 8-19. IOUT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT3	R/W	X	Output current setting for OUT3 Load EEPI3 data when reset

8.6.1.5 IOUT4 Register (Offset = 4h) [reset = X]

IOUT4 is shown in Figure 8-23 and described in Table 8-20.

Return to the Summary Table.

Figure 8-23. IOUT4 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT4					
R-0h		R/W-X					

Table 8-20. IOUT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT4	R/W	X	Output current setting for OUT4 Load EEPI4 data when reset

8.6.1.6 IOUT5 Register (Offset = 5h) [reset = X]

IOUT5 is shown in Figure 8-24 and described in Table 8-21.

Return to the Summary Table.

Figure 8-24. IOUT5 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT5					
R-0h		R/W-X					

Table 8-21. IOUT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT5	R/W	X	Output current setting for OUT5 Load EEPI5 data when reset

8.6.1.7 IOUT6 Register (Offset = 6h) [reset = X]

IOUT6 is shown in Figure 8-25 and described in Table 8-22.

Return to the Summary Table.

Figure 8-25. IOUT6 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT6					
R-0h		R/W-X					

Table 8-22. IOUT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT6	R/W	X	Output current setting for OUT6 Load EEPI6 data when reset

8.6.1.8 IOUT7 Register (Offset = 7h) [reset = X]

IOUT7 is shown in Figure 8-26 and described in Table 8-23.

Return to the Summary Table.

Figure 8-26. IOUT7 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT7					
R-0h		R/W-X					

Table 8-23. IOUT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT7	R/W	X	Output current setting for OUT7 Load EEPI7 data when reset

8.6.1.9 IOUT8 Register (Offset = 8h) [reset = X]

IOUT8 is shown in Figure 8-27 and described in Table 8-24.

Return to the Summary Table.

Figure 8-27. IOUT8 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT8					
R-0h		R/W-X					

Table 8-24. IOUT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT8	R/W	X	Output current setting for OUT8 Load EEPI8 data when reset

8.6.1.10 IOUT9 Register (Offset = 9h) [reset = X]

IOUT9 is shown in Figure 8-28 and described in Table 8-25.

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Figure 8-28. IOUT9 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT9					
R-0h		R/W-X					

Table 8-25. IOUT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT9	R/W	X	Output current setting for OUT9 Load EEPI9 data when reset

8.6.1.11 IOUT10 Register (Offset = Ah) [reset = X]

IOUT10 is shown in Figure 8-29 and described in Table 8-26.

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Figure 8-29. IOUT10 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT10					
R-0h		R/W-X					

Table 8-26. IOUT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT10	R/W	X	Output current setting for OUT10 Load EEPI10 data when reset

8.6.1.12 IOUT11 Register (Offset = Bh) [reset = X]

IOUT11 is shown in Figure 8-30 and described in Table 8-27.

Return to the Summary Table.

Figure 8-30. IOUT11 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_IOUT11					
R-0h		R/W-X					

Table 8-27. IOUT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	CONF_IOUT11	R/W	X	Output current setting for OUT11 Load EEPI11 data when reset

8.6.1.13 PWM0 Register (Offset = 20h) [reset = X]

PWM0 is shown in Figure 8-31 and described in Table 8-28.

Return to the Summary Table.

Figure 8-31. PWM0 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT0							
R/W-X							

Table 8-28. PWM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT0	R/W	X	PWM Dutycycle Register Setting for CH0 Load EEPP0 data when reset

8.6.1.14 PWM1 Register (Offset = 21h) [reset = X]

PWM1 is shown in Figure 8-32 and described in Table 8-29.

Return to the Summary Table.

Figure 8-32. PWM1 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT1							
R/W-X							

Table 8-29. PWM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT1	R/W	X	PWM Dutycycle Register Setting for CH1 Load EEPP1 data when reset

8.6.1.15 PWM2 Register (Offset = 22h) [reset = X]

PWM2 is shown in Figure 8-33 and described in Table 8-30.

Return to the Summary Table.

Figure 8-33. PWM2 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT2							
R/W-X							

Table 8-30. PWM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT2	R/W	X	PWM Dutycycle Register Setting for CH2 Load EEPP2 data when reset

8.6.1.16 PWM3 Register (Offset = 23h) [reset = X]

PWM3 is shown in Figure 8-34 and described in Table 8-31.

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Figure 8-34. PWM3 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT3							
R/W-X							

Table 8-31. PWM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT3	R/W	X	PWM Dutycycle Register Setting for CH3 Load EEPP3 data when reset

8.6.1.17 PWM4 Register (Offset = 24h) [reset = X]

PWM4 is shown in Figure 8-35 and described in Table 8-32.

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Figure 8-35. PWM4 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT4							
R/W-X							

Table 8-32. PWM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT4	R/W	X	PWM Dutycycle Register Setting for CH4 Load EEPP4 data when reset

8.6.1.18 PWM5 Register (Offset = 25h) [reset = X]

PWM5 is shown in Figure 8-36 and described in Table 8-33.

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Figure 8-36. PWM5 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT5							
R/W-X							

Table 8-33. PWM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT5	R/W	X	PWM Dutycycle Register Setting for CH5 Load EEPP5 data when reset

8.6.1.19 PWM6 Register (Offset = 26h) [reset = X]

PWM6 is shown in Figure 8-37 and described in Table 8-34.

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Figure 8-37. PWM6 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT6							
R/W-X							

Table 8-34. PWM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT6	R/W	X	PWM Dutycycle Register Setting for CH6 Load EEPP6 data when reset

8.6.1.20 PWM7 Register (Offset = 27h) [reset = X]

PWM7 is shown in Figure 8-38 and described in Table 8-35.

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Figure 8-38. PWM7 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT7							
R/W-X							

Table 8-35. PWM7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT7	R/W	X	PWM Dutycycle Register Setting for CH7 Load EEPP7 data when reset

8.6.1.21 PWM8 Register (Offset = 28h) [reset = X]

PWM8 is shown in Figure 8-39 and described in Table 8-36.

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Figure 8-39. PWM8 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT8							
R/W-X							

Table 8-36. PWM8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT8	R/W	X	PWM Dutycycle Register Setting for CH8 Load EEPP8 data when reset

8.6.1.22 PWM9 Register (Offset = 29h) [reset = X]

PWM9 is shown in Figure 8-40 and described in Table 8-37.

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Figure 8-40. PWM9 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT9							
R/W-X							

Table 8-37. PWM9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT9	R/W	X	PWM Dutycycle Register Setting for CH9 Load EEPP9 data when reset

8.6.1.23 PWM10 Register (Offset = 2Ah) [reset = X]

PWM10 is shown in Figure 8-41 and described in Table 8-38.

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Figure 8-41. PWM10 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT10							
R/W-X							

Table 8-38. PWM10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT10	R/W	X	PWM Dutycycle Register Setting for CH10 Load EEPP10 data when reset

8.6.1.24 PWM11 Register (Offset = 2Bh) [reset = X]

PWM11 is shown in Figure 8-42 and described in Table 8-39.

Return to the Summary Table.

Figure 8-42. PWM11 Register

7	6	5	4	3	2	1	0
CONF_PWMOUT11							
R/W-X							

Table 8-39. PWM11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_PWMOUT11	R/W	X	PWM Dutycycle Register Setting for CH11 Load EEPP11 data when reset

8.6.1.25 PWML0 Register (Offset = 40h) [reset = Fh]

PWML0 is shown in Figure 8-43 and described in Table 8-40.

Return to the Summary Table.

Figure 8-43. PWML0 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT0			
R-0h				R/W-Fh			

Table 8-40. PWML0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT0	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH0

8.6.1.26 PWML1 Register (Offset = 41h) [reset = Fh]

PWML1 is shown in Figure 8-44 and described in Table 8-41.

Return to the Summary Table.

Figure 8-44. PWML1 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT1			
R-0h				R/W-Fh			

Table 8-41. PWML1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT1	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH1

8.6.1.27 PWML2 Register (Offset = 42h) [reset = Fh]

PWML2 is shown in Figure 8-45 and described in Table 8-42.

Return to the Summary Table.

Figure 8-45. PWML2 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT2			
R-0h				R/W-Fh			

Table 8-42. PWML2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT2	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH2

8.6.1.28 PWML3 Register (Offset = 43h) [reset = Fh]

PWML3 is shown in Figure 8-46 and described in Table 8-43.

Return to the Summary Table.

Figure 8-46. PWML3 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT3			
R-0h				R/W-Fh			

Table 8-43. PWML3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT3	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH3

8.6.1.29 PWML4 Register (Offset = 44h) [reset = Fh]

PWML4 is shown in Figure 8-47 and described in Table 8-44.

Return to the Summary Table.

Figure 8-47. PWML4 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT4			
R-0h				R/W-Fh			

Table 8-44. PWML4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT4	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH4

8.6.1.30 PWML5 Register (Offset = 45h) [reset = Fh]

PWML5 is shown in Figure 8-48 and described in Table 8-45.

Return to the Summary Table.

Figure 8-48. PWML5 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT5			
R-0h				R/W-Fh			

Table 8-45. PWML5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT5	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH5

8.6.1.31 PWML6 Register (Offset = 46h) [reset = Fh]

PWML6 is shown in Figure 8-49 and described in Table 8-46.

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Figure 8-49. PWML6 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT6			
R-0h				R/W-Fh			

Table 8-46. PWML6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT6	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH6

8.6.1.32 PWML7 Register (Offset = 47h) [reset = Fh]

PWML7 is shown in Figure 8-50 and described in Table 8-47.

Return to the Summary Table.

Figure 8-50. PWML7 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT7			
R-0h				R/W-Fh			

Table 8-47. PWML7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT7	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH7

8.6.1.33 PWML8 Register (Offset = 48h) [reset = Fh]

PWML8 is shown in Figure 8-51 and described in Table 8-48.

Return to the Summary Table.

Figure 8-51. PWML8 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT8			
R-0h				R/W-Fh			

Table 8-48. PWML8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT8	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH8

8.6.1.34 PWML9 Register (Offset = 49h) [reset = Fh]

PWML9 is shown in Figure 8-52 and described in Table 8-49.

Return to the Summary Table.

Figure 8-52. PWML9 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT9			
R-0h				R/W-Fh			

Table 8-49. PWML9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT9	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH9

8.6.1.35 PWML10 Register (Offset = 4Ah) [reset = Fh]

PWML10 is shown in Figure 8-53 and described in Table 8-50.

Return to the Summary Table.

Figure 8-53. PWML10 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT10			
R-0h				R/W-Fh			

Table 8-50. PWML10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT10	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH10

8.6.1.36 PWML11 Register (Offset = 4Bh) [reset = Fh]

PWML11 is shown in Figure 8-54 and described in Table 8-51.

Return to the Summary Table.

Figure 8-54. PWML11 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_PWMLOWOUT11			
R-0h				R/W-Fh			

Table 8-51. PWML11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3-0	CONF_PWMLOWOUT11	R/W	Fh	PWM Dutycycle Register Setting lower 4 bits for CH11

8.6.1.37 CONF_EN0 Register (Offset = 50h) [reset = 0h]

CONF_EN0 is shown in Figure 8-55 and described in Table 8-52.

Return to the Summary Table.

Channel enable settings for channel 0 to 7.

Figure 8-55. CONF_EN0 Register

7	6	5	4	3	2	1	0
CONF_ENCH7	CONF_ENCH6	CONF_ENCH5	CONF_ENCH4	CONF_ENCH3	CONF_ENCH2	CONF_ENCH1	CONF_ENCH0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-52. CONF_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONF_ENCH7	R/W	0h	Channel 7 enable register. 0h = Disabled 1h = Enabled
6	CONF_ENCH6	R/W	0h	Channel 6 enable register. 0h = Disabled 1h = Enabled
5	CONF_ENCH5	R/W	0h	Channel 5 enable register. 0h = Disabled 1h = Enabled
4	CONF_ENCH4	R/W	0h	Channel 4 enable register. 0h = Disabled 1h = Enabled
3	CONF_ENCH3	R/W	0h	Channel 3 enable register. 0h = Disabled 1h = Enabled
2	CONF_ENCH2	R/W	0h	Channel 2 enable register. 0h = Disabled 1h = Enabled
1	CONF_ENCH1	R/W	0h	Channel 1 enable register. 0h = Disabled 1h = Enabled
0	CONF_ENCH0	R/W	0h	Channel 0 enable register. 0h = Disabled 1h = Enabled

8.6.1.38 CONF_EN1 Register (Offset = 51h) [reset = 0h]

CONF_EN1 is shown in Figure 8-56 and described in Table 8-53.

Return to the Summary Table.

Channel enable settings for channel 8 to 11.

Figure 8-56. CONF_EN1 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_ENCH11	CONF_ENCH10	CONF_ENCH9	CONF_ENCH8
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-53. CONF_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3	CONF_ENCH11	R/W	0h	Channel 11 enable register. 0h = Disabled 1h = Enabled
2	CONF_ENCH10	R/W	0h	Channel 10 enable register. 0h = Disabled 1h = Enabled
1	CONF_ENCH9	R/W	0h	Channel 9 enable register. 0h = Disabled 1h = Enabled
0	CONF_ENCH8	R/W	0h	Channel 8 enable register. 0h = Disabled 1h = Enabled

8.6.1.39 CONF_DIAGEN0 Register (Offset = 54h) [reset = X]

CONF_DIAGEN0 is shown in Figure 8-57 and described in Table 8-54.

Return to the Summary Table.

Output diagnostics enable settings for channel 0 to 7.

Figure 8-57. CONF_DIAGEN0 Register

7	6	5	4	3	2	1	0
CONF_DIAGENCH7	CONF_DIAGENCH6	CONF_DIAGENCH5	CONF_DIAGENCH4	CONF_DIAGENCH3	CONF_DIAGENCH2	CONF_DIAGENCH1	CONF_DIAGENCH0
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 8-54. CONF_DIAGEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONF_DIAGENCH7	R/W	X	Channel 7 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH7 code when reset
6	CONF_DIAGENCH6	R/W	X	Channel 6 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH6 code when reset
5	CONF_DIAGENCH5	R/W	X	Channel 5 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH5 code when reset
4	CONF_DIAGENCH4	R/W	X	Channel 4 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH4 code when reset
3	CONF_DIAGENCH3	R/W	X	Channel 3 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH3 code when reset
2	CONF_DIAGENCH2	R/W	X	Channel 2 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH2 code when reset
1	CONF_DIAGENCH1	R/W	X	Channel 1 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH1 code when reset
0	CONF_DIAGENCH0	R/W	X	Channel 0 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH0 code when reset

8.6.1.40 CONF_DIAGEN1 Register (Offset = 55h) [reset = X]

CONF_DIAGEN1 is shown in Figure 8-58 and described in Table 8-55.

Return to the Summary Table.

Output diagnostics enable settings for channel 8 to 11.

Figure 8-58. CONF_DIAGEN1 Register

7	6	5	4	3	2	1	0
RESERVED				CONF_DIAGENCH11	CONF_DIAGENCH10	CONF_DIAGENCH9	CONF_DIAGENCH8
R-0h				R/W-X	R/W-X	R/W-X	R/W-X

Table 8-55. CONF_DIAGEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3	CONF_DIAGENCH11	R/W	X	Channel 11 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH11 code when reset
2	CONF_DIAGENCH10	R/W	X	Channel 10 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH10 code when reset
1	CONF_DIAGENCH9	R/W	X	Channel 9 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH9 code when reset
0	CONF_DIAGENCH8	R/W	X	Channel 8 diagnostics enable register. 0h = Disabled 1h = Enabled Load EEP_DIAGENCH8 code when reset

8.6.1.41 CONF_MISC0 Register (Offset = 56h) [reset = X]

CONF_MISC0 is shown in Figure 8-59 and described in Table 8-56.

Return to the Summary Table.

Figure 8-59. CONF_MISC0 Register

7	6	5	4	3	2	1	0
CONF_AUTOSS	CONF_LDO	RESERVED	CONF_EXPEN	RESERVED			
R/W-0h	R/W-X	R-0h	R/W-X	R/W-0h			

Table 8-56. CONF_MISC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONF_AUTOSS	R/W	0h	Auto single-LED short-circuit configuration. 0h = Disabled 1h = Enabled
6	CONF_LDO	R/W	X	LDO output voltage setting. 0h = 5.0 V 1h = 4.4 V Load EEP_LDO code when reset
5	RESERVED	R	0h	RESERVED
4	CONF_EXPEN	R/W	X	PWM exponetinal dimming enable register. 0h = Disabled 1h = Enabled Load EEP_EXPEN code when reset
3-0	RESERVED	R/W	0h	RESERVED

8.6.1.42 CONF_MISC1 Register (Offset = 57h) [reset = X]

CONF_MISC1 is shown in Figure 8-60 and described in Table 8-57.

Return to the Summary Table.

Figure 8-60. CONF_MISC1 Register

7	6	5	4	3	2	1	0
CONF_PWMFREQ				RESERVED		CONF_REFRANGE	
R/W-X				R-0h		R/W-X	

Table 8-57. CONF_MISC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CONF_PWMFREQ	R/W	X	PWM frequency selection register 0h = 200 Hz 1h = 250 Hz 2h = 300 Hz 3h = 350 Hz 4h = 400 Hz 5h = 500 Hz 6h = 600 Hz 7h = 800 Hz 8h = 1000 Hz 9h = 1200 Hz Ah = 2 kHz Bh = 4 kHz Ch = 5.9 kHz Dh = 7.8 kHz Eh = 9.6 kHz Fh = 20.8 kHz Load EEP_PWMFREQ data when reset
3-2	RESERVED	R	0h	RESERVED
1-0	CONF_REFRANGE	R/W	X	Reference current ratio setting register 0h = 64 1h = 128 2h = 256 3h = 512 Load EEP_REFRANGE data when reset

8.6.1.43 CONF_MISC2 Register (Offset = 58h) [reset = X]

CONF_MISC2 is shown in Figure 8-61 and described in Table 8-58.

Return to the Summary Table.

Figure 8-61. CONF_MISC2 Register

7	6	5	4	3	2	1	0
RESERVED	CONF_FLTIMEOUT			CONF_ADCLOWSUPTH			
R-0h	R/W-X			R/W-X			

Table 8-58. CONF_MISC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6-4	CONF_FLTIMEOUT	R/W	X	FlexWire timeout timer setting register. 0h = 1 ms 1h = 125 µs 2h = 250 µs 3h = 500 µs 4h = 1.25 ms 5h = 2.5 ms 6h = 5 ms 7h = 10 ms Load EEP_FLTIMEOUT data when reset
3-0	CONF_ADCLOWSUPTH	R/W	X	ADC Supply monitor threshold setting register. 0h = 10 V 1h = 12 V 2h = 14 V 3h = 16 V 4h = 18 V 5h = 20 V 6h = 22 V 7h = 24 V 8h = 26 V 9h = 28 V Ah = 30 V Bh = 32 V Ch = 34 V Dh = 36 V Eh = 38 V Fh = 40 V Load EEP_ADCLOWSUPTH data when reset

8.6.1.44 CONF_MISC3 Register (Offset = 59h) [reset = X]

CONF_MISC3 is shown in Figure 8-62 and described in Table 8-59.

Return to the Summary Table.

Figure 8-62. CONF_MISC3 Register

7	6	5	4	3	2	1	0
CONF_ODIOUT				CONF_ODPW			
R/W-X				R/W-X			

Table 8-59. CONF_MISC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CONF_ODIOUT	R/W	X	On-demand diagnostics output current setting register. 0x0 to 0xE: IOUT = (CONF_ODIOUT*4+1)/64*I(FULL_RANGE) 0xF: ODIOUT is using its channel setting current Load EEP_ODIOUT data when reset
3-0	CONF_ODPW	R/W	X	On-demand diagnostics pulse-width setting EEPROM register. 0h = 100 µs 1h = 20 µs 2h = 30 µs 3h = 50 µs 4h = 80 µs 5h = 150 µs 6h = 200 µs 7h = 300 µs 8h = 500 µs 9h = 800 µs Ah = 1 ms Bh = 1.2 ms Ch = 1.5 ms Dh = 2 ms Eh = 3 ms Fh = 5 ms Load EEP_ODPW data when reset

8.6.1.45 CONF_MISC4 Register (Offset = 5Ah) [reset = X]

CONF_MISC4 is shown in Figure 8-63 and described in Table 8-60.

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Figure 8-63. CONF_MISC4 Register

7	6	5	4	3	2	1	0
CONF_WDTIMER				RESERVED			
R/W-X				R-0h			

Table 8-60. CONF_MISC4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CONF_WDTIMER	R/W	X	Watchdog timer setting EEPROM register. 0h = Disabled, do not automatically enter fail-safe state 1h = 200 µs 2h = 500 µs 3h = 1 ms 4h = 2 ms 5h = 5 ms 6h = 10 ms 7h = 20 ms 8h = 50 ms 9h = 100 ms Ah = 200 ms Bh = 500 ms Ch = 0 µs; direct enter fail-safe state Dh = 0 µs; direct enter fail-safe state Eh = 0 µs; direct enter fail-safe state Fh = 0 µs; direct enter fail-safe state Load EEP_WDTIMER data when reset
3-0	RESERVED	R	0h	RESERVED

8.6.1.46 CONF_MISC5 Register (Offset = 5Bh) [reset = X]

CONF_MISC5 is shown in Figure 8-64 and described in Table 8-61.

Return to the Summary Table.

Figure 8-64. CONF_MISC5 Register

7	6	5	4	3	2	1	0
CONF_ADCSHORTTH							
R/W-X							

Table 8-61. CONF_MISC5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_ADCSHORTTH	R/W	X	ADC short detection threshold setting register. Load EEP_ADCSHORTTH data when rest

8.6.1.47 CLR Register (Offset = 60h) [reset = 0h]

CLR is shown in Figure 8-65 and described in Table 8-62.

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Configuration register for register clear and state configuration

Figure 8-65. CLR Register

7	6	5	4	3	2	1	0
RESERVED		CONF_FORCEFS	CLR_REG	CONF_FORCEERR	CLR_FS	CLR_FAULT	CLR_POR
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-62. CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5	CONF_FORCEFS	R/W	0h	Write 1 to force device into Fail-safe state from normal state, automatically reset to 0.
4	CLR_REG	R/W	0h	Write 1 to clear device register settings to default values, automatically reset to 0.
3	CONF_FORCEERR	R/W	0h	Write 1 to force error setting register, automatically reset to 0. 0x0: $\overline{ERR}$ output = HIGH 0x1: $\overline{ERR}$ output = LOW;
2	CLR_FS	R/W	0h	Write to force the device out of Fail-safe states to normal state, automatically reset to 0.
1	CLR_FAULT	R/W	0h	Write 1 to clear all fault flags, automatically reset to 0.
0	CLR_POR	R/W	0h	Write 1 to clear POR flag, automatically reset to 0.

8.6.1.48 CONF_LOCK Register (Offset = 61h) [reset = Fh]

CONF_LOCK is shown in Figure 8-66 and described in Table 8-63.

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Configuration register for register lock configuration

Figure 8-66. CONF_LOCK Register

7	6	5	4	3	2	1	0
RESERVED				CONF_CLRLOCK	CONF_CONFLOCK	CONF_IOUTLOCK	CONF_PWMLOCK
R-0h				R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 8-63. CONF_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3	CONF_CLRLOCK	R/W	1h	CLR register (address 60h) lock bit 0x0: CLR register write-protect disabled. 0x1: CLR register write-protected enabled.
2	CONF_CONFLOCK	R/W	1h	Configuration (CONF_x) registers lock bit 0x0: Configuration setting register write-protect disabled 0x1: Configuration setting register write-protected enabled
1	CONF_IOUTLOCK	R/W	1h	IOUT registers (CONF_IOUTx) lock bit 0x0: Output current setting register write-protect disabled 0x1: Output current setting register write-protected enabled.
0	CONF_PWMLOCK	R/W	1h	PMW dutycyle registers (CONF_PWMOUTx +CONF_PWMLOWOUTx) lock bit 0x0: PWM Register write-protect disabled 0x1: PWM Register write-protected enabled.

8.6.1.49 CONF_MISC6 Register (Offset = 62h) [reset = 0h]

CONF_MISC6 is shown in Figure 8-67 and described in Table 8-64.

Return to the Summary Table.

Figure 8-67. CONF_MISC6 Register

7	6	5	4	3	2	1	0
CONF_STAYINEEP	CONF_EEPREADBACK	RESERVED	CONF_ADCCH				
R/W-0h	R/W-0h	R-0h	R/W-0h				

Table 8-64. CONF_MISC6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONF_STAYINEEP	R/W	0h	Stay in EEPROM state setting. 0h = EEPROM mode disabled 1h = EEPROM mode enableds
6	CONF_EEPREADBACK	R/W	0h	Setting this bit allow EEPROM to overwrite configuration registers. Automatically returns to 0.
5	RESERVED	R	0h	RESERVED
4-0	CONF_ADCCH	R/W	0h	ADC Channel Selection Register, write this channel will automatically initiate ADC conversion.

8.6.1.50 CONF_MISC7 Register (Offset = 63h) [reset = 0h]

CONF_MISC7 is shown in Figure 8-68 and described in Table 8-65.

Return to the Summary Table.

Figure 8-68. CONF_MISC7 Register

7	6	5	4	3	2	1	0
RESERVED		CONF_EXTCLK	CONF_SHAREPWM	RESERVED		CONF_READSHADOW	CONF_EEPMODE
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 8-65. CONF_MISC7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	CONF_EXTCLK	R/W	0h	External CLK selection 0x0: Use internal clock source for PWM generator 0x1: Use external clock source for PWM generator
4	CONF_SHAREPWM	R/W	0h	Setting all channel PWM dutycycle to be same as CH0 0x0: All channel PWM dutycycle is set independently 0x1: All channel PWM dutycycle is the same as CH0
3-2	RESERVED	R	0h	Reserved
1	CONF_READSHADOW	R/W	0h	Setting EEPROM read back source. 0x0: From EEPROM 0x1: From EEPROM shadow registers
0	CONF_EEPMODE	R/W	0h	EEPROM Programming State Setting. 0x0: Disable EEPMODE Programming State 0x1: Enable EEPMODE Programming State

8.6.1.51 CONF_MISC8 Register (Offset = 64h) [reset = 0h]

CONF_MISC8 is shown in Figure 8-69 and described in Table 8-66.

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Figure 8-69. CONF_MISC8 Register

7	6	5	4	3	2	1	0
CONF_MASKREF	CONF_MASKCRC	CONF_MASKSHORT	CONF_MASKOPEN	CONF_MASKTSD	CONF_EEPPROG	CONF_SSSTART	CONF_INVDIAGSTART
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-66. CONF_MISC8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONF_MASKREF	R/W	0h	Reference fault mask register. 0x0: Reference fault will be reported to $\overline{ERR}$ output 0x1: Reference fault will not be reported to $\overline{ERR}$ output
6	CONF_MASKCRC	R/W	0h	CRC fault mask register. 0x0: CRC fault will be reported to $\overline{ERR}$ output 0x1: CRC fault will not be reported to $\overline{ERR}$ output
5	CONF_MASKSHORT	R/W	0h	SHORT fault mask register. 0x0: Short-circuit fault will be reported to $\overline{ERR}$ output. 0x1: Short-circuit fault will not be reported to $\overline{ERR}$ output;
4	CONF_MASKOPEN	R/W	0h	OPEN fault mask register. 0x0: Open-circuit fault will be reported to $\overline{ERR}$ output 0x1: Open-circuit fault will not be reported to $\overline{ERR}$ output
3	CONF_MASKTSD	R/W	0h	Over temperature shutdown mask to $\overline{ERR}$ output. 0x0: TSD Fault unmasked to $\overline{ERR}$ output 0x1: TSD Fault masked to $\overline{ERR}$ output, output will be shutdown
2	CONF_EEPPROG	R/W	0h	EEPROM burning start in EEPROM mode only, automatically returns to 0
1	CONF_SSSTART	R/W	0h	Single LED Short diagnostics start, automatically returns to 0
0	CONF_INVDIAGSTART	R/W	0h	Invisible Diagnostics start, automatically returns to 0

8.6.1.52 CONF_MISC9 Register (Offset = 65h) [reset = 0h]

CONF_MISC9 is shown in Figure 8-70 and described in Table 8-67.

Return to the Summary Table.

Figure 8-70. CONF_MISC9 Register

7	6	5	4	3	2	1	0
CONF_EEPGATE							
R/W-0h							

Table 8-67. CONF_MISC9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CONF_EEPGATE	R/W	0h	EEPROM Gate for Access Password

8.6.1.53 FLAG0 Register (Offset = 70h) [reset = 3h]

FLAG0 is shown in Figure 8-71 and described in Table 8-68.

Return to the Summary Table.

Users read this register to understand if the device is working properly. It includes general fault flags, power, temperature, output failures.

Figure 8-71. FLAG0 Register

7	6	5	4	3	2	1	0
RESERVED	FLAG_REF	FLAG_FS	FLAG_OUT	FLAG_PRETSD	FLAG_TSD	FLAG_POR	FLAG_ERR
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-1h

Table 8-68. FLAG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	FLAG_REF	R	0h	Reference fault flag. 0x0: No reference fault is detected. 0x1: Device has reference fault.
5	FLAG_FS	R	0h	Fail-safe flag. 0x0: Device is not in fail-safe mode. 0x1: Device is in fail-safe mode.
4	FLAG_OUT	R	0h	Output fault flag. 0x0: No fault is detected on output channels. 0x1: Device has at least one fault detected on output channels.
3	FLAG_PRETSD	R	0h	Overtemperature pre-shut down flag. 0x0: No over-temperature pre-shutdown is detected. 0x1: Device has triggered over temperature pre-shutdown threshold.
2	FLAG_TSD	R	0h	Overtemperature shut down flag. 0x0: No over-temperature shutdown is detected. 0x1: Device has triggered over temperature shutdown.
1	FLAG_POR	R	1h	Power-on-reset flag. 0x0: No power-on-reset 0x1: Power-on-reset triggered Write 1 to CLEAR_POR will clear the bit
0	FLAG_ERR	R	1h	Error output flag. 0x0: No error flag 0x1: Device has at least one error flag

8.6.1.54 FLAG1 Register (Offset = 71h) [reset = X]

FLAG1 is shown in Figure 8-72 and described in Table 8-69.

Return to the Summary Table.

Users read this register to understand if the device is working properly. It includes general fault flags, power, temperature, output failures.

Figure 8-72. FLAG1 Register

7	6	5	4	3	2	1	0
RESERVED		FLAG_EXTFS	FLAG_PROGREADY	FLAG_ADCLOWSUP	FLAG_ADCDONE	FLAG_ODREADY	FLAG_EEPCRC
R-0h		R-X	R-0h	R-0h	R-0h	R-0h	R-X

Table 8-69. FLAG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5	FLAG_EXTFS	R	X	FS pin voltage indicator 0x0: FS pin voltage is logic low 0x1: FS pin voltage is logic high
4	FLAG_PROGREADY	R	0h	EEPROM burning completion flag. 0x0: EEPROM burning not completed or not started 0x1: EEPROM burning completed
3	FLAG_ADCLOWSUP	R	0h	Flag for low supply voltage detection. 0x0: Supply is above preset ADC threshold 0x1: Supply has dropped below preset ADC threshold.
2	FLAG_ADCDONE	R	0h	Flag for ADC conversion completition. 0x0: ADC data not available. 0x1: ADC data available with conversion completed, read ADC_OUT to clear FLAG_ADCDONE.
1	FLAG_ODREADY	R	0h	Flag for on-demand diagnostics. 0x0: on-demand diagnostics not completed or not started. 0x1: on-demand diagnostics completed.
0	FLAG_EEPCRC	R	X	Flag for EEPROM CRC check failure. 0x0: EEPROM CRC passes 0x1: EEPROM CRC check fails

8.6.1.55 FLAG2 Register (Offset = 72h) [reset = X]

FLAG2 is shown in Figure 8-73 and described in Table 8-70.

Return to the Summary Table.

ADC conversion output register for supply

Figure 8-73. FLAG2 Register

7	6	5	4	3	2	1	0
ADC_SUPPLY							
R-X							

Table 8-70. FLAG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADC_SUPPLY	R	X	ADC conversion output register for supply

8.6.1.56 FLAG3 Register (Offset = 73h) [reset = 0h]

FLAG3 is shown in Figure 8-74 and described in Table 8-71.

Return to the Summary Table.

ADC Conversion Output

Figure 8-74. FLAG3 Register

7	6	5	4	3	2	1	0
ADC_OUT							
R-0h							

Table 8-71. FLAG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADC_OUT	R	0h	ADC Conversion output register

8.6.1.57 FLAG4 Register (Offset = 74h) [reset = 0h]

FLAG4 is shown in Figure 8-75 and described in Table 8-72.

Return to the Summary Table.

Users read this register to understand if there is any LED open-circuit, LED short-circuit or Single-LED short-circuit fault detected after on-demand diagnostics.

Figure 8-75. FLAG4 Register

7	6	5	4	3	2	1	0
FLAG_ODDIAG CH7	FLAG_ODDIAG CH6	FLAG_ODDIAG CH5	FLAG_ODDIAG CH4	FLAG_ODDIAG CH3	FLAG_ODDIAG CH2	FLAG_ODDIAG CH1	FLAG_ODDIAG CH0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-72. FLAG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FLAG_ODDIAGCH7	R	0h	Channel 7 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
6	FLAG_ODDIAGCH6	R	0h	Channel 6 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
5	FLAG_ODDIAGCH5	R	0h	Channel 5 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
4	FLAG_ODDIAGCH4	R	0h	Channel 4 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
3	FLAG_ODDIAGCH3	R	0h	Channel 3 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
2	FLAG_ODDIAGCH2	R	0h	Channel 2 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
1	FLAG_ODDIAGCH1	R	0h	Channel 1 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
0	FLAG_ODDIAGCH0	R	0h	Channel 0 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected

8.6.1.58 FLAG5 Register (Offset = 75h) [reset = 0h]

FLAG5 is shown in Figure 8-76 and described in Table 8-73.

Return to the Summary Table.

Users read this register to understand if there is any LED open-circuit, LED short-circuit or Single-LED short-circuit fault detected after on-demand diagnostics.

Figure 8-76. FLAG5 Register

7	6	5	4	3	2	1	0
RESERVED				FLAG_ODDIAGCH11	FLAG_ODDIAGCH10	FLAG_ODDIAGCH9	FLAG_ODDIAGCH8
R-0h				R-0h	R-0h	R-0h	R-0h

Table 8-73. FLAG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3	FLAG_ODDIAGCH11	R	0h	Channel 11 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
2	FLAG_ODDIAGCH10	R	0h	Channel 10 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
1	FLAG_ODDIAGCH9	R	0h	Channel 9 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected
0	FLAG_ODDIAGCH8	R	0h	Channel 8 on-demand diagnostics fault flag bit. 0x0: on-demand diagnostics fault not detected 0x1: on-demand diagnostics fault detected

8.6.1.59 FLAG7 Register (Offset = 77h) [reset = EFh]

FLAG7 is shown in Figure 8-77 and described in Table 8-74.

Return to the Summary Table.

EEPROM CRC check reference should be burnt in the end of production line if any EEPROM register is changed.

Figure 8-77. FLAG7 Register

7	6	5	4	3	2	1	0
CALC_EEPCRC							
R-B3h							

Table 8-74. FLAG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CALC_EEPCRC	R	B3h	EEPROM CRC reference Reset value is 09h for TPS929121A version

8.6.1.60 FLAG8 Register (Offset = 78h) [reset = X]

FLAG8 is shown in Figure 8-78 and described in Table 8-75.

Return to the Summary Table.

Calculated CRC result

Figure 8-78. FLAG8 Register

7	6	5	4	3	2	1	0
CALC_CONFCRC							
R-X							

Table 8-75. FLAG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CALC_CONFCRC	R	X	Calculated CRC result for all CONFx registers

8.6.1.61 FLAG11 Register (Offset = 7Bh) [reset = 0h]

FLAG11 is shown in Figure 8-79 and described in Table 8-76.

Return to the Summary Table.

Users read this register to understand if there is any LED open-circuit fault detected.

Figure 8-79. FLAG11 Register

7	6	5	4	3	2	1	0
FLAG_OPENCH7	FLAG_OPENCH6	FLAG_OPENCH5	FLAG_OPENCH4	FLAG_OPENCH3	FLAG_OPENCH2	FLAG_OPENCH1	FLAG_OPENCH0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-76. FLAG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FLAG_OPENCH7	R	0h	Channel 7 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
6	FLAG_OPENCH6	R	0h	Channel 6 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
5	FLAG_OPENCH5	R	0h	Channel 5 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
4	FLAG_OPENCH4	R	0h	Channel 4 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
3	FLAG_OPENCH3	R	0h	Channel 3 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
2	FLAG_OPENCH2	R	0h	Channel 2 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
1	FLAG_OPENCH1	R	0h	Channel 1 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
0	FLAG_OPENCH0	R	0h	Channel 1 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected

8.6.1.62 FLAG12 Register (Offset = 7Ch) [reset = 0h]

FLAG12 is shown in Figure 8-80 and described in Table 8-77.

Return to the Summary Table.

Users read this register to understand if there is any LED open-circuit fault detected.

Figure 8-80. FLAG12 Register

7	6	5	4	3	2	1	0
RESERVED				FLAG_OPENCH11	FLAG_OPENCH10	FLAG_OPENCH9	FLAG_OPENCH8
R-0h				R-0h	R-0h	R-0h	R-0h

Table 8-77. FLAG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3	FLAG_OPENCH11	R	0h	Channel 11 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
2	FLAG_OPENCH10	R	0h	Channel 10 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
1	FLAG_OPENCH9	R	0h	Channel 9 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected
0	FLAG_OPENCH8	R	0h	Channel 8 open-circuit fault flag bit. 0x0: open-circuit fault not detected 0x1: open-circuit fault detected

8.6.1.63 FLAG13 Register (Offset = 7Dh) [reset = 0h]

FLAG13 is shown in Figure 8-81 and described in Table 8-78.

Return to the Summary Table.

Users read this register to understand if there is any LED short-circuit fault detected.

Figure 8-81. FLAG13 Register

7	6	5	4	3	2	1	0
FLAG_SHORT CH7	FLAG_SHORT CH6	FLAG_SHORT CH5	FLAG_SHORT CH4	FLAG_SHORT CH3	FLAG_SHORT CH2	FLAG_SHORT CH1	FLAG_SHORT CH0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-78. FLAG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FLAG_SHORTCH7	R	0h	Channel 7 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected
6	FLAG_SHORTCH6	R	0h	Channel 6 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected
5	FLAG_SHORTCH5	R	0h	Channel 5 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected
4	FLAG_SHORTCH4	R	0h	Channel 4 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected
3	FLAG_SHORTCH3	R	0h	Channel 3 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected
2	FLAG_SHORTCH2	R	0h	Channel 2 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected
1	FLAG_SHORTCH1	R	0h	Channel 1 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected
0	FLAG_SHORTCH0	R	0h	Channel 0 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected

8.6.1.64 FLAG14 Register (Offset = 7Eh) [reset = 0h]

FLAG14 is shown in Figure 8-82 and described in Table 8-79.

Return to the Summary Table.

Users read this register to understand if there is any LED short-circuit fault detected.

Figure 8-82. FLAG14 Register

7	6	5	4	3	2	1	0
RESERVED				FLAG_SHORTCH11	FLAG_SHORTCH10	FLAG_SHORTCH9	FLAG_SHORTCH8
R-0h				R-0h	R-0h	R-0h	R-0h

Table 8-79. FLAG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3	FLAG_SHORTCH11	R	0h	Channel 11 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected
2	FLAG_SHORTCH10	R	0h	Channel 10 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected
1	FLAG_SHORTCH9	R	0h	Channel 9 short-circuit fault flag bit. 0b: short-circuit fault not detected 0x1: short-circuit fault detected
0	FLAG_SHORTCH8	R	0h	Channel 8 short-circuit fault flag bit. 0x0: short-circuit fault not detected 0x1: short-circuit fault detected

8.6.1.65 EEPI0 Register (Offset = 80h) [reset = 3Fh]

EEPI0 is shown in Figure 8-83 and described in Table 8-80.

Return to the Summary Table.

EEPROM Output Current Setting for CH0

Figure 8-83. EEPI0 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT0					
R-0h		R/W-3Fh					

Table 8-80. EEPI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT0	R/W	3Fh	Output current setting for OUT0

8.6.1.66 EEPI1 Register (Offset = 81h) [reset = 3Fh]

EEPI1 is shown in Figure 8-84 and described in Table 8-81.

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EEPROM Output Current Setting for CH1

Figure 8-84. EEPI1 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT1					
R-0h		R/W-3Fh					

Table 8-81. EEPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT1	R/W	3Fh	Output current setting for OUT1

8.6.1.67 EEPI2 Register (Offset = 82h) [reset = 3Fh]

EEPI2 is shown in Figure 8-85 and described in Table 8-82.

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EEPROM Output Current Setting for CH2

Figure 8-85. EEPI2 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT2					
R-0h		R/W-3Fh					

Table 8-82. EEPI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT2	R/W	3Fh	Output current setting for OUT2

8.6.1.68 EEPI3 Register (Offset = 83h) [reset = 3Fh]

EEPI3 is shown in Figure 8-86 and described in Table 8-83.

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EEPROM Output Current Setting for CH3

Figure 8-86. EEPI3 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT3					
R-0h		R/W-3Fh					

Table 8-83. EEPI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT3	R/W	3Fh	Output current setting for OUT3

8.6.1.69 EEPI4 Register (Offset = 84h) [reset = 3Fh]

EEPI4 is shown in Figure 8-87 and described in Table 8-84.

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EEPROM Output Current Setting for CH4

Figure 8-87. EEPI4 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT4					
R-0h		R/W-3Fh					

Table 8-84. EEPI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT4	R/W	3Fh	Output current setting for OUT4

8.6.1.70 EEPI5 Register (Offset = 85h) [reset = 3Fh]

EEPI5 is shown in Figure 8-88 and described in Table 8-85.

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EEPROM Output Current Setting for CH5

Figure 8-88. EEPI5 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT5					
R-0h		R/W-3Fh					

Table 8-85. EEPI5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT5	R/W	3Fh	Output current setting for OUT5

8.6.1.71 EEPI6 Register (Offset = 86h) [reset = 3Fh]

EEPI6 is shown in Figure 8-89 and described in Table 8-86.

Return to the Summary Table.

EEPROM Output Current Setting for CH6

Figure 8-89. EEPI6 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT6					
R-0h		R/W-3Fh					

Table 8-86. EEPI6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT6	R/W	3Fh	Output current setting for OUT6

8.6.1.72 EEPI7 Register (Offset = 87h) [reset = 3Fh]

EEPI7 is shown in Figure 8-90 and described in Table 8-87.

Return to the Summary Table.

EEPROM Output Current Setting for CH7

Figure 8-90. EEPI7 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT7					
R-0h		R/W-3Fh					

Table 8-87. EEPI7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT7	R/W	3Fh	Output current setting for OUT7

8.6.1.73 EEPI8 Register (Offset = 88h) [reset = 3Fh]

EEPI8 is shown in Figure 8-91 and described in Table 8-88.

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EEPROM Output Current Setting for CH8

Figure 8-91. EEPI8 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT8					
R-0h		R/W-3Fh					

Table 8-88. EEPI8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT8	R/W	3Fh	Output current setting for OUT8

8.6.1.74 EEPI9 Register (Offset = 89h) [reset = 3Fh]

EEPI9 is shown in Figure 8-92 and described in Table 8-89.

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EEPROM Output Current Setting for CH9

Figure 8-92. EEPI9 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT9					
R-0h		R/W-3Fh					

Table 8-89. EEPI9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT9	R/W	3Fh	Output current setting for OUT9

8.6.1.75 EEPI10 Register (Offset = 8Ah) [reset = 3Fh]

EEPI10 is shown in Figure 8-93 and described in Table 8-90.

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EEPROM Output Current Setting for CH10

Figure 8-93. EEPI10 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT10					
R-0h		R/W-3Fh					

Table 8-90. EEPI10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT10	R/W	3Fh	Output current setting for OUT10

8.6.1.76 EEPI11 Register (Offset = 8Bh) [reset = 3Fh]

EEPI11 is shown in Figure 8-94 and described in Table 8-91.

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EEPROM Output Current Setting for CH11

Figure 8-94. EEPI11 Register

7	6	5	4	3	2	1	0
RESERVED		EEP_IOUT11					
R-0h		R/W-3Fh					

Table 8-91. EEPI11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-0	EEP_IOUT11	R/W	3Fh	Output current setting for OUT11

8.6.1.77 EEPP0 Register (Offset = A0h) [reset = FFh]

EEPP0 is shown in Figure 8-95 and described in Table 8-92.

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EEPROM Output PWM Duty-cycle Setting for CH0

Figure 8-95. EEPP0 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT0							
R/W-FFh							

Table 8-92. EEPP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT0	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH0

8.6.1.78 EEPP1 Register (Offset = A1h) [reset = FFh]

EEPP1 is shown in Figure 8-96 and described in Table 8-93.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH1

Figure 8-96. EEPP1 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT1							
R/W-FFh							

Table 8-93. EEPP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT1	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH1

8.6.1.79 EEPP2 Register (Offset = A2h) [reset = FFh]

EEPP2 is shown in Figure 8-97 and described in Table 8-94.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH2

Figure 8-97. EEPP2 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT2							
R/W-FFh							

Table 8-94. EEPP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT2	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH2

8.6.1.80 EEPP3 Register (Offset = A3h) [reset = FFh]

EEPP3 is shown in Figure 8-98 and described in Table 8-95.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH3

Figure 8-98. EEPP3 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT3							
R/W-FFh							

Table 8-95. EEPP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT3	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH3

8.6.1.81 EEPP4 Register (Offset = A4h) [reset = FFh]

EEPP4 is shown in Figure 8-99 and described in Table 8-96.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH4

Figure 8-99. EEPP4 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT4							
R/W-FFh							

Table 8-96. EEPP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT4	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH4

8.6.1.82 EEPP5 Register (Offset = A5h) [reset = FFh]

EEPP5 is shown in Figure 8-100 and described in Table 8-97.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH5

Figure 8-100. EEPP5 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT5							
R/W-FFh							

Table 8-97. EEPP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT5	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH5

8.6.1.83 EEPP6 Register (Offset = A6h) [reset = FFh]

EEPP6 is shown in Figure 8-101 and described in Table 8-98.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH6

Figure 8-101. EEPP6 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT6							
R/W-FFh							

Table 8-98. EEPP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT6	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH6

8.6.1.84 EEPP7 Register (Offset = A7h) [reset = FFh]

EEPP7 is shown in Figure 8-102 and described in Table 8-99.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH7

Figure 8-102. EEPP7 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT7							
R/W-FFh							

Table 8-99. EEPP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT7	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH7

8.6.1.85 EEPP8 Register (Offset = A8h) [reset = FFh]

EEPP8 is shown in Figure 8-103 and described in Table 8-100.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH8

Figure 8-103. EEPP8 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT8							
R/W-FFh							

Table 8-100. EEPP8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT8	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH8

8.6.1.86 EEPP9 Register (Offset = A9h) [reset = FFh]

EEPP9 is shown in Figure 8-104 and described in Table 8-101.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH9

Figure 8-104. EEPP9 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT9							
R/W-FFh							

Table 8-101. EEPP9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT9	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH9

8.6.1.87 EEPP10 Register (Offset = AAh) [reset = FFh]

EEPP10 is shown in Figure 8-105 and described in Table 8-102.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH10

Figure 8-105. EEPP10 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT10							
R/W-FFh							

Table 8-102. EEPP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT10	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH10

8.6.1.88 EEPP11 Register (Offset = ABh) [reset = FFh]

EEPP11 is shown in Figure 8-106 and described in Table 8-103.

Return to the Summary Table.

EEPROM Output PWM Duty-cycle Setting for CH11

Figure 8-106. EEPP11 Register

7	6	5	4	3	2	1	0
EEP_PWMOUT11							
R/W-FFh							

Table 8-103. EEPP11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_PWMOUT11	R/W	FFh	PWM Dutycycle EEPROM Register Setting for CH11

8.6.1.89 EEPM0 Register (Offset = C0h) [reset = 0h]

EEPM0 is shown in Figure 8-107 and described in Table 8-104.

Return to the Summary Table.

Channel enable setting in fail-safe state 0 for channel 0 to 7.

Figure 8-107. EEPM0 Register

7	6	5	4	3	2	1	0
EEP_FS0CH7	EEP_FS0CH6	EEP_FS0CH5	EEP_FS0CH4	EEP_FS0CH3	EEP_FS0CH2	EEP_FS0CH1	EEP_FS0CH0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-104. EEPM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EEP_FS0CH7	R/W	0h	CH7 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
6	EEP_FS0CH6	R/W	0h	CH6 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
5	EEP_FS0CH5	R/W	0h	CH5 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
4	EEP_FS0CH4	R/W	0h	CH4 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
3	EEP_FS0CH3	R/W	0h	CH3 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
2	EEP_FS0CH2	R/W	0h	CH2 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
1	EEP_FS0CH1	R/W	0h	CH1 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
0	EEP_FS0CH0	R/W	0h	CH0 setting in fail-safe state 0. 0h = Disabled 1h = Enabled

8.6.1.90 EEPM1 Register (Offset = C1h) [reset = 0h]

EEPM1 is shown in Figure 8-108 and described in Table 8-105.

Return to the Summary Table.

Channel enable setting in fail-safe state 0 for channel 8 to 11.

Figure 8-108. EEPM1 Register

7	6	5	4	3	2	1	0
RESERVED				EEP_FS0CH11	EEP_FS0CH10	EEP_FS0CH9	EEP_FS0CH8
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-105. EEPM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3	EEP_FS0CH11	R/W	0h	CH11 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
2	EEP_FS0CH10	R/W	0h	CH10 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
1	EEP_FS0CH9	R/W	0h	CH9 setting in fail-safe state 0. 0h = Disabled 1h = Enabled
0	EEP_FS0CH8	R/W	0h	CH8 setting in fail-safe state 0. 0h = Disabled 1h = Enabled

8.6.1.91 EEPM2 Register (Offset = C2h) [reset = FFh]

EEPM2 is shown in Figure 8-109 and described in Table 8-106.

Return to the Summary Table.

Channel enable setting in fail-safe state 1 for channel 0 to 7.

Figure 8-109. EEPM2 Register

7	6	5	4	3	2	1	0
EEP_FS1CH7	EEP_FS1CH6	EEP_FS1CH5	EEP_FS1CH4	EEP_FS1CH3	EEP_FS1CH2	EEP_FS1CH1	EEP_FS1CH0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 8-106. EEPM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EEP_FS1CH7	R/W	1h	CH7 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
6	EEP_FS1CH6	R/W	1h	CH6 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
5	EEP_FS1CH5	R/W	1h	CH5 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
4	EEP_FS1CH4	R/W	1h	CH4 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
3	EEP_FS1CH3	R/W	1h	CH3 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
2	EEP_FS1CH2	R/W	1h	CH2 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
1	EEP_FS1CH1	R/W	1h	CH1 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
0	EEP_FS1CH0	R/W	1h	CH0 setting in fail-safe state 1. 0h = Disabled 1h = Enabled

8.6.1.92 EEPM3 Register (Offset = C3h) [reset = Fh]

EEPM3 is shown in Figure 8-110 and described in Table 8-107.

Return to the Summary Table.

Channel enable setting in fail-safe state 1 for channel 8 to 11.

Figure 8-110. EEPM3 Register

7	6	5	4	3	2	1	0
RESERVED				EEP_FS1CH11	EEP_FS1CH10	EEP_FS1CH9	EEP_FS1CH8
R-0h				R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 8-107. EEPM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3	EEP_FS1CH11	R/W	1h	CH11 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
2	EEP_FS1CH10	R/W	1h	CH10 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
1	EEP_FS1CH9	R/W	1h	CH9 setting in fail-safe state 1. 0h = Disabled 1h = Enabled
0	EEP_FS1CH8	R/W	1h	CH8 setting in fail-safe state 1. 0h = Disabled 1h = Enabled

8.6.1.93 EEPM4 Register (Offset = C4h) [reset = FFh]

EEPM4 is shown in Figure 8-111 and described in Table 8-108.

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Figure 8-111. EEPM4 Register

7	6	5	4	3	2	1	0
EEP_DIAGENCH7	EEP_DIAGENCH6	EEP_DIAGENCH5	EEP_DIAGENCH4	EEP_DIAGENCH3	EEP_DIAGENCH2	EEP_DIAGENCH1	EEP_DIAGENCH0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 8-108. EEPM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EEP_DIAGENCH7	R/W	1h	Channel 7 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
6	EEP_DIAGENCH6	R/W	1h	Channel 6 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
5	EEP_DIAGENCH5	R/W	1h	Channel 5 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
4	EEP_DIAGENCH4	R/W	1h	Channel 4 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
3	EEP_DIAGENCH3	R/W	1h	Channel 3 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
2	EEP_DIAGENCH2	R/W	1h	Channel 2 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
1	EEP_DIAGENCH1	R/W	1h	Channel 1 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
0	EEP_DIAGENCH0	R/W	1h	Channel 0 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled

8.6.1.94 EEPM5 Register (Offset = C5h) [reset = Fh]

EEPM5 is shown in Figure 8-112 and described in Table 8-109.

Return to the Summary Table.

Figure 8-112. EEPM5 Register

7	6	5	4	3	2	1	0
RESERVED				EEP_DIAGENCH11	EEP_DIAGENCH10	EEP_DIAGENCH9	EEP_DIAGENCH8
R-0h				R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 8-109. EEPM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	RESERVED
3	EEP_DIAGENCH11	R/W	1h	Channel 11 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
2	EEP_DIAGENCH10	R/W	1h	Channel 10 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
1	EEP_DIAGENCH9	R/W	1h	Channel 9 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled
0	EEP_DIAGENCH8	R/W	1h	Channel 8 diagnostics enable EEPROM register. 0h = Disabled 1h = Enabled

8.6.1.95 EEPM6 Register (Offset = C6h) [reset = 0h]

EEPM6 is shown in Figure 8-113 and described in Table 8-110.

Return to the Summary Table.

Figure 8-113. EEPM6 Register

7	6	5	4	3	2	1	0
RESERVED	EEP_LDO	RESERVED	EEP_EXPEN	EEP_DEVADDR			
R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h			

Table 8-110. EEPM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	EEP_LDO	R/W	0h	LDO output voltage setting. 0h = 5.0 V 1h = 4.4 V
5	RESERVED	R	0h	RESERVED
4	EEP_EXPEN	R/W	0h	PWM generator exponetinal dimmng enable register. 0h = Disabled 1h = Enabled
3-0	EEP_DEVADDR	R/W	0h	Device slave address EEPROM register 0h = slave address is 0000b 1h = slave address is 0001b 2h = slave address is 0010b 3h = slave address is 0011b 4h = slave address is 0100b 5h = slave address is 0101b 6h = slave address is 0110b 7h = slave address is 0111b 8h = slave address is 1000b 9h = slave address is 1001b Ah = slave address is 1010b Bh = slave address is 1011b Ch = slave address is 1100b Dh = slave address is 1101b Eh = slave address is 1110b Fh = slave address is 1111b Reset value is 8h for TPS929121A version

8.6.1.96 EEPM7 Register (Offset = C7h) [reset = A7h]

EEPM7 is shown in Figure 8-114 and described in Table 8-111.

Return to the Summary Table.

Figure 8-114. EEPM7 Register

7	6	5	4	3	2	1	0
EEP_PWMFREQ				EEP_INTADDR	EEP_OFAF	EEP_REFRANGE	
R/W-Ah				R/W-0h	R/W-1h	R/W-3h	

Table 8-111. EEPM7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	EEP_PWMFREQ	R/W	Ah	PWM frequency selection EEPROM register 0h = 200 Hz 1h = 250 Hz 2h = 300 Hz 3h = 350 Hz 4h = 400 Hz 5h = 500 Hz 6h = 600 Hz 7h = 800 Hz 8h = 1000 Hz 9h = 1200 Hz Ah = 2 kHz Bh = 4 kHz Ch = 5.9 kHz Dh = 7.8 kHz Eh = 9.6 kHz Fh = 20.8 kHz
3	EEP_INTADDR	R/W	0h	Slave address selection bit. 0x0: Deivce slave address set by ADDR2/ADDR1/ADDR0 pins configuration 0x1: Device slave address set by EEP_DEVADDR EEPROM register
2	EEP_OFAF	R/W	1h	Output failure state setting. 0x0: One-fails-others-on. 0x1: One-fails-all-fail.
1-0	EEP_REFRANGE	R/W	3h	Reference current ratio setting EEPROM register 0h = 64 1h = 128 2h = 256 3h = 512

8.6.1.97 EEPM8 Register (Offset = C8h) [reset = 3h]

EEPM8 is shown in Figure 8-115 and described in Table 8-112.

Return to the Summary Table.

Figure 8-115. EEPM8 Register

7	6	5	4	3	2	1	0
RESERVED	EEP_FLTIMEOUT			EEP_ADCLOWSUPTH			
R-0h	R/W-0h			R/W-3h			

Table 8-112. EEPM8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	REVSERVED
6-4	EEP_FLTIMEOUT	R/W	0h	FlexWire timeout timer setting EEPROM register. 0h = 1 ms 1h = 125 µs 2h = 250 µs 3h = 500 µs 4h = 1.25 ms 5h = 2.5 ms 6h = 5 ms 7h = 10 ms
3-0	EEP_ADCLOWSUPTH	R/W	3h	ADC Supply monitor threshold setting EEPROM register. 0h = 5 V 1h = 6 V 2h = 7 V 3h = 8 V 4h = 9 V 5h = 10 V 6h = 11 V 7h = 12 V 8h = 13 V 9h = 14 V Ah = 15 V Bh = 16 V Ch = 17 V Dh = 18 V Eh = 19 V Fh = 20 V

8.6.1.98 EEPM9 Register (Offset = C9h) [reset = 0h]

EEPM9 is shown in Figure 8-116 and described in Table 8-113.

Return to the Summary Table.

Figure 8-116. EEPM9 Register

7	6	5	4	3	2	1	0
EEP_ODIOUT				EEP_ODPW			
R/W-0h				R/W-0h			

Table 8-113. EEPM9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	EEP_ODIOUT	R/W	0h	On-demand diagnostics output current setting EEPROM register. 0x0 to 0xE: IOUT = (CONF_ODIOUT*4+1)/64*I(FULL_RANGE) 0xF: ODIOUT is using its channel setting current
3-0	EEP_ODPW	R/W	0h	On-demand diagnostics pulse-width setting EEPROM register. 0h = 100 µs 1h = 20 µs 2h = 30 µs 3h = 50 µs 4h = 80 µs 5h = 150 µs 6h = 200 µs 7h = 300 µs 8h = 500 µs 9h = 800 µs Ah = 1 ms Bh = 1.2 ms Ch = 1.5 ms Dh = 2 ms Eh = 3 ms Fh = 5 ms

8.6.1.99 EEPM10 Register (Offset = CAh) [reset = 0h]

EEPM10 is shown in Figure 8-117 and described in Table 8-114.

Return to the Summary Table.

Figure 8-117. EEPM10 Register

7	6	5	4	3	2	1	0
EEP_WDTIMER				EEP_INITTIMER			
R/W-0h				R/W-0h			

Table 8-114. EEPM10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	EEP_WDTIMER	R/W	0h	Watchdog timer setting EEPROM register. 0h = Disabled, do not automatically enter fail-safe state 1h = 200 µs 2h = 500 µs 3h = 1 ms 4h = 2 ms 5h = 5 ms 6h = 10 ms 7h = 20 ms 8h = 50 ms 9h = 100 ms Ah = 200 ms Bh = 500 ms Ch = 0 µs; direct enter fail-safe state Dh = 0 µs; direct enter fail-safe state Eh = 0 µs; direct enter fail-safe state Fh = 0 µs; direct enter fail-safe state
3-0	EEP_INITTIMER	R/W	0h	Initialization timer setting EEPROM register. 0h = 0 ms 1h = 50 ms 2h = 20 ms 3h = 10 ms 4h = 5 ms 5h = 2 ms 6h = 1 ms 7h = 500 µs 8h = 200 µs 9h = 100 µs Ah = 50 µs Bh = 50 µs Ch = 50 µs Dh = 50 µs Eh = 50 µs Fh = 50 µs

8.6.1.100 EEPM11 Register (Offset = CBh) [reset = 0h]

EEPM11 is shown in Figure 8-118 and described in Table 8-115.

Return to the Summary Table.

Figure 8-118. EEPM11 Register

7	6	5	4	3	2	1	0
EEP_ADCSHORTTH							
R/W-0h							

Table 8-115. EEPM11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_ADCSHORTTH	R/W	0h	ADC short detection threshold setting EEPROM register

8.6.1.101 EEPM15 Register (Offset = CFh) [reset = 23h]

EEPM15 is shown in Figure 8-119 and described in Table 8-116.

Return to the Summary Table.

Figure 8-119. EEPM15 Register

7	6	5	4	3	2	1	0
EEP_CRC							
R/W-B3h							

Table 8-116. EEPM15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEP_CRC	R/W	B3h	CRC reference for all EEPROM register, manufacture default CRC code is B3h for TPS929121 and 09h for TPS929121A version.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS929121-Q1 device with FlexWire interface easily generates independent brightness and ON/OFF control for large amount LED units. It allows each single LED as a pixel in large LED array or string to display a complicated pattern or animation under accurate control. The FlexWire interface also uses the CAN physical layer through external CAN transceiver for data transmission between master controller (MCU) and TPS929121-Q1, which allows the TPS929121-Q1 to be controlled by control module far away in long distance. With these features, the single TPS929121-Q1 or multiple TPS929121-Q1 devices can drive large volume LEDs with digital control interface for automotive rear-lamp applications. The long distance, reliable off-board communication with high EMC performance simplifies the system design in lower cost for automotive application.

The TPS929121-Q1 also operates as a standalone LED driver without master controller. The fail-safe state is design to ensure the TPS929121-Q1 keeps operating in case the communication loss or master controller (MCU) damaged. TPS929121-Q1 can also use the fail-safe state without master-controller design for traditional automotive rear-lamp applications.

9.2 Typical Application

9.2.1 Smart Rear Lamp With Distributed LED drivers

Use multiple TPS929121-Q1 devices to control large numbers of LED pixels for rear-lamp animation.

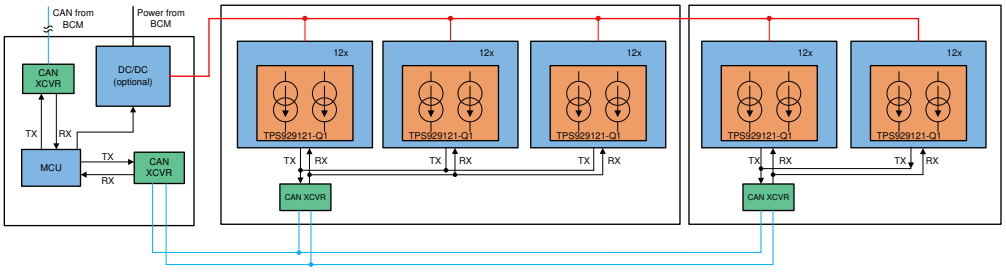


Figure 9-1. System Block Diagram

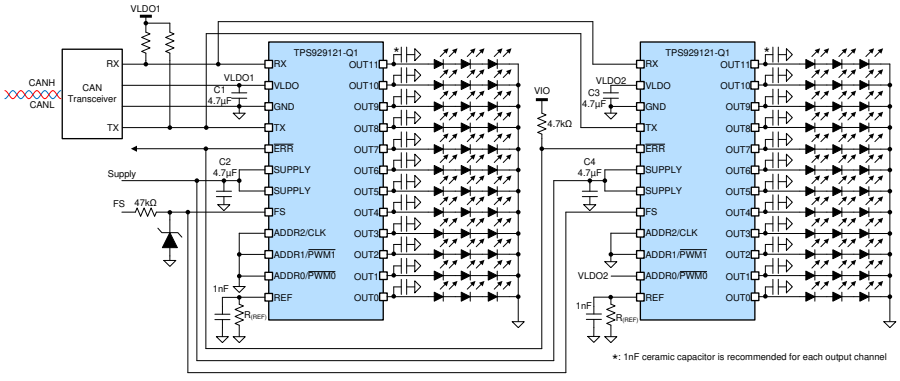


Figure 9-2. Typical Application Schematic

9.2.2 Design Requirements

Input voltage ranges from 9 V to 16 V, and a total of 60 LED strings with 3 LEDs in each string are required in one rear-lamp housing. The 60 LED strings must be controlled independently to achieve the animation effect. The maximum forward voltage of single LED $V_{(F\_MAX)}$ = 2.5 V, minimum forward voltage $V_{(F\_MIN)}$ = 1.9 V, and each string current $I_{(LED)}$ = 50 mA. The 36 strings of LED, and 24 strings of LED and MCU must be placed in three different boards due to the shape of the rear-lamp housing.

9.2.3 Detailed Design Procedure

STEP 1: Determine the architecture at system level.

Because MCU is located in a speared board to the LED boards, the CAN physical layer must be utilized for off-board long distance communication between LED driver boards and MCU board. The overall system block diagram is shown in Figure 9-2 and the typical schematic for 24 strings of LED board is shown in Figure 9-2. The pullup resistors for RX and TX interface may or may not be required, depending the model of the CAN transceiver. Normally the pullup resistor value for RX and TX must be about 10 kΩ. TI recommends putting a 4.7-µF ceramic capacitor on the VLDO output to keep the voltage stable. Because only one CAN transceiver is required per one PCB board, the CAN transceiver must only be powered by one LDO output of the TPS929121-Q1. DO NOT tie the LDO outputs for all TPS929121-Q1 in one PCB board. TI also recommends placing a 4.7-µF decoupling ceramic capacitor close to the SUPPLY pin of each TPS929121-Q1 to obtain good EMC performance.

STEP 2: Thermal analysis for the worst application conditions.

Normally the thermal analysis is necessary for linear LED-driver applications to ensure that the operation junction temperature of TPS929121-Q1 is well managed. The total power consumption on the TPS929121-Q1 itself is one important factor determining operation junction temperature, and it can be calculated by using Equation 8.

$$P_{(MAX)} = \left(V_{(SUPPLY\_MAX)} - V_{(LED\_MIN)}\right) \times I_{(CH)} \times N_{(CH)} \tag{8}$$

where

- $V_{(SPPLY\_MAX)}$ is maximum supply voltage
- $V_{(LED\_MIN)}$ is minimum output voltage
- $I_{(CH)}$ is channel current
- $N_{(CH)}$ is number of used channels

Based on the worst-case analysis for maximum power consumption on device, either optimizing PCB layout for better power dissipation as *Layout Example* describing or implementing a DC-to-DC converter in previous stage on MCU board can be considered. The DC-to-DC such as a buck converter or buck-boost converter can regulate the batter voltage to be a stable supply for the TPS929121-Q1 with sufficient headroom. It minimizes the power combustion on the TPS929121-Q1 itself as well as the whole system. In this application, the DC-to-DC converter with 8.5-V output voltage can make sure current output on each output channel of TPS929121-Q1 is stable. The calculated maximum power dissipation on the device is 1.68 W as Equation 9.

$$\begin{aligned} P_{(MAX)} &= \left(V_{(SUPPLY\_REG)} - V_{(LED\_MIN)}\right) \times I_{(CH)} \times N_{(CH)} \\ &= \left(8.5 - 1.9 \times 3\right) \times 0.05 \times 12 = 1.68\text{W} \end{aligned} \tag{9}$$

where

- $V_{(SPPLY\_MAX)}$ is maximum supply voltage
- $V_{(LED\_MIN)}$ is minimum output voltage
- $I_{(CH)}$ is channel current
- $N_{(CH)}$ is number of used channels

STEP 3: Set up the slave address for individual TPS929121-Q1.

The slave address of TPS929121-Q1 can be configured by ADDR2/ADDR1/ADDR0 pins or EEP_DEVADDR selected by EEP_INTADDR. The detail description is explained in *UART Interface Address Setting*. If the total number of TPS929121-Q1 is less than 8, TI recommends using ADDR2/ADDR1/ADDR0 pins for slave device configuration.

STEP 4: DC current setup for each LED string.

The DC current for all output channel can be programable by external resistor, $R_{(REF)}$ and internal register CONF_REFRANGE. The resistor value can be calculated by using Figure 9-2. The manufacturer default value for $K_{(REF)}$ is 512. If the other number rather than 512 is chosen for DC current setting, the selected code needs to burnt into EEPROM register EEP_REFRANGE to change the default value for CONF_REFRANGE. A 1-nF ceramic capacitor could be placed in parallel with $R_{(REF)}$ resistor to improve the noise immunity. The CONF_IOUTx register can be used to program DC current for each output channel independently mainly for dot correction purpose. The code setting for CONF_IOUTx must be decided in the end of production line according to the LED calibration result. The detail calculation is described in *64-Step Programmable High-Side Constat-Current Output*.

$$R_{(REF)} = \frac{V_{(REF)}}{I_{(FULL\_RANGE)}} \times K_{(REF)} \tag{10}$$

where

- $V_{(REF)}$ = 1.235 V typically
- $K_{(REF)}$ = 64, 128, 256 or 512 (default)

Table 9-1. Reference Current Range Setting

CURRENT (mA)	CONF_REFRANGE	$K_{(REF)}$	REF RESISTOR VALUE (kΩ)
50	11b	512	12.7
	10b	256	6.34
	01b	128	3.16
	00b	64	1.58

TI recommends placing a 1-nF ceramic capacitor on each of output channels to achieve good EMC performance.

STEP 5: Design the configuration for PWM generator. Basically there are three main parameters for PWM generator must be considered including:

- PWM frequency set by CONF_PWMFREQ. The detail calculation and description is explained in *PWM Dimming Frequency*. The default value of CONF_PWMFREQ can be changed by burning the target value to EEP_PWMFREQ.
- PWM dutycycle set by CONF_PWMOUTx and CONF_PWMLOWOUTx. The detail calculation and description is explained in *Linear Birhgtness Control*. The default value of CONF_PWMOUTx can be changed by burning the target value to EEP_PWMFREQ.
- PWM dimming method set by CONF_EXPEN. The detail calculation and description is explained in *Exponential Brightness Control*. The default value of CONF_EXPEN can be changed by burning the target value to EEP_PWMFREQ.

STEP 6: Design the diagnostics configuration. The diagnostics configuration for both normal state and fail-safe states must be set up properly based on the system requirements. The following configuration registers need to designed:

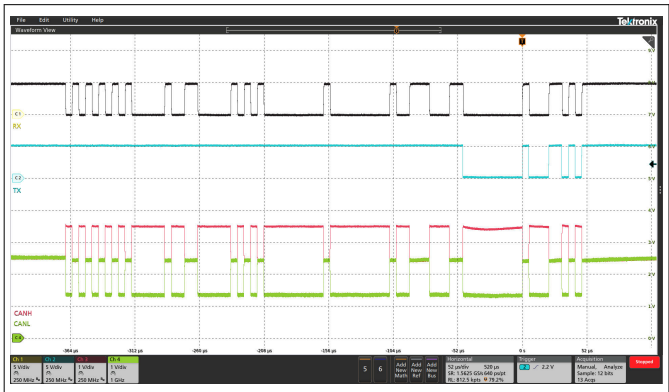
- Low-supply warning threshold set by CONF_ADCLOWSUPTH. The detail calculation and description is explained in *Low-Supply Warning Diagnostics in Normal State*. The default value of CONF_ADCLOWSUPTH can be changed by burning the target value to EEP_ADCLOWSUPTH.

- Diagnostics enabling setup for each channel by CONF_DIAGENCHx. The diagnostics for each channel can be enabled or disabled by CONF_DIAGENCHx register. The detail description is explained in *Fault Masking*. The default value of CONF_DIAGENCHx can be changed by burning the target value to EEP_DIAGENCHx.
- On-demand invisible diagnostic current and pulse setup by CONF_ODIOUT and CONF_ODPW. The detail calculation and description is explained in *On-Demand Off-State Invisible Diagnostics*. The default value of CONF_ODIOUT and CONF_ODPW can be changed by burning the target value to EEP_ODIOUT and EEP_ODPW.
- Auto single-LED short-circuit configuration by CONF_AUTOSS and CONF_ADCSHORTTH. The detail calculation and description is explained in *Automatic Single-LED Short-Circuit (AutoSS) Detection in Normal State*. The default value of CONF_AUTOSS and CONF_ADCSHORTTH can be changed by burning the target value to EEP_AUTOSS and EEP_ADCSHORTTH.
- Fail-safe state access watchdog timer setup by CONF_WDTIMER. The detail calculation and description is explained in *Normal State*. The default value of CONF_WDTIME can be changed by burning the target value to EEP_WDTIMER.
- Channel setup in fail-safe states. Each output channels can be enabled or disabled independently in fail-safe state 0 and fail-safe state 1 by EEP_FS0CHx and EEPFS1CHx. In fail-safe state, the FS pin can be used as control signal to change device operating in fail-safe state 0 or fail-safe state 1. The manufacture defaults EEP_FS0CHx to 0 and EEP_FS1CHx to 1, so supply logic low voltage to FS pin turns off all the output channels in fail-safe state 0 and supply logic high voltage to FS pin turns on all the output channels in fail-safe state 1. With this configuration, input a PWM signal to FS pin can also achieve brightness control for all output channels. The detail calculation and description is explained in *Fail-Safe States*.
- One-fails-all-fail setup by EEP_OFAF. If the one-fails-all-fail can be enabled by burning 1 to EEP_OFAF according to system requirements. Tie the $\overline{ERR}$ pins for all TPS929121-Q1 in the system together with a single 4.7-kΩ pullup resistor to realize the one-fails-all-fail feature. The detail calculation and description is explained in *Programmable Output Failure State*.
- CRC check reference calculation for EEP_CRC. Once all EEPROM register data is designed, the CRC reference value for all EEPROM register needs to calculated and burnt into EEP_CRC. The detail calculation and description is explained in *EEPROM CRC Error in Normal State*.

STEP 7: EEPROM burning solution design.

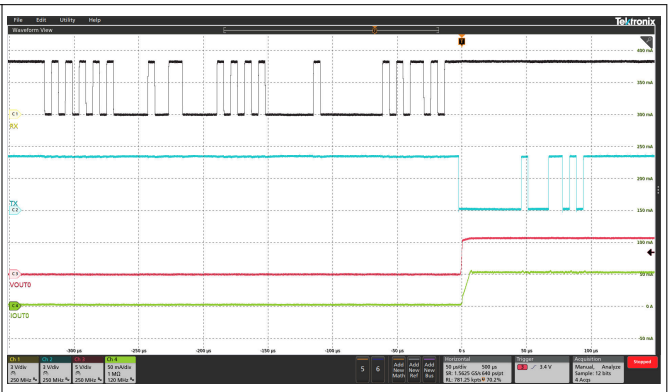
TI recommends that the EEPROM burning be done in the end of production line; the detail flow is introduced in *EEPROM Register Access and Burn* .

9.2.4 Application Curves



CH1 = RX CH2 = TC CH3 = CANH
CH4 = CANL

Figure 9-3. CAN Transceiver Operating



CH1 = RX CH2 = TX CH3 = $V_{(OUT0)}$
CH4 = $I_{(OUT0)}$

Figure 9-4. Output Control By FlexWire Interface

10 Power Supply Recommendations

The TPS929121-Q1 is designed to operate from an automobile electrical power system within the range specified in *Power Supply (SUPPLY)*. The $V_{(SUPPLY)}$ input must be protected from reverse voltage and voltage dump condition over 40 V. The impedance of the input supply rail must be low enough that the input current transient does not cause drop below LED string required forward voltage. If the input supply is connected with long wires, additional bulk capacitance may be required in addition to normal input capacitor.

11 Layout

11.1 Layout Guidelines

Thermal dissipation is the primary consideration for TPS929121-Q1 layout. TI recommends large thermal dissipation area connected to thermal pads with multiple thermal vias. Place the capacitor for both SUPPLY input and VLDO output as closed as possible to the pins. The $R_{(REF)}$ resistor must also be placed as closed as possible to the REF pin.

11.2 Layout Example

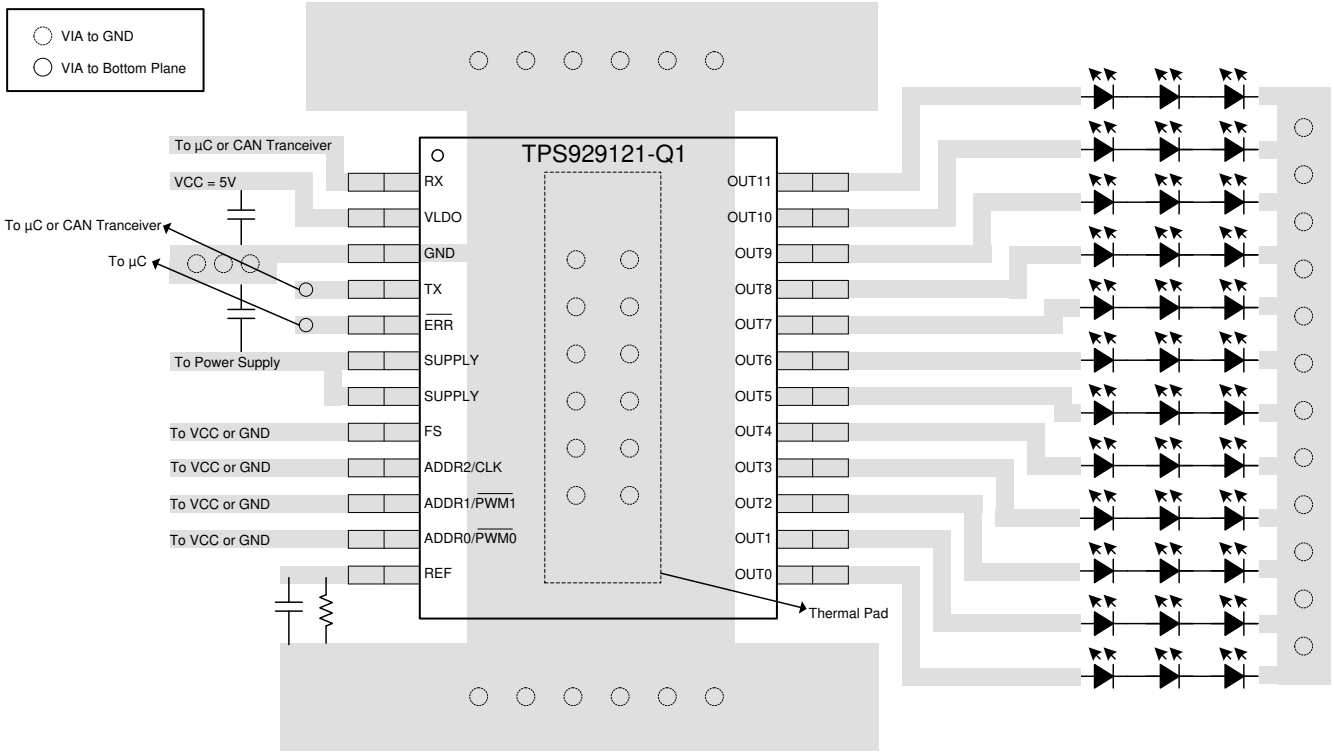


Figure 11-1. TPS929121-Q1 Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS929121AQPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	929121AQ	Samples
TPS929121QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	929121Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

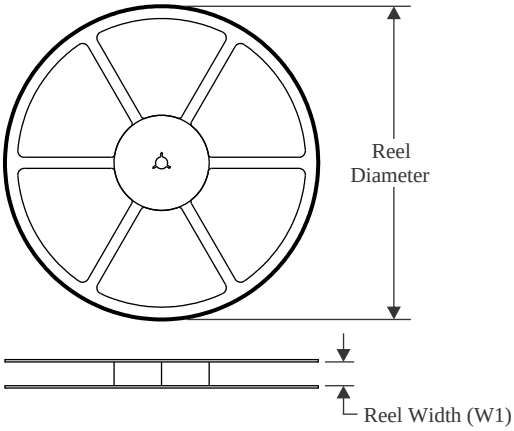
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

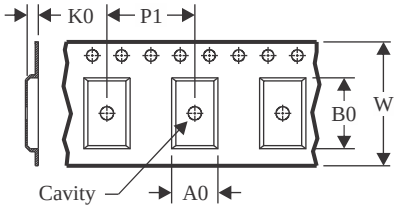
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

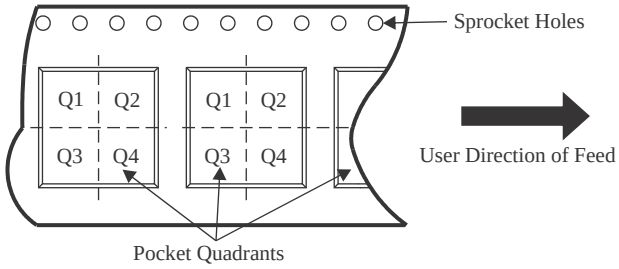


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

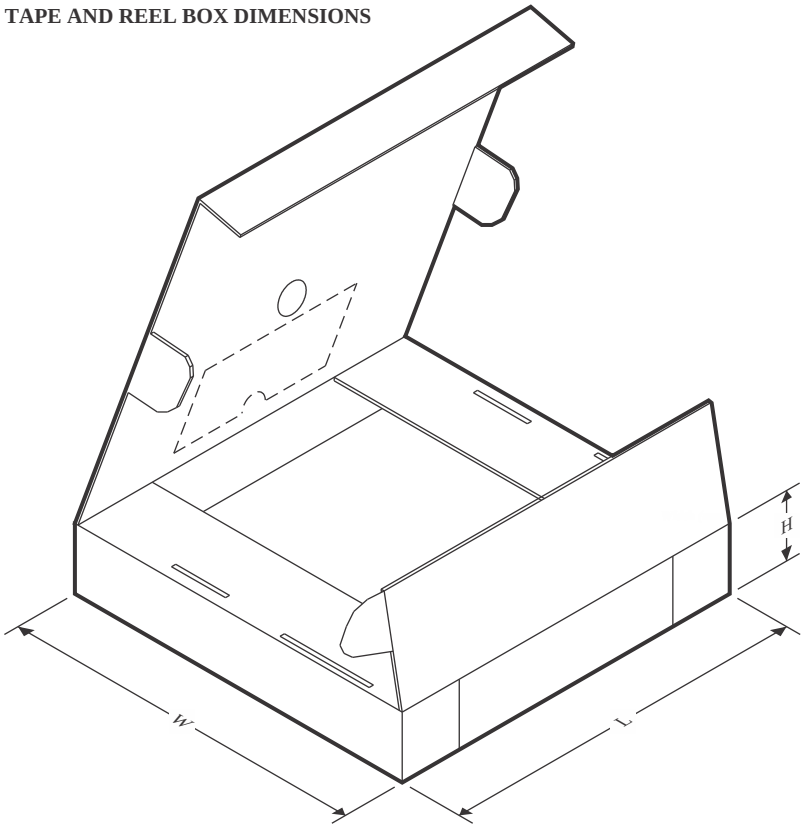
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS929121AQPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS929121QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS929121AQPWPRQ1	HTSSOP	PWP	24	2000	356.0	356.0	35.0
TPS929121QPWPRQ1	HTSSOP	PWP	24	2000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

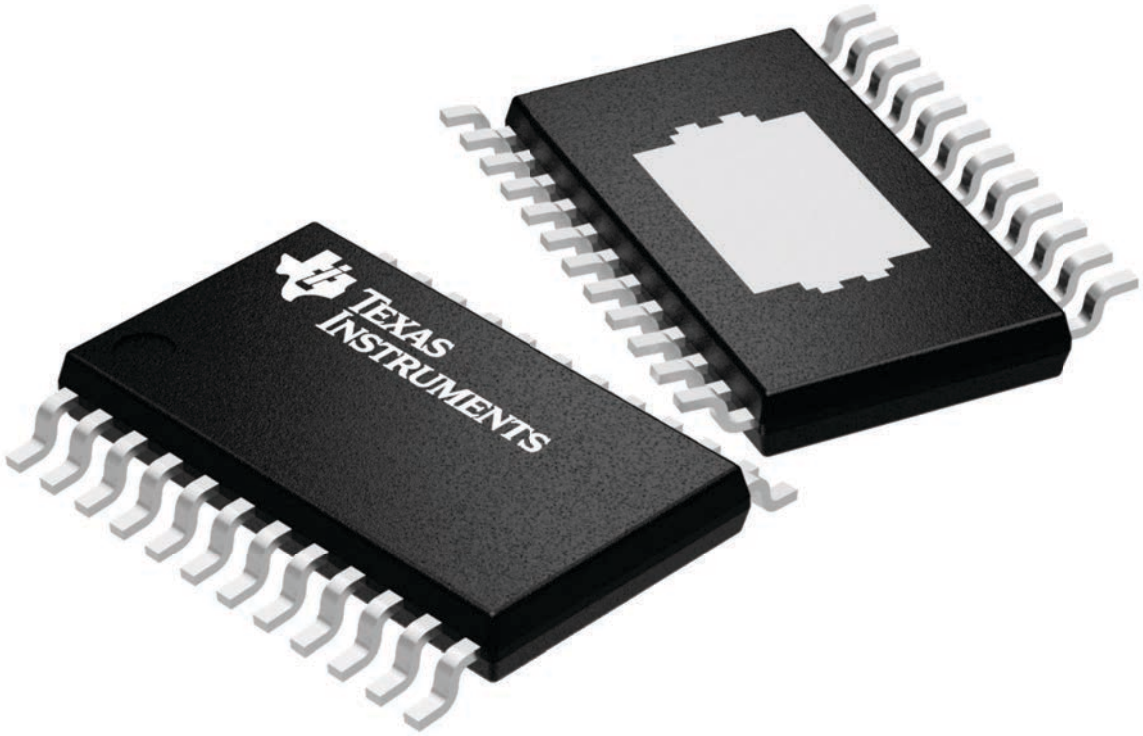
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

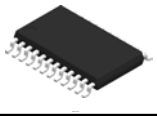
4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

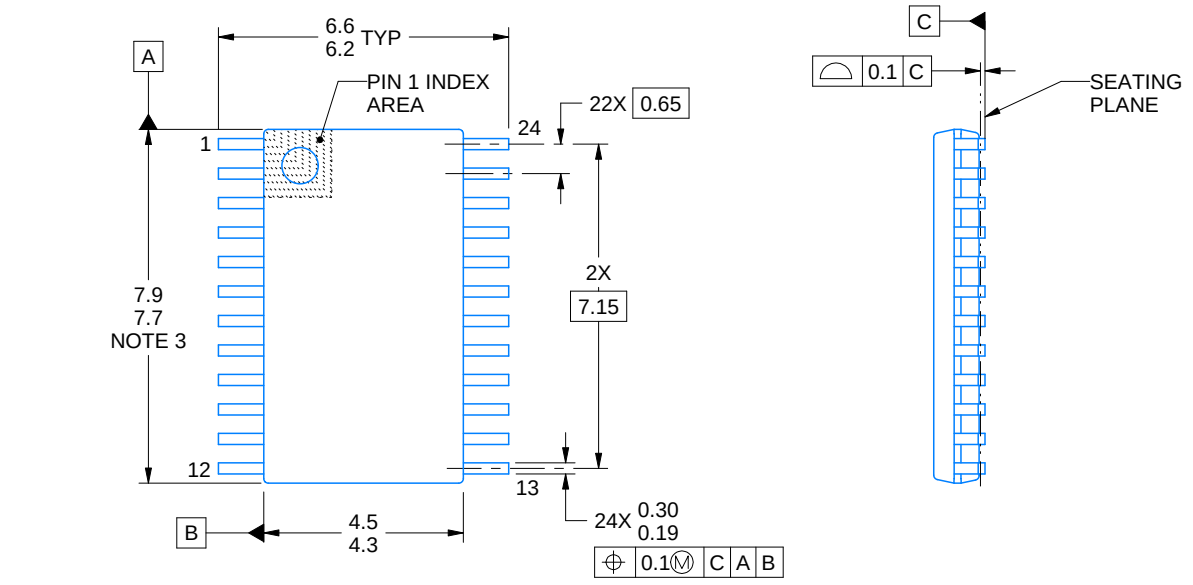


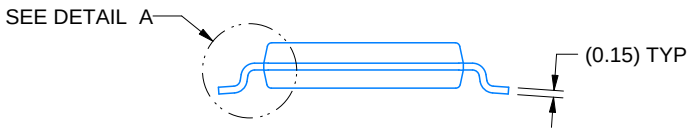
PACKAGE OUTLINE

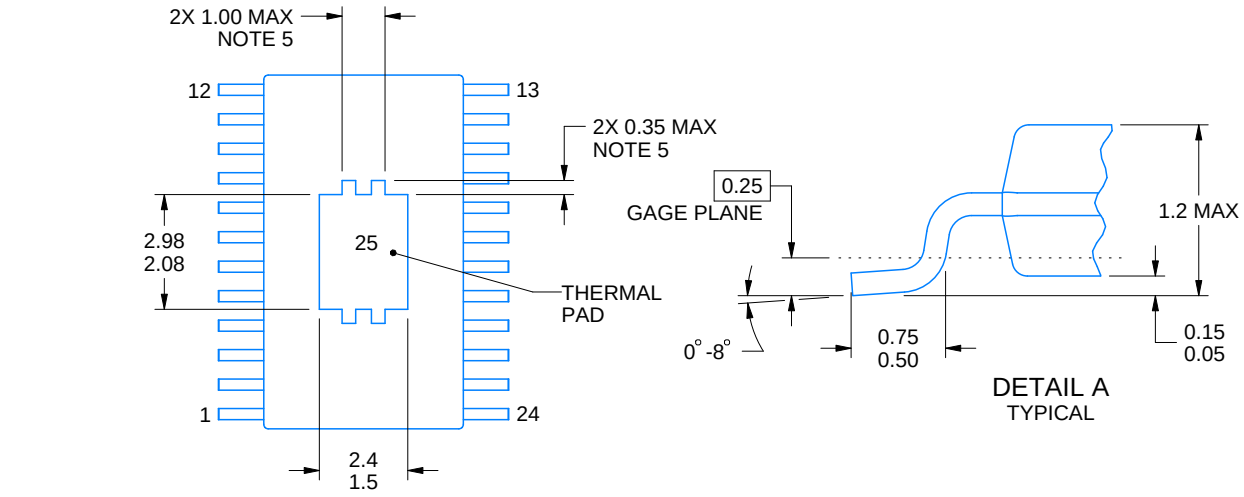
PWP0024P

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE







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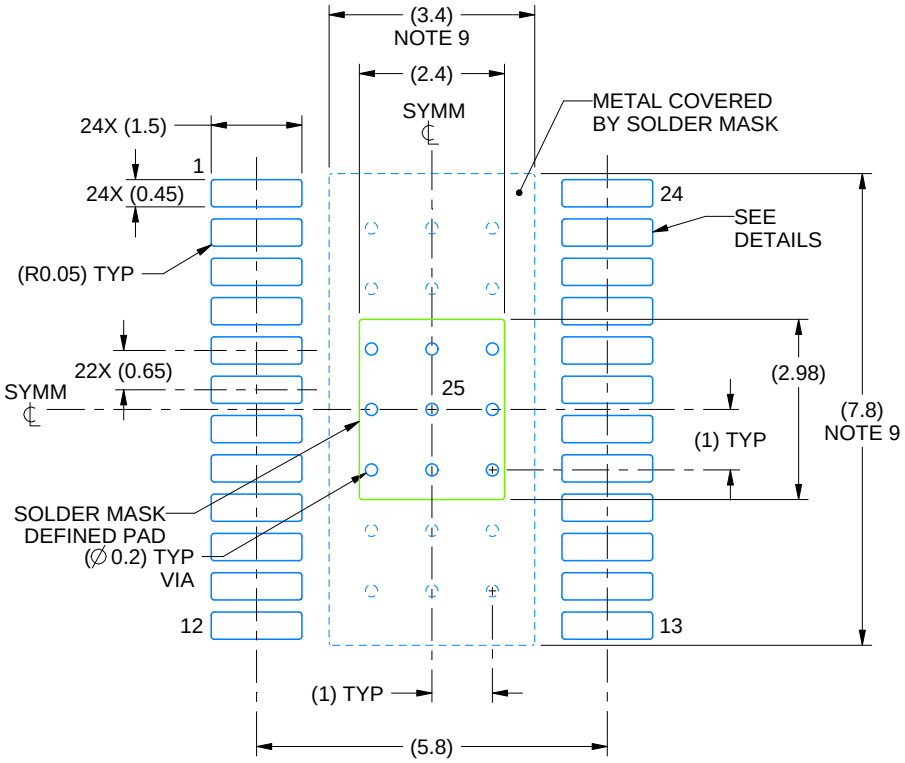
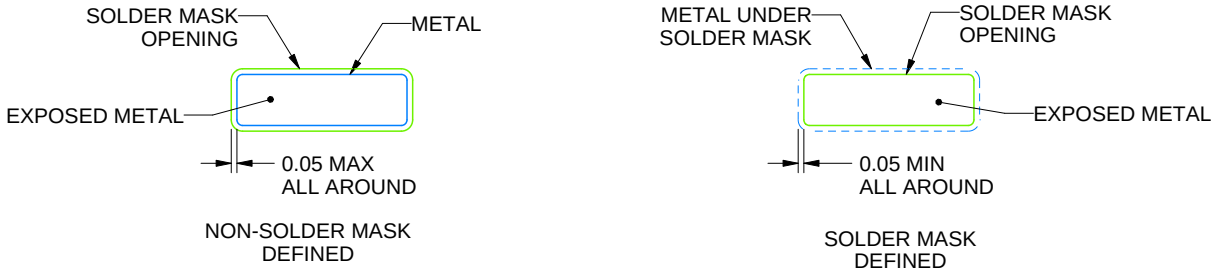
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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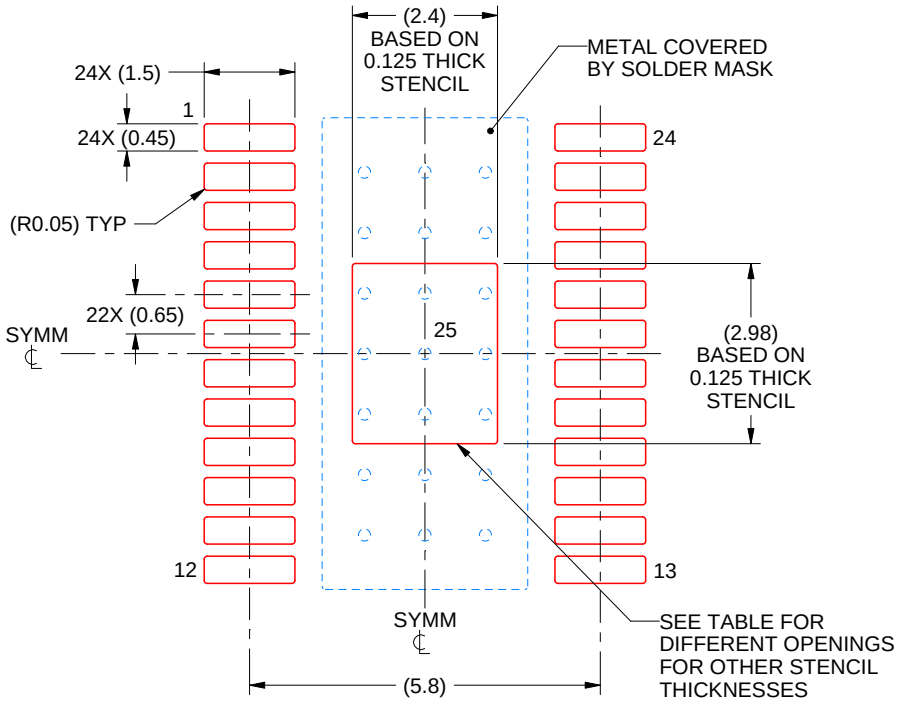
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 3.33
0.125	2.40 X 2.98 (SHOWN)
0.15	2.19 X 2.72
0.175	2.03 X 2.52

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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