THE DATASHEET OF

CSR1001A04-IQQA-R

CSR µEnergy® CSR1001™ QFN

Bluetooth low energy Single-mode IC

Production Information

CSR1001A04
Issue 5

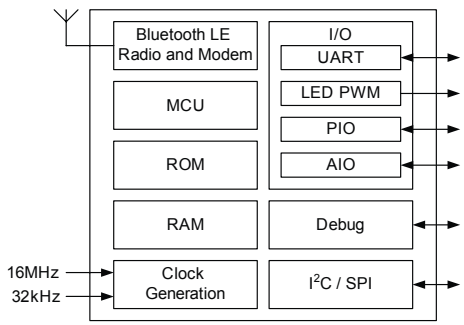
Features

- 128KB memory: 64KB RAM and 64KB ROM
- Bluetooth® v4.0 specification
- 7.5dBm Bluetooth low energy maximum transmit output power
- -92.5dBm Bluetooth low energy receive sensitivity
- Support for Bluetooth v4.0 specification host stack including ATT, GATT, SMP, L2CAP, GAP
- RSSI monitoring for proximity applications
- <600nA current consumption in dormant mode
- 32kHz and 16MHz crystal or system clock
- Switch-mode power supply
- Programmable general purpose PIO controller
- 10-bit ADC
- 32 digital PIOs
- 3 analogue AIOs
- UART
- I²C / SPI for EEPROM / flash memory ICs and peripherals
- Debug SPI
- 3 PWM modules
- Wake-up interrupt and watchdog timer
- QFN 56-lead, 8 x 8 x 0.9mm, 0.5mm pitch

General Description

CSR1001 QFN is a CSR µEnergy platform device. CSR µEnergy are CSR's single-mode Bluetooth low energy products for the Bluetooth Smart market.

CSR µEnergy enables ultra low-power connectivity and basic data transfer for applications previously limited by the power consumption, size constraints and complexity of other wireless standards. The CSR µEnergy platform provides everything required to create a Bluetooth low energy product with RF, baseband, MCU, qualified Bluetooth v4.0 stack and customer application running on a single IC.



Applications

- Building an ecosystem using Bluetooth low energy

CSR is the industry leader for Bluetooth low energy, also known as Bluetooth Smart. Bluetooth Smart energy enables the transfer of simple data sets between compact devices opening up a completely new class of Bluetooth applications such as watches, TV remote controls, medical sensors and fitness trainers.

Bluetooth low energy takes less time to make a connection than conventional Bluetooth wireless technology and can consume approximately 1/20th of the power of Bluetooth Basic Rate. CSR1001 QFN supports profiles for sensors, watches, HIDs and time synchronisation.

Typical Bluetooth low energy applications:

- Sports and fitness
- Healthcare
- Home entertainment
- Office and mobile accessories
- Automotive
- Commercial
- Watches
- Human interface devices

Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
CSR1001 QFN	QFN-56-lead (Pb free)	8 x 8 x 0.9mm 0.5mm pitch	Tape and reel	CSR1001A04-IQQA-R

Note:

The minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

CSR1001 QFN Development Kit Ordering Information

Description	Order Number
CSR1001 QFN Development Kit example design	DK-CSR1001-10049-2A

Contacts

General information	www.csr.com
Information on this product	Sales@csr.com
Customer support for this product	www.csrsupport.com
Details of compliance and standards	Product.compliance@csr.com
Help with this document	Comments@csr.com

Device Details

Bluetooth Radio

- On-chip balun (50Ω impedance in TX and RX modes)
- No external trimming is required in production
- Bluetooth v4.0 specification compliant

Bluetooth Transmitter

- 7.5dBm RF transmit power with level control from integrated 6-bit DAC over a dynamic range >30dB
- No external power amplifier or TX/RX switch required

Bluetooth Receiver

- -92.5dBm sensitivity
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Fast AGC for enhanced dynamic range

Bluetooth Stack

CSR's protocol stack runs on the integrated MCU:

- Support for Bluetooth v4.0 specification features:
  - Master and slave operation
  - Including encryption
- Software stack in firmware includes:
  - GAP
  - L2CAP
  - Security manager
  - Attribute protocol
  - Attribute profile
  - Bluetooth low energy profile support

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter

Baseband and Software

- Hardware MAC for all packet types enables packet handling without the need to involve the MCU

Physical Interfaces

- SPI master interface
- SPI programming and debug interface
- I²C
- Digital PIOs
- Analogue AIOs
- UART

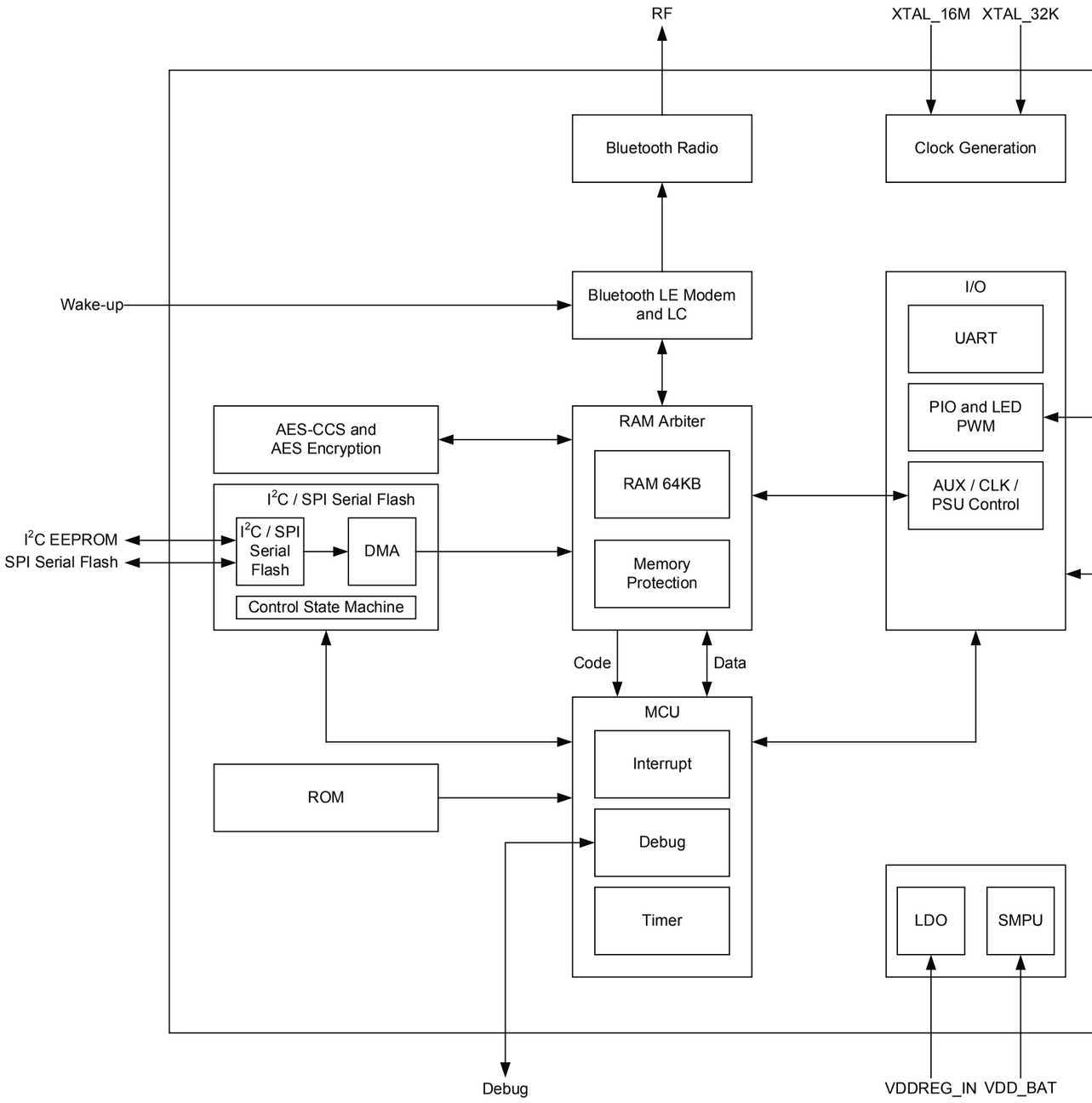
Auxiliary Features

- Battery monitor
- Power management features include software shutdown and hardware wake-up
- CSR1001 QFN can run in low power modes from an external 32.768kHz clock signal
- Integrated switch-mode power supply
- Linear regulator (internal use only)
- Power-on-reset cell detects low supply voltage

Package

- 56-lead 8 x 8 x 0.9mm, 0.5mm pitch QFN

Functional Block Diagram



Document History

Revision	Date	Change Reason
1	21 JUL 11	Original publication of this document.
2	27 OCT 11	Updates to Absolute Maximum Ratings, Recommended Operating Conditions and CSR Green Semiconductor Products and RoHS Compliance details.
3	06 JAN 12	Updates to schematic and wake-up options.
4	16 JAN 12	Update to schematic.
5	08 APR 13	Updates include: ■ Removal of NDA statement. ■ Temperature sensor added. ■ Battery monitor added. ■ SPI timing diagram added. ■ Change from VDD to VDD_PADS in Digital Terminals. ■ Auxiliary ADC and DAC parameters added.

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

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Refer to www.csrsupport.com for compliance and conformance to standards information.

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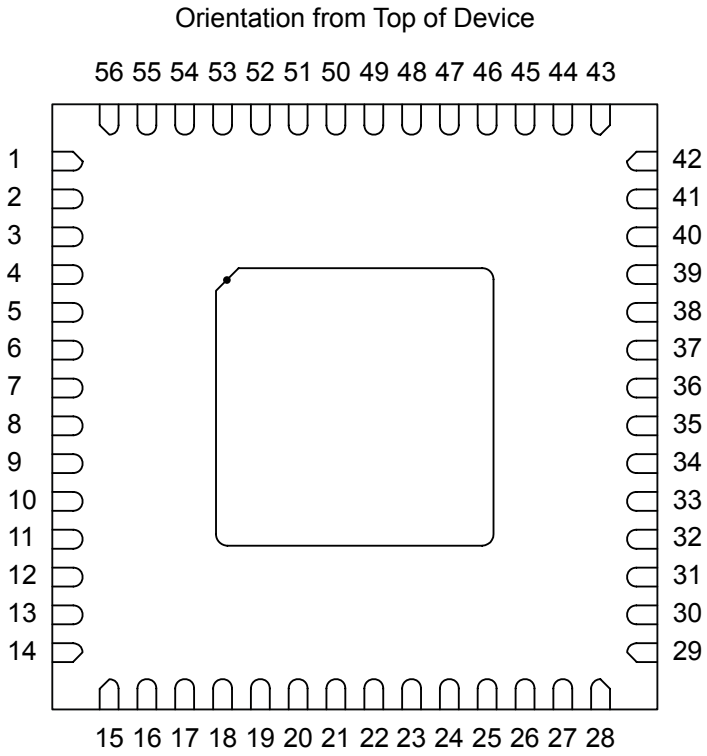
1.1 Pinout Diagram



G-TW-0005575.3.2

Figure 1.1: Pinout Diagram

1.2 Device Terminal Functions

Radio	Lead	Pad Type	Supply Domain	Description
RF	10	RF	VDD_RADIO[a]	Bluetooth transmitter / receiver.

[a] The VDD_RADIO domain is generated from VDD_REG_IN, see Figure 6.1.

Synthesiser and Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_32K_OUT	4	Analogue	VDD_BAT	Drive for sleep clock crystal.
XTAL_32K_IN	5	Analogue	VDD_BAT	32.768kHz sleep clock input.
XTAL_16M_OUT	14	Analogue	VDD_ANA[b]	Drive for crystal.
XTAL_16M_IN	15	Analogue	VDD_ANA[b]	Reference clock input.

[b] The VDD_ANA domain is generated from VDD_REG_IN, see Figure 6.1.

I²C Interface	Lead	Pad Type	Supply Domain	Description
I2C_SDA	54	Bidirectional, tristate, with weak internal pull-up	VDD_PADS	I²C data input / output or SPI serial flash data output (SF_DOUT). If connecting to SPI serial flash, connect this pin to SO on the serial flash. See Section 5.3.
I2C_SCL	53	Input with weak internal pull-up	VDD_PADS	I²C clock or SPI serial flash clock output (SF_CLK), see Section 5.3.

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[31]	51	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line
PIO[30]	49			
PIO[29]	48			
PIO[28]	46			
PIO[27]	44			
PIO[26]	43			
PIO[25]	41			
PIO[24]	40			
PIO[23]	38			
PIO[22]	37			
PIO[21]	35			
PIO[20]	33			
PIO[19]	32	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line
PIO[18]	30			
PIO[17]	29			
PIO[16]	27			
PIO[15]	26			
PIO[14]	23			
PIO[13]	22			
PIO[12]	20			
PIO[11]	47			
PIO[10]	45			
PIO[9]	42			
PIO[8] / DEBUG_MISO	39	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or debug SPI MISO selected by SPI_PIO#.

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[7] / DEBUG_MOSI	34	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or debug SPI MOSI selected by SPI_PIO#
PIO[6] / DEBUG_CS#	31	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or debug SPI chip select (CS#) selected by SPI_PIO#.
PIO[5] / DEBUG_CLK	28	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or debug SPI CLK selected by SPI_PIO#.
PIO[4] / SF_CS#	25	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or SPI serial flash chip select (SF_CS#), see Section 5.3.
PIO[3] / SF_DIN	24	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or SPI serial flash data (SF_DIN) input. If connecting to SPI serial flash, this pin connects to SI on the serial flash. See Section 5.3.
PIO[2]	52	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or I²C power.
PIO[1] / UART_RX	21	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or UART RX.
PIO[0] / UART_TX	19	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or UART TX.
AIO[2]	16	Bidirectional analogue	VDD_AUX[c]	Analogue programmable I/O line.
AIO[1]	17			
AIO[0]	18			

[c] The VDD_AUX domain is generated from VDD_REG_IN, see Figure 6.1.

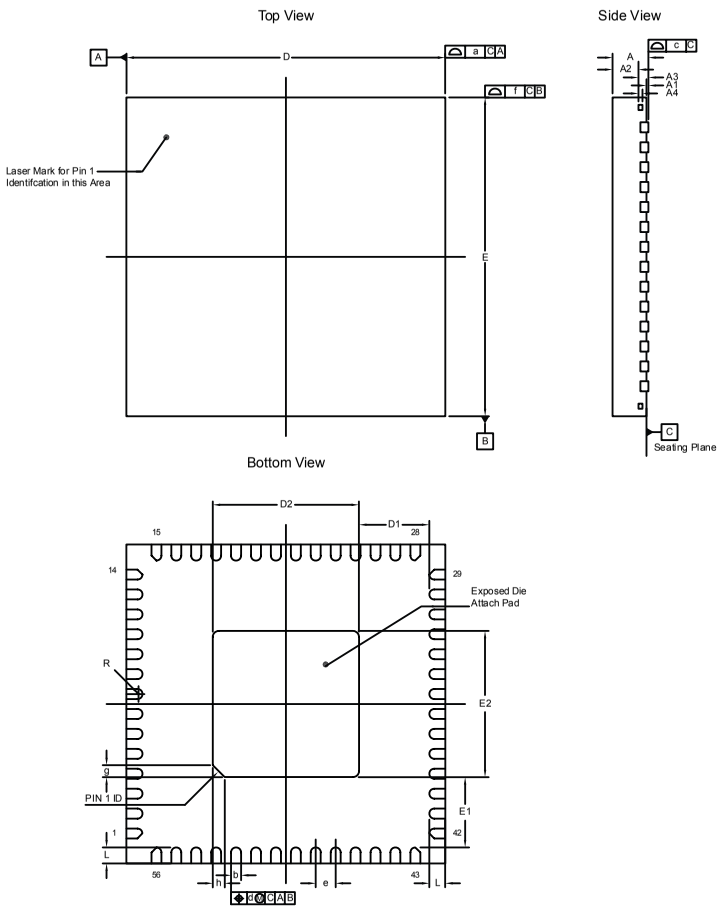
Test and Debug	Lead	Pad Type	Supply Domain	Description
SPI_PIO#	50	Input with strong internal pull-down	VDD_PADS	Selects SPI debug on PIO[8:5].

Wake-up	Lead	Pad Type	Supply Domain	Description
WAKE	6	Input has no internal pull-up or pull-down, use external pull-down.	VDD_BAT	Input to wake CSR1001 QFN from hibernate or dormant.

Power Supplies and Control	Lead	Description
VDD_BAT	3	Battery input and regulator enable (active high).
VDD_BAT_SMPS	1	Input to high-voltage switch-mode regulator.
SMPS_LX	56	High-voltage switch-mode regulator output.
VDD_CORE	7, 55	Positive supply for digital domain.
VDD_PADS	36	Positive supply for all digital I/O ports PIO[31:0].
VDD_REG_IN	8	Positive supply for Bluetooth radio and digital linear regulator.
VDD_XTAL	13	Leave unconnected. **Note:** Add connection to a 470nF decoupling capacitor to this pin, see Section 7. The decoupling capacitor is not fitted in normal operation.
VSS	Exposed pad	Ground connections.

Unconnected Terminals	Lead	Description
N/C	2, 9, 11 and 12	Leave unconnected.

1.3 Package Dimensions



Dimension	Min	Typ	Max	Dimen
A	-	-	0.90	d
A1	-	-	0.05	E
A2	-	0.65	0.70	E1
A3	-	0.20	-	E2
A4	-	0.10	-	e
a	-	0.10	-	f
b	0.18	0.25	0.30	g
c	-	0.05	-	h
D	7.90	8.00	8.10	L
D1	-	1.76	-	R
D2	3.57	3.67	3.77	
Notes	1. Dimensioning and tolerances 2. Pin #1 identifier is placed on t Exact shape and size of this f 3. Package warpage 0.08mm m			
Description	56-lead Quad Flat No-lead Packag			
Size	8 x 8 x 0.9mm			**JEDEC**
Pitch	0.5			**Units**

1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 8 x 8 x 0.9mm QFN 56-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- CSR recommends that the PCB land pattern is in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

1.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

2 Bluetooth Modem

2.1 RF Ports

CSR1001 QFN contains an integrated balun which provides a single-ended RF TX / RX port pin. No matching components are needed as the receive mode impedance is 50Ω and the transmitter has been optimised to deliver power in to a 50Ω load.

2.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being significantly desensitised.

An ADC digitises the IF received signal.

2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the balanced port of the integrated balun.

2.2.2 RSSI Analogue to Digital Converter

The ADC samples the RSSI voltage on a packet-by-packet basis and implements a fast AGC. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

2.3 RF Transmitter

2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit packet, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.3.2 Power Amplifier

The internal PA has a maximum 7.5dBm output power without needing an external RF PA.

2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v4.0 specification.

2.5 Baseband

2.5.1 Physical Layer Hardware Engine

Dedicated logic performs:

- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation

The hardware supports all optional and mandatory features of Bluetooth v4.0 specification.

3 Clock Generation

The Bluetooth reference clock for the system is generated from an external 16MHz clock source, see Figure 3.1. All the CSR1001 QFN internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the external reference clock source or a sleep clock frequency of 32.768kHz, see Figure 3.1.

3.1 Clock Architecture

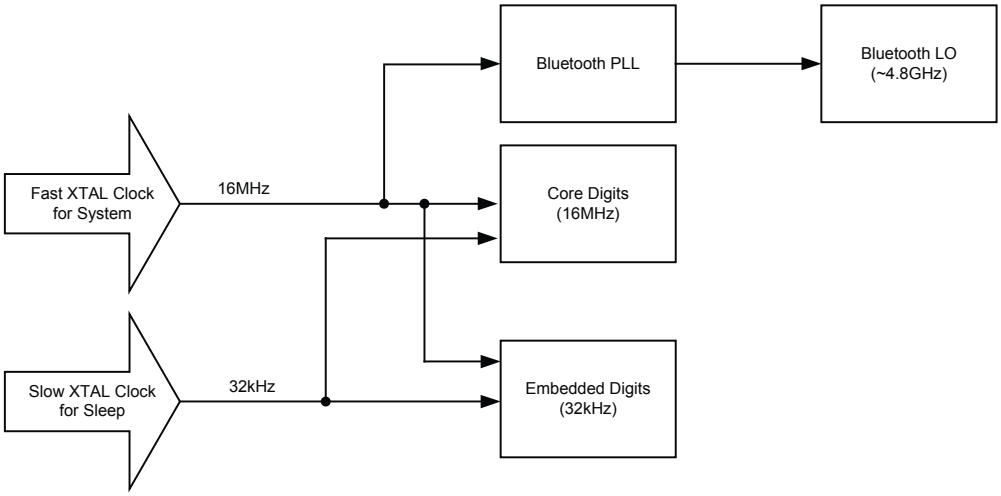


Figure 3.1: Clock Architecture

3.2 Crystal Oscillator: XTAL_16M_IN and XTAL_16M_OUT

CSR1001 QFN contains crystal driver circuits. This operates with an external crystal and capacitors to form a Pierce oscillator. Figure 3.2 shows the external crystal is connected to pins XTAL_16M_IN and XTAL_16M_OUT.

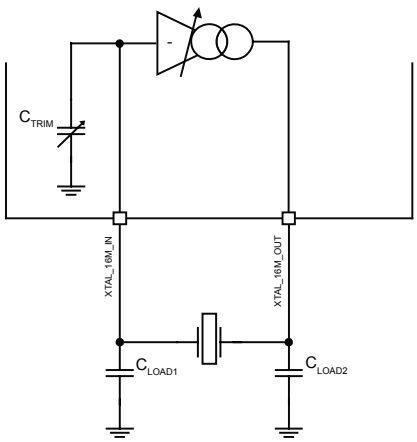


Figure 3.2: Crystal Driver Circuit

Note:

C_{TRIM} is the internal trimmable capacitance in Table 3.1.

C_{LOAD1} and C_{LOAD2} in combination with C_{TRIM} and any parasitic capacitance provide the load capacitance required by the crystal.

3.2.1 Crystal Specification

Table 3.1 shows the specification for an external crystal.

Parameter	Min	Typ	Max	Unit
Frequency	-	16	-	MHz
Frequency tolerance (without trimming) (a)	-	-	±25	ppm
Frequency trim range(b)	-	±50	-	ppm
Drive level	-	-	100	µW
Equivalent series resistance	-	-	60	Ω
Load capacitance	-	9	-	pF
Pullability	10	-	-	ppm/pF

Table 3.1: Crystal Specification

(a) Use integrated load capacitors to trim initial frequency tolerance in production or to trim frequency over temperature, increasing the allowable frequency tolerance.

(b) Frequency trim range is dependent on crystal load capacitor values and crystal pullability.

3.2.2 Frequency Trim

CSR1001 QFN contains variable integrated capacitors to allow for fine-tuning of the crystal resonant frequency. This firmware-programmable feature allows accurate trimming of crystals on a per-device basis on the production line. The resulting trim value is stored in non-volatile memory.

3.3 Sleep Clock

The sleep clock is an externally provided 32.768kHz clock that is used during deep sleep and in other low-power modes. Figure 3.3 shows the sleep clock crystal driver circuit.

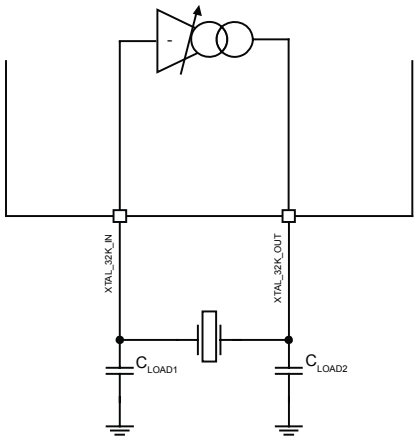


Figure 3.3: Sleep Clock Crystal Driver Circuit

Note:

C_{LOAD1} and C_{LOAD2} in combination with any parasitic capacitance provide the load capacitance required by the crystal.

3.3.1 Crystal Specification

Table 3.2 shows the requirements for the sleep clock.

Sleep Clock	Min	Typ	Max	Units
Frequency	30	32.768	35	kHz
Frequency tolerance[a] [b]	-	-	250	±ppm
Frequency trim range	-	50	-	±ppm
Drive level	-	0.4	-	V
Load capacitance	-	-	1	pF
Equivalent series resistance	40	-	65	kΩ
Duty cycle	30:70	50:50	70:30	%

Table 3.2: Sleep Clock Specification

[a] The frequency of the slow clock is periodically calibrated against the system clock. As a result the rate of change of the frequency is more important than the maximum deviation. To meet the accuracy requirements the frequency should not drift due to temperature or other effects by more than 80ppm in any 5 minute period.

[b] CSR1001 QFN can correct for ±1% by using the fast clock to calibrate the slow clock.

4 Microcontroller, Memory and Baseband Logic

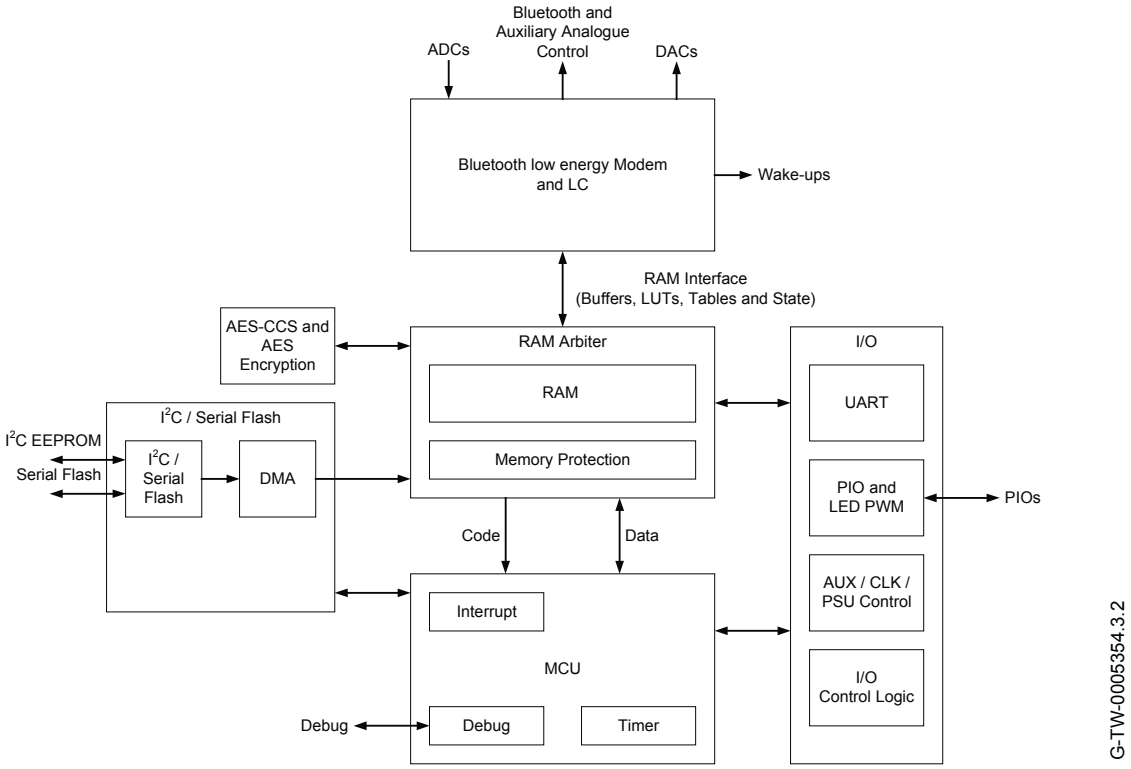


Figure 4.1: Baseband Digits Block Diagram

4.1 System RAM

64KB of integrated RAM supports the RISC MCU and is shared between the ring buffers used to hold data for each active connection and the general-purpose memory required by the Bluetooth stack.

4.2 Internal ROM

CSR1001 QFN has 64KB of internal ROM. This memory is provided for system firmware implementation. If the internal ROM holds valid program code, on boot-up, this is copied into the program RAM.

4.3 Microcontroller

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and external interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

4.4 Programmable I/O Ports, PIO and AIO

32 lines of programmable bidirectional I/O are provided. They are all powered from VDD_PADS.

PIO lines are software-configurable as weak pull-up, weak pull-down, strong pull-up or strong pull-down.

Note:

At reset all PIO lines are inputs with weak pull-downs.

Any of the PIO lines can be configured as interrupt request lines or to wake the IC from deep sleep mode. Table 4.1 lists the options for waking the IC from the sleep modes.

Sleep Mode	Wake-up Options
Dormant	Can only be woken by the WAKE pin.
Hibernate	Can be woken by the WAKE pin or by the watchdog timer.
Deep Sleep	Can be woken by any PIO configured to wake the IC.

Table 4.1: Wake Options for Sleep Modes

The CSR1001 QFN supports alternative functions on the PIO lines:

- SPI interface, see Section 1.2 and Section 5.4
- UART, see Section 1.2 and Section 5.1.1
- LED flasher / PWM module, see Section 4.5

Note:

CSR cannot guarantee that the PIO assignments remain as described. Implementation of the PIO lines is firmware build-specific, for more information see the relevant software release note.

CSR1001 QFN has 3 general-purpose analogue interface pins, AIO[2:0].

4.5 LED Flasher / PWM Module

CSR1001 QFN contains a LED flasher / PWM module that works in sleep modes.

These functions are controlled by the on-chip firmware.

4.6 Temperature Sensor

CSR1001 QFN contains a temperature sensor that measures the temperature of the die to an accuracy of 1 °C.

4.7 Battery Monitor

CSR1001 QFN contains an internal battery monitor that reports the battery voltage to the software.

5 Serial Interfaces

5.1 Application Interface

5.1.1 UART Interface

The CSR1001 QFN UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

2 signals implement the UART function, UART_TX and UART_RX. When CSR1001 QFN is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices.

UART configuration parameters, e.g. baud rate and data format, are set using CSR1001 QFN firmware.

When selected in firmware PIO[0] is assigned to a UART_TX output and PIO[1] is assigned to a UART_RX input, see Section 1.2.

The UART CTS and RTS signals can be assigned to any PIO pin by the on-chip firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

Table 5.1 shows the possible UART settings for the CSR1001 QFN.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	2Mbaud (≤1%Error)
Flow control		CTS / RTS
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 5.1: Possible UART Settings

5.1.1.1 UART Configuration While in Deep Sleep

The maximum baud rate is 9600 baud during deep sleep.

5.2 Master I²C Interface

The master I²C interface communicates to EEPROM, external peripherals or sensors. An external EEPROM connection can hold the program code externally to the CSR1001 QFN. The maximum clock speed is 400kHz.

Figure 5.1 shows an example of an EEPROM connected to the I²C interface where I2C_SCL, I2C_SDA and PIO[2] are connected to the external EEPROM. The PIO[2] pin supplies the power to the EEPROM supply pin, e.g. VDD. At boot-up, if there is no valid ROM image in the CSR1001 QFN ROM area the CSR1001 QFN tries to boot from the I²C interface, see Figure 5.3. This involves reading the code from the external EEPROM and loading it into the internal CSR1001 QFN RAM.

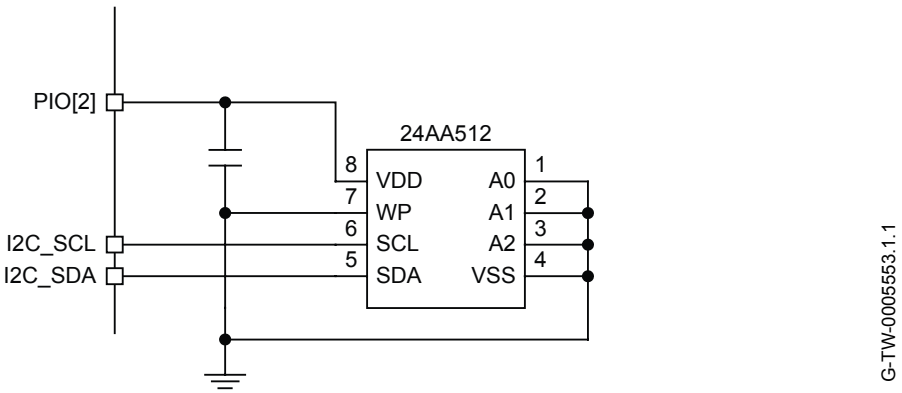


Figure 5.1: Example of an I²C Interface EEPROM Connection

5.3 SPI Master Interface

The SPI master memory interface in the CSR1001 QFN is overlaid on the I²C interface and uses a further 3 PIOs for the extra pins, see Table 5.2.

SPI Flash Interface	Pin
Flash_VDD	PIO[2]
SF_DIN	PIO[3]
SF_CS#	PIO[4]
SF_CLK	I2C_SCL
SF_DOUT	I2C_SDA

Table 5.2: SPI Master Serial Flash Memory Interface

Note:

If an application using CSR1001 QFN is designed to boot from SPI serial flash, it is possible for the firmware to map the I²C interface to alternative PIOs.

Figure 5.2 shows simple SPI timing diagram.

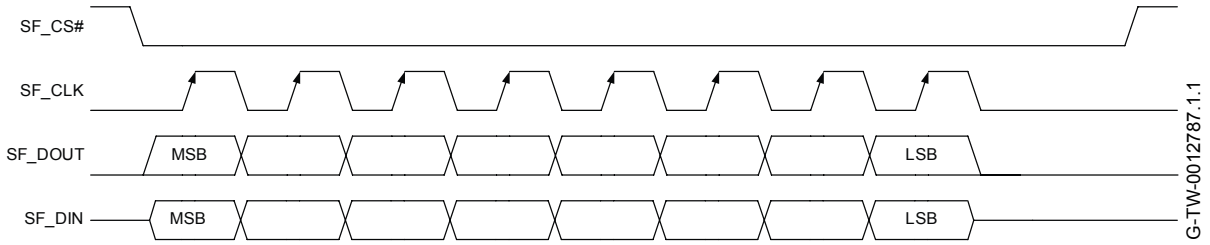


Figure 5.2: SPI Timing Diagram

The boot-up sequence for CSR1001 QFN is controlled by hardware and firmware. Figure 5.3 shows the sequence of loading RAM with content from RAM, EEPROM and SPI serial flash.

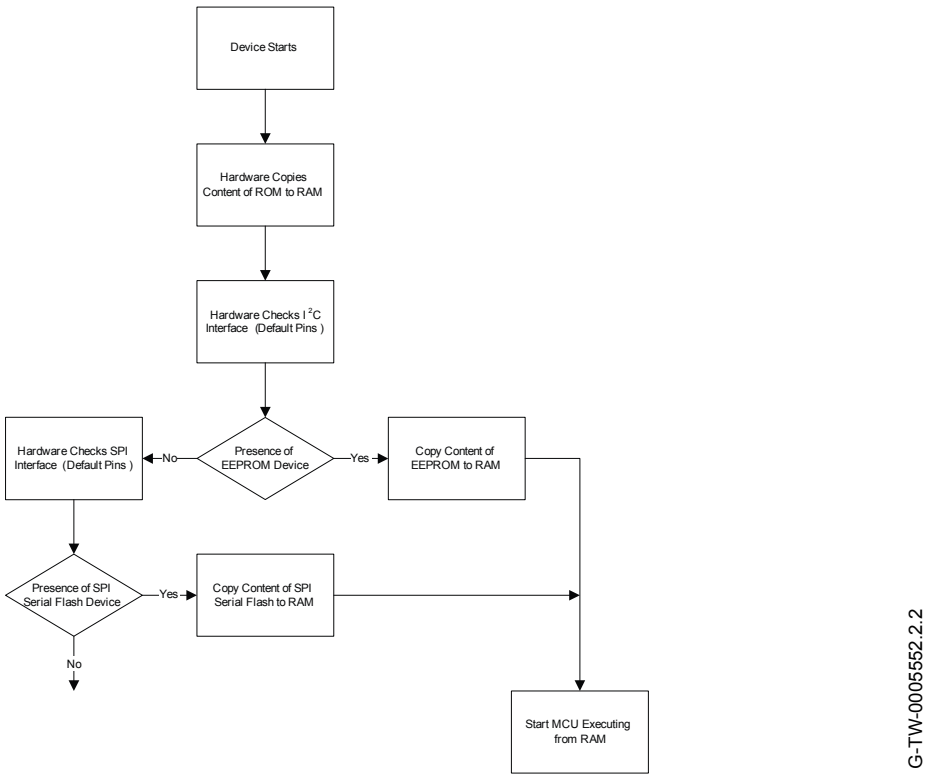


Figure 5.3: Memory Boot-up Sequence

5.4 Programming and Debug Interface

Important Note:

The CSR1001 QFN debug SPI interface is available in SPI slave mode to enable an external MCU to program and control the CSR1001 QFN, generally via libraries or tools supplied by CSR. The protocol of this interface is proprietary. The 4 SPI debug lines directly support this function.

The SPI programs, configures and debugs the CSR1001 QFN. It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header.

Take SPI_PIO#_SEL high to enable the SPI debug feature on PIO[8:5].

CSR1001 QFN uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

Data is written or read one word at a time, or the auto-increment feature is available for block access.

5.4.1 Instruction Cycle

The CSR1001 QFN is the slave and receives commands on DEBUG_MOSI and outputs data on DEBUG_MISO. Table 5.3 shows the instruction cycle for a SPI transaction.

1	Reset the SPI interface	Hold DEBUG_CS# high for 2 DEBUG_CLK cycles
2	Write the command word	Take DEBUG_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take DEBUG_CS# high

Table 5.3: Instruction Cycle for a SPI Transaction

With the exception of reset, DEBUG_CS# must be held low during the transaction. Data on DEBUG_MOSI is clocked into the CSR1001 QFN on the rising edge of the clock line DEBUG_CLK. When reading, CSR1001 QFN replies to the master on DEBUG_MISO with the data changing on the falling edge of the DEBUG_CLK. The master provides the clock on DEBUG_CLK. The transaction is terminated by taking DEBUG_CS# high.

The auto increment operation on the CSR1001 QFN cuts down on the overhead of sending a command word and the address of a register for each read or write, especially when large amounts of data are to be transferred. The auto increment offers increased data transfer efficiency on the CSR1001 QFN. To invoke auto increment, DEBUG_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word written or read.

5.4.2 Multi-slave Operation

Do not connect the CSR1001 QFN in a multi-slave arrangement by simple parallel connection of slave MISO lines. When CSR1001 QFN is deselected (DEBUG_CS# = 1), the DEBUG_MISO line does not float. Instead, CSR1001 QFN outputs `0` if the processor is running or `1` if it is stopped.

6 Power Control and Regulation

CSR1001 QFN contains 2 regulators:

- 1 switch-mode regulator, which generates the main supply rail from the battery
- 1 low-voltage linear regulator

Figure 6.1 shows the configuration for the power control and regulation with the CSR1001 QFN.

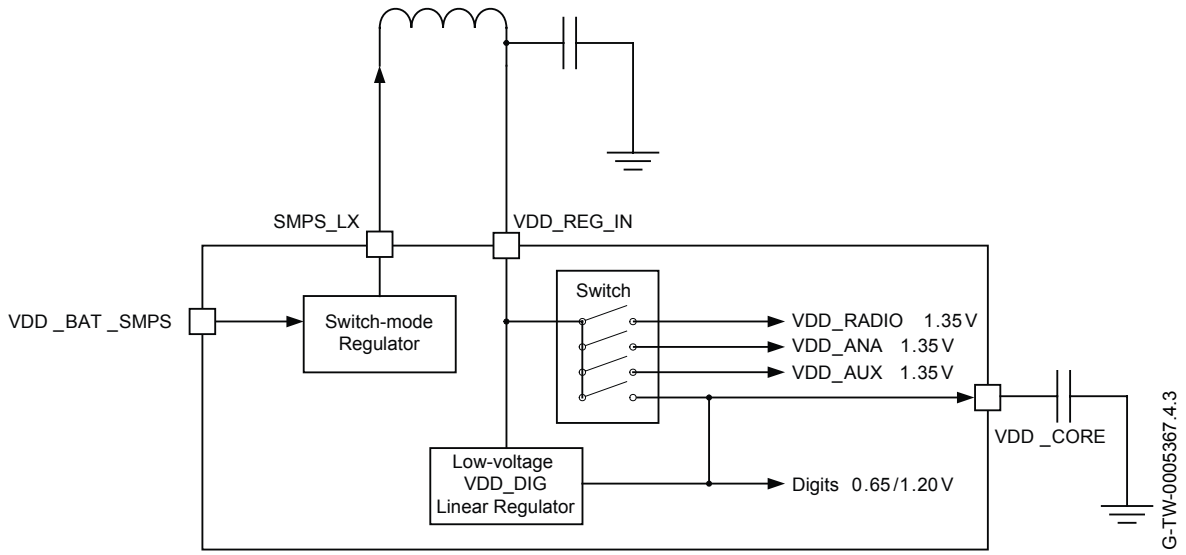


Figure 6.1: Voltage Regulator Configuration

6.1 Switch-mode Regulator

The switch-mode regulator generates the main rail from the battery supply, VDD_BAT_SMPS. The main rail supplies the lower regulated voltage to a further digital linear regulator and also to the analogue sections of the CSR1001 QFN.

The switch-mode regulator generates typically 1.35V.

6.2 Low-voltage VDD_DIG Linear Regulator

The integrated low-voltage VDD_DIG linear regulator powers the CSR1001 QFN digital circuits. The input voltage range is 0.65V to 1.35V. It can supply programmable voltages of 0.65V to 1.20V to the digital area of the CSR1001 QFN. The maximum output current for this regulator is 30mA.

Connect a minimum 470nF low ESR capacitor, e.g. MLC, to the VDD_CORE output pin. Software controls the output voltage.

Important Note:

This regulator is only for CSR internal use. Section 7 shows CSR's recommended circuit connection.

6.3 Reset

CSR1001 QFN is reset by:

- Power-on reset
- Software-configured watchdog timer

6.3.1 Digital Pin States on Reset

Table 6.1 shows the pin states of CSR1001 QFN on reset. PU and PD default to weak values unless specified otherwise.

Pin Name / Group	On Reset
I2C_SDA	Strong PU
I2C_SCL	Strong PU
PIO[31:0]	Weak PD

Table 6.1: Pin States on Reset

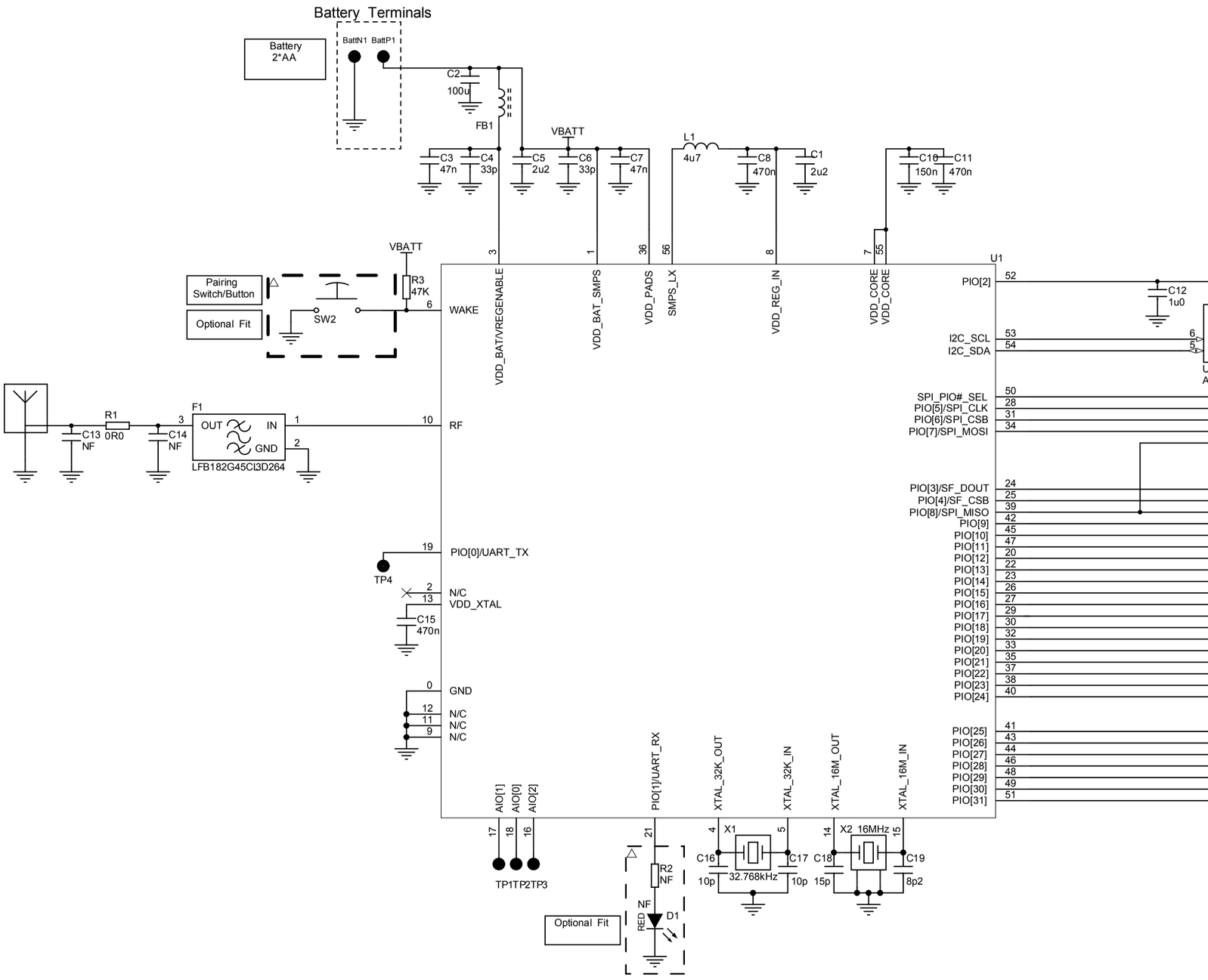
6.3.2 Power-on Reset

Table 6.2 shows how the power-on reset occurs.

Power-on Reset	Typ	Unit
Reset release on VDD_DIG rising	1.05	V
Reset assert on VDD_DIG falling	1.00	
Reset assert on VDD_DIG falling (Sleep mode)	0.60	
Hysteresis	50	mV

Table 6.2: Power-on Reset

7 Example Application Schematic



8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Rating	Min	Max	Unit
Storage temperature	-40	85	°C
Battery (VDD_BAT) operation[a]	1.8	3.6	V
I/O supply voltage	-0.4	3.6	V
Other terminal voltages[b]	VSS - 0.4	VDD + 0.4	V

[a] CSR1001 QFN is reliable and qualifiable to 4.2V, but there will be minor deviations in performance relative to published performance values for 1.8V to 3.6V.

[b] VDD = Terminal Supply Domain.

8.2 Recommended Operating Conditions

Operating Condition	Min	Typ	Max	Unit
Operating temperature range	-30	-	85	°C
Battery (VDD_BAT) operation[a]	1.8	-	3.6	V
I/O supply voltage (VDD_PADS)[b]	1.2	-	3.6	V

[a] CSR1001 QFN is reliable and qualifiable to 4.2V, but there will be minor deviations in performance relative to published performance values for 1.8V to 3.6V.

[b] Safe to 4.2V if VDD_BAT = 4.2V.

8.3 Input/Output Terminal Characteristics

8.3.1 Switch-mode Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	1.8	-	3.6	V
Output voltage	0.65	1.35	1.35	V
Temperature coefficient	-200	-	200	ppm/°C
Normal Operation				
Output noise, frequency range 100Hz to 100kHz	-	-	0.4	mV rms
Settling time, settling to within 10% of final value	-	-	30	µs
Output current (I_{max})	-	-	50	mA
Quiescent current (excluding load, I_{load} < 1mA)	-	-	20	µA
Ultra Low-power Mode				
Output current (I_{max})	-	-	100	µA
Quiescent current	-	-	1	µA

8.3.2 Low-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	0.65	-	1.35	V
Output voltage	0.65	-	1.20	V

Important Note:

This regulator is only for CSR internal use. Section 7 shows CSR's recommended circuit connection.

8.3.3 Digital Terminals

Input Voltage Levels	Min	Typ	Max	Unit
V_{IL} input logic level low	-0.4	-	0.4	V
V_{IH} input logic level high	0.7 x VDD_PADS	-	VDD_PADS + 0.4	V
T_r/T_f	-	-	25	ns

Output Voltage Levels	Min	Typ	Max	Unit
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 x VDD_PADS	-	-	V
T_r/T_f	-	-	5	ns

Input and Tristate Currents	Min	Typ	Max	Unit
With strong pull-up	-150	-40	-10	µA
I²C with strong pull-up	-250	-	-	µA
With strong pull-down	10	40	150	µA
With weak pull-up	-5.0	-1.0	-0.33	µA
With weak pull-down	0.33	1.0	5.0	µA
C_I input capacitance	1.0	-	5.0	pF

8.3.4 AIO

Input/Output Voltage Levels	Min	Typ	Max	Unit
Input voltage	0	-	VDD_AUX	V
Output voltage	0	-	VDD_AUX	V

8.3.4.1 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range[a]		0	-	VDD_AUX	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		1.38	1.69	2.75	µs
Sample rate[b]		-	-	700	Samples/s

[a] LSB size = VDD_AUX/1023

[b] The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

8.3.4.2 Auxiliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	10	Bits
Supply voltage, VDD_ANA	1.30	1.35	1.40	V
Output voltage range	0	-	VDD_AUX	V
Full-scale output voltage	1.30	1.35	1.40	V
LSB size	0	1.32	2.64	mV
Offset	-1.32	0	1.32	mV
Integral non-linearity	-1	0	1	LSB
Settling time	-	-	250	ns

Important Note:

Access to the auxiliary DAC is firmware-dependent, for more information about its availability contact CSR.

8.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 8.1 shows the ESD handling maximum ratings.

Condition	Class	Max Rating
Human Body Model Contact Discharge per JEDEC EIA/JESD22-A114	2	2000V (all pins)
Machine Model Contact Discharge per JEDEC EIA/JESD22-A115	200V	200V (all pins)
Charged Device Model Contact Discharge per JEDEC EIA/JESD22-C101	III	500V (all pins)

Table 8.1: ESD Handling Ratings

9 Current Consumption

Table 9.1 shows CSR1001 QFN total typical current consumption measured at the battery.

Mode	Description	Total Typical Current at 3V
Dormant	All functions are shut down. To wake them up, toggle the WAKE pin.	<600nA
Hibernate	VDD_PADS = ON, REFCLK = OFF, SLEEPCLK = ON, VDD_BAT = ON	<1.5µA
Deep sleep	VDD_PADS = ON, REFCLK = OFF, SLEEPCLK = ON, VDD_BAT = ON, RAM = ON, digital circuits = ON, SMPS = ON (low-power mode), 1ms wake-up time	<5µA
Idle	VDD_PADS = ON, REFCLK = ON, SLEEPCLK = ON, VDD_BAT = ON, RAM = ON, digital circuits = ON, MCU = IDLE, <1µs wake-up time	~1mA
RX / TX active	-	~16mA @ 3V peak current

Table 9.1: Current Consumption

10 CSR Green Semiconductor Products and RoHS Compliance

CSR confirms that CSR Green semiconductor products comply with the following regulatory requirements:

- Restriction on Hazardous Substances directive guidelines in the EU RoHS Directive 2011/65/EU[1].
- EU REACH, Regulation (EC) No 1907/2006[1]:
  - List of substances subject to authorisation (Annex XIV)
  - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
  - When requested by customers, notification of substances identified on the Candidate List as Substances of Very High Concern (SVHC)[1].
- POP regulation (EC) No 850/2004[1]
- EU Packaging and Packaging Waste, Directive 94/62/EC[1]
- Montreal Protocol on substances that deplete the ozone layer.
- Conflict minerals, Section 1502, Dodd-Frank Wall Street Reform and Consumer Protection act, which affects columbite-tantalite (coltan / tantalum), cassiterite (tin), gold, wolframite (tungsten) or their derivatives. CSR is a fabless semiconductor company: all manufacturing is performed by key suppliers. CSR have mandated that the suppliers shall not use materials that are sourced from "conflict zone mines" but understand that this requires accurate data from the EICC programme. CSR shall provide a complete EICC / GeSI template upon request.

CSR has defined the "CSR Green" standard based on current regulatory and customer requirements including free from bromine, chlorine and antimony trioxide.

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

This identifies the main environmental compliance regulatory restrictions CSR specify. For more information on the full "CSR Green" standard, contact product.compliance@csr.com.

[1] Including applicable amendments to EU law which are published in the EU Official Journal, or SVHC Candidate List updates published by the European Chemicals Agency (ECHA).

11 CSR1001 QFN Software Stack

CSR1001 QFN is supplied with Bluetooth v4.0 specification compliant stack firmware. Figure 11.1 shows that the CSR1001 QFN software architecture enables the Bluetooth processing and the application program to run on the internal RISC MCU.

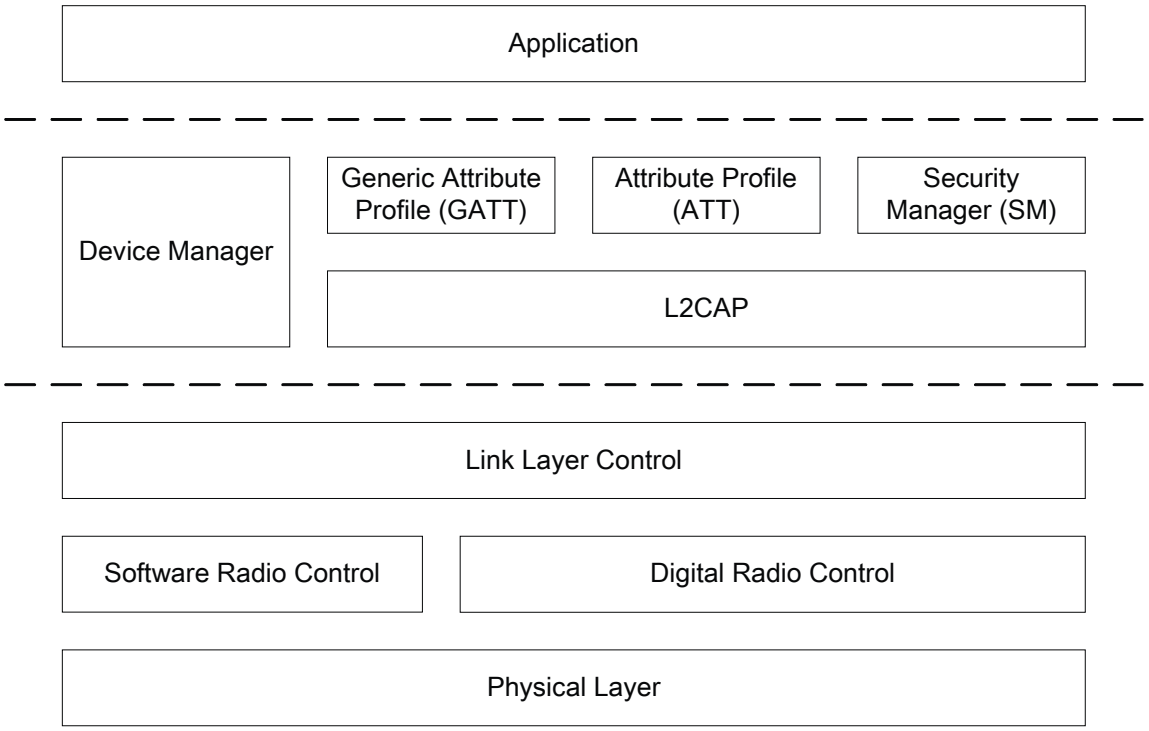


Figure 11.1: Software Architecture

12 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

12.1 Tape Orientation

Figure 12.1 shows the CSR1001 QFN packing tape orientation.

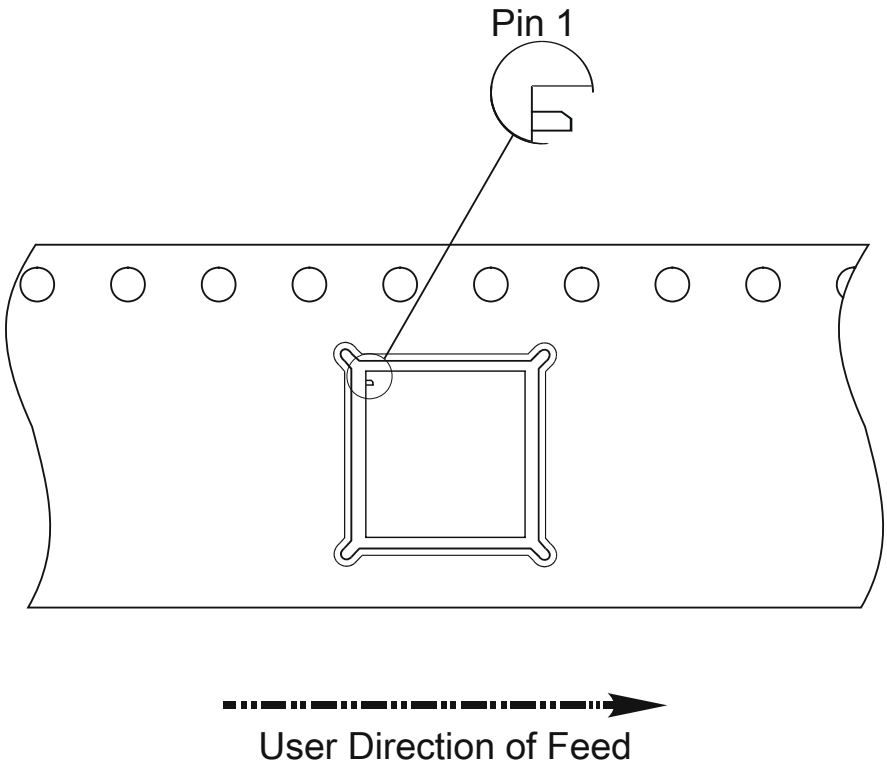


Figure 12.1: Tape Orientation

G-TW-0002812.2.2

12.2 Tape Dimensions

Figure 12.2 shows the dimensions of the tape for the CSR1001 QFN.

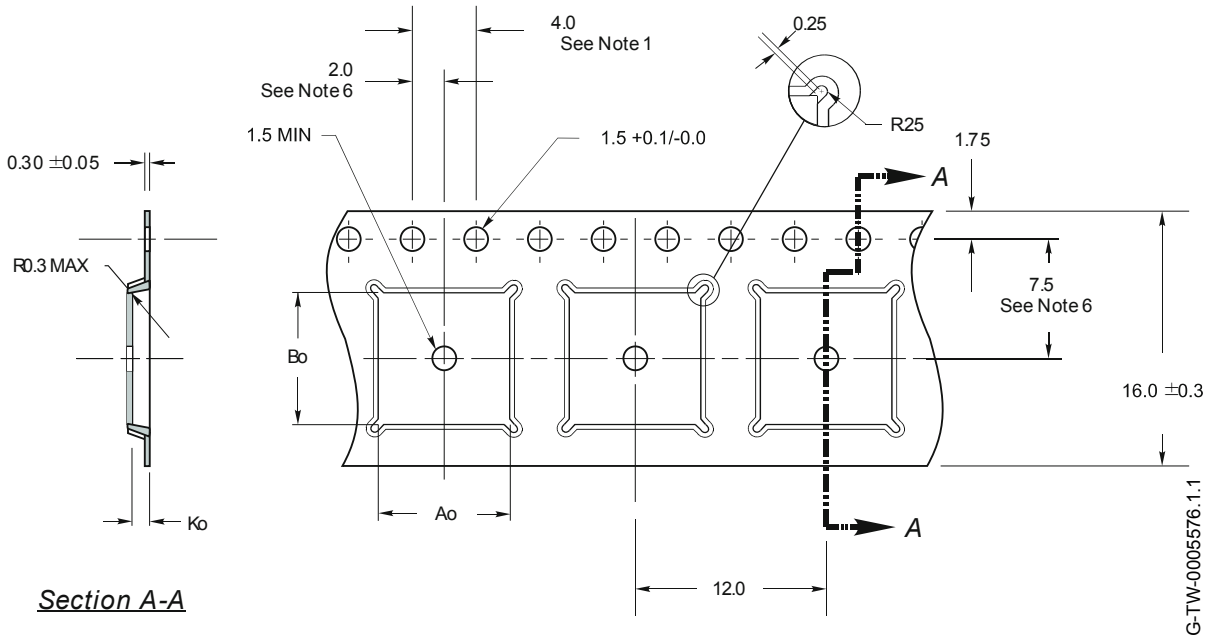


Figure 12.2: Tape Dimensions

A_0	B_0	K_0	Unit	Notes
8.3	8.3	1.1	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2. 2. Camber not to exceed 1mm in 100mm. 3. Material: PS + C. 4. A_0 and B_0 measured as indicated. 5. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier 6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

12.3 Reel Information

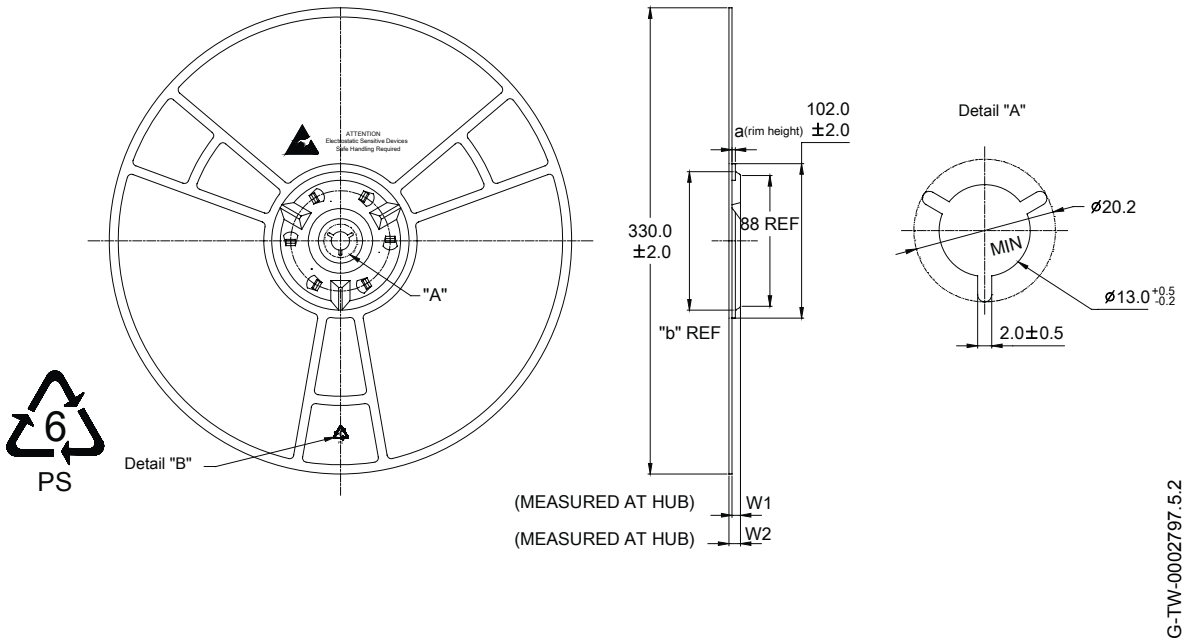


Figure 12.3: Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
8 x 8 x 0.9mm QFN	16	4.5	98.0	16.4 (3.0/-0.2)	19.1	mm

12.4 Moisture Sensitivity Level

CSR1001 QFN is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

13 Document References

Document	Reference, Date
Core Specification of the Bluetooth System.	Bluetooth Specification Version 4.0, 17 December 2009
CSR1001 QFN Performance Specification.	CS-217296-SP
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).	JESD22-A114
Environmental Compliance Statement for CSR Green Semiconductor Products.	CB-001036-ST
IC Packing and Labelling Specification.	CS-112584-SP
Moisture / Reflow Sensitivity Classification for Nonhermitic Solid State Surface Mount Devices.	IPC / JEDEC J-STD-020
Typical Solder Reflow Profile for Lead-free Devices.	CS-116434-AN

Terms and Definitions

Term	Definition
AC	Alternating Current
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
AIO	Analogue Input/Output
ATT	ATTribute protocol
balun	balanced/unbalanced interface or device that changes a balanced output to an unbalanced input or vice versa
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
CSR	Cambridge Silicon Radio
CTS	Clear To Send
dBm	Decibels relative to 1 mW
DC	Direct Current
DNL	Differential Non Linearity (ADC accuracy parameter)
e.g.	*exempli gratia*, for example
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
EIA	Electronic Industries Alliance
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
GAP	Generic Access Profile
GATT	Generic ATTribute protocol
GSM	Global System for Mobile communications
HID	Human Interface Device
I²C	Inter-Integrated Circuit Interface
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
INL	Integral Non-Linearity (ADC accuracy parameter)
IPC	See www.ipc.org

Term	Definition
IQ	In-Phase and Quadrature
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
KB	Kilobyte
L2CAP	Logical Link Control and Adaptation Protocol
LC	An inductor (L) and capacitor (C) network
LED	Light-Emitting Diode
LNA	Low Noise Amplifier
LSB	Least Significant Bit (or Byte)
MAC	Medium Access Control
MCU	MicroController Unit
MISO	Master In Slave Out
MLC	MultiLayer Ceramic
MOSI	Master Out Slave In
NSMD	Non-Solder Mask Defined
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PD	Pull-down
PIO	Parallel Input/Output
PIO	Programmable Input/Output, also known as general purpose I/O
plc	public limited company
ppm	parts per million
PU	Pull-Up
PWM	Pulse Width Modulation
QFN	Quad-Flat No-lead
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)

Term	Definition
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RTS	Request To Send
RX	Receive or Receiver
SIG	(Bluetooth) Special Interest Group
SMP	Security Manager Protocol
SPI	Serial Peripheral Interface
TCXO	Temperature Compensated crystal Oscillator
TV	TeleVision
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator
W-CDMA	Wideband Code Division Multiple Access

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