



**THE DATASHEET OF
CSP2510CPG8**





3.3V PHASE-LOCK LOOP CLOCK DRIVER ZERO DELAY BUFFER

IDTCSP2510C

FEATURES:

- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes one clock input to one bank of ten outputs
- Output enable bank control
- External feedback (FBIN) pin is used to synchronize the outputs to the clock input signal
- No external RC network required for PLL loop stability
- Operates at 3.3V V_{DD}
- t_{pd} Phase Error at 133MHz: < ±150ps
- Jitter (peak-to-peak) at 133MHz: < ±75ps @ 133MHz
- Spread Spectrum Compatible
- Operating frequency 25MHz to 140MHz
- Available in 24-Pin TSSOP package

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

DESCRIPTION:

The CSP2510C is a high performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (F_{OUT}) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CSP2510C operates at 3.3V.

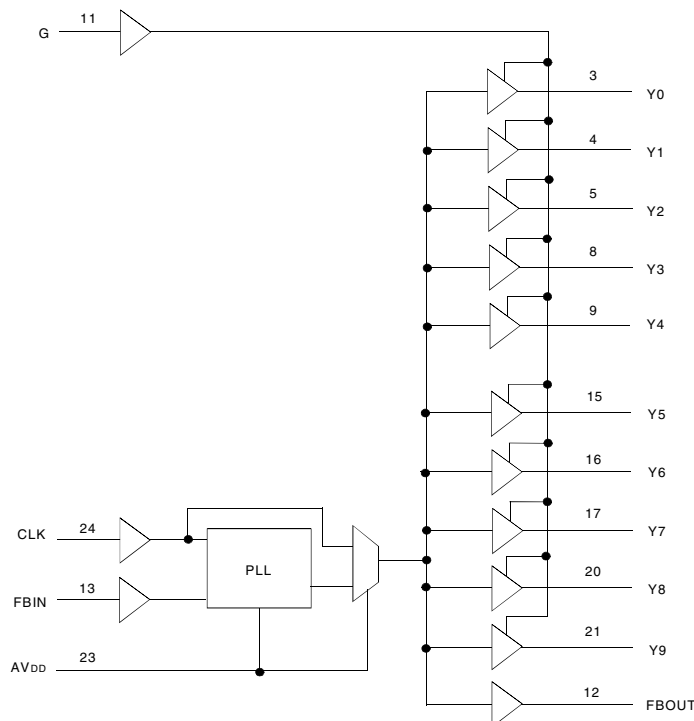
One bank of ten outputs provide low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. The outputs can be enabled or disabled via the control G input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CSP2510C does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CSP2510C requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for the test purposes by strapping AV_{DD} to ground.

The CSP2510C is specified for operation from 0°C to +85°C. This device is also available (on special order) in Industrial temperature range (-40°C to +85°C). See ordering information for details.

FUNCTIONAL BLOCK DIAGRAM

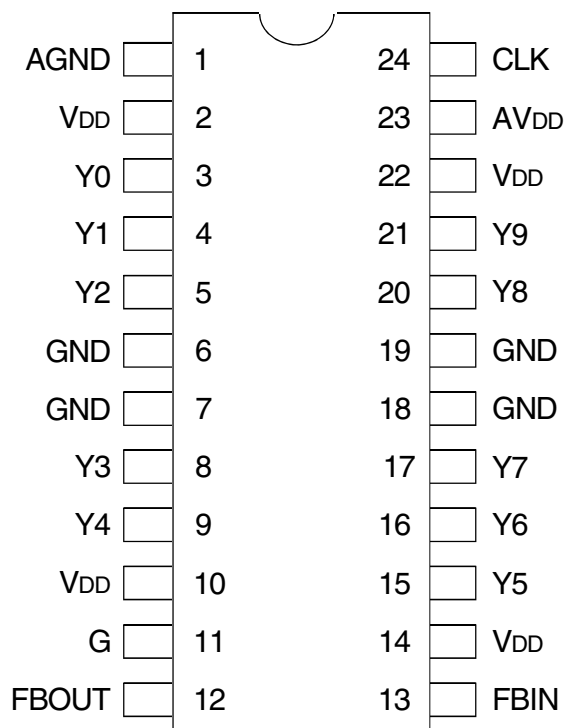


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

0°C TO 85°C TEMPERATURE RANGE

NOVEMBER 2008

PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Max | Unit |
|--|--|-------------------------------|------|
| V _{DD} | Supply Voltage Range | -0.5 to +4.6 | V |
| V _I ⁽¹⁾ | Input Voltage Range | -0.5 to +6.5 | V |
| V _O ^(1,2) | Voltage range applied to any output in the high or low state | -0.5 to V _{DD} + 0.5 | V |
| I _{IK} (V _I < 0) | Input clamp current | -50 | mA |
| I _{OK} (V _O < 0 or V _O > V _{DD}) | Terminal Voltage with Respect to GND (inputs V _{IH} 2.5, V _{IL} 2.5) | ±50 | mA |
| I _O (V _O = 0 to V _{DD}) | Continuous Output Current | ±50 | mA |
| V _{DD} or GND | Continuous Current | ±100 | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _J | Junction Temperature | +150 | °C |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

CAPACITANCE

| Parameter | Description | Min. | Typ. | Max. | Unit |
|-----------------|---|------|------|------|------|
| C _{IN} | Input Capacitance V _I = V _{DD} or GND | — | 5 | — | pF |
| C _O | Output Capacitance V _O = V _{DD} or GND | — | 6 | — | pF |
| C _L | Load Capacitance | — | 30 | — | pF |

NOTE:

- Unused inputs must be held HIGH or LOW to prevent them from floating.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Description | Min. | Max. | Unit |
|------------------------------------|--------------------------------|------|------|------|
| V _{DD} , AV _{DD} | Power Supply Voltage | 3 | 3.6 | V |
| T _A | Operating Free-Air Temperature | 0 | +85 | °C |

PIN DESCRIPTION

| Terminal | | Type | Description |
|----------|-----------------------------------|--------|---|
| Name | No. | | |
| CLK | 24 | I | Clock input. CLK provides the clock signal to be distributed by the CSP2510C clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal. |
| FBIN | 13 | I | Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN. |
| G | 11 | I | Output bank enable. G is the output enable for outputs Y(0:9). When G is low, outputs Y(0:9) are disabled to a logic-low state. When G is high, all outputs Y(0:9) are enabled and switch at the same frequency as CLK. |
| FBOUT | 12 | O | Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. |
| Y (0:9) | 3, 4, 5, 8, 9, 15, 16, 17, 20, 21 | O | Clock outputs. These outputs provide low-skew copies of CLK. Output bank Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by de-asserting the G control input. |
| AVDD | 23 | Power | Analog power supply. AVDD provides the power reference for the analog circuitry. In addition, AVDD can be used to bypass the PLL for test purposes. When AVDD is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. |
| AGND | 1 | Ground | Analog ground. AGND provides the ground reference for the analog circuitry. |
| VDD | 2, 10, 14, 22 | Power | Power supply |
| GND | 6, 7, 18, 19 | Ground | Ground |

STATIC FUNCTION TABLE (AVDD = 0V)

| Inputs | | Outputs | |
|--------|---------|---------|---------|
| G | CLK | Y (0:9) | FBOUT |
| L | L | L | L |
| L | H | L | H |
| H | H | H | H |
| H | L | L | L |
| H | running | running | running |

DYNAMIC FUNCTION TABLE (AVDD = 3.3V)

| Inputs | | Outputs | |
|--------|---------|---------------------------|---------------------------|
| G | CLK | Y (0:9) | FBOUT |
| X | L | L | L |
| L | running | L | running in phase with CLK |
| L | H | L | H |
| H | running | running in phase with CLK | running in phase with CLK |
| H | H | H | H |

DC ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE⁽¹⁾

| Symbol | Description | Test Conditions | V _{DD} | Min. | Typ. ⁽²⁾ | Max. | Unit |
|---------------------------------|---------------------------------------|--|-------------------------|-----------------------|---------------------|------|------|
| V _{IK} | Input Clamp Voltage | I _I = -18mA | 3V | — | — | -1.2 | V |
| V _{IH} | Input HIGH Level | | — | 2 | — | — | V |
| V _{IL} | Input LOW Level | | — | — | — | 0.8 | V |
| V _{OH} | HIGH Level Output Voltage | I _{OH} = -100μA | Min. to Max. | V _{DD} - 0.2 | — | — | V |
| | | I _{OH} = -12mA | 3V | 2.1 | — | — | |
| | | I _{OH} = -6mA | 3V | 2.4 | — | — | |
| V _{OL} | LOW Level Output Voltage | I _{OL} = 100μA | Min. to Max. | — | — | 0.2 | V |
| | | I _{OL} = 12mA | 3V | — | — | 0.8 | |
| | | I _{OL} = 6mA | 3V | — | — | 0.55 | |
| I _I | Input Current | V _I = V _{DD} or GND | 3.6V | — | — | ±5 | μA |
| I _{DD} | Supply Current | V _I = V _{DD} or GND, AV _{DD} = GND, I _O = 0, Outputs: LOW or HIGH | 3.6V | — | — | 10 | μA |
| ΔI _{DD} | Change in Supply Current | One input at V _{DD} - 0.6V, other inputs at V _{DD} or GND | 3.3V to 3.6V | — | — | 500 | μA |
| C _{PD} | Power Dissipation Capacitance | | 3.6V | — | 10 | 14 | pF |
| I _{DDA} ⁽³⁾ | AV _{DD} Power Supply Current | | AV _{DD} = 3.3V | — | 10 | — | mA |

NOTES:

- For Industrial devices, operating free-air temperature = -40°C to +85°C.
- For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
- For I_{DD} of AV_{DD}, see TYPICAL CHARACTERISTICS.

TIMING REQUIREMENTS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE⁽¹⁾

| | | Min. | Max. | Unit |
|------------------|-----------------------------------|------|------|------|
| f _{CLK} | Clock frequency | 25 | 140 | MHz |
| | Input clock duty cycle | 40% | 60% | |
| | Stabilization time ⁽²⁾ | — | 1 | ms |

NOTES:

- For Industrial devices, operating free-air temperature = -40°C to +85°C.
- Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, $C_L = 30\text{pF}^{(1)}$

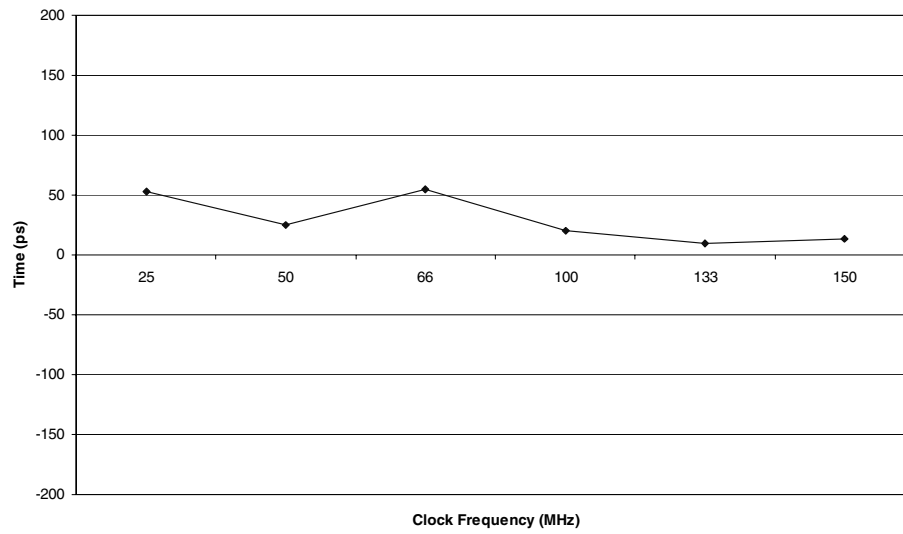
| Parameter ⁽²⁾ | From (Input) | To (Output) | $V_{DD} = 3.3V \pm 0.3V$ | | | Unit |
|--|--|-------------------------|--------------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $t_{\text{PHASE error}}$ | $100\text{MHz} < \text{CLK}\uparrow < 133\text{MHz}$ | $\text{FBIN}\uparrow$ | -150 | — | 150 | ps |
| $t_{\text{PHASE error-jitter}}^{(3)}$ | $\text{CLK}\uparrow = 133\text{MHz}$ | $\text{FBIN}\uparrow$ | -50 | — | 50 | ps |
| $t_{\text{SK}(o)}^{(4)}$ | Any Y (133MHz) | Any Y | — | — | 150 | ps |
| Jitter (cycle-cycle) (peak-to-peak) | $\text{CLK} = 133\text{MHz}$ | Any Y or FBOUT | -75 | — | 75 | ps |
| Duty cycle reference ⁽⁵⁾ | $\text{CLK} = 133\text{MHz}$ | Any Y or FBOUT | 45 | — | 55 | % |
| t_R | | Any Y or FBOUT | 0.8 | — | 2.1 | ns |
| t_F | | Any Y or FBOUT | 0.8 | — | 2.7 | ns |

NOTES:

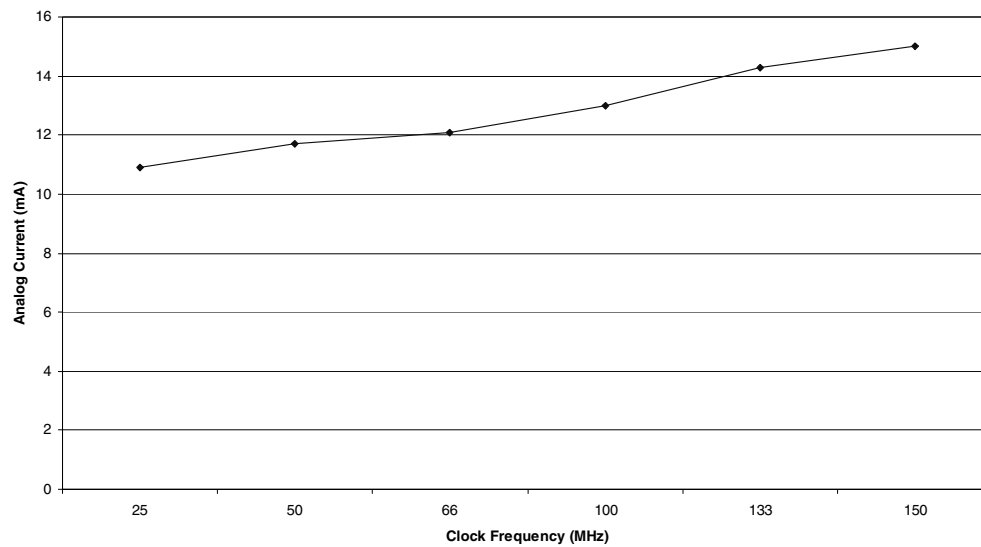
1. For Industrial devices, operating free-air temperature = -40°C to +85°C. See PARAMETER MEASUREMENT INFORMATION.
2. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
3. Phase error does not include jitter.
4. The $t_{\text{SK}(o)}$ specification is only valid for equal loading of all outputs.
5. See TYPICAL CHARACTERISTICS.

TYPICAL CHARACTERISTICS

Phase Error vs Clock Frequency
AV_{DD} and V_{DD} = 3.3V
T_a = 25°C

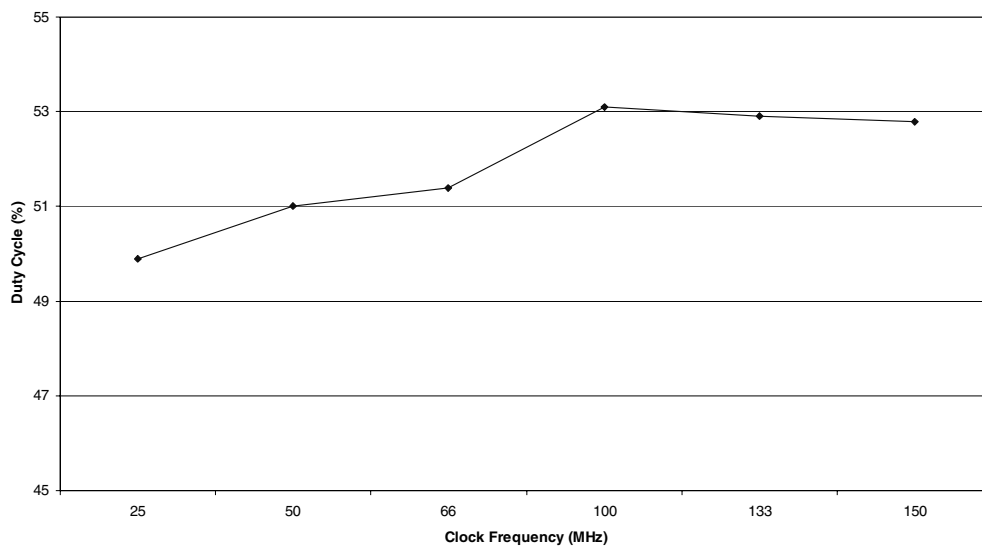


Analog Supply Current vs. Clock Frequency
AV_{DD} and V_{DD} = 3.3V
T_a = 25°C

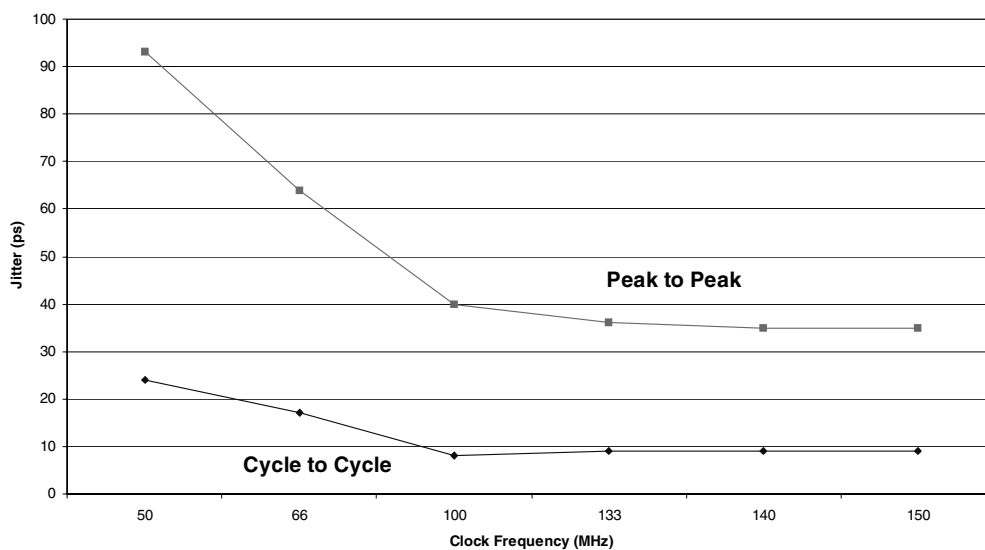


TYPICAL CHARACTERISTICS (CONT.)

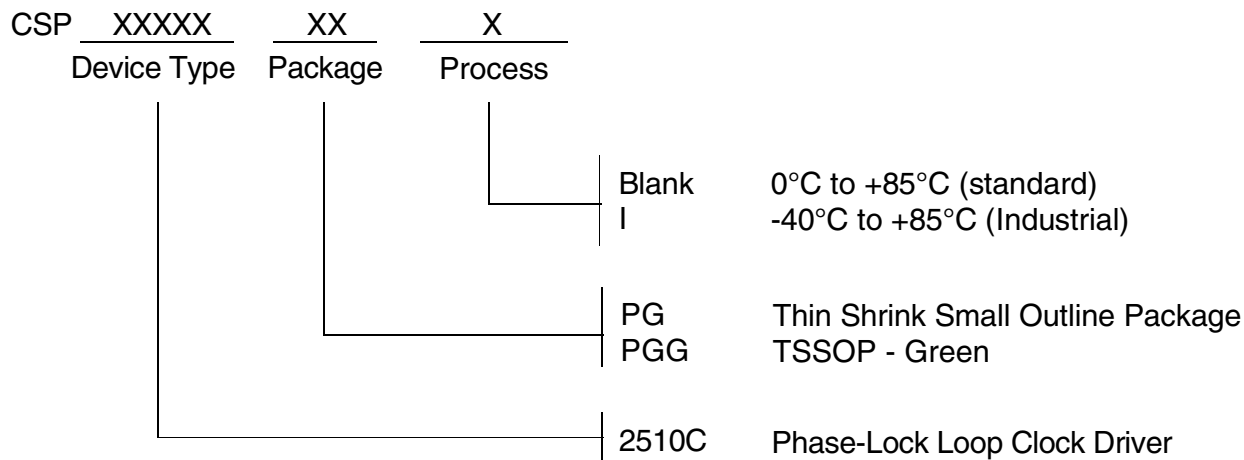
Output Duty Cycle vs Clock Frequency
AV_{DD} and V_{DD} = 3.3V
Ta = 25C



Jitter vs Clock Frequency
Av_{CC} and V_{CC} = 3.3V
Ta = 25C



ORDERING INFORMATION



CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
logichelp@idt.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View CSP2510CPG8 on WIN SOURCE](#)
- ⊖ [IDT, Integrated Device Technology Inc Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management