# THE DATASHEET OF

# SIGC100T60R3EX1SA1

# IGBT

TRENCHSTOP™ IGBT3 Chip

# SIGC100T60R3E

Data Sheet

Industrial Power Control

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# SIGC100T60R3E

## TRENCHSTOP™ IGBT3 Chip

**Features:**

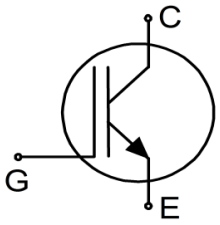
- 600V trench & field stop technology
- Low $V_{CEsat}$
- Low turn-off losses
- Short tail current
- Positive temperature coefficient
- Easy paralleling

**Recommended for:**

- Power modules
- Discrete components

**Applications:**

- Drives
- White goods
- Resonant applications




| Chip Type | $V_{CE}$ | $I_{Cn}$ | Die Size | Package |
|---|---|---|---|---|
| SIGC100T60R3E | 600V | 200A | 9.73mm x 10.23mm | Sawn on foil |

**Mechanical Parameters**

| | | | |
|---|---|---|---|
| Die size | | 9.73 x 10.23 | $mm^2$ |
| Emitter pad size | | See chip drawing | |
| Gate pad size | | 1.62 x 0.82 | |
| Area total | | 99.54 | |
| Silicon thickness | | 70 | µm |
| Wafer size | | 200 | mm |
| Maximum possible chips per wafer | | 254 | |
| Passivation frontside | | Photoimide | |
| Pad metal | | 3200nm AlSiCu | |
| Backside metal | | Ni Ag – system<br>To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process | |
| Die bond | | Electrically conductive epoxy glue and soft solder | |
| Wire bond | | Al, ≤500µm | |
| Reject ink dot size | | ∅ 0.65mm; max. 1.2mm | |
| Storage environment (<6 months) | for original and sealed MBB bags | Ambient atmosphere air, temperature 17°C – 25°C | |
| | for open MBB bags | Acc. IEC 62258-3; Section 9.4 Storage Environment. | |

## Maximum Ratings

**In general, from reliability and lifetime point of view, the lower the operation junction temperature and/or the applied voltage, the greater the expected lifetime of any semiconductor device.**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Collector-emitter voltage, $T_{vj}$=25°C | $V_{CE}$ | 600 | V |
| DC collector current, limited by $T_{vj\,max}$ [1] | $I_C$ | - | A |
| Pulsed collector current, $t_p$ limited by $T_{vj\,max}$ [2] | $I_{C,puls}$ | 600 | A |
| Gate-emitter voltage | $V_{GE}$ | ±20 | V |
| Virtual junction temperature | $T_{vj}$ | -40 ... +175 | °C |
| Short circuit data [1/2/3] $V_{GE}$=15V, $V_{CC}$=360V, $T_{vj}$=150°C | $t_{sc}$ | 6 | µs |
| Reverse bias safe operating area (RBSOA) [2] | $I_{C,max}$ = 400A, $V_{CEmax}$ = 600V, $T_{vj} \leq$ 150°C | | |

**Static Characteristics** (tested on wafer), $T_{vj}$=25°C

| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| Collector-emitter breakdown voltage | $V_{(BR)CES}$ | $V_{GE}$=0V, $I_C$=4mA | 600 | - | - | V |
| Collector-emitter saturation voltage | $V_{CEsat}$ | $V_{GE}$=15V, $I_C$=60A | 0.86 | 1.03 | 1.20 | |
| Gate-emitter threshold voltage | $V_{GE(th)}$ | $I_C$=3.2mA, $V_{GE}$=$V_{CE}$ | 5.0 | 5.8 | 6.5 | |
| Zero gate voltage collector current | $I_{CES}$ | $V_{CE}$=600V, $V_{GE}$=0V | - | - | 10.1 | µA |
| Gate-emitter leakage current | $I_{GES}$ | $V_{CE}$=0V, $V_{GE}$=20V | - | - | 600 | nA |
| Integrated gate resistor | $r_G$ | | - | 2 | - | Ω |

**Electrical Characteristics** [2]

| Parameter | | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min. | typ. | max. | |
| Collector-emitter saturation voltage | $T_{vj}$=25°C | $V_{CEsat}$ | $V_{GE}$=15V, $I_C$=200A | - | 1.45 | 1.9 | V |
| | $T_{vj}$=150°C | | | - | 1.7 | - | |
| Input capacitance | | $C_{ies}$ | $V_{CE}$=25V, $V_{GE}$=0V, $f$=1MHz $T_{vj}$=25°C | - | 12335 | - | pF |
| Output capacitance | | $C_{oes}$ | | - | 769 | - | |
| Reverse transfer capacitance | | $C_{res}$ | | - | 366 | - | |

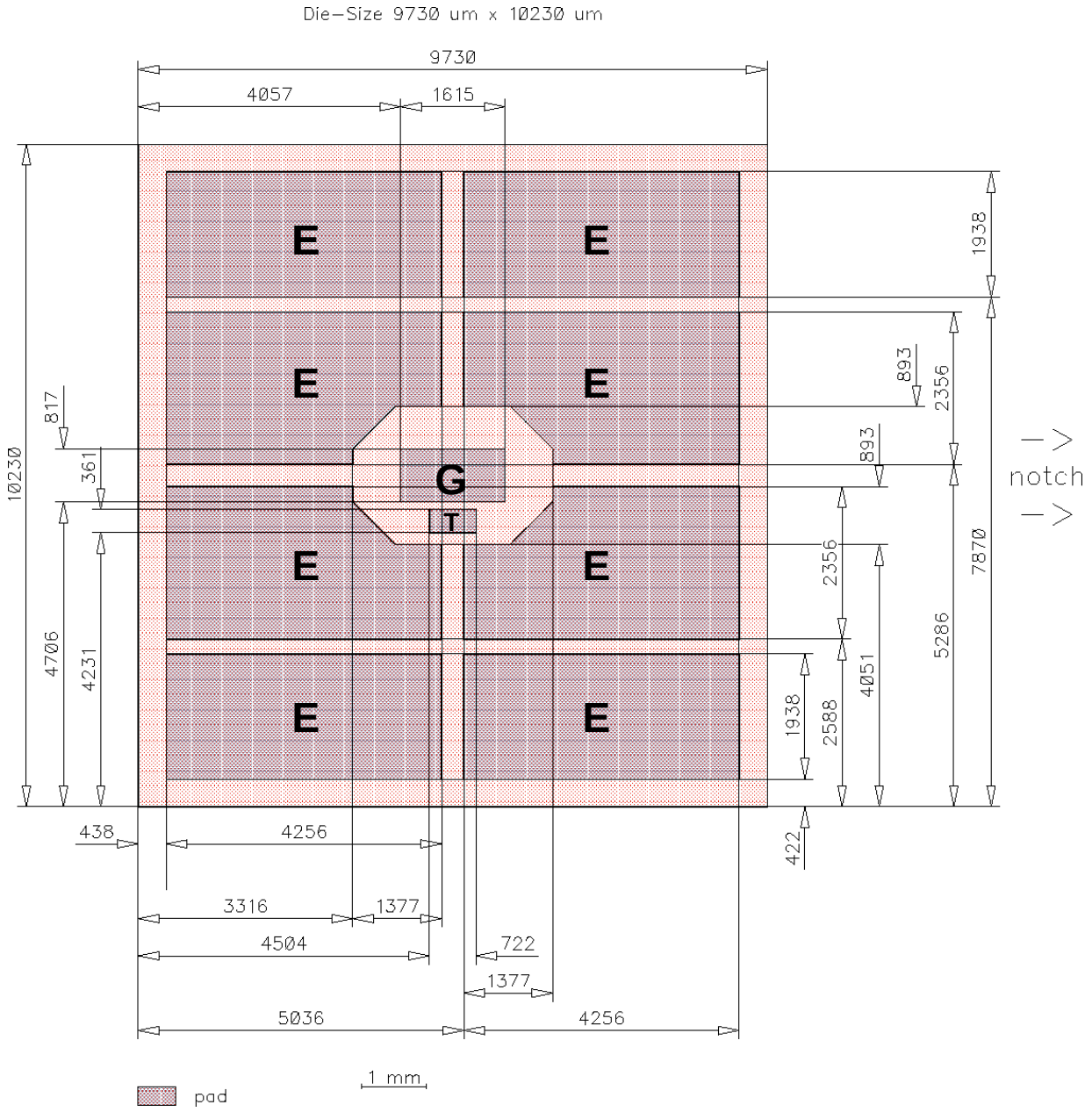
[1] Depending on thermal properties of assembly.
[2] Not subject to production test - verified by design/characterization.
[3] Allowed number of short circuits: <1000; time between short circuits: >1s.

**Further Electrical Characteristics**

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

| | | |
|---|---|---|
| Application example | - | - |

**Chip Drawing**




**E** = Emitter
**G** = Gate
**T** = Test pad do not contact

**Bare Die Product Specifics**

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

**Description**

| |
|---|
| AQL 0.65 for visual inspection according to failure catalogue |
| Electrostatic Discharge Sensitive Device according to MIL-STD 883 |

**Revision History**

| Revision | Subjects (major changes since last revision) | Date |
|---|---|---|
| 2.0 | Release of final datasheet, change of wafer size to 200 mm | 09.04.2010 |
| 2.1 | Additional Basic Type, editorial changes, maximum possible chips per wafer corrected, $V_{CEsat}$ tested at 30% of $I_C$ and additional $V_{CEsat}$ specification at $T_{vj}$ 150°C | 26.07.2017 |
| | | |

**Relevant Application Notes**

| | |
|---|---|
| | |

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