



THE DATASHEET OF STP12IE90F4





STP12IE90F4

Emitter Switched Bipolar Transistor
ESBT[®] 900 V - 12 A - 0.083 Ω

General features

$V_{CS(ON)}$	I_C	$R_{CS(ON)}$
1V	12A	0.083 Ω

- High voltage / high current Cascode configuration
- Low equivalent on resistance
- Very fast-switch up to 150 kHz
- Squared RBSOA up to 900V
- Very low C_{iss} driven by $R_G = 47\Omega$
- Very low turn-off cross over time

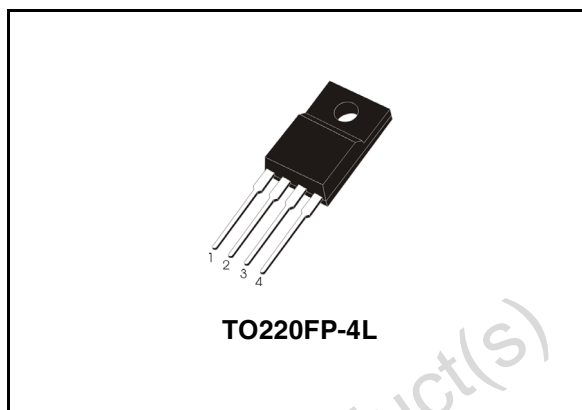
Applications

- Flyback SMPS for adapter
- Flyback / forward SMPS for desktop

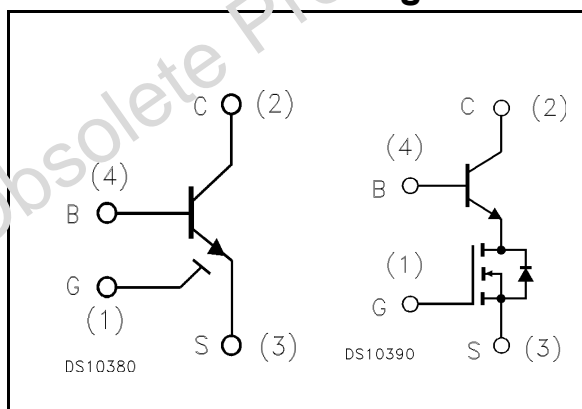
Description

The STP12IE90F4 is manufactured in Monolithic ESBT Technology, aimed to provide best performances in high frequency / high voltage applications.

It is designed for use in Gate Driver, based topologies.



Internal schematic diagrams



Order codes

Part Number	Marking	Package	Packing
STP12IE90F4	P12IE90F4	TO220FP-4L	Tube

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1 Electrical ratings

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
$V_{CS(SS)}$	Collector-source voltage ($V_{BS} = V_{GS} = 0\text{ V}$)	900	V
$V_{BS(OS)}$	Base-source voltage ($I_C = 0, V_{GS} = 0\text{ V}$)	30	V
$V_{SB(OS)}$	Source-base voltage ($I_C = 0, V_{GS} = 0\text{ V}$)	17	V
V_{GS}	Gate-source voltage	± 17	V
I_C	Collector current	12	A
I_{CM}	Collector peak current ($t_P < 5\text{ms}$)	36	A
I_B	Base current	6	A
I_{BM}	Base peak current ($t_P < 5\text{ms}$)	10	A
P_{tot}	Total dissipation at $T_c = 25^\circ\text{C}$	21	W
T_{stg}	Storage temperature	-40 to 150	$^\circ\text{C}$
T_J	Max. operating junction temperature	150	$^\circ\text{C}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	6	$^\circ\text{C/W}$

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 3. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{CS(SS)}	Collector-source current (V _{BS} = V _{GS} = 0)	V _{CE} = 900V			100	μA
I _{BS(OS)}	Base-source current (I _C = 0, V _{GS} = 0)	V _{BS(OS)} = 30V			10	μA
I _{SB(OS)}	Source-base current (I _C = 0, V _{GS} = 0)	V _{SB(OS)} = 17V			100	μA
I _{GS(OS)}	Gate-source leakage	V _{GS} = ± 17V			100	nA
V _{CS(ON)}	Collector-source ON voltage	V _{GS} = 10V I _C = 12A I _B = 2.4A V _{GS} = 10V I _C = 6A I _B = 0.6A		1 0.6		V V
h _{FE}	DC current gain	V _{GS} = 10V I _C = 12A V _{CS} = 1V V _{GS} = 10V I _C = 6A V _{CS} = 1V		5 15		
V _{BS(ON)}	Base Source ON voltage	V _{GS} = 10V I _C = 12A I _B = 2.4A V _{GS} = 10V I _C = 6A I _B = 0.6A		1.5 1.2		V V
V _{GS(th)}	Gate threshold voltage	V _{BS} = V _{GS} I _B = 250μA	2	3	4	V
C _{iss}	Input capacitance	V _{CS} = 25V f = 1MHz V _{GS} = 0V		520		pF
Q _{GS(tot)}	Gate-source Charge	V _{CS} = 25V V _{GS} = 10V V _{CB} = 0V I _C = 4A		21.3		nC
t _s t _f	INDUCTIVE LOAD Storage time Fall time	V _{GS} = 10V R _G = 47Ω V _{Clamp} = 720V t _p = 4μs I _C = 6A I _B = 1.2A		610 10		ns ns
t _s t _f	INDUCTIVE LOAD Storage time Fall time	V _{GS} = 10V R _G = 47Ω V _{Clamp} = 720V t _p = 4μs I _C = 6A I _B = 0.6A		360 10		ns ns
V _{CSW}	Maximum collector-source voltage switched without snubber	R _G = 47Ω h _{FE} = 5 I _C = 12A	900			V

Table 3. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CS(dyn)}$	Collector-source dynamic voltage (500ns)	$V_{CC} = V_{Clamp} = 400V$ $V_{GS} = 10V$ $I_C = 6A$ $I_B = 1.2A$ $t_{peak} = 500ns$ $R_G = 47\Omega$ $I_{Bpeak} = 6A (I_C)$		3.37		V
$V_{CS(dyn)}$	Collector-source dynamic voltage (1 μ s)	$V_{CC} = V_{Clamp} = 400V$ $V_{GS} = 10V$ $I_C = 6A$ $I_B = 1.2A$ $t_{peak} = 500ns$ $R_G = 47\Omega$ $I_{Bpeak} = 6A (I_C)$		1.75		V

2.1 Electrical characteristics (curves)

Figure 1. DC current gain

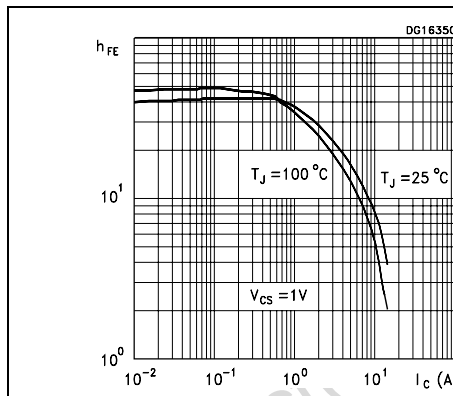


Figure 2. Collector-source On voltage

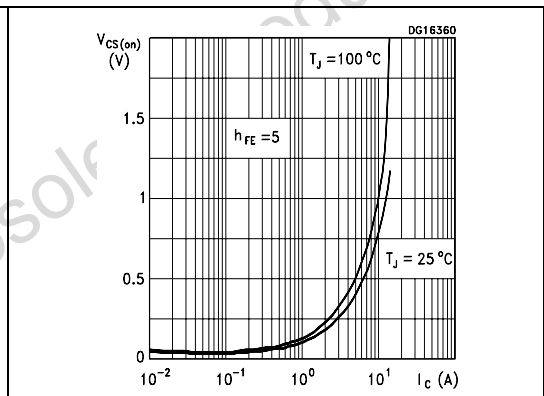


Figure 3. Collector-source On voltage

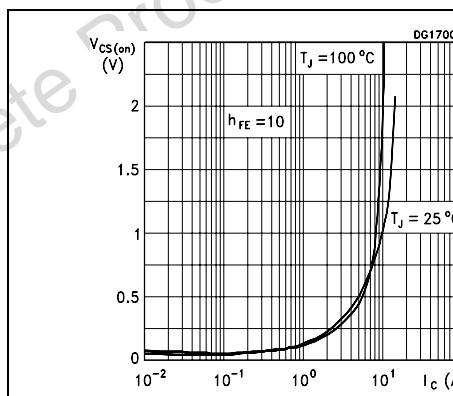


Figure 4. Base-source On voltage

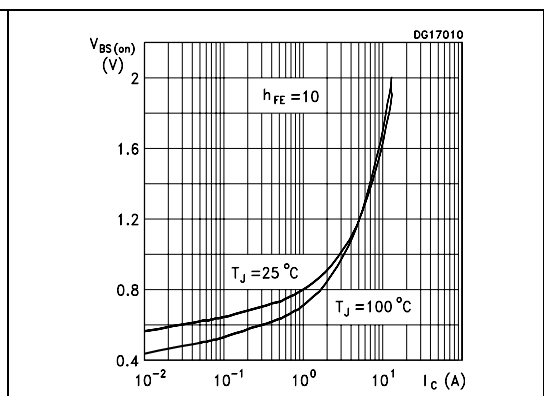


Figure 5. Reverse biased SOA

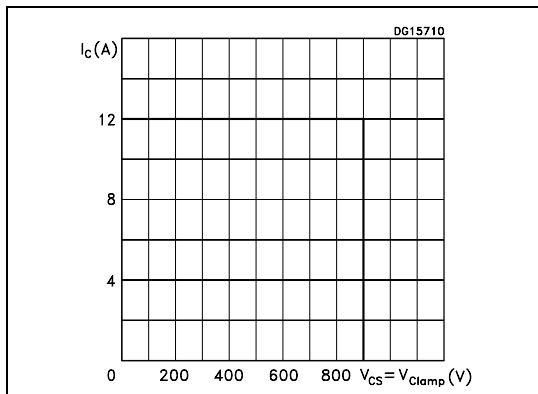


Figure 6. Dynamic collector-emitter voltage

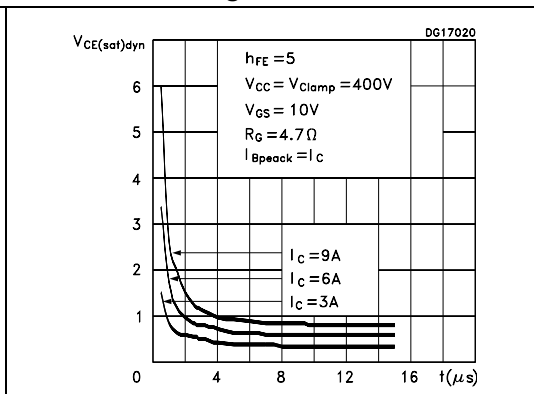
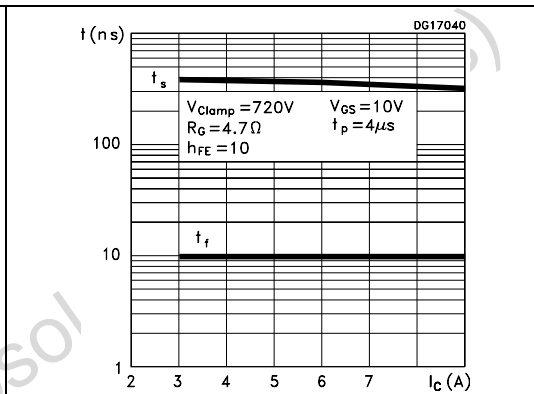
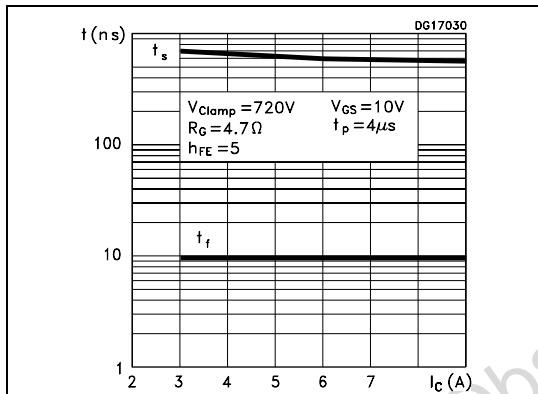


Figure 7. Inductive load switching time Figure 8. Inductive load switching time



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2.2 Test circuits

Figure 9. Static $V_{CS(ON)}$ test circuits

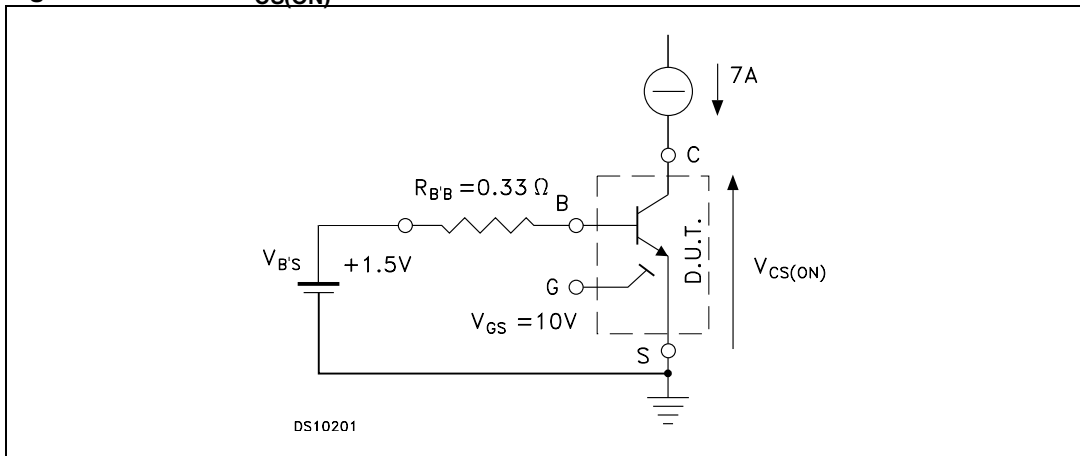
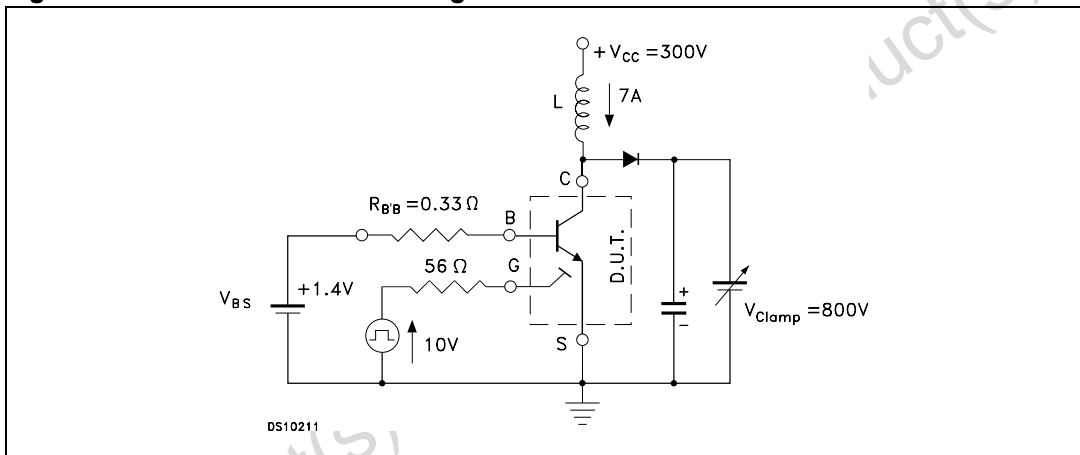


Figure 10. Inductive load switching and RBSOA test circuit



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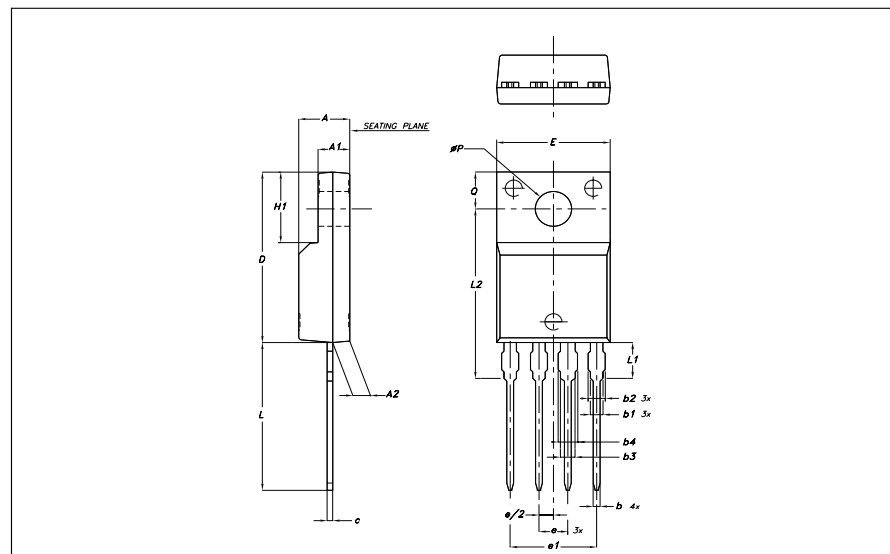
3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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TO220FP-4L MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	4.30		4.70
A1	2.60		3
A2	1.30	1.50	1.70
b	0.50		0.70
b1	1.05		
b2			1.30
b3	1.25		
b4			1.50
c	0.45	0.50	0.60
D	15.50		15.90
E	9.80		10.20
e	2.29	2.54	2.79
e1		7.62	
H1	6.30		6.70
L		13.60	
L1		3.30	
L2	15.40		15.80
Dia P	3		3.40
Q	3.30		3.50



4 Revision history

Table 4. Revision history

Date	Revision	Changes
28-Jul-2006	1	Initial release.
16-Jan-2007	2	New graphics

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