THE DATASHEET OF

ISL94202IRTZ-T7A

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ISL94202

Standalone 3 to 8 Cell Li-Ion Battery Pack Monitor

The ISL94202 is a battery pack monitor IC that supports from three to eight series connected cells. It provides complete battery monitoring and pack control. The ISL94202 provides automatic shutdown and recovery from out-of-bounds conditions and automatically controls pack cell balancing.

The ISL94202 is highly configurable as a stand-alone unit, but can be used with an optional external Microcontroller (MCU), which communicates to the ISL94202 through an I^2C interface.

The ISL94202 supersedes the ISL94203 for all future designs, as the ISL94202 operates in both parallel and series power FET configurations.

Applications

- Power tools
- Battery back-up systems
- Light electric vehicles
- Portable equipment
- Energy storage systems
- Solar farms
- Medical equipment
- Hospital beds
- Monitoring equipment
- Ventilators

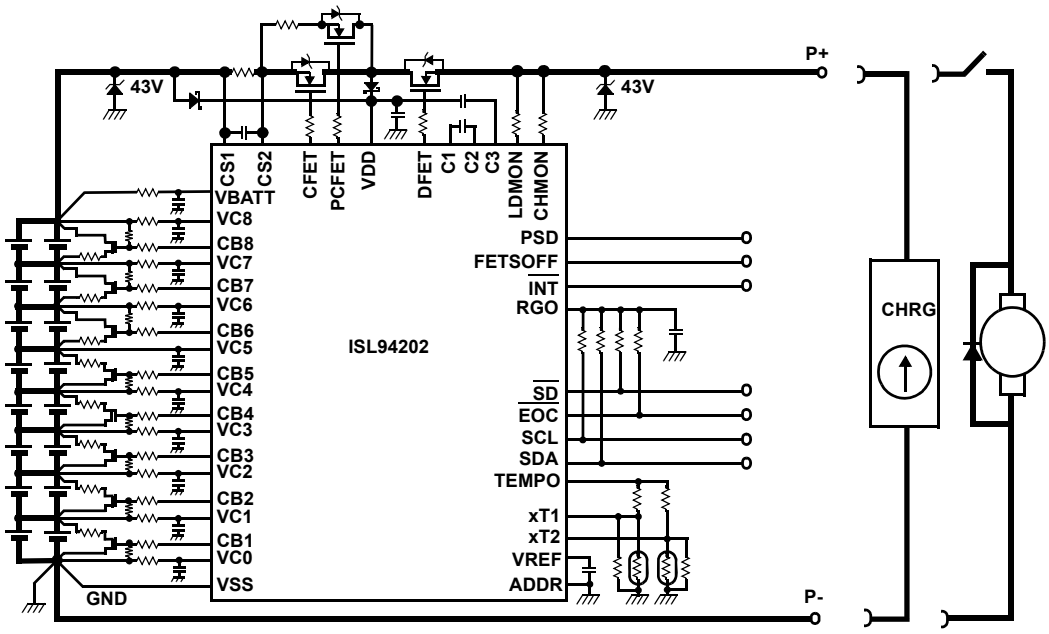
Features

- Eight cell voltage monitors support Li-ion CoO_2, Li-ion Mn_2O_4, Li-ion $FePO_4$, and other chemistries
- Stand-alone pack control - no MCU needed
- Multiple voltage protection options (each programmable to 4.8V; 12-bit digital value) and selectable overcurrent protection levels
- Programmable detection/recovery times for overvoltage, undervoltage, overcurrent, and short-circuit conditions
- Configuration/calibration registers maintained in EEPROM
- Open Wire battery connection detection
- Integrated charge/discharge FET drive circuitry with built-in charge pump supports high-side N-channel FETs
- Cell balancing uses external FETs with internal state machine or an optional external MCU
- Enters low power states after periods of inactivity
  - Charge or discharge current detection resumes normal scan rates

Related Literature

For a full list of related documents, visit our website:

- ISL94202 device page



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1. Overview

1.1 Block Diagram

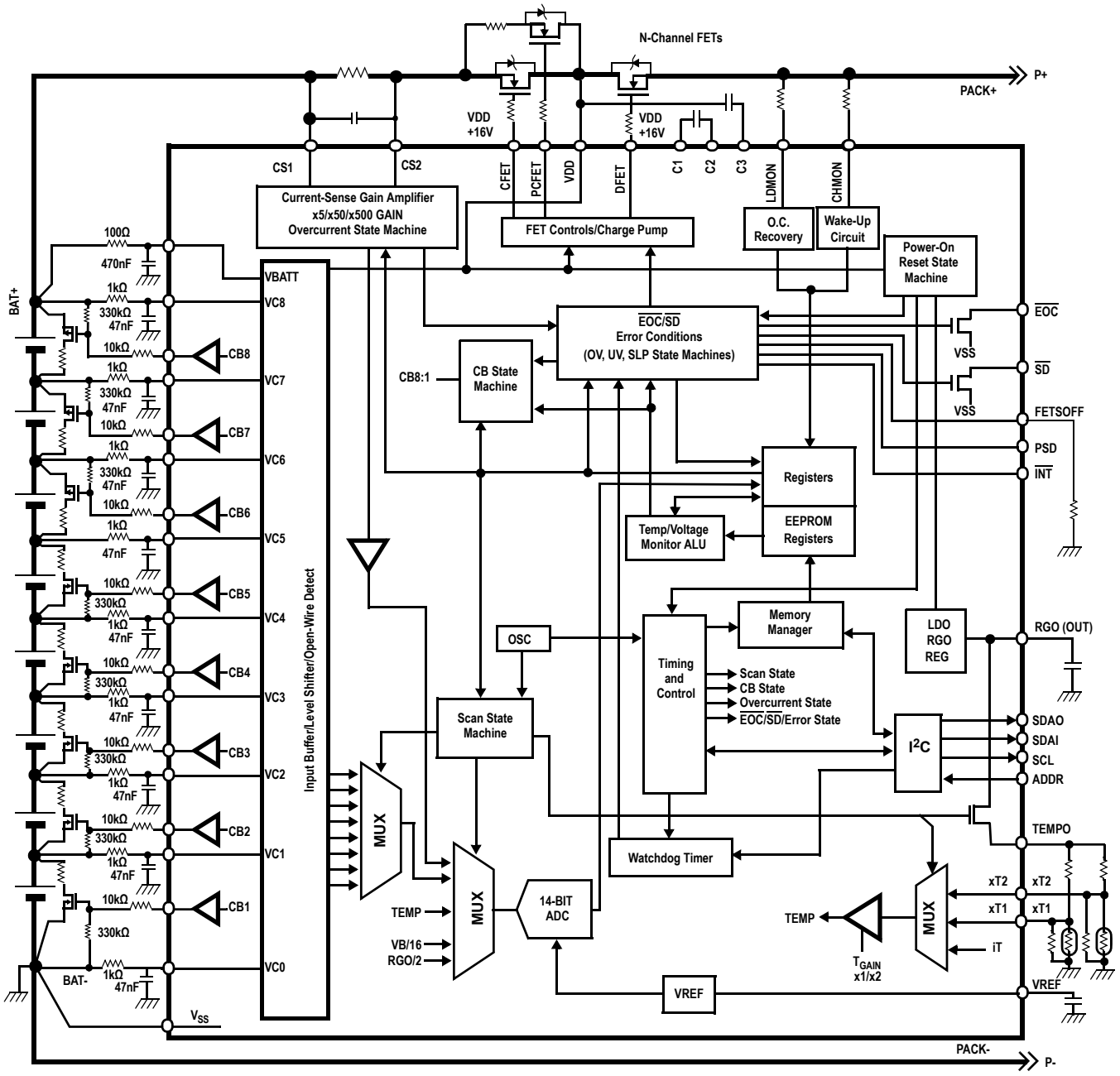


Figure 2. Block Diagram

1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL94202IRTZ	94202 IRTZ	-40 to +85	-	48 Ld TQFN	L48.6x6
ISL94202IRTZ-T	94202 IRTZ	-40 to +85	4k	48 Ld TQFN	L48.6x6
ISL94202IRTZ-T7	94202 IRTZ	-40 to +85	1k	48 Ld TQFN	L48.6x6
ISL94202IRTZ-T7A	94202 IRTZ	-40 to +85	250	48 Ld TQFN	L48.6x6
ISL94202EVKIT1Z	Evaluation Kit				

Notes:

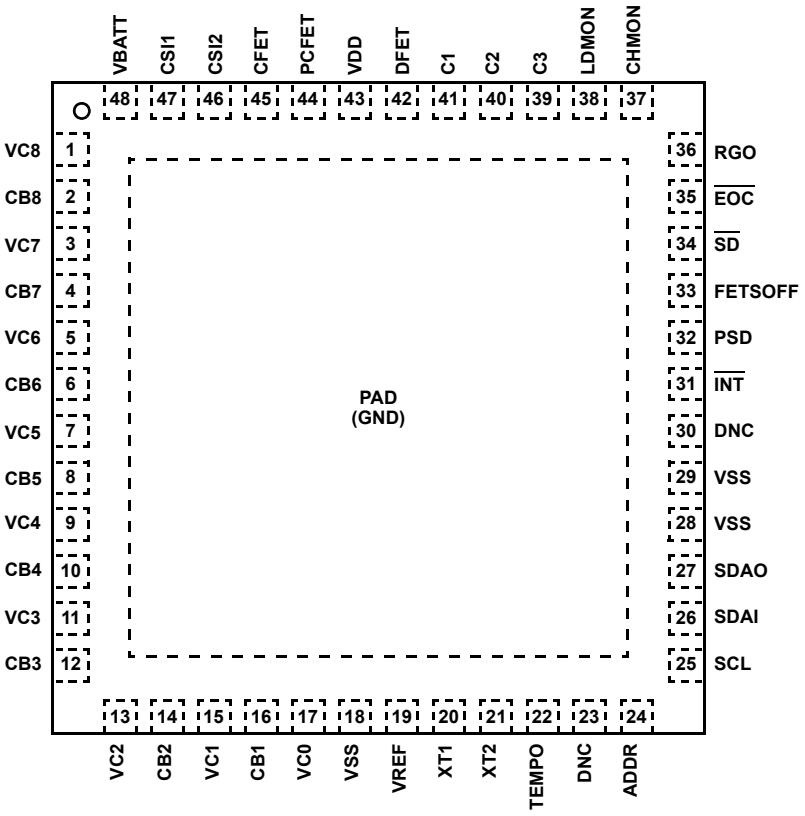
1. See TB347 for details on reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL94202 device page. For more information on MSL, see TB363.

Table 1. Key Differences Between Family of Parts

Part Number	Cells Supported		Pack Voltage (Op)		Cell Balance	IPack Sense	Fuel Gauge	Charge/Discharge FET		Supply Current (Typ)		Standalone	Internal ADC	Daisy Chain
	Min	Max	Min (V)	Max (V)				Config.	Location	Normal	Sleep			
ISL94202	3	8	4	36	External	High Side	No	Both	High Side	348µA	13µA	State Machine	14b	No
ISL94203	3	8	4	36	External	High Side	No	Parallel	High Side	348µA	13µA	State Machine	14b	No
ISL94208	4	6	8	27	Internal	Low Side	No	Both	Low Side	850µA	2µA	No	N/A	No
ISL94212	6	12	6	60	External	No	No	N/A	N/A	3.31mA	12µA	No	14b	Yes
RAJ240100	3	10	4	50	Both	Low Side	Yes	Both	High Side	50µA	1µA	Int MCU	18b	No
RAJ240090	3	8	4	50	Both	Low Side	Yes	Both	High Side	50µA	1µA	Int MCU	18b	No
RAJ240080	2	5	4	28	Both	Low Side	Yes	Both	High Side	50µA	1µA	Int MCU	18b	No

1.3 Pin Configuration

48 Ld TQFN
TOP VIEW



1.4 Pin Descriptions

Pin Number	Symbol	Description
1, 3, 5, 7, 9, 11, 13, 15, 17	VC[8:0]	**Battery Cell n voltage sense input.** These pins monitor the voltage of the battery pack cells. The voltage is level shifted to a ground reference and is monitored internally by an ADC converter. VCn connects to the positive terminal of a battery cell (CELLN) and VC(n-1) connects to the negative terminal of CELLN.
2, 4, 6, 8, 10, 12, 14, 16	CB[8:1]	**Cell Balancing FET control output n.** An internal drive circuit controls an external FET that is used to divert a portion of the current around a cell while the cell charges or adds to the current pulled from a cell during discharge to perform a cell voltage balancing operation. This function is generally used to reduce the voltage on an individual cell relative to other cells in the pack. The cell balancing FETs are turned on or off by an internal cell balance state machine or an external MCU.
18, 28, 29	VSS	**Ground**. This pin connects to the most negative terminal in the battery string. If separate analog and digital ground planes are used they should be connected together at the VSS pins.
19	VREF	**Voltage Reference Output.** This output is the a 1.8V reference voltage used by the internal circuitry (ADC). This pin should not be loaded as this could cause significant ADC error. The VREF pin should be connected to GND through a 1µF capacitor.
20	XT1	**Temperature monitor inputs.** These pins input the voltage across two external NTC thermistors used to determine the temperature of the cells and or the power FET.
21	XT2	
22	TEMPO	**Temperature Monitor Output Reference.** This pin outputs a voltage to be used in a divider that consists of a fixed resistor and a thermistor. The thermistor is located in close proximity to the cells or a power FET. The TEMPO output is connected internally to the VRGO voltage through a PMOS switch only during a measurement of the temperature, otherwise the TEMPO output is off.
23, 30	DNC	Do not connect, pin must be floated.
24	ADDR	**Serial Address.** This is an address input for an I^2C communication link to allow for two devices on one bus.
25	SCL	**Serial Clock.** This is the clock input for an I^2C communication link.

Pin Number	Symbol	Description
26	SDAI	**Serial Data.** These are the data lines for an I^2C interface. When connected together, they form the standard bidirectional interface for the I^2C bus (recommended).
27	SDAO	
31	$\overline{INT}$	**Interrupt.** This pin goes active low when there is an external MCU connected to the ISL94202 and MCU communication fails to send a slave byte within a watchdog timer period. This is a CMOS type output.
32	PSD	**Pack Shutdown.** This pin is set high when any cell voltage reaches the OVLO threshold (OVLO flag). Optionally, PSD is also set if there is a voltage differential between any two cells that is greater than a specified limit (CELLF flag) or if there is an open-wire condition. This pin can be used with external circuitry for blowing a fuse in the pack or as an interrupt to an external MCU.
33	FETSOFF	**FETSOFF.** This input allows an external MCU to turn off both Power FET and CB outputs. This pin should be pulled low when inactive or tied to ground if unused.
34	$\overline{SD}$	**Shutdown.** This output indicates that the ISL94202 detected a failure condition that would result in the DFET turning off. This could be undervoltage, over-temperature, under-temperature, etc. The $\overline{SD}$ pin also goes active if there is any charge overcurrent condition. This is an open-drain output.
35	$\overline{EOC}$	**End-of-Charge.** This output indicates that the ISL94202 detected a fully charged condition. This is defined by any cell voltage exceeding an EOC voltage (as defined by an EOC value in EEPROM).
36	RGO	**Regulator Output.** This is the 2.5V regulator output.
37	CHMON	**Charge Monitor.** This pin is used to detect a charger connection. When the IC is in the Powerdown State or SLEEP Mode, connecting this pin to the charger wakes up the device. When the IC recovers from a charge overcurrent condition, this pin is used to determine if the charger is removed prior to turning on the power FETs.
38	LDMON	**Load Monitor.** This pin is used to detect a load connection. When the IC is in the SLEEP Mode, connecting this pin to a load wakes up the device. When the IC recovers from a discharge overcurrent or short-circuit condition, this pin is used to determine if the load is removed prior to turning on the power FETs.
39, 40, 41	C[3:1]	**Charge Pump Capacitors.** These external capacitors are used by the charge pump to drive the power FETs.
42	DFET	**Discharge FET Control.** The ISL94202 controls the gate of a Discharge N-channel FET through this pin. The FET is turned on by the ISL94202 if all conditions are acceptable. The ISL94202 turns off the FET if an out-of-bounds condition occurs. The FET can be turned off by an external MCU by writing to the DFET control bit. The DFET output is also turned off by the FETSOFF pin. The FET output cannot be turned on by an external MCU if there are any out-of-bounds conditions.
43	VDD	**Power Supply.** This pin provides the operating voltage for the IC circuitry.
44	PCFET	**Precharge FET Control.** The ISL94202 controls the gate of a Precharge N-channel FET through this pin. The FET is turned on by the ISL94202 under precharge conditions, a trickle charge of the cells at the low end of the charge range. The ISL94202 turns off the FET if an out-of-bounds condition occurs. The FET can be turned off by an external MCU by writing to the PCFET control bit. The PCFET output is also turned off by the FETSOFF pin. The FET output cannot be turned on by an external MCU if there are any out-of-bounds conditions. Either the PCFET or the CFET turn on, but not both.
45	CFET	**Charge FET Control.** The ISL94202 controls the gate of a Charge N-channel FET through this pin. The FET is turned on by the ISL94202 if all conditions are acceptable. The ISL94202 turns off the FET if an out-of-bounds condition occurs. The FET can be turned off by an external MCU by writing to the CFET control bit. The CFET output is also turned off by the FETSOFF pin. The FET output cannot be turned on by an external MCU if there are any out-of-bounds conditions. Either the PCFET or the CFET turn on, but not both.
46	CSI2	**Current-Sense Inputs.** These pins connect the ISL94202 current-sense circuit to the external sense resistor to measure the differential voltage. The sense resistor is typically in the range of 0.2mΩ to 5mΩ.
47	CSI1	
48	VBATT	**Input Level Shifter Supply and Battery Pack Voltage Input.** This pin powers the input level shifters and is also used to monitor the voltage of the battery stack. The voltage is internally divided by 32 and connected to an ADC converter through a MUX.
PAD	GND	**Thermal Pad.** This pad should connect to ground.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum (Note 4)	Unit
Power Supply Voltage, VDD	VSS - 0.5	VSS+ 45.0	V
Cell Voltage (VC, VBATT)			
VCn	-0.5	VBATT + 0.5	V
VCn - VSS (n = 8)	-0.5	45.0	V
VCn - VSS (n = 6, 7)	-0.5	36.0	V
VCn - VSS (n = 4, 5)	-0.5	27.0	V
VCn - VSS (n = 2, 3)	-0.5	17.0	V
VCn - VSS (n = 1)	-0.5	7.0	V
VCn - VSS (n = 0)	-0.5	3.0	V
VCn - VC(n-1) (n = 2 to 12)	-3.0	7.0	V
VC1 - VC0	-0.5	7.0	V
Cell Balance Pin Voltages (VCB)			
VCBn - VC(n-1), n = 1 to 5	-0.5	7.0	V
VCn - VCBn, n = 6 to 8	-0.5	7.0	V
Terminal Voltage			
ADDR, xT1, xT2, FETSOFF, PSD, $\overline{INT}$	-0.5	VRGO +0.5	V
SCL, SDAI, SDAO, $\overline{EOC}$, $\overline{SD}$	-0.5	5.5	V
CFET, PCFET, C1, C2, C3	VDD - 0.5	VDD + 15.5 (60V max)	V
DFET, CHMON, LDMON	-0.5	VDD + 15.0 (60V max)	V
Terminal Current			
RGO		25	mA
Current-Sense Voltage			
VBATT, CS1, CS2	-0.5	VDD +1.0	V
VBATT - CS1, VBATT - CS2	-0.5	+0.5	V
CS1 - CS2	-0.5	+0.5	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2014)	1.5		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Note:

4. Devices are characterized, but not production tested, at Absolute Maximum Voltages.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld QFN Package (Notes 5, 6)	28	0.75

Notes:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
6. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Continuous Package Power Dissipation		400	mW
Maximum Junction Temperature		+125	°C
Storage Temperature Range	-55	+125	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range	-40	+85	°C
Operating Voltage			
VDD	4V	36	V
VCn-VC(n-1) Specified Range	2.0	4.3	V
VCn-VC(n-1) Extended Range	1.0	4.4	V
VCn-VC(n-1) Maximum Range (any cell)	0.5	4.8	V

2.4 Electrical Specifications

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C.**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Power-Up Condition – Threshold Rising (Device becomes operational)	V_{PORR1}	V_{DD} minimum voltage at which device operation begins (CFET turns on; CHMON = V_{DD})		6.0		V
	V_{PORR2}	CHMON minimum voltage at which device operation begins (CFET turns on; V_{DD} > 6.0V)		V_{DD}		V
Powerdown Condition – Threshold Falling	V_{PORF}	V_{DD} minimum voltage device remains operational (RGO turns off)		3.0		V
2.5V Regulated Voltage	V_{RGO}	I_{RGO} = 3mA	**2.4**	2.5	**2.6**	V
1.8V Reference Voltage	V_{REF}		**1.79**	1.8	**1.81**	V
VBATT Input Current - V_{BATT}	I_{VBATT}	Input current; NORMAL/IDLE/DOZE Modes V_{DD} = 33.6V		38	**45**	µA
		Input current; SLEEP/Powerdown Modes V_{DD} = 33.6V			**1**	µA

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
V_{DD} Supply Current	I_{VDD1}	Device active (NORMAL Mode) (No error conditions) CFET, PCFET, DFET = OFF; V_{DD} = 33.6V		310	**370**	µA
	I_{VDD2}	Device active (IDLE Mode) (No error conditions) IDLE = 1 CFET, PCFET, DFET = OFF; V_{DD} = 33.6V		215	**275**	µA
	I_{VDD3}	Device active (DOZE Mode) (No error conditions) DOZE = 1 CFET, PCFET, DFET = OFF; V_{DD} = 33.6V		210	**265**	µA
	I_{VDD4}	FET drive current (I_{VDD} increase when FETs are on - NORMAL/IDLE/DOZE Modes); V_{DD} = 33.6V		215		µA
	I_{VDD5}	Device active (SLEEP Mode); SLEEP = 1; V_{DD} = 33.6V				
		0°C to +60°C		13	30	µA
		-40°C to +85°C			**50**	µA
	I_{VDD6}	Powerdown PDWN = 1; V_{DD} = 33.6V			**1**	µA
Input Bias Current	ICS1	V_{DD} = V_{BATT} = VCS1 = VCS2 = 33.6V (NORMAL, IDLE, DOZE)		10	**15**	µA
		V_{DD} = V_{BATT} = VCS1 = VCS2 = 33.6V (SLEEP, Powerdown)				
		0°C to +60°C			1	µA
		-40°C to +85°C			**3**	µA
	ICS2	V_{DD} = V_{BATT} = VCS1 = VCS2 = 33.6V (NORMAL, IDLE, DOZE)		10	**15**	µA
		V_{DD} = V_{BATT} = VCS1 = VCS2 = 33.6V (SLEEP, Powerdown)				
		0°C to +60°C			1	µA
		-40°C to +85°C			**3**	µA
VCn Input Current	I_{VCN}	Cell input leakage current AO2:AO0 = 0000H (NORMAL/IDLE/DOZE; not sampling cells)	-1		**1**	µA
CBn Input Current	I_{CBN}	Cell Balance pin leakage current (no balance active)	-1		**1**	µA
Temperature Monitor Specifications						
External Temperature Accuracy	V_{XT1}	External temperature monitoring error. ADC voltage error when monitoring xT1 input. TGain = 0; (xTn = 0.2V to 0.737V)	-25		**15**	mV
Internal Temperature Monitor Output (See: "Temperature Monitoring/Response" on page 135)	T_{INT25}	$[iTB:iT0]_{10}$*1.8/4095/GAIN GAIN = 2 (TGain bit = 0) Temperature = +25°C		0.276		V
	V_{INTMON}	Change in $[iTB:iT0]_{10}$*1.8/4095/GAIN GAIN = 2 (TGain bit = 0) Temperature = -40°C to +85°C		1.0		mV/°C

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Cell Voltage Monitor Specifications						
Cell Monitor Voltage Accuracy (Relative)	V_{ADCR}	Relative cell measurement error (Maximum absolute cell measurement error - Minimum absolute cell measurement error) VCn -VC(n-1) = 2.4V to 4.2V; 0°C to +60°C		3	10	mV
		VCn -VC(n-1) = 0.1V to 4.7V; 0°C to +60°C			15	mV
		VCn -VC(n-1) = 0.1V to 4.7V; -40°C to +85°C			**30**	mV
Cell Monitor Voltage Accuracy (Absolute)	V_{ADC}	Absolute cell measurement error (Cell measurement error compared with voltage at the cell) VCn - VC(n-1) = 2.4V to 4.2V; 0°C to +60°C	-15		15	mV
		VCn - VC(n-1) = 0.1V to 4.7V; 0°C to +60°C	-20		20	mV
		VCn - VC(n-1) = 0.1V to 4.7V; -40°C to +85°C	**-30**		**30**	mV
V_{BATT} Voltage Accuracy	V_{BATT}	V_{BATT} - $[VBB:VB0]_{10}$*32*1.8/4095; 0°C to +60°C	-200		200	mV
		-40°C to +85°C	**-270**		**270**	mV
Current-Sense Amplifier Specifications						
Charge Current Threshold	VCCTH	VCS1-VCS2, CHING set (charging)		-100		µV
Discharge Current Threshold	VDCTH	VCS1-VCS2, DCHING set (discharging)		100		µV
Current-Sense Accuracy	VIA1	V_{IA1} = $([ISNSB:ISNS0]_{10}$*1.8/4095)/5; CHING bit set; Gain = 5 VCS1 = 26.4V, VCS2 - VCS1 = + 100mV	**97**	102	**107**	mV
	VIA2	V_{IA2} = $([ISNSB:ISNS0]_{10}$*1.8/4095)/5; DCHING bit set; Gain = 5 VCS1 = 26.4V, VCS2 - VCS1 = - 100mV	**-107**	-102	**-97**	mV
	VIA3	V_{IA3} = $([ISNSB:ISNS0]_{10}$*1.8/4095)/50; CHING bit set; Gain = 50 VCS1 = 26.4V, VCS2 - VCS1 = + 10mV	**8.0**	10.0	**12.0**	mV
	VIA4	V_{IA4} = $([ISNSB:ISNS0]_{10}$*1.8/4095)/50; DCHING bit set; Gain = 50 VCS1 = 26.4V, VCS2 - VCS1 = - 10mV	**-12.0**	-10.0	**-8.0**	mV
	VIA5	V_{IA3} = $([ISNSB:ISNS0]_{10}$*1.8/4095)/500; CHING bit set; Gain = 500 VCS1 = 26.4V, VCS2 - VCS1 = + 1mV 0°C to +60°C	0.5	1.0	1.5	mV
		-40°C to +85°C	**0.4**		**1.6**	mV
	VIA6	V_{IA4} = $([ISNSB:ISNS0]_{10}$*1.8/4095)/500; DCHING bit set; Gain = 500 VCS1 = 26.4V, VCS2 - VCS1 = - 1mV 0°C to +60°C	-1.5	-1.0	-0.5	mV
		-40°C to +85°C	**-1.6**		**-0.4**	mV

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Overcurrent/Short-Circuit Protection Specifications						
Discharge Overcurrent Detection Threshold	V_{OCD}	V_{OCD} = 4mV [OCD2:0] = 0,0,0	**2.6**	4.0	**5.4**	mV
		V_{OCD} = 8mV [OCD2:0] = 0,0,1	**6.4**	8.0	**9.6**	mV
		V_{OCD} = 16mV [OCD2:0] = 0,1,0	**12.8**	16.0	**19.2**	mV
		V_{OCD} = 24mV [OCD2:0] = 0,1,1	**20**	25	**30**	mV
		V_{OCD} = 32mV [OCD2:0] = 1,0,0 (default)	**26.4**	33.0	**39.6**	mV
		V_{OCD} = 48mV [OCD2:0] = 1,0,1	**42.5**	50.0	**57.5**	mV
		V_{OCD} = 64mV [OCD2:0] = 1,1,0	**60.3**	67.0	**73.7**	mV
		V_{OCD} = 96mV [OCD2:0] = 1,1,1	**90**	100	**110**	mV
Discharge Overcurrent Detection Time	t_{OCDT}	[OCDTA:OCDT0] = 0A0H (160ms) (default) Range: 0ms to 1023ms 1ms/step 0s to 1023s; 1s/step		160		ms
Short-Circuit Detection Threshold	V_{SCD}	V_{SCD} = 16mV [SCD2:0] = 0,0,0	**10.4**	16.0	**21.6**	mV
		V_{SCD} = 24mV [SCD2:0] = 0,0,1	**18**	24	**30**	mV
		V_{SCD} = 32mV [SCD2:0] = 0,1,0	**26**	33	**40**	mV
		V_{SCD} = 48mV [SCD2:0] = 0,1,1	**42**	49	**56**	mV
		V_{SCD} = 64mV [SCD2:0] = 1,0,0	**60**	67	**74**	mV
		V_{SCD} = 96mV [SCD2:0] = 1,0,1 (default)	**90**	100	**110**	mV
		V_{SCD} = 128mV [SCD2:0] = 1,1,0	**127**	134	**141**	mV
		V_{SCD} = 256mV [SCD2:0] = 1,1,1	**249**	262	**275**	mV
Short-Circuit Current Detection Time	t_{SCT}	[SCTA:SCT0] = 0C8H (200µs) (default) Range: 0µs to 1023µs; 1µs/step 0ms to 1023ms 1ms/step		200		µs
Charge Overcurrent Detection Threshold	V_{OCC}	V_{OCC} = 1mV [OCC2:0] = 0,0,0	**0.2**	1.0	**2.1**	mV
		V_{OCC} = 2mV [OCC2:0] = 0,0,1	**0.7**	2.0	**3.3**	mV
		V_{OCC} = 4mV [OCC2:0] = 0,1,0	**2.8**	4.0	**5.2**	mV
		V_{OCC} = 6mV [OCC2:0] = 0,1,1	**4.5**	6.0	**7.5**	mV
		V_{OCC} = 8mV [OCC2:0] = 1,0,0 (default)	**6.6**	8.0	**9.8**	mV
		V_{OCC} = 12mV [OCC2:0] = 1,0,1	**9.6**	12.0	**14.4**	mV
		V_{OCC} = 16mV [OCC2:0] = 1,1,0	**14.5**	17.0	**19.6**	mV
		V_{OCC} = 24mV [OCC2:0] = 1,1,1	**22.5**	25.0	**27.5**	mV
Overcurrent Charge Detection Time	t_{OCCT}	[OCCTA:OCCT0] = 0A0H (160ms) (default) Range: 0ms to 1023ms 1ms/step 0s to 1023s; 1s per step		160		ms
Charge Monitor Input Threshold (Falling Edge)	V_{CHMON}	µCCMON bit = 1; CMON_EN bit = 1	**8.2**	8.9	**9.8**	V
Load Monitor Input Threshold (Rising Edge)	V_{LDMON}	µCLMON bit = 1; LMON_EN bit = 1	**0.45**	0.60	**0.75**	V
Load Monitor Output Current	I_{LDMON}	µCLMON bit = 1; LMON_EN bit = 1		62		µA

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Voltage Protection Specifications						
Overvoltage Lockout Threshold (Rising Edge - Any Cell) [VCn-VC(n-1)]	V_{OVLO}	[OVLOB:OVLO0] = 0E80H (4.35V) (default) Range: 12-bit value (0V to 4.8V)		4.35		V
Overvoltage Lockout Recovery Threshold - All Cells	V_{OVLOR}	Falling edge		V_{OVR}		V
Undervoltage Lockout Threshold (Falling Edge - Any Cell) [VCn-VC(n-1)]	V_{UVLO}	[UVLOB:UVLO0] = 0600H (1.8V) (default) Range: 12-bit value (0V to 4.8V)		1.8		V
Undervoltage Lockout Recovery Threshold - All Cells	V_{UVLOR}	Rising edge		V_{UVR}		V
Overvoltage Lockout Detection Time	t_{OVLO}	NORMAL Mode 5 consecutive samples over the limit (minimum = 160ms, maximum = 192ms)		176		ms
Undervoltage Lockout Detection Time	t_{UVLO}	NORMAL Mode 5 consecutive samples under the limit (minimum = 160ms, maximum = 192ms)		176		ms
Overvoltage Threshold (Rising Edge - Any Cell) [VCn-VC(n-1)]	V_{OV}	[OVLB:OVL0] = 0E2AH (4.25V) (default) Range: 12-bit value (0V to 4.8V)		4.25		V
Overvoltage Recovery Voltage (Falling Edge - All Cells) [VCn-VC(n-1)]	V_{OVR}	[OVRB:OVR0] = 0DD5H (4.15V) (default) Range: 12-bit value (0V to 4.8V)		4.15		V
Overvoltage Detection/Release Time	t_{OVT}	[OVTA:OVT0] = 201H (1s) (default) Range: 0ms to 1023ms; 1ms/step 0s to 1023s; 1s/step		1		s
Undervoltage Threshold (Falling Edge - Any Cell) [VCn-VC(n-1)]	V_{UV}	[UVLB:UVL0] = 0900H (2.7V) (default) Range: 12-bit value (0V to 4.8V)		2.7		V
Undervoltage Recovery Voltage (Rising Edge - All Cells) [VCn-VC(n-1)]	V_{UVR}	[UVRB:UVR0] = 0A00H (3.0V) (default) Range: 12-bit value (0V to 4.8V)		3.0		V
Undervoltage Detection Time	t_{UVT}	[UVTA:UVT0] = 201H (1s) (default) Range: 0ms to 1023ms; 1ms/step 0s to 1023s; 1s/step		1		s
Undervoltage Release Time	t_{UVTR}	[UVTA:UVT0] = 201H (1s) + 3s (default) Range: (0ms to 1023ms) + 3s; 1ms/step (0s to 1023s) + 3s; 1s/step		3		s
SLEEP Level Voltage Threshold (Falling Edge - Any Cell) [VCn-VC(n-1)]	V_{SLV}	[SLVB:SLV0] = 06AAH (2.0V) (default) Range: 12-bit value (0V to 4.8V)		2.0		V
SLEEP Detection Time	t_{SLT}	[SLTA:SLT0] = 201H (1s) (default) Range: 0ms to 1023ms; 1ms/step 0s to 1023s; 1s/step		1		s
Low Voltage Charge Threshold (Falling Edge - Any Cell) [VCn-VC(n-1)]	V_{LVCH}	[LVCHB:LVCH0] = 07AAH (2.3V) (default) Range: 12-bit value (0V to 4.8V) Precharge if any cell is below this voltage		2.3		V
Low Voltage Charge Threshold Hysteresis	V_{LVCHH}			117		mV

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
End-of-Charge Threshold (Rising Edge - Any Cell) [VCn-VC(n-1)]	V_{EOC}	[EOCSB:EOCS0] = 0E00H (4.2V) (default) Range: 12-bit value (0V to 4.8V)		4.2		V
End-of-Charge Threshold Hysteresis	V_{EOCTH}			117		mV
SLEEP Mode Timer	t_{SMT}	[MOD7:MOD0] = 0DH (off) (default) Range: 0s to 255 minutes		90		min
Watchdog Timer	t_{WDT}	[WDT4:WDT0] = 1FH (31s) (default) Range: 0s to 31s		31		s
Temperature Protection Specifications						
Internal Temperature Shutdown Threshold	T_{ITSD}	[IOTB:IOT0] = 02D8H		115		°C
Internal Temperature Recovery	T_{ITRCV}	[IOTRB:IOTR0] = 027DH		95		°C
External Temperature Output Voltage	V_{TEMPO}	Voltage output at TEMPO pin (during temperature scan); I_{TEMPO} = 1mA	**2.30**	2.45	**2.60**	V
External Temperature Limit Threshold (Hot) - xT1 or xT2 Charge, Discharge, Cell Balance (see Figure 39)	T_{XTH}	xTn Hot threshold. Voltage at V_{TEMPI}, xT1 or xT2 = 04B6H, TGain = 0 ~+55°C; thermistor = 3.535k Detected by COT, DOT, CBOT bits = 1		0.265		V
External Temperature Recovery Threshold (Hot) - xT1 or xT2 Charge, Discharge, Cell Balance (see Figure 39)	T_{XTHR}	xTn Hot recovery voltage at V_{TEMPI} xT1 or xT2 = 053EH, TGain = 0 (~+50°C; thermistor = 4.161k) Detected by COT, DOT, CBOT bits = 0		0.295		V
External Temperature Limit Threshold (Cold) - xT1 or xT2 Charge, Discharge, Cell Balance (see Figure 39)	T_{XTC}	xTn Cold threshold. Voltage at V_{TEMPI} xT1 or xT2 = 0BF2H, TGain = 0 (~ -10°C; thermistor = 42.5k) Detected by CUT, DUT, CBUT bits		0.672		V
External Temperature Recovery Threshold (Cold) - xT1 or xT2 Charge, Discharge, Cell Balance (see Figure 39)	T_{XTCH}	xTn Cold recovery voltage at V_{TEMPI}. xT1 or xT2 = 0A93H, TGain = 0 (~5°C; thermistor = 22.02k) Detected by CUT, DUT, CBUT bits		0.595		V
Cell Balance Specifications						
Cell Balance FET Gate Drive Current		CB1 to CB5 (current out of pin)	**15**	25	**35**	µA
		CB6 to CB8 (current into pin)	**15**	25	**35**	µA
Cell Balance Maximum Voltage Threshold (Rising Edge - Any cell) [CELMAX]	V_{CBMX}	[CBVUB:CBVU0] = 0E00H (4.2V) (default) Range: 12-bit value (0V to 4.8V)		4.2		V
Cell Balance Maximum Threshold Hysteresis	V_{CBMXH}			117		mV
Cell Balance Minimum Voltage Threshold (Falling Edge - Any cell) [CELMIN]	V_{CBMN}	[CBVLB:CBVL0] = 0A00H (3.0V) (default) Range: 12-bit value (0V to 4.8V)		3.0		V
Cell Balance Minimum Threshold Hysteresis	V_{CBMNH}			117		mV
Cell Balance Maximum Voltage Delta Threshold (Rising Edge - Any Cell) [VCn-VC(n-1)]	V_{CBDU}	[CBDUB:CBD0] = 06AAH (2.0V) (default) Range: 12-bit value (0V to 4.8V)		2.0		V
Cell Balance Maximum Voltage Delta Threshold Hysteresis	V_{CBDUH}			117		mV

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Wake-Up Specifications						
Device CHMON Pin Voltage Threshold (Wake on Charge) (Rising Edge)	V_{WKUP1}	CHMON pin rising edge Device wakes up and sets SLEEP flag LOW	**7.0**	8.0	**9.0**	V
Device LDMON Pin Voltage Threshold (Wake on Load) (Falling Edge)	V_{WKUP2}	LDMON pin falling edge Device wakes up and sets SLEEP flag LOW	**0.15**	0.40	**0.70**	V
Open-Wire Specifications						
Open-Wire Current	I_{OW}			1.0		mA
Open-Wire Detection Threshold	V_{OW1}	VCn-VC(n-1); VCn is open. (n = 2, 3, 4, 5, 6, 7, 8). Open-wire detection active on the VCn input.		-0.3		V
	V_{OW2}	VC1-VC0; VC1 is open. Open-wire detection active on the VC1 input.		0.4		V
	V_{OW3}	VC0-VSS; VC0 is open. Open-wire detection active on the VC0 input.		1.25		V
FET Control Specifications						
DFET Gate Voltage	V_{DFET1}	(ON) 100µA load; V_{DD} = 36V	**47**	52	**57**	V
	V_{DFET2}	(ON) 100µA load; V_{DD} = 6V	**8**	9	**10**	V
	V_{DFET3}	(OFF)		0		V
CFET Gate Voltage (ON)	V_{CFET1}	(ON) 100µA load; V_{DD} = 36V	**47**	52	**57**	V
	V_{CFET2}	(ON) 100µA load; V_{DD} = 6V	**8**	9	**10**	V
	V_{CFET3}	(OFF)		V_{DD}		V
PCFET Gate Voltage (ON)	V_{PFET1}	(ON) 100µA load; V_{DD} = 36V	**47**	52	**57**	V
	V_{PFET2}	(ON) 100µA load; V_{DD} = 6V	**8**	9	**10**	V
	V_{PFET3}	(OFF)		V_{DD}		V
FET Turn-Off Current (DFET)	$I_{DF(OFF)}$		**14**	15	**16**	mA
FET Turn-Off Current (CFET)	$I_{CF(OFF)}$		**9**	13	**17**	mA
FET Turn-Off Current (PCFET)	$I_{PF(OFF)}$		**9**	13	**17**	mA
FETSOFF Rising Edge Threshold	$V_{FO(IH)}$	FETSOFF rising edge threshold. Turn off FETs		1.8		V
FETSOFF Falling Edge Threshold	$V_{FO(IL)}$	FETSOFF falling edge threshold. Turn on FETs		1.2		V
Serial Interface Characteristics (Note 8)						
Input Buffer Low Voltage (SCL, SDA)	V_{IL}	Voltage relative to V_{SS} of the device	**-0.3**		**V_{RGO} x 0.3**	V
Input Buffer High Voltage (SCL, SDAI, SDAO)	V_{IH}	Voltage relative to V_{SS} of the device	**V_{RGO} x 0.7**		**V_{RGO} + 0.1**	V
Output Buffer Low Voltage (SDA)	V_{OL}	I_{OL} = 1mA			**0.4**	V
SDA, SCL Input Buffer Hysteresis	I^2CHYST	SLEEP bit = 0	**0.05 x V_{RGO}**			V
SCL Clock Frequency	f_{SCL}				**400**	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{IN}	Any pulse narrower than the maximum spec is suppressed.			**50**	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	From SCL falling crossing V_{IH} (minimum), until SDA exits the V_{IL} (maximum) to V_{IH} (minimum) window			**0.9**	µs

V_{DD} = 26.4V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface specification limits apply across operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Time the Bus Must Be Free Before Start of New Transmission	t_{BUF}	SDA crossing V_{IH} (minimum) during a STOP condition to SDA crossing V_{IH} (minimum) during the following START condition	**1.3**			µs
Clock Low Time	t_{LOW}	Measured at the V_{IL} (maximum) crossing	**1.3**			µs
Clock High Time	t_{HIGH}	Measured at the V_{IH} (minimum) crossing	**0.6**			µs
Start Condition Set-Up Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge, both crossing the V_{IH} (minimum) level	**0.6**			µs
Start Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing V_{IL} (maximum) to SCL falling edge crossing V_{IH} (minimum)	**0.6**			µs
Input Data Set-Up Time	$t_{SU:DAT}$	From SDA exiting the V_{IL} (maximum) to V_{IH} (minimum) window to SCL rising edge crossing V_{IL} (minimum)	**100**			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing V_{IH} (minimum) to SDA entering the V_{IL} (maximum) to V_{IH} (minimum) window	**0**		**0.9**	µs
Stop Condition Set-Up Time	$t_{SU:STO}$	From SCL rising edge crossing V_{IH} (minimum) to SDA rising edge crossing V_{IL} (maximum)	**0.6**			µs
Stop Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing V_{IH} (minimum)	**0.6**			µs
Data Output Hold Time	t_{DH}	From SCL falling edge crossing V_{IL} (maximum) until SDA enters the V_{IL} (maximum) to V_{IH} (minimum) window	**0**			ns
SDA and SCL Rise Time	t_R	From V_{IL} (maximum) to V_{IH} (minimum)			**300**	ns
SDA and SCL Fall Time	t_F	From V_{IH} (minimum) to V_{IL} (maximum)			**300**	ns
SDA and SCL Bus Pull-Up Resistor Off-Chip	R_{OUT}	Maximum is determined by t_R and t_F For C_B = 400pF, maximum is 2kΩ ~ 2.5kΩ For C_B = 40pF, maximum is 15kΩ ~ 20kΩ	**1**			kΩ
Input Leakage (SCL, SDA)	I_{LI}		**-10**		**10**	µA
EEPROM Write Cycle Time	t_{WR}	+25°C			**30**	ms

Notes:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Device MIN and/or MAX values are based on temperature limits established by characterization and are not production tested.
8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

2.5 Symbol Table

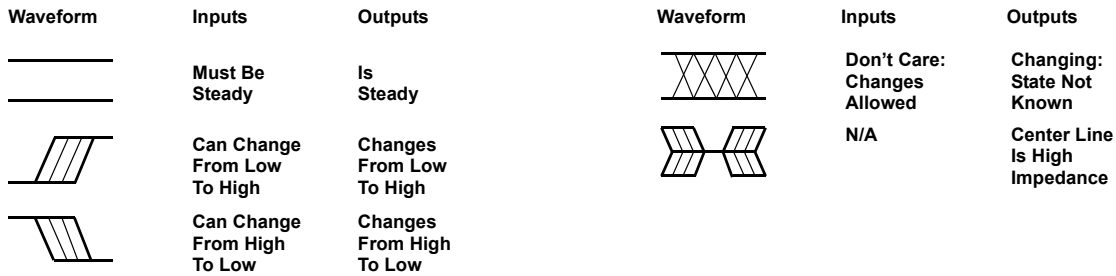


Figure 3. Symbol Table

3. Typical Performance Curves

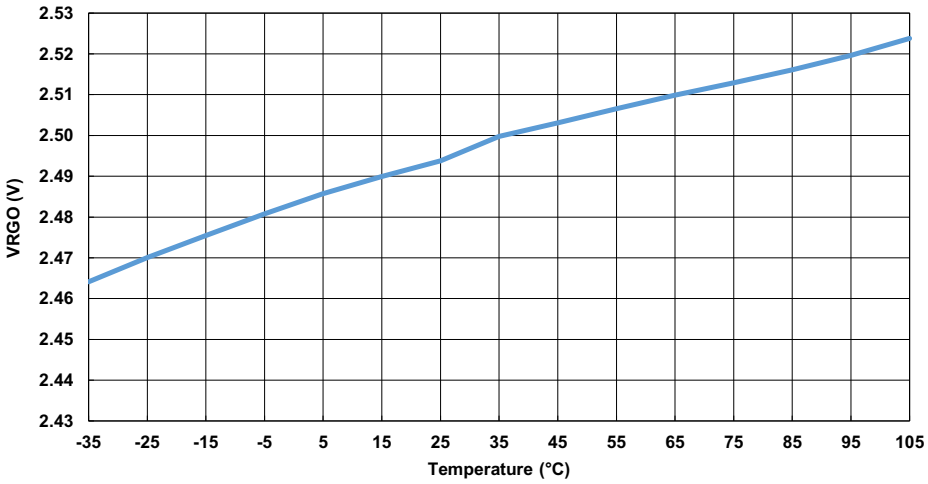


Figure 4. VRGO vs Temperature

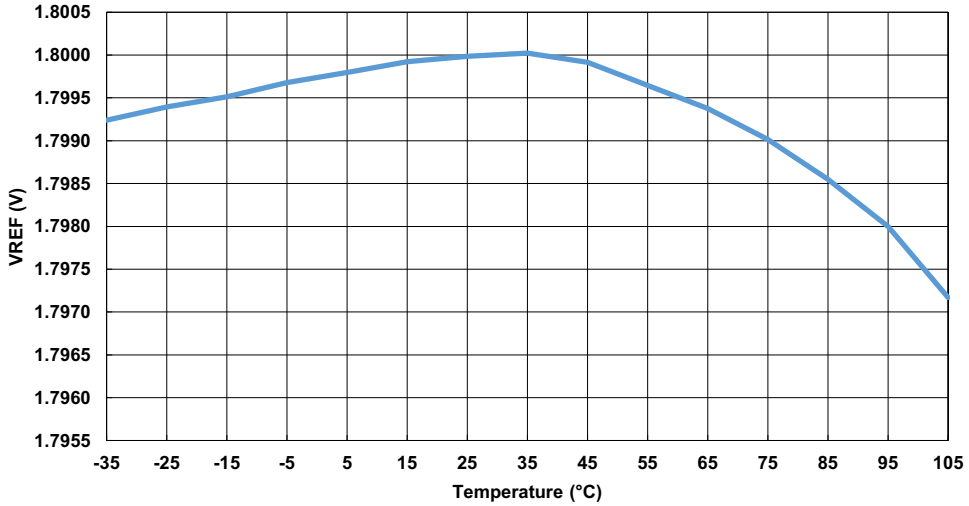


Figure 5. V_{REF} vs Temperature

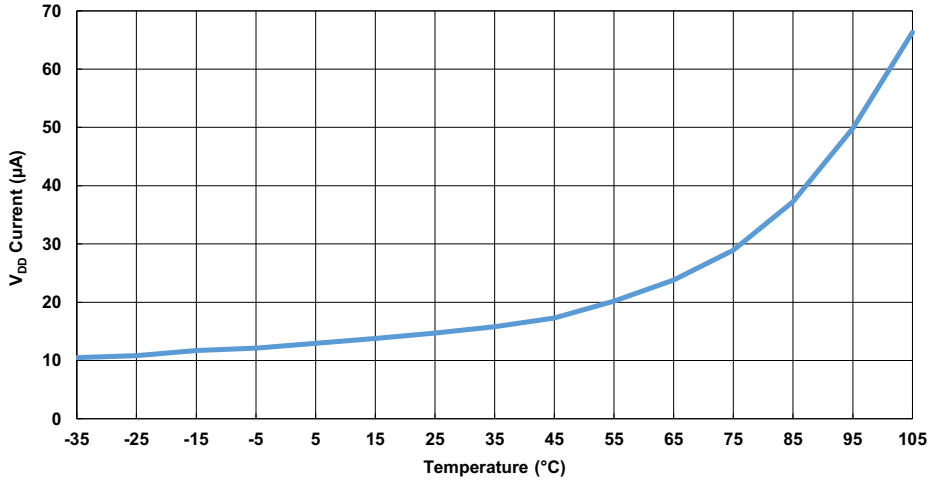


Figure 6. V_{DD} Current vs Temperature - SLEEP

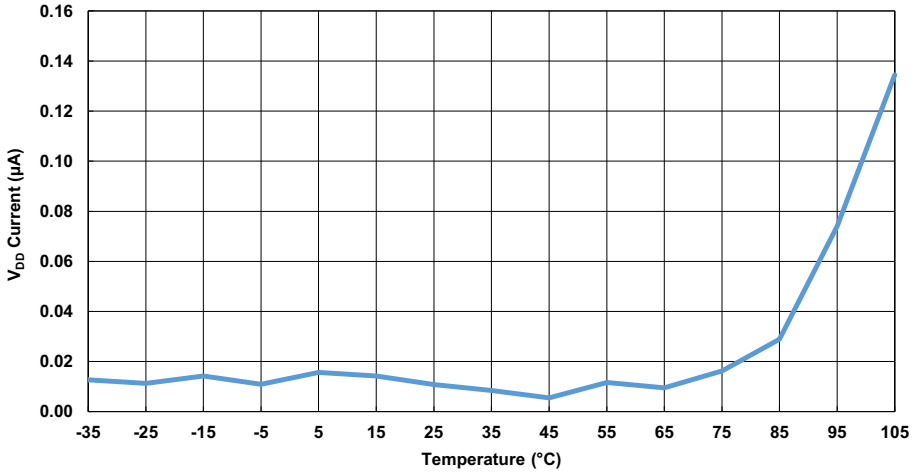


Figure 7. V_{DD} Current vs Temperature - Powerdown

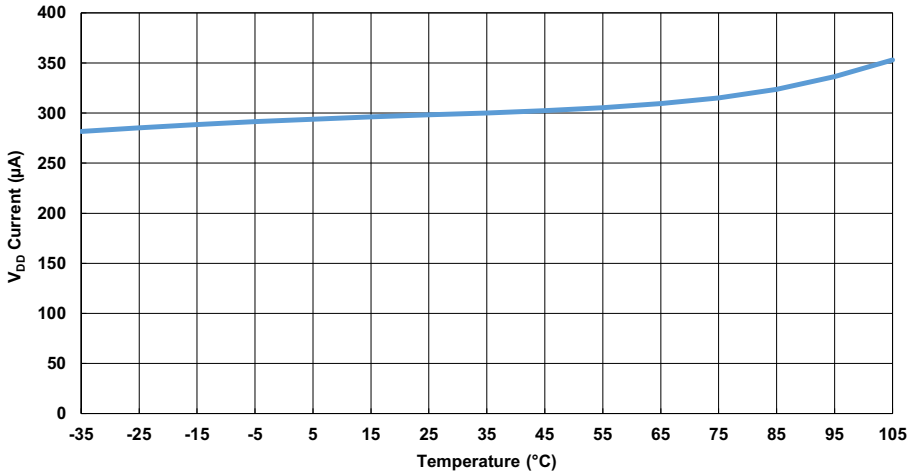


Figure 8. V_{DD} Current vs Temperature - Normal

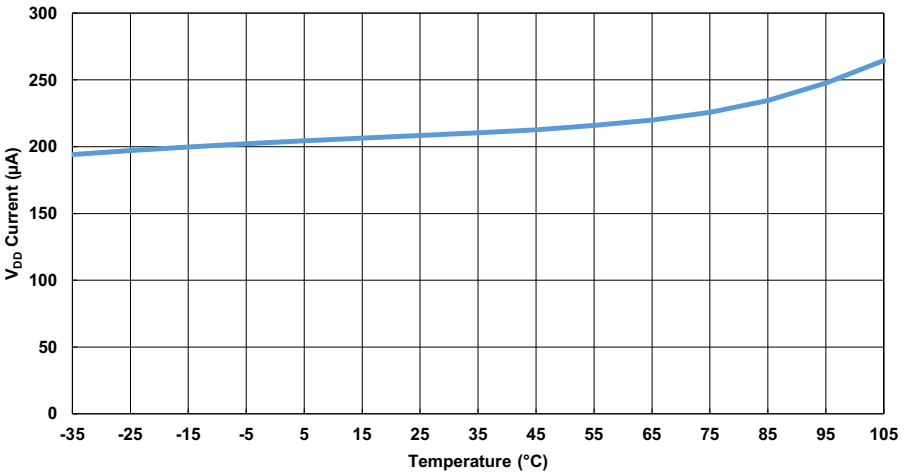


Figure 9. V_{DD} Current vs Temperature - Idle

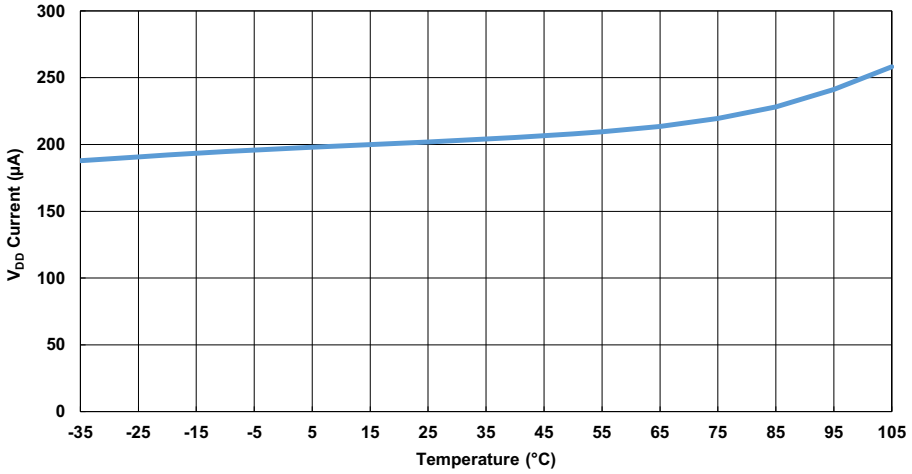


Figure 10. V_{DD} Current vs Temperature - Doze

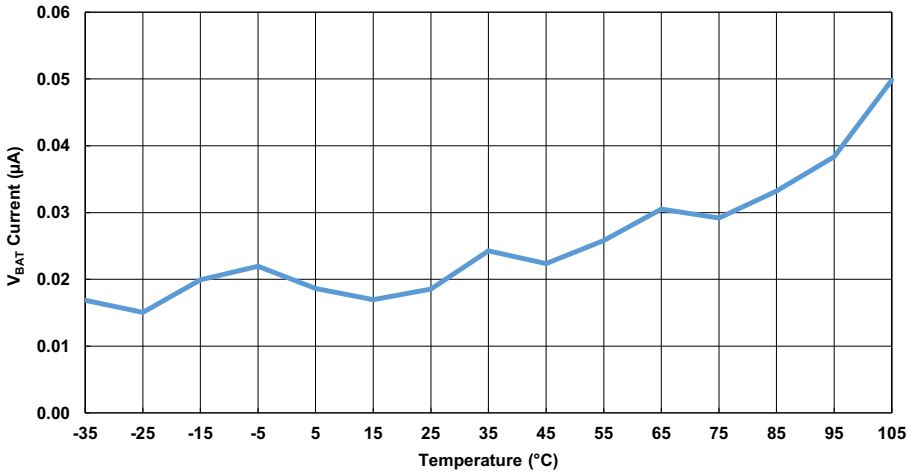


Figure 11. V_{BAT} Current vs Temperature - Sleep

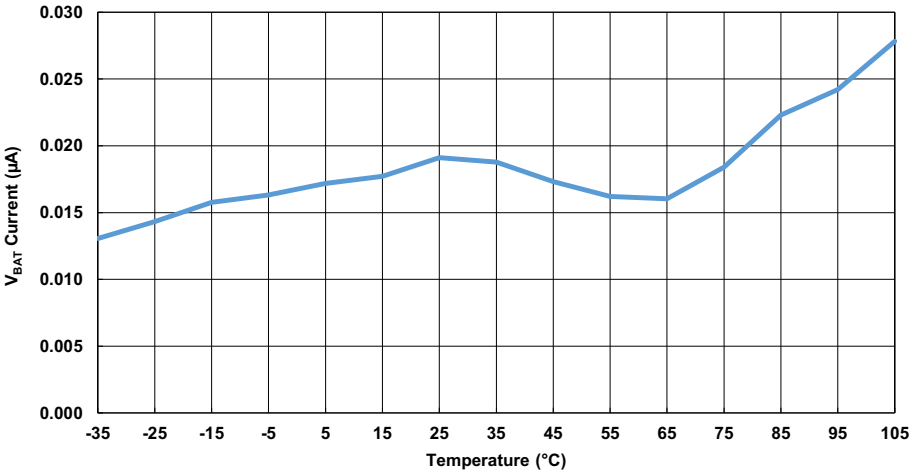


Figure 12. V_{BAT} Current vs Temperature - Powerdown

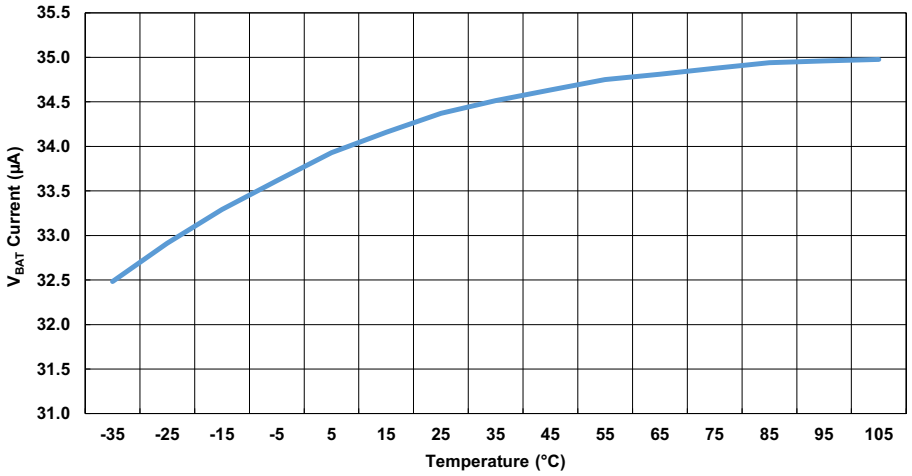


Figure 13. V_{BAT} Current vs Temperature - Normal

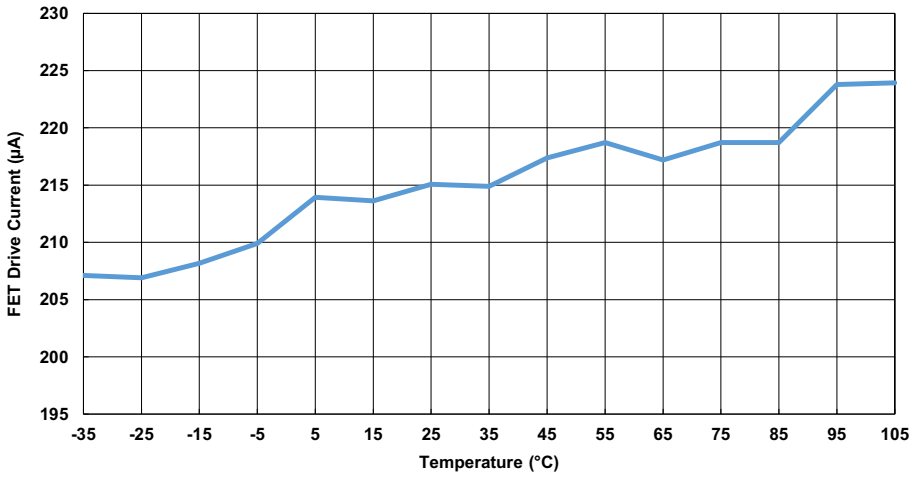


Figure 14. Power FET Drive Current vs Temperature

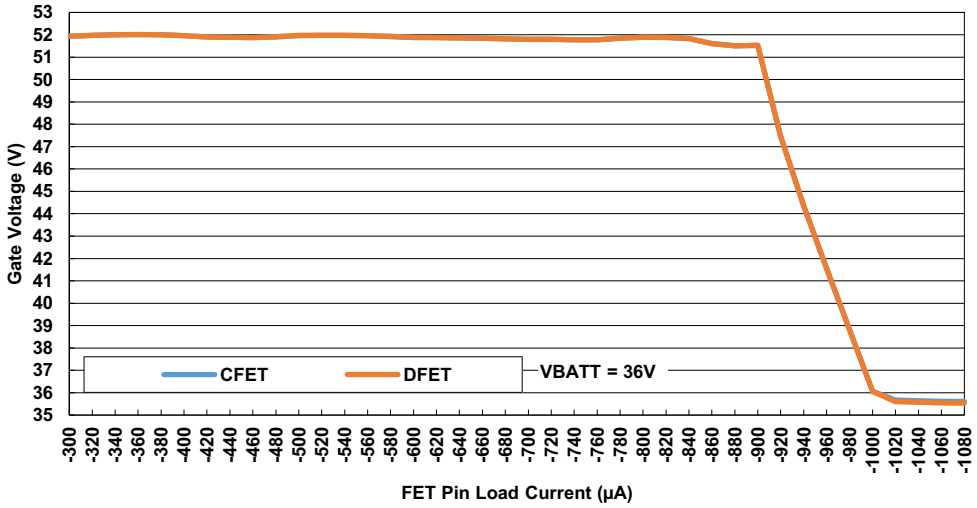


Figure 15. FET Gate Voltage vs Load Current

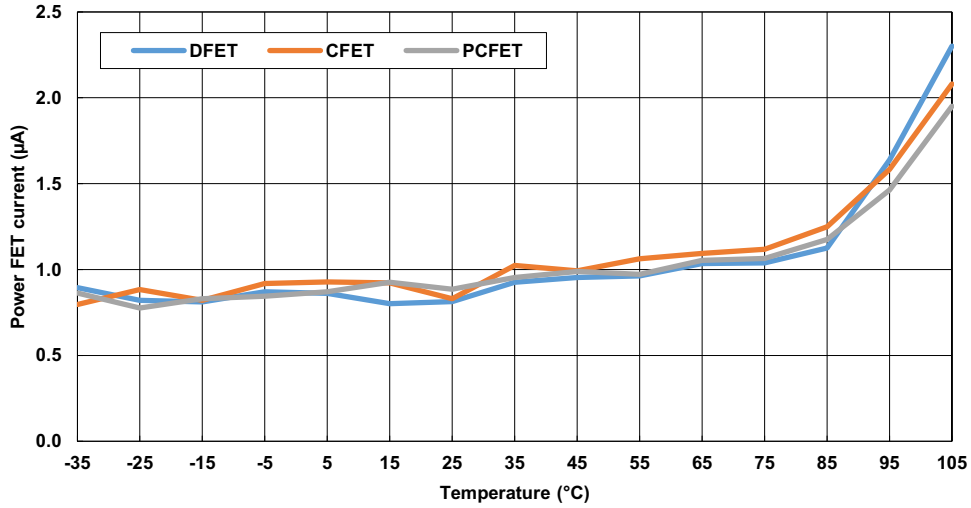


Figure 16. Power FET Pin Leakage Current (OFF) vs Temperature

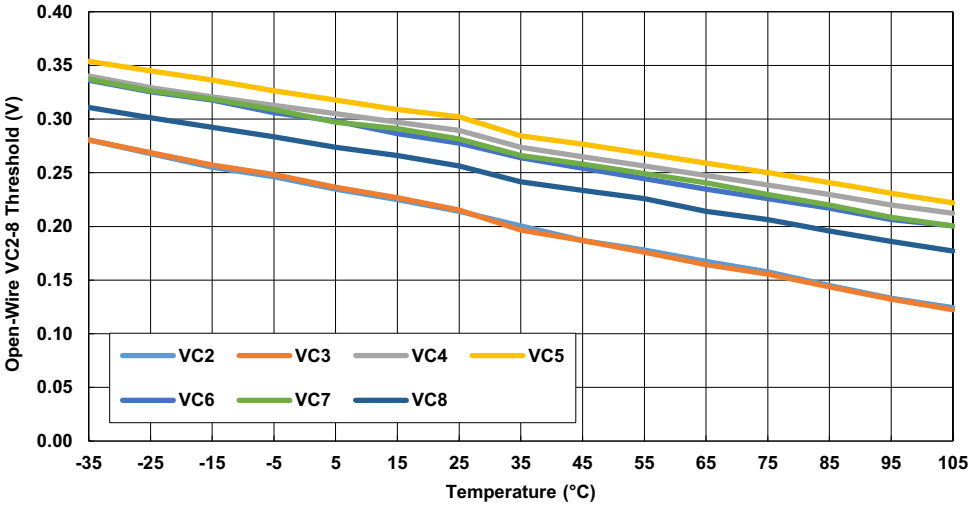


Figure 17. Open-Wire VC2-8 Threshold vs Temperature

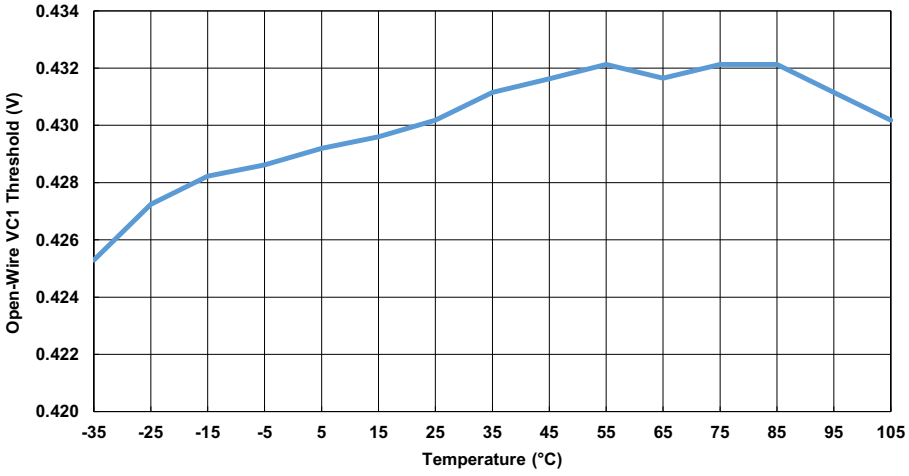


Figure 18. VC1 Open-Wire Threshold vs Temperature

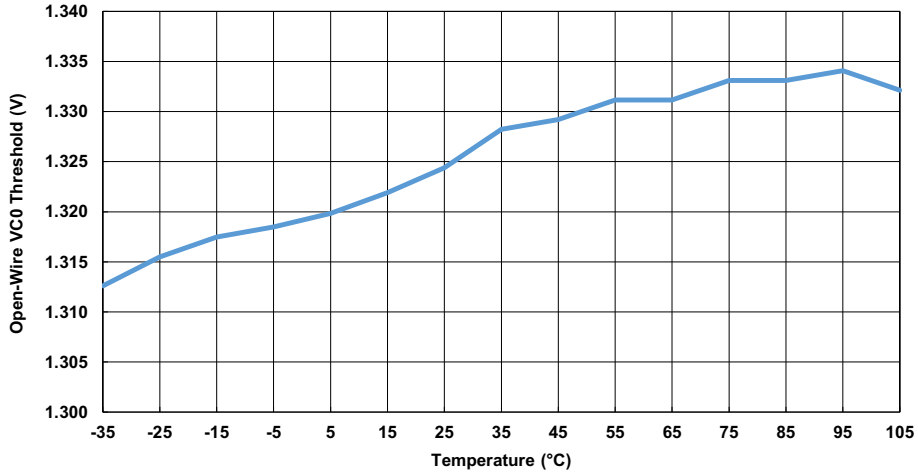


Figure 19. VC0 Open-Wire Threshold vs Temperature

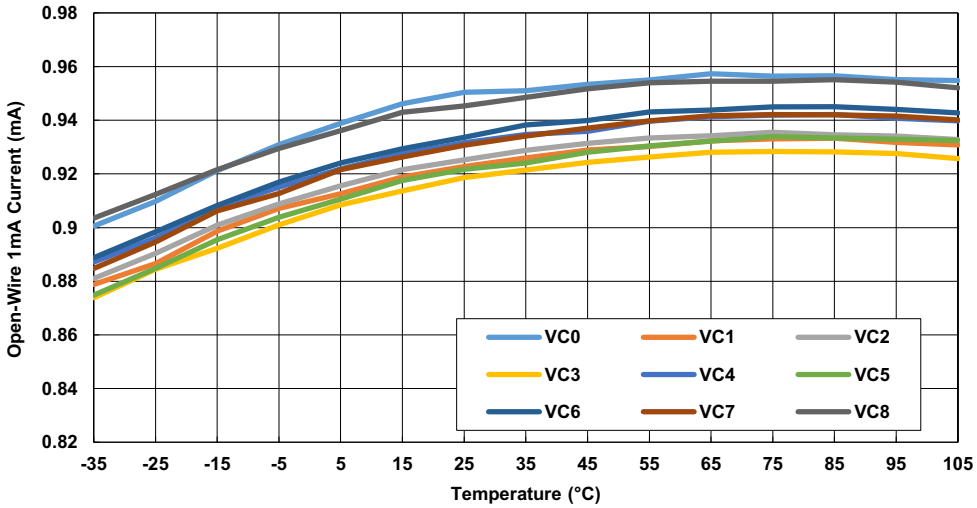


Figure 20. Open-Wire Current vs Temperature

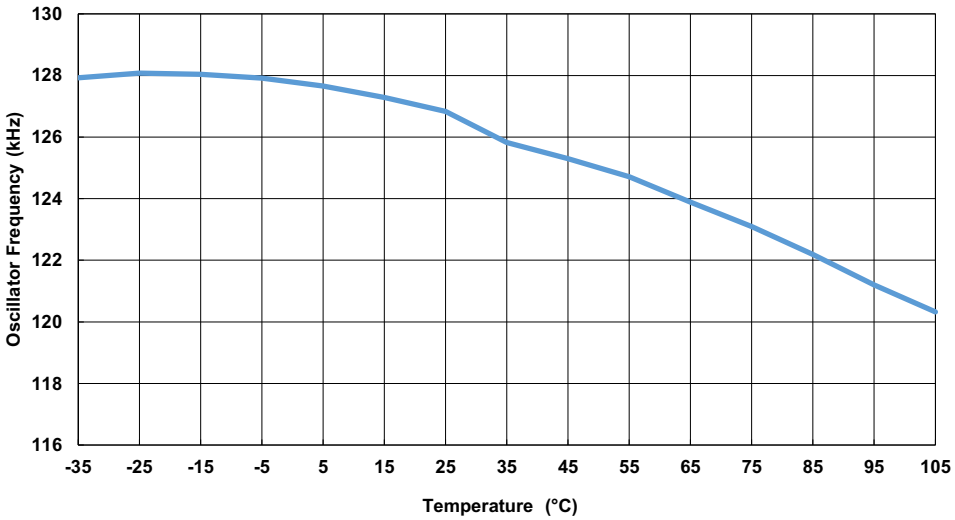


Figure 21. OSC Frequency vs Temperature

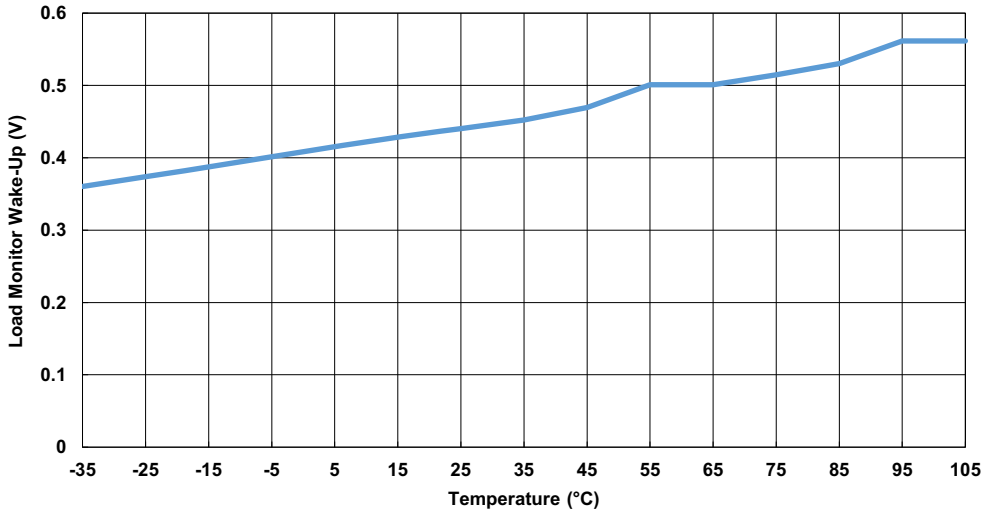


Figure 22. LDMON Wake-Up Threshold vs Temperature

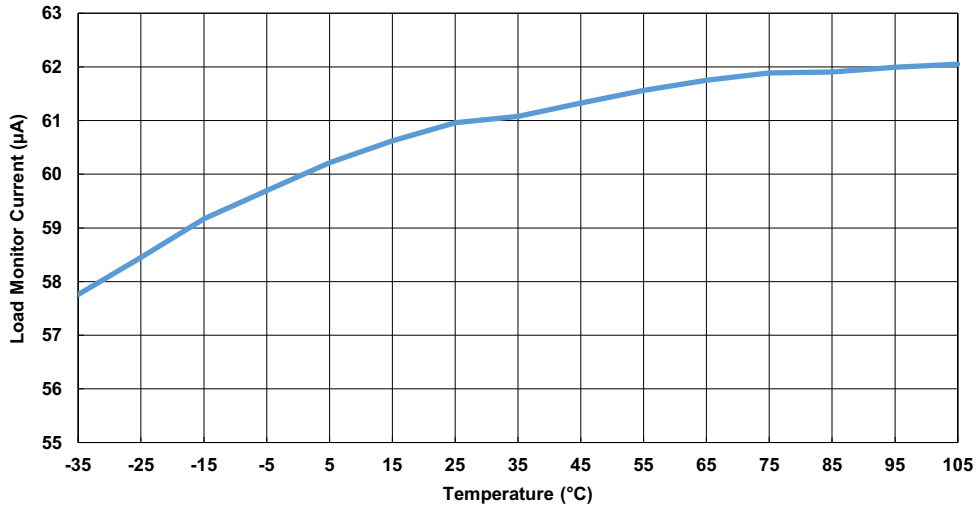


Figure 23. LDMON Detection Current vs Temperature

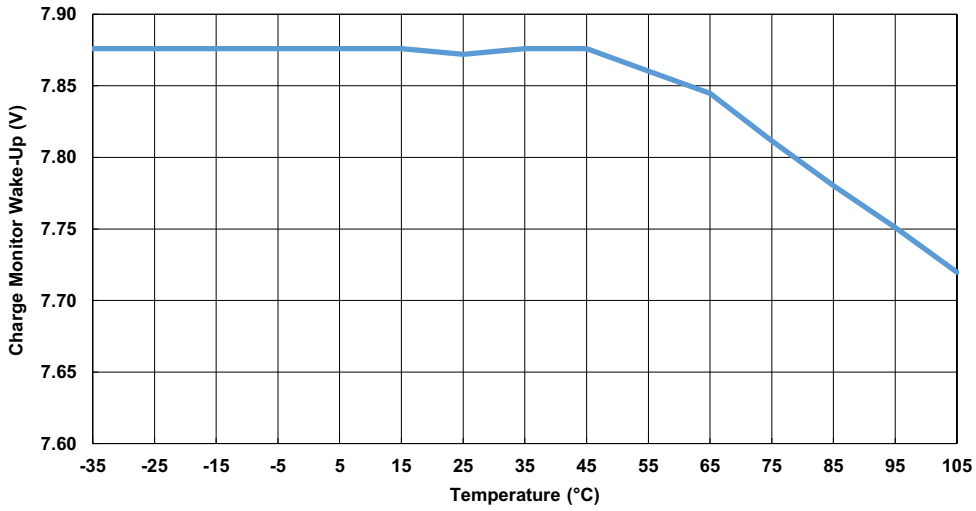


Figure 24. CHMON Wake-Up Threshold vs Temperature

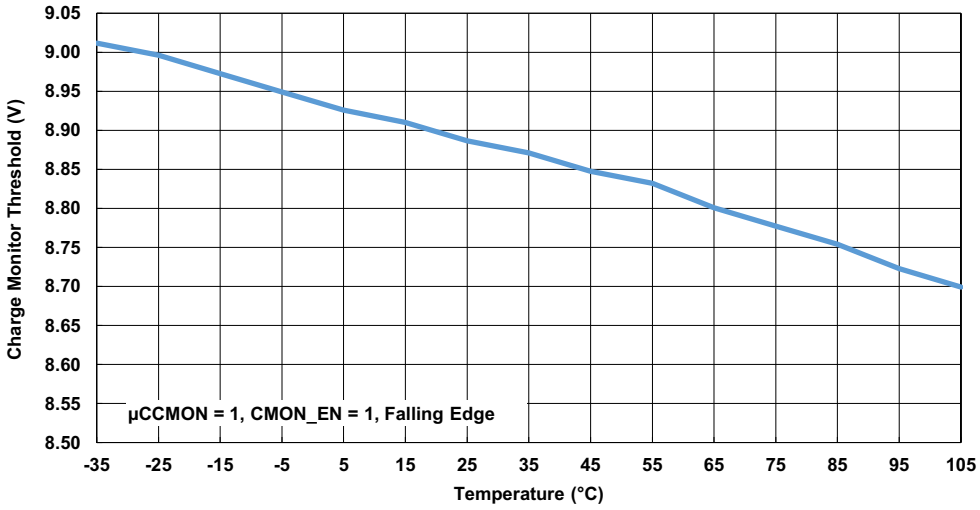


Figure 25. CHMON Recovery Threshold vs Temperature

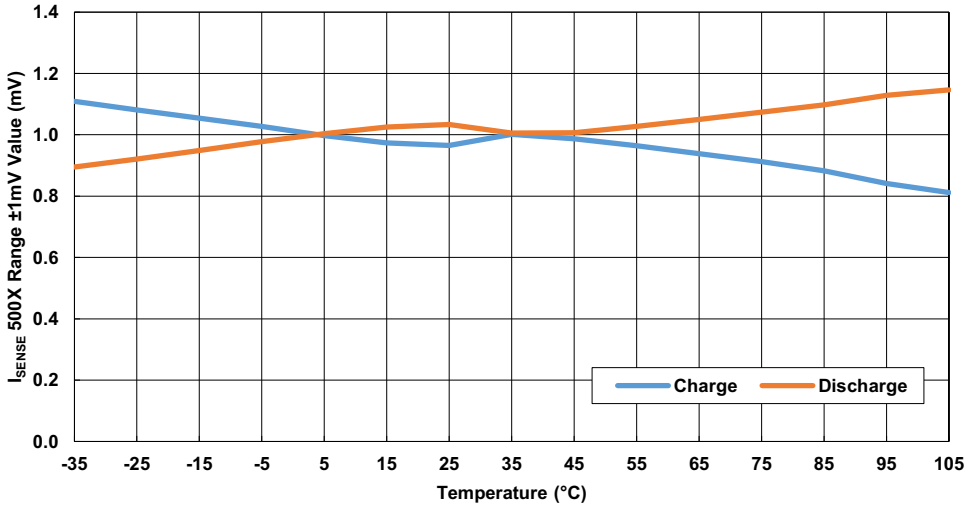


Figure 26. I_{SENSE} Voltage 500x Gain (1mV) vs Temperature

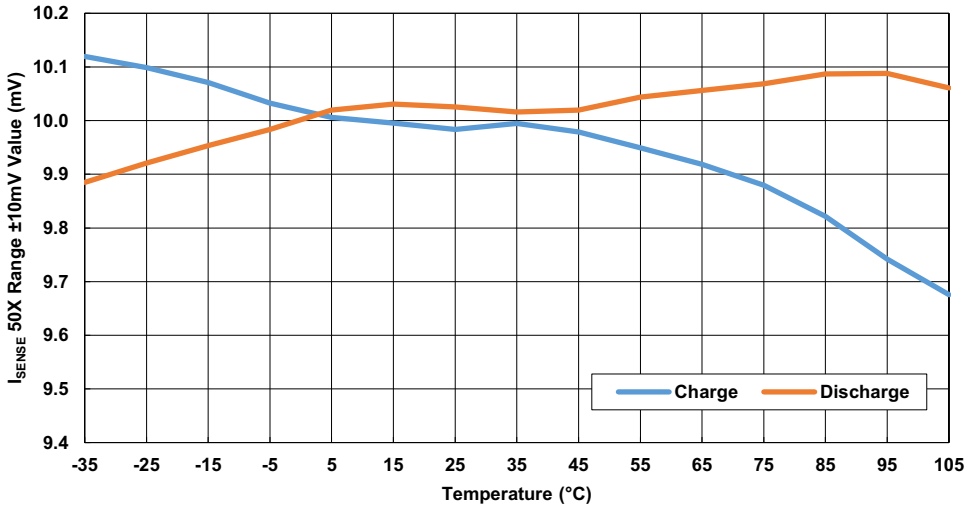


Figure 27. I_{SENSE} Voltage 50x Gain (10mV) vs Temperature

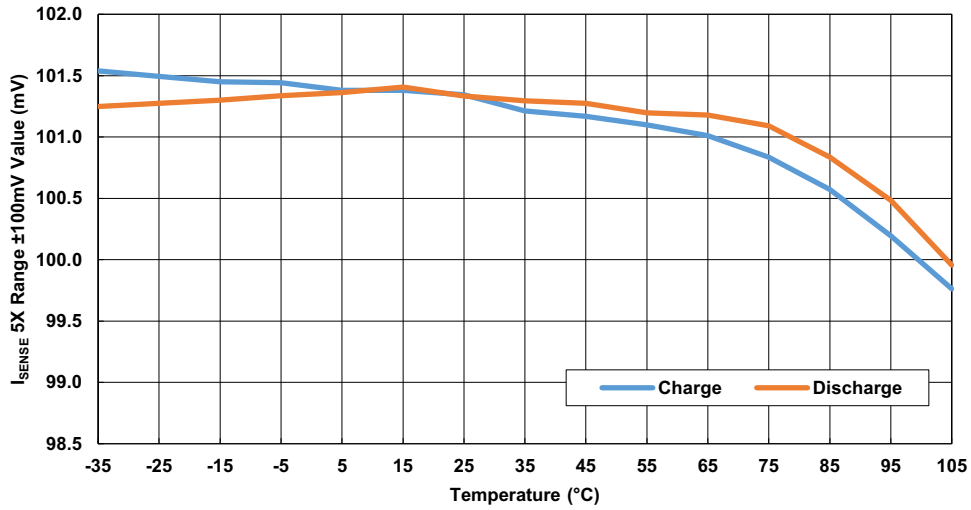


Figure 28. I_{SENSE} Voltage 5x Gain (100mV) vs Temperature

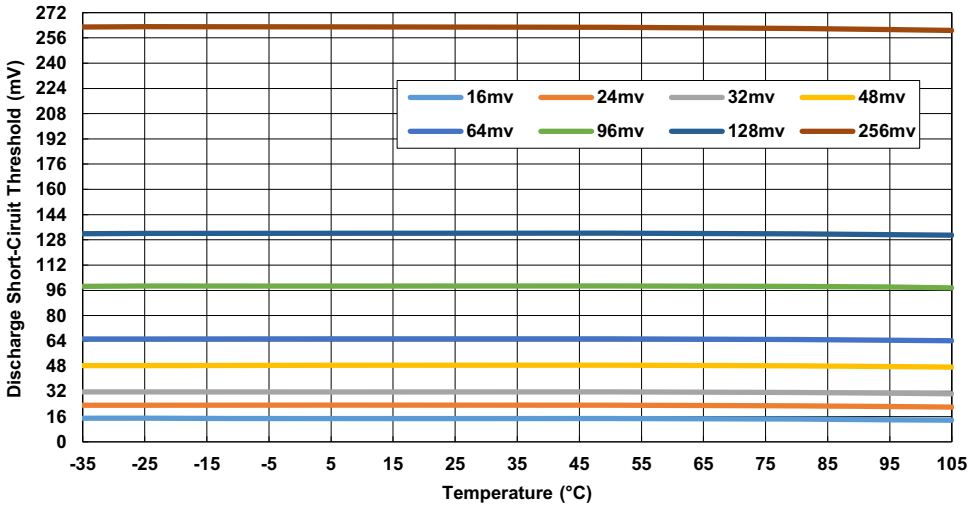


Figure 29. Discharge Short-Circuit Threshold vs Temperature

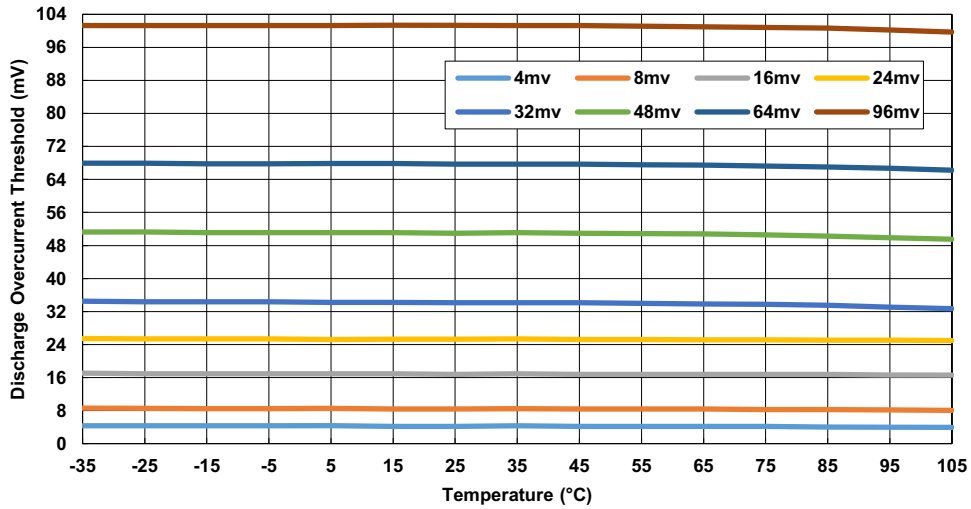


Figure 30. Discharge Overcurrent Threshold vs Temperature

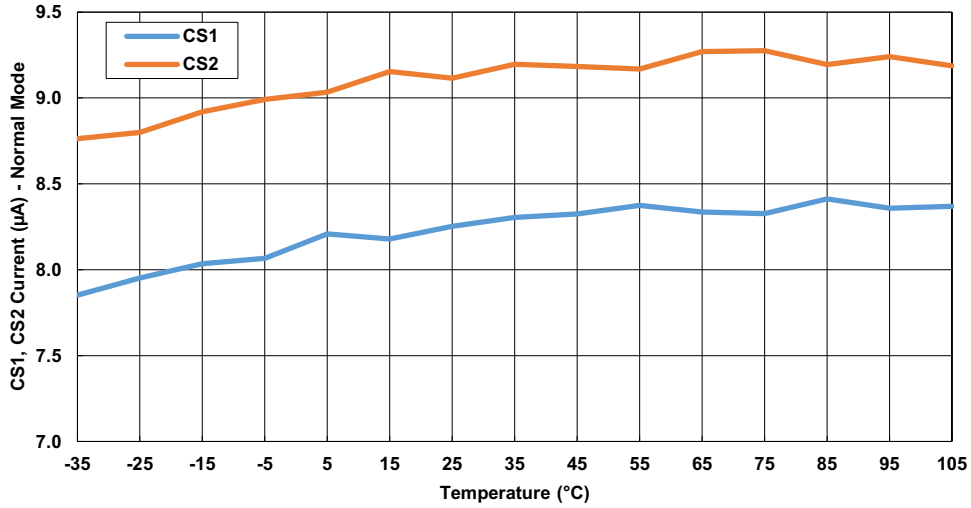


Figure 31. CS1 and CS2 Input Current vs Temperature

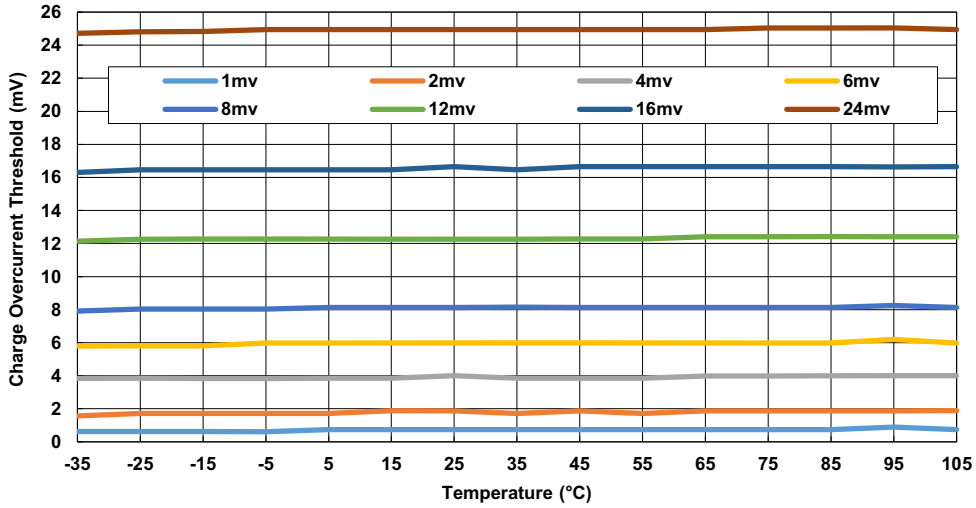


Figure 32. Charge Overcurrent Threshold vs Temperature

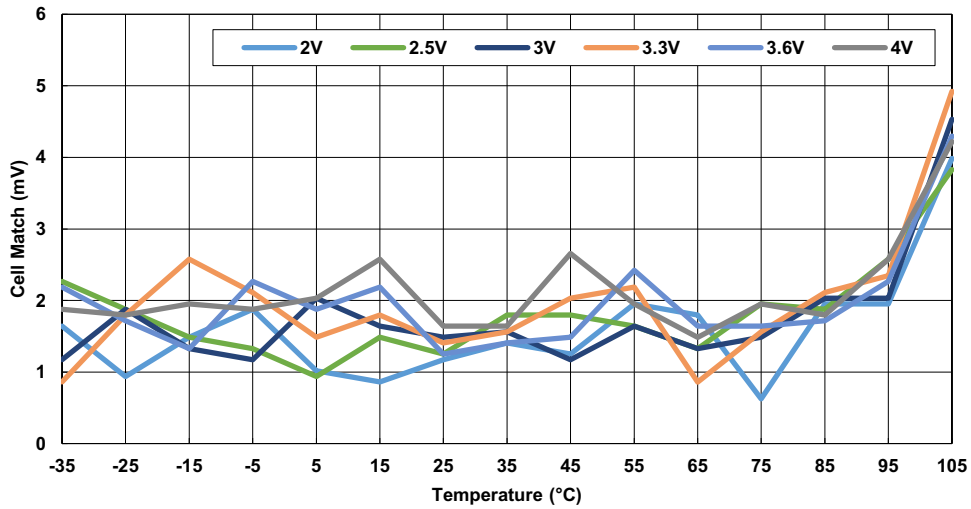


Figure 33. Cell Error vs Temperature

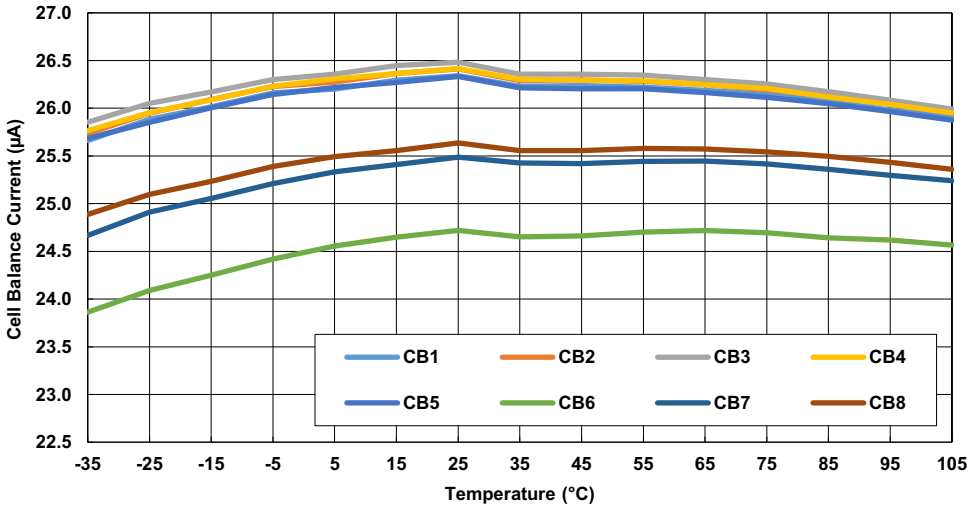


Figure 34. Cell Balance FET Drive Current vs Temperature

4. System Registers

Customer specific operation of the ISL94202 is accomplished through the use of Control/Status Registers and EEPROM. Each register or EEPROM location contains eight bits, accessible using a 7-bit device address plus an 8th bit that indicates a read or a write, followed by the register address. For details about reading and writing registers, see the specific register descriptions in Table 2 and in "Communication Interface" on page 141. EEPROM programming is covered in "Control/Data Registers" on page 138 and "EEPROM Access" on page 147.

The configuration registers are a set of volatile registers that enable customizable operation. These registers are initialized on POR (Power On Reset) by the device from the values stored in the EEPROM. They can be modified through the I^2C port by an MCU, unless the device is in SLEEP Mode or Powerdown. A 1 written to a control or configuration bit causes the action to be taken.

Status Registers include device measurement results, status bits that indicate operational Modes and fault indicator bits. Status Registers are not initialized from EEPROM. Some status registers are used by an external MCU to override device functionality. A 1 read from a status bit indicates that the condition exists.

One status register enables read/write access control of the EEPROM. The EEPROM is a set of non-volatile registers that store configuration parameters (only). Read/write access to these registers is gated by "0x89 - EEPROM Enable" on page 85.

Operation of the ISL94202 is determined by the settings of the configuration registers and measurement results stored in the status registers. The configuration register value must be changed to affect a change in operation. Changes to the EEPROM can only affect an operational change following a POR.

4.1 0x00-0x4B Configuration Registers

Configuration Registers are listed below in Table 2. Each listing includes the register page and address, register name with link for the detailed description, a depiction of the contents with bit names, EEPROM factory default, and the type of register (Read or Read/Write). The ISL94202 is configured for applications by accessing these registers.

Each configuration register is mapped to an EEPROM location that shares the same address. Bit "0x89 - EEPROM Enable" on page 85 determines which is accessed when reading from or writing to these shared addresses.

The ranges and step-sizes listed for threshold registers are the ideal values to be used for calculation purposes. Threshold settings that would require operation outside of the recommended operating conditions are not supported.

Reserved bits (RSV) should be ignored when reading registers and must be set to 0 when writing to them.

Table 2. Register List

Page #	Register Address (Hex)	Register Name	Bit Function 7	6	5	4	3	2	1	0	Factory Default (Hex)	Type
EEPROM/Configuration Registers												
35	00	V_{CELL} OV LSB	V_{CELL} Overvoltage Threshold COV [7:0]								2A	R/W
	01	CDPW, V_{CELL} OV MSB	Charge Detect Pulse-Width CPW3 - CPW0				V_{CELL} Overvoltage Threshold COV [B:8]				1E	R/W
36	02	V_{CELL} OVR LSB	V_{CELL} Overvoltage Recovery Threshold OVR [7:0]								D4	R/W
	03	V_{CELL} OVR MSB	RSV	RSV	RSV	RSV	V_{CELL} Overvoltage Recovery Threshold OVR [B:8]				0D	R/W
37	04	V_{CELL} UV LSB	V_{CELL} Undervoltage Threshold UVL [7:0]								FF	R/W
	05	LDPW, V_{CELL} UV MSB	Load Detect Pulse Width LPW3 - LPW0				V_{CELL} Undervoltage Threshold UVL [B:8]				18	R/W

Table 2. Register List (Continued)

Page #	Register Address (Hex)	Register Name	Bit Function 7	6	5	4	3	2	1	0	Factory Default (Hex)	Type
38	06	V_{CELL} UVR LSB	V_{CELL} Undervoltage Recovery Threshold UVR [7:0]								FF	R/W
	07	V_{CELL} UVR MSB	RSV	RSV	RSV	RSV	V_{CELL} Undervoltage Recovery Threshold UVR [B:8]				09	R/W
38	08	V_{CELL} OVLO LSB	V_{CELL} Overvoltage Lockout Threshold OVLO [7:0]								7F	R/W
	09	V_{CELL} OVLO MSB	RSV	RSV	RSV	RSV	V_{CELL} Overvoltage Lockout Threshold OVLO [B:8]				0E	R/W
39	0A	V_{CELL} UVLO LSB	V_{CELL} Undervoltage Lockout Threshold UVLO [7:0]								00	R/W
	0B	V_{CELL} UVLO MSB	RSV	RSV	RSV	RSV	V_{CELL} Undervoltage Lockout Threshold UVLO [B:8]				06	R/W
40	0C	V_{CELL} EOC LSB	V_{CELL} End-of-Charge Threshold EOC [7:0]								FF	R/W
	0D	V_{CELL} EOC MSB	RSV	RSV	RSV	RSV	V_{CELL} End-of-Charge Threshold EOC [B:8]				0D	R/W
40	0E	V_{CELL} LVCL LSB	V_{CELL} Low Voltage Charge Level LVCL [7:0]								AA	R/W
	0F	V_{CELL} LVCL MSB	RSV	RSV	RSV	RSV	V_{CELL} Low Voltage Charge Level LVCL [B:8]				07	R/W
41	10	V_{CELL} OVDT LSB	V_{CELL} Overvoltage Delay Timer OVDT [7:0]								01	R/W
	11	V_{CELL} OVDTU, V_{CELL} OVDT MSB	RSV	RSV	RSV	RSV	V_{CELL} Overvoltage Delay Timer Unit OVDTU [1:0]		V_{CELL} Overvoltage Delay Timer OVDT [9:8]		08	R/W
42	12	V_{CELL} UVDT LSB	V_{CELL} Undervoltage Delay Time UVDT [7:0]								01	R/W
	13	V_{CELL} UVDTU, V_{CELL} UVDT MSB	RSV	RSV	RSV	RSV	V_{CELL} Undervoltage Delay Timer Unit UVDTU [1:0]		V_{CELL} Undervoltage Delay Timer UVDT [9:8]		08	R/W
43	14	OWT LSB	Open-Wire Timing OWT [7:0]								14	R/W
	15	OWTU, OWT MSB	RSV	RSV	RSV	RSV	RSV	RSV	Open-Wire Timing Unit OWTU	Open-Wire Timing OWT [8]	02	R/W
43	16	DOCT LSB	Discharge Overcurrent Timer DOCT [7:0]								A0	R/W
	17	DOC , DOCTU, DOCT MSB	RSV	Discharge Overcurrent Threshold DOC [2:0]			Discharge Overcurrent Timer Unit DOCTU [1:0]		Discharge Overcurrent Timer DOCT [9:8]		44	R/W
46	18	COCT LSB	Charge Overcurrent Timer COCT [7:0]								A0	R/W
	19	COC, COCTU, COCT MSB	RSV	Charge Overcurrent Threshold COC [2:0]			Charge Overcurrent Timer Unit COCTU [1:0]		Charge Overcurrent Timer COCT [9:8]		44	R/W
48	1A	DSCT LSB	Discharge Short-Circuit Timer DSCT [7:0]								C8	R/W
	1B	DSC, DSCTU, DSCT MSB	RSV	Discharge Short-Circuit Threshold DSC [2:0]			Discharge Short-Circuit Timer Unit DSCTU [1:0]		Discharge Short-Circuit Timer DSCT [9:8]		60	R/W
49	1C	CBMIN LSB	Cell Balance Minimum Voltage CBMIN [7:0]								55	R/W
	1D	CBMIN MSB	RSV	RSV	RSV	RSV	Cell Balance Minimum Voltage CBMIN [B:8]				0A	R/W
50	1E	CBMAX LSB	Cell Balance Maximum Voltage CBMAX [7:0]								70	R/W
	1F	CBMAX MSB	RSV	RSV	RSV	RSV	Cell Balance Maximum Voltage CBMAX [B:8]				0D	R/W

Table 2. Register List (Continued)

Page #	Register Address (Hex)	Register Name	Bit Function 7	6	5	4	3	2	1	0	Factory Default (Hex)	Type
50	20	CBMIND LSB	Cell Balance Minimum Delta Voltage CBMIND [7:0]								10	R/W
	21	CBMIND MSB	RSV	RSV	RSV	RSV	Cell Balance Minimum Delta Voltage CBMIND [B:8]				00	R/W
51	22	CBMAXD LSB	Cell Balance Maximum Delta Voltage CBMAXD [7:0]								AB	R/W
	23	CBMAXD MSB	RSV	RSV	RSV	RSV	Cell Balance Maximum Delta Voltage CBMAXD [B:8]				01	R/W
52	24	CBON LSB	Cell Balance On-Time CBON [7:0]								02	R/W
	25	CBONU, CBON MSB	RSV	RSV	RSV	RSV	Cell Balance On Time Unit CBONU [1:0]		Cell Balance On Time CBON [9:8]		08	R/W
53	26	CBOFF LSB	Cell Balance Off-Time CBOFF [7:0]								02	R/W
	27	CBOFFU, CBOFF MSB	RSV	RSV	RSV	RSV	Cell Balance Off Time Unit CBOFFU [1:0]		Cell Balance Off Time CBOFF [9:8]		08	R/W
53	28	CBUT LSB	Cell Balance Under-Temperature Limit CBUT [7:0]								F2	R/W
	29	CBUT MSB	RSV	RSV	RSV	RSV	Cell Balance Under-Temperature Limit CBUT [B:8]				0B	R/W
54	2A	CBUTR LSB	Cell Balance Under-Temperature Recovery Level CBUTR [7:0]								93	R/W
	2B	CBUTR MSB	RSV	RSV	RSV	RSV	Cell Balance Under-Temperature Recovery Level CBUTR [B:8]				0A	R/W
55	2C	CBOT LSB	Cell Balance Over-Temperature Limit CBOT [7:0]								B6	R/W
	2D	CBOT MSB	RSV	RSV	RSV	RSV	Cell Balance Over-Temperature Limit CBOT [B:8]				04	R/W
56	2E	CBOTR LSB	Cell Balance Over-Temperature Recovery Level CBOTR [7:0]								3E	R/W
	2F	CBOTR MSB	RSV	RSV	RSV	RSV	Cell Balance Over-Temperature Recovery Level CBOTR [B:8]				05	R/W
56	30	COT LSB	Charge Over-Temperature Limit COT [7:0]								B6	R/W
	31	COT MSB	RSV	RSV	RSV	RSV	Charge Over-Temperature Limit COT [B:8]				04	R/W
57	32	COTR LSB	Charge Over-Temperature Recovery Level COTR [7:0]								3E	R/W
	33	COTR MSB	RSV	RSV	RSV	RSV	Charge Over-Temperature Recovery Level COTR [B:8]				05	R/W
58	34	CUT LSB	Charge Under-Temperature Limit CUT [7:0]								F2	R/W
	35	CUT MSB	RSV	RSV	RSV	RSV	Charge Under-Temperature Limit CUT [B:8]				0B	R/W
58	36	CUTR LSB	Charge Under-Temperature Recovery Level CUTR [7:0]								93	R/W
	37	CUTR MSB	RSV	RSV	RSV	RSV	Charge Under-Temperature Recovery Level CUTR [B:8]				0A	R/W
59	38	DOT LSB	Discharge Over-Temperature Voltage DOT [7:0]								B6	R/W
	39	DOT MSB	RSV	RSV	RSV	RSV	Discharge Over-Temperature Limit DOT [B:8]				04	R/W
60	3A	DOTR LSB	Discharge Over-Temperature Recovery Level DOTR [7:0]								3E	R/W
	3B	DOTR MSB	RSV	RSV	RSV	RSV	Discharge Over-Temperature Recovery Level DOTR [B:8]				05	R/W
61	3C	DUT LSB	Discharge Under-Temperature Limit DUT [7:0]								F2	R/W
	3D	DUT MSB	RSV	RSV	RSV	RSV	Discharge Under-Temperature Limit DUT [B:8]				0B	R/W

Table 2. Register List (Continued)

Page #	Register Address (Hex)	Register Name	Bit Function 7	6	5	4	3	2	1	0	Factory Default (Hex)	Type
61	3E	DUTR LSB	Discharge Under-Temperature Recovery Voltage DUTR [7:0]								93	R/W
	3F	DUTR MSB	RSV	RSV	RSV	RSV	Discharge Under-Temperature Recovery Voltage DUTR [B:8]				0A	R/W
62	40	IOT LSB	Internal Over-Temperature Voltage Limit IOT [7:0]								64	R/W
	41	IOT MSB	RSV	RSV	RSV	RSV	Internal Over-temperature voltage Limit IOT [B:8]				06	R/W
63	42	IOTR LSB	Internal Over-Temperature Recovery Voltage IOTR [7:0]								10	R/W
	43	IOTR MSB	RSV	RSV	RSV	RSV	Internal Over-temperature Recovery Voltage IOTR [B:8]				06	R/W
64	44	V_{CELL} SLV LSB	V_{CELL} SLEEP Level Voltage SLV [7:0]								AA	R/W
	45	V_{CELL} SLV MSB	RSV	RSV	RSV	RSV	V_{CELL} SLEEP Level Voltage SLV [B:8]				06	R/W
64	46	SDT LSB	SLEEP Delay Timer SDT [7:0]								0F	R/W
	47	WDT, SDTU, SDT MSB	Watchdog Timer WDT4 - WDT0					SLEEP Delay Timer Unit SDTU[1:0]		SLEEP Delay Timer SDT [8]	FC	R/W
66	48	MODE_T	SLEEP Mode MOD7 - MOD4				IDLE/DOZE Mode MOD3 - MOD0				FF	R/W
66	49	CELL_S	Cell Select (Enable) CELL8 - CELL1								83	R/W
67	4A	Setup 0	CFPSD	RSV	XT2M	TGain	RSV(0)	PCFET	DOWD	OWPSD	00	R/W
68	4B	Setup 1	CBDD	CBDC	DFOUV	CFOOV	UVLOPD	RSV	RSV	CBEOC	40	R/W

4.1.1 0x00-01 CDPW & V_{CELL} OV

The Charger Detection Pulse Width setting and upper 4 bits of the V_{Cell} Overvoltage threshold setting are stored at address 0x01. The lower 8 bits of the V_{Cell} Overvoltage threshold setting are stored at address 0x00.

Table 3. CDPW & OV

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	COV7	COV6	COV5	COV4	COV3	COV2	COV1	COV0	Value
0x00 Default	0	0	1	0	1	0	1	0	0x2A
Bit Name	CDPW3	CDPW2	CDPW1	CDPW0	COVB	COVA	COV9	COV8	Value
0x01 Default	0	0	0	1	1	1	1	0	0x1E

4.1.1.1 V_{CELL} OV

The V_{Cell} Overvoltage threshold sets the upper operational voltage limit for enabled ("0x49 Cell Select" on page 67) cells. Each time a cell voltage is measured it is compared to this threshold. If any cell voltage rises above this threshold for longer than the setting of "0x10-11 VC_{ELL} OV Timer" on page 41, CFET is turned OFF and fault bit "0x80.0 OVF" on page 73 is set. This action is also dependent on the setting of register "0x4B.4 CFODOV" on page 69 and bits "0x87.6 µCFET" on page 82.

The threshold "0x02-03 V_{CELL} OVR" on page 36 sets the voltage level the cells must drop below before the OV fault clears and allows the CFET to turn back on.

The threshold setting is 12-bits split across two 8-bit registers at addresses:

- 0x00.[7:0]: Lower 8 bits
- 0x01.[3:0]: Upper 4 bits

The formula to convert the register decimal value to voltage is:

$$V_{CELL}OV = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default setting results in a threshold voltage of ~4.25V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{V_{CELL}OV \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

4.1.1.2 0x01.7:4 CDPW

The Charge Detection Pulse Width bits set the length of time the ISL94202 CHMON pin function is enabled. If the pin voltage is above the Charge Monitor Input threshold (“V_{CHMON}” on page 16 or “VWKUP1” on page 19) at the end of the set time, the device assumes a charger is present and reacts accordingly. Each Least Significant Bit (LSB) is 1ms, which provides for a programmable range from 0ms to 15ms. The default setting is 1ms. This setting determines how long the charger connection node is loaded (“ILDMON” on page 16) by the “CHMON Pin (37)” on page 99. If a charger is present, the voltage remains above the threshold and a charger is detected. In the absence of a charger or other device that maintains the voltage under this load current, the voltage drops below the detection threshold and no charger is detected (see “0x82.1 CH_PRSNT” on page 77).

4.1.2 0x02-03 V_{CELL} OVR

The 12-bit V_{CELL} Overvoltage Recovery threshold setting is shared between two registers. The upper 4 bits of the setting are stored in the lower 4 bits of 0x03 while the remaining 8 bits of OVR are stored in 0x02 as shown in Table 4. The upper 4 bits of register 0x03 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 4. OVR

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0	Value
0x02 Default	1	1	0	1	0	1	0	0	0xD4
Bit Name	RSV	RSV	RSV	RSV	OVRB	OVRA	OVR9	OVR8	Value
0x03 Default	0	0	0	0	1	1	0	1	0x0D

The V_{CELL}OVR setting must be less than the V_{CELL}OV threshold for proper operation. The difference between OV and OVR settings functions as hysteresis. If an overvoltage fault (“0x80.0 OVF” on page 73) is detected, the cell voltages must drop below the OVR threshold for the setting “0x10-11 VC_{ELL} OV Timer” on page 41 for the fault bit to clear, then the device enables the power FETs (assuming no faults present). This action is also dependent on the setting of “0x4B.4 CFODOV” on page 69 and bit “0x87.6 µCFET” on page 82.

The OVR threshold also sets the recovery voltage to clear and “0x80.1 OVLOF” on page 73 from “0x08-09 V_{CELL}-OVLO” on page 38 condition.

The formula to convert the register decimal value to voltage is:

$$V_{CELL}OVR = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~4.149V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{V_{CELL}OVR \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

4.1.3 0x04-05 LDPW & V_{CELL} UV

The Load Detect Pulse Width setting and the upper 4 bits of the V_{CELL} Undervoltage threshold setting are stored at address 0x05 as shown in Table 5. The lower 8 bits of the V_{CELL} Undervoltage threshold setting are stored at address 0x04.

Table 5. LDPW & UV

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	UVT7	UVT6	UVT5	UVT4	UVT3	UVT2	UVT1	UVT0	Value
0x04 Default	1	1	1	1	1	1	1	1	0xFF
Bit Name	LDPW3	LDPW2	LDPW1	LDPW0	UVTB	UVTA	UVT9	UVT8	Value
0x05 Default	0	0	0	1	0	1	1	1	0x18

4.1.3.1 V_{CELL} UV

The V_{CELL} Undervoltage threshold sets the lower operational voltage limit for all cells. Each time a cell voltage is measured it is compared to this threshold. If any cell voltage falls below this threshold voltage for longer than the setting of "0x12-13 V_{CELL} UV Timer" on page 42, DFET is turned OFF and fault bit "0x80.2 UVF" on page 72 is set. This action is also dependent on the setting of register "0x4B.5 DFODUV" on page 69 and bits "0x87.6 µCFET" on page 82.

For recovery from this fault see "0x06-07 V_{CELL} UVR" on page 38.

The threshold setting is 12-bits split across two 8-bit registers at addresses:

- 0x04.[7:0]: Lower 8 bits
- 0x05.[3:0]: Upper 4 bits

The formula to convert the register decimal value to voltage is:

$$V_{CELL}UV = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~2.699V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{V_{CELL}UV \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

4.1.3.2 0x05.7:4 LDPW

The Load Detection Pulse Width bits set the length of time the ISL94202 LDMON pin function is enabled. If the pin voltage is below the Load Monitor Input threshold ("V_{LDMON}" on page 16 or "VWKUP2" on page 19) at the end of the set time, the device assumes a load is present and reacts accordingly. Each LSB is 1ms, providing for a programmable range from 0ms to 15ms. The default setting is 1ms. This setting determines how long the load connection node is loaded ("ILDMON" on page 16) by the "LDMON Pin (38)" on page 104, if a load is present the voltage drops below the threshold and a load is detected. In the absence of a load the voltage remains above the detection threshold and no load is detected (see "0x82.0 LD_PRSNT" on page 77).

4.1.4 0x06-07 V_{CELL} UVR

The V_{CELL} Undervoltage Recovery threshold setting is shared between two registers. The upper 4 bits of the UVR setting are stored in the lower 4 bits of 0x07 while the remaining 8 bits of OVR are stored in 0x06 as shown in Table 6. The upper 4 bits of register 0x07 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 6. UVR

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	UVR7	UVR6	UVR5	UVR4	UVR3	UVR2	UVR1	UVR0	Value
0x06 Default	1	1	1	1	1	1	1	1	0xFF
Bit Name	RSV	RSV	RSV	RSV	UVRB	UVRA	UVR9	UVR8	Value
0x07 Default	0	0	0	0	1	0	0	0	0x09

The V_{CELL}UVR setting must be greater than the V_{CELL}UV threshold for proper operation. The difference between UV and UVR settings functions as hysteresis. If an undervoltage fault ("0x80.2 UVF" on page 72) is detected, the cell voltages must rise above the UVR threshold for the setting "0x12-13 V_{CELL} UV Timer" on page 42 for the fault bit to clear, then the device enables the power FETs (assuming no faults present). This action is also dependent on the setting of "0x4B.5 DFODUV" on page 69 and bit "0x87.6 µCFET" on page 82.

The UVR threshold also governs recovery from "0x0A-0B V_{CELL} UVLO" on page 39.

The formula to convert the register decimal value to voltage is:

$$V_{CELL}UVR = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~3.0V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{V_{CELL}UVR \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

4.1.5 0x08-09 V_{CELL} OVLO

The V_{CELL} Overvoltage Lockout threshold setting is shared between two registers. The upper 4 bits of the OVLO setting are stored in the lower 4 bits of 0x09 while the remaining 8 bits of OVLO are stored in 0x08 as shown in Table 7. The upper 4 bits of register 0x09 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 7. OVLO

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	OVLO7	OVLO6	OVLO5	OVLO4	OVLO3	OVLO2	OVLO1	OVLO0	Value
0x08 Default	0	1	1	0	1	1	1	1	0x7F
Bit Name	RSV	RSV	RSV	RSV	OVLOB	OVLOA	OVLO9	OVLO8	Value
0x09 Default	0	0	0	0	1	1	1	0	0x0E

If any cell voltage rises above the V_{CELL}OVLO threshold for 5 consecutive measurements, the device enters an Overvoltage Lockout condition. This causes the CFET/PCFET to turn OFF, bit "0x80.1 OVLOF" on page 73 is set, the cell balance FETs are turned OFF, and the "PSD Pin (32)" on page 98 is set to active high. Neither CFET or

PCFET can be enabled during an OVLO. The OVLO function can be disabled by setting the OVLO threshold to 0x0FFF.

V_{CELL}OVLO must be set greater than V_{CELL}OV for proper operation.

Recovery is determined by the setting of "0x02-03 V_{CELL} OVR" on page 36. Typically an Overvoltage Lockout is intended to flag a voltage considered too high to safely discharge.

The formula for converting from register digital value to voltage is:

$$V_{CELL}OVLO = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~3.0V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{V_{CELL}OVLO \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

4.1.6 0x0A-0B V_{CELL} UVLO

The V_{CELL} Undervoltage Lockout threshold setting is shared between two registers. The upper 4 bits of the UVLO setting are stored in the lower 4 bits of 0x0B while the remaining 8 bits of UVLO are stored in 0x0A as shown in Table 8. The upper 4 bits of register 0x0B are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 8. UVLO

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	UVLO7	UVLO6	UVLO5	UVLO4	UVLO3	UVLO2	UVLO1	UVLO0	Value
0x0A Default	0	0	0	0	0	0	0	0	0x00
Bit Name	RSV	RSV	RSV	RSV	UVLOB	UVLOA	UVLO9	UVLO8	Value
0x0B Default	0	0	0	0	0	1	1	0	0x06

If any cell voltage falls below the V_{CELL}UVLO threshold for 5 consecutive measurements, the device enters an Undervoltage Lockout condition. This causes the DFET to turn OFF, bit "0x80.3 UVLOF" on page 72 is set, and the cell balance FETs are turned OFF. If bit "0x4B.3 UVLOPD" on page 70 is set to 1, a UVLO condition forces the part into the Powerdown State ("System Modes" on page 119). This action occurs regardless of the MCU FET control bits setting ("0x87.6 µCFET" on page 82). The UVLO function can be disabled by setting UVLO to 0x0000.

V_{CELL}UVLO must be set below V_{CELL}UV for proper operation.

Recovery is determined by the setting of "0x06-07 V_{CELL} UVR" on page 38. Typically an Undervoltage Lockout is intended to flag a voltage considered to low to safely charge.

The formula for converting from register digital value to voltage is:

$$V_{CELL}UVLO = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~1.8V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{V_{CELL}UVLO \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

4.1.7 0x0C-0D V_{CELL} EOC

The V_{CELL} End-of-Charge threshold (VEOC) setting is shared between two registers. The upper 4 bits of the VEOC setting are stored in the lower 4 bits of 0x0D while the remaining 8 bits of VEOC are stored in 0x0C as shown in Table 9. The upper 4 bits of register 0x0D are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 9. VEOC

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0	Value
0x0C Default	1	1	1	1	1	1	1	1	0xFF
Bit Name	RSV	RSV	RSV	RSV	EOCB	EOCA	EOC9	EOC8	Value
0x0D Default	0	0	0	0	1	1	0	1	0x0D

If any cell voltage rises above the V_{CELL}EOC threshold, the device enters an End-of-Charge condition. This sets bit “0x81.7 VEOC” on page 73 and the “EOC Pin (35)” on page 99 is pulled low. The $\overline{EOC}$ output can signal an external MCU or enable an LED circuit to signal a fully charged pack.

An VEOC condition also effects cell balancing operation, see “0x4B.0 CB_EOC” on page 70 for more information.

The formula for converting from register digital value to voltage is:

$$V_{CELL}EOC = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~4.199V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{V_{CELL}EOC \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

4.1.8 0x0E-0F V_{CELL} LVCL

The V_{CELL} Low Voltage Charge Level setting is shared between two registers. The upper 4 bits of the LVCL setting are stored in the lower 4 bits of 0x0F while the remaining 8 bits of LVCL are stored in 0x0E as shown in Table 10. The upper 4 bits of register 0x0F are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 10. LVCL

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	LVCL7	LVCL6	LVCL5	LVCL4	LVCL3	LVCL2	LVCL1	LVCL0	Value
0x0E Default	1	0	1	0	1	0	1	0	0xAA
Bit Name	RSV	RSV	RSV	RSV	LVCLB	LVCLA	LVCL9	LVCL8	Value
0x0F Default	0	0	0	0	0	1	1	1	0x07

If any cell voltage falls below the V_{CELL}LVCL, the device sets bit "0x82.7 LVCHG" on page 76 to 1. If any cell voltage falls below this level and "0x4A.2 PCFETE" on page 68 is set to 1, the device turns on the PCFET output instead of the CFET output to enable initial trickle charging of the cells. After the cell voltages rise above V_{CELL}LVCL, CFET is enabled and PCFET is disabled.

To disable the Pre-Charge FET function set bit PCFETE to 0 and set V_{CELL}LVCL to 0x0000.

The formula for converting from register digital value to voltage is:

$$V_{CELL}LVCL = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~2.3V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{V_{CELL}LVCL \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

4.1.9 0x10-11 V_{CELL} OV Timer

The 12-bit V_{CELL} Overvoltage Delay Timer setting is shared between two registers. The upper 4 bits of the OVDT setting are stored in the lower 4 bits of 0x11 while the remaining 8 bits of OVDT are stored in 0x10 as shown in Table 11. The upper 4 bits of register 0x11 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 11. OVDT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	OVDT7	OVDT6	OVDT5	OVDT4	OVDT3	OVDT2	OVDT1	OVDT0	Value
0x10 Default	0	0	0	0	0	0	0	1	0x01
Bit Name	RSV	RSV	RSV	RSV	OVDTU1	OVDTU0	OVDT9	OVDT8	Value
0x11 Default	0	0	0	0	1	0	0	0	0x08

A V_{CELL}OV condition ("V_{CELL} OV" on page 35) must be present for at least the time specified by this setting for the device to enter an Overvoltage condition. The OVDT 12-bit value is split into a 2-bit unit selection value ("V_{CELL} OVDTU" on page 41) and a 10-bit time value ("V_{CELL} OVDT" on page 42).

4.1.9.1 V_{CELL} OVDTU

Bits 0x11.3 OVDTU1 and 0x11.2 OVDTU0 are the unit selection bits for the V_{CELL}OVDT value. The following settings are available:

- 00 - µsec
- 01 - msec
- 10 - sec (default)
- 11 - min

4.1.9.2 V_{CELL} OVDT

The bits OVDT9 - OVDT0 set the 10-bit number of units value used to time an Overvoltage condition. The valid range is 0 - 1023.

The 12-bit Timer setting is split across two 8-bit registers at addresses:

- 0x10.[7:0]: Lower 8 bits - OVDT
- 0x11.[1:0]: Upper 2 bits - OVDT
- 0x11.[3:2]: 2 bit - OVDTU

The default Timer is 1s. Multiply the 10-bit number of units value by the unit value to calculate the delay time.

4.1.10 0x12-13 V_{CELL} UV Timer

The 12-bit V_{CELL} Undervoltage Delay Timer setting is shared between two registers. The upper 4 bits of the UVDT setting are stored in the lower 4 bits of 0x13 while the remaining 8 bits of UVDT are stored in 0x12 as shown in Table 12. The upper 4 bits of register 0x13 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 12. UVDT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	UVDT7	UVDT6	UVDT5	UVDT4	UVDT3	UVDT2	UVDT1	UVDT0	Value
0x12 Default	0	0	0	0	0	0	0	1	0x01
Bit Name	RSV	RSV	RSV	RSV	UVDTU1	UVDTU0	UVDT9	UVDT8	Value
0x13 Default	0	0	0	0	1	0	0	0	0x08

A V_{CELL}UV condition ("VCELL UV" on page 37) must be present for at least the time specified by this setting for the device to enter an Undervoltage condition. The UVDT 12-bit value is split into a 2-bit unit selection value ("V_{CELL} UVDTU" on page 42) and a 10-bit time value ("V_{CELL} UVDT" on page 42).

4.1.10.1 V_{CELL} UVDTU

Bits 0x13.3 UVDTU1 and 0x13.2 UVDTU0 are the unit selection bits of the UVDT value. The following settings are available:

- 00 - µsec
- 01 - msec
- 10 - sec (default)
- 11 - min

4.1.10.2 V_{CELL} UVDT

The bits UVDT9 - UVDT0 set the 10-bit number of units value used to time an Undervoltage condition. The valid range is 0 - 1023.

The 12-bit Timer setting is split across two 8-bit registers at addresses:

- 0x12.[7:0]: Lower 8 bits - UVDT
- 0x13.[1:0]: Upper 2 bits - UVDT
- 0x13.[3:2]: 2-bit - UVDTU

The default Timer is 1s. Multiply the 10-bit number of units value by the unit value to calculate the delay time.

4.1.11 0x14-15 OWT

The 10-bit Open-Wire Timing value sets the on-time of the open-wire test pulse and is shared between two registers. The 1-bit unit selector of the OWT setting (OWTU0) is stored in 0x15.[1]. The upper 1 bit of the OWT value is stored in 0x15.[0] and the remaining 8 bits of OWT value are stored in 0x14.[7:0] as shown in Table 13. The upper 6 bits of register 0x15 are reserved and should be ignored on read-back and set to 00 0000 when writing to the register.

Table 13. OWT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	OWT7	OWT6	OWT5	OWT4	OWT3	OWT2	OWT1	OWT0	Value
0x14 Default	0	0	0	1	0	1	0	0	0x14
Bit Name	RSV	RSV	RSV	RSV	RSV	RSV	OWTU	OWT8	Value
0x15 Default	0	0	0	0	0	0	1	0	0x02

4.1.11.1 OWTU

Bit 0x15.1 OWTU is the unit selection bit of the OWT value. The following settings are available:

- 0 - µsec
- 1 - msec (default)

4.1.11.2 OWT

The bits OWT8 - OWT0 set the 9-bit number of units value used to set the width of the open-wire pulse (see "Open Wire" on page 126). The valid range is 0 - 511.

The 10-bit Timer setting is split across two 8-bit registers at addresses:

- 0x14.[7:0]: Lower 8 bits - OWT
- 0x15.[0]: Upper 1 bit - OWT
- 0x15.[1]: 1-bit - OWTU

The default Timer is 20ms. Multiply the 9-bit number of units value by the unit value to calculate the pulse width.

4.1.12 0x16-17 DOC & DOCT

The Discharge Overcurrent threshold and its associated timer setting, Discharge Overcurrent Timing, are shared between two registers. These values set the requirements for the device to detect/indicate a Discharge Overcurrent condition. The 3-bit DOC threshold value is stored in 0x17.[6:4]. The 2-bit unit selector for the DOCT (DOCTU) is stored in 0x17.[3:2]. The upper 2-bits of the DOCT value is stored in the lower 2 bits of register 0x17 (0x17.[1:0]) and the lower 8-bits of the DOCT value is stored in register 0x16. This is shown in Table 14. The upper Most Significant Bit (MSB) of register 0x17 is reserved and should be ignored on read-back and set to 0 when writing to the register.

Timing regarding a Discharge overcurrent condition and recovery can be seen in Figure 35 on page 45 and is described in detail in "DOCR" on page 45.

Table 14. DOC

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	DOCT7	DOCT6	DOCT5	DOCT4	DOCT3	DOCT2	DOCT1	DOCT0	Value
0x16 Default	1	0	1	0	0	0	0	0	0xA0
Bit Name	RSV	DOC2	DOC1	DOC0	DOCTU1	DOCTU0	DOCT9	DOCT8	Value
0x17 Default	0	1	0	0	0	1	0	0	0x44

A Discharge Overcurrent condition exists if the voltage across the external sense resistor exceeds the limits set by the DOC threshold for the time specified by DOCT & DOCTU. In a Discharge Overcurrent condition the DOC fault bit “0x81.2 DOCF” on page 74 and the Load Present bit “0x82.0 LD_PRSNT” on page 77 are both set to 1.

If bit “0x87.6 µCFET” on page 82 is set to 0 (default), the Power FETs turn off automatically, otherwise the external MCU is responsible for turning off the Power FETs by clearing register bits “0x86.1 CFET” on page 81 and “0x86.0 DFET” on page 82.

4.1.12.1 0x17.[6:4] DOC

The Discharge Overcurrent bits (DOC2 - DOC0) are a 3-bit selector used to set the voltage required across the current sense resistor to trigger a Discharge Overcurrent condition. The possible settings and their corresponding voltages are listed in Table 15. The default DOC threshold is 32mV with a range of 4mV to 96mV.

Table 15. DOC Threshold Voltages

DOC Setting	Threshold (mV)	Equivalent Current (A)				
		0.3mΩ	0.5mΩ	1mΩ	2mΩ	5mΩ
000	4	13.3	8	4	2	0.8
001	8	26.6	16	8	4	1.6
010	16	53.3	32	16	8	3.2
011	24	80	48	24	12	4.8
100 (default)	32	106.7	64	32	16	6.4
101	48	(Note 9)	96	48	24	9.6
110	64	(Note 9)	(Note 9)	64	32	12.8
111	96	(Note 9)	(Note 9)	(Note 9)	48	19.2

Note:
9. These selections may not be reasonable due to sense resistor power dissipation.

4.1.12.2 0x17.[3:2] DOCTU

The Discharge Overcurrent Timing Unit selection bits 0x17.3 DOCTU1 and 0x17.2 DOCTU0 set the DOCT time unit value. The following settings are available:

- 00 - µsec
- 01 - msec (default)
- 10 - sec
- 11 - min

4.1.12.3 0x16-17 DOCT

The Discharge Overcurrent Timing bits DOCT9 - DOCT0 set the 10-bit number of units value used to define a Discharge Overcurrent condition. The valid range is 0 - 1023.

The 12-bit Timer setting is split across two 8-bit registers at addresses:

- 0x16.[7:0]: Lower 8 bits - DOCT
- 0x17.[1:0]: Upper 2 bits - DOCT

The default DOC Timer setting is 160ms. Multiply the 10-bit DOCT number of units value by the DOCTU unit value to calculate the delay time that must be exceeded to declare a Discharge Overcurrent condition. The timer selectable range is from 1µs to 1023 minutes.

4.1.12.4 DOCR

If the ISL94202 detects a DOC (or DSC) condition, the Discharge Overcurrent Recovery process begins. The load monitor circuit is enabled after ~3s and then the LDMON pin injects ~60µA ("ILDMON" on page 16) of current into the load for a duration of "0x05.7:4 LDPW" on page 37 every 256ms (see Figure 35). With a load present the LDMON pin voltage falls below threshold "V_{LDMON}" on page 16 and bit "0x82.0 LD_PRSNT" on page 77 is set to 1. After the load is removed or rises to a sufficiently high resistance, the LDMON pin voltage rises above the threshold, which results in the LD_PRSNT bit clearing to 0.

If the µCFET bit is set to 0 and the load monitor detects that the load has been removed (LD_PRSNT = 0), the power FETs are re-enabled (assuming no other faults) and the fault bit "0x81.2 DOCF" on page 74 is cleared.

If the µCFET bit is set to 1 and LD_PRSNT along with the DOC fault bit clear, the external MCU must re-enable the FETs using bits "0x86.1 CFET" on page 81 and "0x86.0 DFET" on page 82.

An external MCU can also override the load monitoring function by setting the bit "0x87.4 µCLMON" on page 83 to 1 and periodically pulsing the bit "0x86.6 LMON_EN" on page 80. When pulsing the LMON_EN bit, the MCU must also check the status of the LD_PRSNT bit. If the µCLMON bit is set to 1, the external MCU must set the bit "0x86.7 CLR_LERR" on page 80 to 1 to reset the DOC bit. When LD_PRSNT and DOC fault is cleared, the MCU can turn on the power FETs because the load has been removed.

For more information on the load monitoring circuit, see "LDMON Pin (38)" on page 104.

Example timing of a Discharge Overcurrent condition and Recovery is shown in Figure 35.

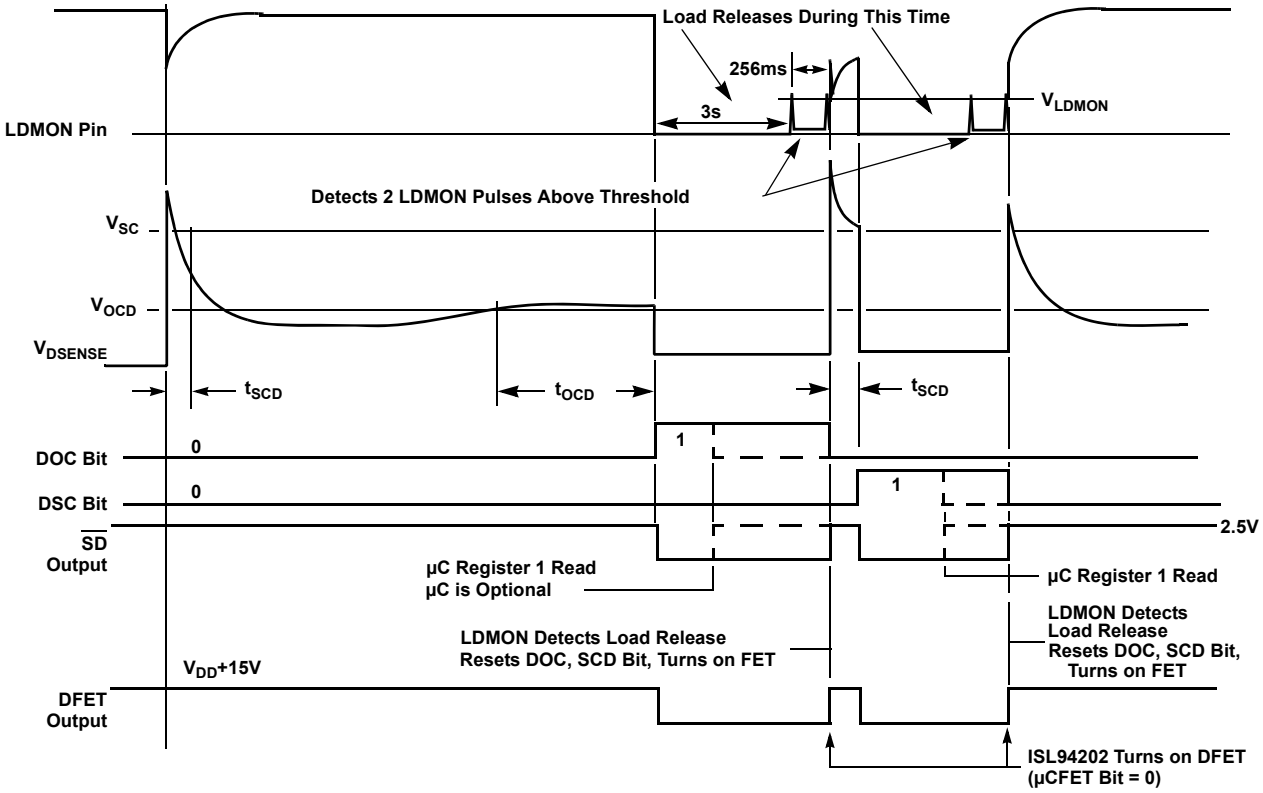


Figure 35. DOC and DSC Recovery

4.1.13 0x18-19 COC & COCT

The Charge Overcurrent threshold and its associated timer setting, Charge Overcurrent Timing, are shared between two registers. These values together set the requirements for the device to detect/indicate a Charge Overcurrent condition. The 3-bit COC threshold value is stored in 0x19.[6:4]. The 2-bit unit selector for the COCT (COCTU) is stored in 0x19.[3:2]. The upper 2 bits of the COCT value is stored in the lower 2 bits of register 0x19 (0x19.[1:0]) and the lower 8 bits of the COCT value is stored in register 0x18. This is shown in Table 16. The upper MSB of register 0x19 are reserved and should be ignored on read-back and set to 0 when writing to the register.

Timing regarding a Charge Overcurrent condition and recovery can be seen in Figure 35 on page 45 and is described in detail in "COCR" on page 47.

Table 16. COC

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	COCT7	COCT6	COCT5	COCT4	COCT3	COCT2	COCT1	COCT0	Value
0x18 Default	1	0	1	0	0	0	0	0	0xA0
Bit Name	RSV	COC2	COC1	COC0	COCTU1	COCTU0	COCT9	COCT8	Value
0x19 Default	0	1	0	0	0	1	0	0	0x44

A Charge Overcurrent condition exists if the voltage across the external current sense resistor exceeds the limits set by COC threshold for the time specified by COCT & COCTU. In a Charge Overcurrent condition the fault bit "0x81.1 COCF" on page 75 and the bit "0x82.1 CH_PRSNT" on page 77 are both set to 1.

If bit "0x87.6 µCFET" on page 82 is set to 0 (default), the Power FETs turn off automatically, otherwise the external MCU is responsible for turning off the Power FETs by clearing register bits 0x86.[1] for CFET and 0x86.[0] for DFET.

4.1.13.1 0x19.[6:4] COC

The Charge Overcurrent bits (COC2 - COC0) are a 3-bit selector used to set the voltage required across the current sense resistor to trigger a Charge Overcurrent condition. The possible settings and their corresponding voltages are listed in Table 17. The default COC threshold is 8mV, with a range from 1mV to 24mV.

Table 17. COC Threshold Voltages

COC Setting	Threshold (mV)	Equivalent Current (A)				
		0.3mΩ	0.5mΩ	1mΩ	2mΩ	5mΩ
000	1	3.33	2	1	0.5	0.2
001	2	6.67	4	2	1	0.4
010	4	13.33	8	4	2	0.8
011	6	20	12	6	3	1.2
100 (default)	8	26.67	16	8	4	1.6
101	12	40	24	12	6	2.4
110	16	53.33	32	16	8	3.2
111	24	80	48	24	12	4.8

4.1.13.2 0x19.[3:2] COCTU

The Charge Overcurrent Timing Unit selection bits 0x19.3 COCTU1 and 0x19.2 COCTU0 and set the COCT time unit value. The following settings are available:

- 00 - µsec
- 01 - msec (default)
- 10 - sec
- 11 - min

4.1.13.3 0x18-19 COCT

The Charge Overcurrent Timing bits COCT9 - COCT0 set the 10-bit number of units value used to define a Charge Overcurrent condition. The valid range is 0 - 1023.

The 12-bit Timer setting is split across two 8-bit registers at addresses:

- 0x18.[7:0]: Lower 8 bits - COCT
- 0x19.[1:0]: Upper 2 bits - COCT

The default COC Timer setting is 160ms. Multiply the 10-bit COCT number of units value by the COCTU unit value to calculate the delay time that must be exceeded to declare a Charge Overcurrent condition. The timer selectable range is from 1µs to 1023 minutes.

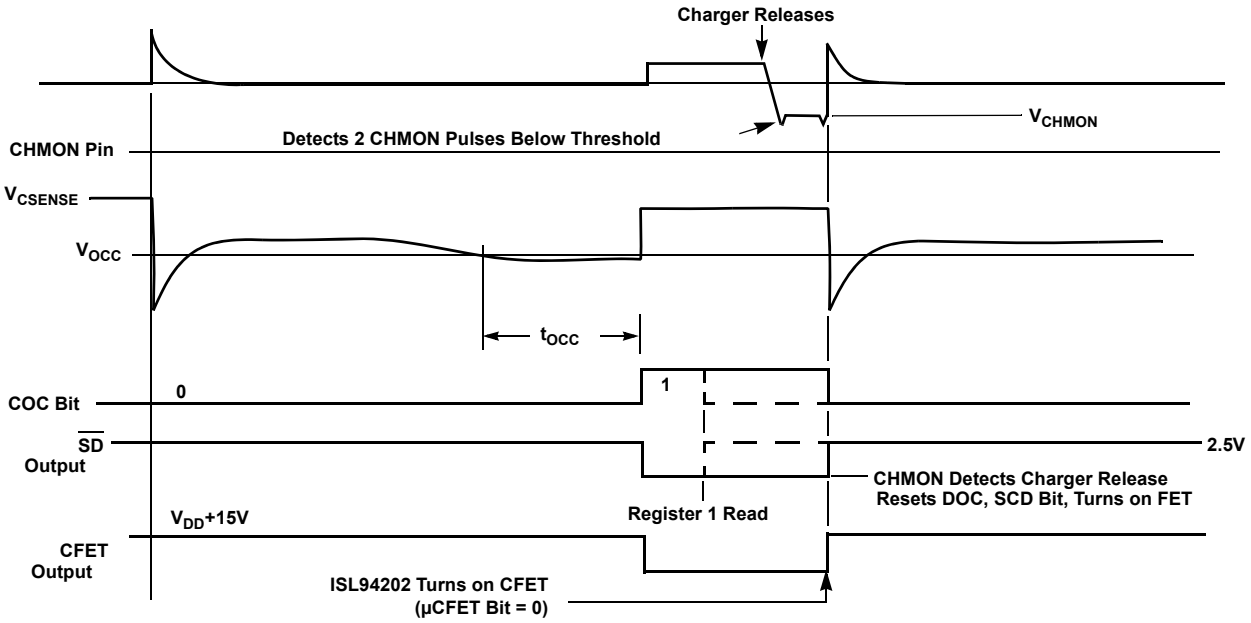


Figure 36. COC Recovery

4.1.13.4 COCR

If the ISL94202 detects a Charge Overcurrent (COC) condition, the Charge Overcurrent Recovery process begins. The charger monitor circuit is enabled after ~3s, then the CHMON pin pulls ~60µA (“ILDMON” on page 16) of current from the charger node for a duration of “0x01.7:4 CDPW” on page 36 every 256ms (see Figure 36). With a charger present the CHMON pin voltage is above threshold “V_{CHMON}” on page 16 and bit “0x82.1 CH_PRSNT” on page 77 is set to 1. After the charger is removed, the CHMON pin voltage drops below the threshold, resulting in the CH_PRSNT bit clearing to 0.

If the µCFET bit is set to 0 and the charger monitor detects the charger has been removed for 2 consecutive sample periods (CH_PRSNT = 0), the power FETs are re-enabled (assuming no other faults) and the fault bit “0x81.1 COCF” on page 75 is cleared. If the µCFET bit is set to 1, the external MCU must re-enable the FETs using bits “0x86.1 CFET” on page 81 and “0x86.0 DFET” on page 82.

An external MCU can override the charger monitoring function by setting the bit “0x87.3 µCCMON” on page 83 to 1 and periodically pulsing the bit “0x86.4 CMON_EN” on page 81. When pulsing the CMON_EN bit, the MCU must also check the status of the CH_PRSNT bit. If the µCCMON bit is set to 1, the external MCU must set the bit “0x86.5 CLR_CERR” on page 81 to 1 to reset the COC bit. When CH_PRSNT and COC fault is cleared, the MCU can turn on the power FETs because the charger has been removed.

For more information on the charger detection circuit, see section “CHMON Pin (37)” on page 99.

Example timing of a Charge Overcurrent condition and recovery is shown in Figure 36 on page 47.

4.1.14 0x1A-1B DSC & DSCT

The Discharge Short-Circuit threshold and its associated timer setting, Discharge Short-Circuit Timing, are shared between two registers. These values set the requirements for the device to detect/indicate a Discharge Short-Circuit condition. The 3-bit DSC threshold value is stored in 0x1B.[6:4]. The 2-bit unit selector for the DSCT (DSCTU) is stored in 0x1B.[3:2]. The upper 2 bits of the DSCT value is stored in the lower 2 bits of register 0x1B (0x1B.[1:0]) and the lower 8 bits of the DSCT value is stored in register 0x1A. This is shown in Table 18. The upper MSB of register 0x1B are reserved and should be ignored on read-back and set to 0 when writing to the register.

Timing regarding a Discharge overcurrent condition and recovery can be seen in Figure 35 on page 45 and is described in detail in "DSCR" on page 49.

Table 18. DSC

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	DSCT7	DSCT6	DSCT5	DSCT4	DSCT3	DSCT2	DSCT1	DSCT0	Value
0x1A Default	1	1	0	0	1	0	0	0	0xC8
Bit Name	RSV	DSC2	DSC1	DSC0	DSCTU1	DSCTU0	DSCT9	DSCT8	Value
0x1B Default	0	1	1	0	0	0	0	0	0x60

A Discharge Short-Circuit condition exists if the voltage across the external sense resistor exceeds the limits set by DSC threshold for the time specified by DSCT & DSCTU. In a Discharge Short-Circuit condition the DSC fault bit "0x81.3 DSCF" on page 74 and the LD_PRSNT bit "0x82.0 LD_PRSNT" on page 77 are both set to 1.

During a Discharge Short-Circuit Condition the power FETs turn off regardless of the condition of bit "0x87.6 µCFET" on page 82.

4.1.14.1 0x1B.[6:4] DSC

The Discharge Short-Circuit bits (DSC2 - DSC0) are a 3-bit selector used to set the voltage required across the current sense resistor to trigger a Discharge Short-Circuit condition. The possible settings and their corresponding voltages are listed in Table 19. The default DSC threshold is 128mV, with a range from 16mV to 256mV.

Table 19. DSC Threshold Voltages

DSC Setting	Threshold (mV)	Equivalent Current (A)				
		0.3mΩ	0.5mΩ	1mΩ	2mΩ	5mΩ
000	16	53.3	32	16	8	3.2
001	24	80	48	24	12	4.8
010	32	106.67	64	32	16	6.4
011	48	160	96	48	24	9.6
100	64	213.33	128	64	32	12.8
101	96	(Note 10)	192	96	48	19.2
110 (default)	128	(Note 10)	(Note 10)	128	64	25.6
111	256	(Note 10)	(Note 10)	(Note 10)	128	51.2

Note:
10. These selections may not be reasonable due to sense resistor power dissipation.

4.1.14.2 0x1B.[3:2] DSCTU

The Discharge Short-Circuit Timing Unit selection bits 0x1B.3 DSCTU1 and 0x1B.2 DSCTU0 set the DSCT time unit value. The following settings are available:

- 00 - µsec (default)
- 01 - msec
- 10 - sec
- 11 - min

4.1.14.3 0x1B.[1:0] - 0x1A.[7:0] DSCT

The Discharge Short-Circuit Timing bits DSCT9 - DSCT0 set the 10-bit number of units value used to define a Discharge Short-Circuit condition. The valid range is 0 - 1023.

The 12-bit Timer setting is split across two 8-bit registers at addresses:

- 0x1A.[7:0]: Lower 8 bits - DSCT
- 0x1B.[1:0]: Upper 2 bits - DSCT

The default DSC Timer setting 200µs. Multiply the 10-bit DSCT number of units value by the DSCTU unit value to calculate the delay time that must be exceeded to declare a Discharge Short-Current condition. The timer selectable range is from 1µs to 1023 minutes.

4.1.14.4 DSCR

If the ISL94202 detects a DSC (or DOC) condition the Discharge Overcurrent Recovery process begins. The load monitor circuit is enabled after ~3s and the LDMON pin injects ~60µA (“ILDMON” on page 16) of current into the load for a duration of “0x05.7:4 LDPW” on page 37 every 256ms (see Figure 35). With a load present the LDMON pin, voltage falls below threshold “V_{LDMON}” on page 16 and bit “0x82.0 LD_PRSNT” on page 77 is set to 1. After the load is removed or rises to a sufficiently high resistance, the LDMON pin voltage rises above the threshold, resulting in the LD_PRSNT bit clearing to 0.

If the µCFET bit is set to 0 and the load monitor detects the load has been removed (LD_PRSNT = 0), the power FETs are re-enabled (assuming no other faults) and the fault bit “0x81.3 DSCF” on page 74 is cleared.

If the µCFET bit is set to 1 and LD_PRSNT along with the DSC fault bit clear, the external MCU must re-enable the FETs using bits “0x86.1 CFET” on page 81 and “0x86.0 DFET” on page 82.

An external MCU can also override the load monitoring function by setting the bit “0x87.4 µCLMON” on page 83 to 1 and periodically pulsing the bit “0x86.6 LMON_EN” on page 80. When pulsing the LMON_EN bit, the MCU must also check the status of the LD_PRSNT bit. If the µCLMON bit is set to 1, the external MCU must set the bit “0x86.7 CLR_LERR” on page 80 to 1 to reset the DSC bit. When LD_PRSNT and DSC fault is cleared, the MCU can turn on the power FETs because the load has been removed.

For more information on the load monitoring circuit, see section “LDMON Pin (38)” on page 104.

Example timing of a Discharge Overcurrent condition and Recovery is shown in Figure 35 on page 45.

4.1.15 0x1C-1D CBMIN

The 12-bit Cell Balance Minimum voltage threshold setting is shared between two registers. The upper 4 bits of the CBMIN setting are stored in the lower 4 bits of 0x1D while the remaining 8 bits of CBMIN are stored in 0x1C as shown in Table 20. The upper 4 bits of register 0x1D are reserved, it should be ignored on read-back and set to 0000 when writing to the register.

Table 20. CBMIN

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBMIN7	CBMIN6	CBMIN5	CBMN4	CBMIN3	CBMIN2	CBMIN1	CBMIN0	Value
0x1C Default	0	1	0	1	0	1	0	1	0x55
Bit Name	RSV	RSV	RSV	RSV	CBMINB	CBMINA	CBMIN9	CBMIN8	Value
0x1D Default	0	0	0	0	1	0	1	0	0x0A

Cell Balancing is inhibited and the bit “0x83.3 CBUV” on page 78 is set to 1 if all cell voltages are below this threshold. This is a Cell Balance Undervoltage condition. At least one cell voltage must rise above the CBMIN threshold to recover from a Cell Balance Undervoltage condition and clear the CBUV bit.

The formula for converting from register digital value to voltage is:

$$CBMIN = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~3.1V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CBMIN \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

See “Cell Balancing” on page 122 for more information on cell balancing operation.

4.1.16 0x1E-1F CBMAX

The 12-bit Cell Balance Maximum voltage threshold setting is shared between two registers. The upper 4 bits of the CBMAX setting are stored in the lower 4 bits of 0x1F while the remaining 8 bits of CBMAX are stored in 0x1E as shown in Table 21. The upper 4 bits of register 0x1F are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 21. CBMAX

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBMAX7	CBMAX6	CBMAX5	CBMAX4	CBMAX3	CBMAX2	CBMAX1	CBMAX0	Value
0x1E Default	0	1	1	1	0	0	0	0	0x70
Bit Name	RSV	RSV	RSV	RSV	CBMAXB	CBMAXA	CBMAX9	CBMAX8	Value
0x1F Default	0	0	0	0	1	1	0	1	0x0D

Cell Balancing is inhibited and the bit “0x83.2 CBOV” on page 78 is set to 1 if all cell voltages are above this threshold. This is a Cell Balance Overvoltage condition. At least one cell voltage must drop below the CBMAX threshold to recover from a Cell Balance Overvoltage condition and clear the CBOV bit.

The formula for converting from register digital value to voltage is:

$$CBMAX = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~4.03V.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CBMAX \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

See “Cell Balancing” on page 122 for more information on cell balancing operation.

4.1.17 0x20-21 CBMINDV

The 12-bit Cell Balance Minimum Differential Voltage threshold setting is shared between two registers. The upper 4 bits of the CBMINDV setting are stored in the lower 4 bits of 0x21 while the remaining 8 bits of CBMINDV are stored in 0x20 as shown in Table 22 on page 51. The upper 4 bits of register 0x21 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 22. CBMINDV

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBMINDV7	CBMINDV6	CBMINDV5	CBMINDV4	CBMINDV3	CBMINDV2	CBMINDV1	CBMINDV0	Value
0x20 Default	0	0	0	1	0	0	0	0	0x10
Bit Name	RSV	RSV	RSV	RSV	CBMINDVB	CBMINDVA	CBMINDV9	CBMINDV8	Value
0x21 Default	0	0	0	0	0	0	0	0	0x00

If the difference between $CELL_N$ and the lowest voltage cell is less than this value, cell balancing for $CELL_N$ is disabled. Conversely, if the voltage difference between $CELL_N$ and the lowest voltage cell is between CBMINDV and "0x22-23 CBMAXDV" on page 51, cell balancing of $CELL_N$ is enabled.

Note: Cell balancing for $CELL_N$ is not enabled if its voltage is less than CBMIN or greater than CBMAX.

The formula for converting from register digital value to voltage is:

$$CBMINDV = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~18.75mV.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CBMINDV \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

Voltage measurement accuracy is specified to ±10mV at room temperature. Setting CBMINDV to less than 10mV can result in cell balance algorithm non-convergence and is not recommended. See "Cell Balancing" on page 122 for more information on cell balancing operation.

4.1.18 0x22-23 CBMAXDV

The 12-bit Cell Balance Maximum Differential Voltage threshold setting is shared between two registers. The upper 4 bits of the CBMAXDV setting are stored in the lower 4 bits of 0x23 while the remaining 8 bits of CBMAXDV are stored in 0x22 as shown in Table 23. The upper 4 bits of register 0x23 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 23. CBMAXDV

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBMAXDV7	CBMAXDV6	CBMAXDV5	CBMAXDV4	CBMAXDV3	CBMAXDV2	CBMAXDV1	CBMAXDV0	Value
0x22 Default	1	0	1	0	1	0	1	1	0xAB
Bit Name	RSV	RSV	RSV	RSV	CBMAXDVB	CBMAXDVA	CBMAXDV9	CBMAXDV8	Value
0x23 Default	0	0	0	0	0	0	0	1	0x01

If the difference between $CELL_N$ and the lowest voltage cell is larger than "0x20-21 CBMINDV" on page 50, and the voltage on $CELL_N$ is between CBMINDV and CBMAXDV, cell balancing of $CELL_N$ is enabled.

Note: Cell balancing for $CELL_N$ is not enabled if its voltage is less than CBMIN or greater than CBMAX.

Conversely, if the difference between $CELL_N$ and the lowest voltage cell is larger than CBMAXDV, cell balancing for $CELL_N$ is disabled and the fault bit "0x81.4 CELLF" on page 74 is set to 1. This is considered a serious fault leading to the pack being disabled. A CELLF condition triggers the ISL94202 to test for an "Open Wire" on page 126.

The formula for converting from register digital value to voltage is:

$$CBMAXDV = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of ~500mV.

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CBMAXDV \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

See "Cell Balancing" on page 122 for more information on cell balancing operation.

4.1.19 0x24-25 CBON Timer

The 12-bit Cell Balance On Time value is shared between two registers. The 2-bit unit selector for CBON (CBONU) is stored in 0x25.[3:2]. The upper 2 bits of the CBON value is stored in the lower 2 bits of register 0x25 and the lower 8 bits of the CBON value is stored in register 0x24. This is shown in Table 24. The upper 4 bits of register 0x25 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 24. CBON

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBON7	CBON6	CBON5	CBON4	CBON3	CBON2	CBON1	CBON0	Value
0x24 Default	0	0	0	0	0	0	1	0	0x02
Bit Name	RSV	RSV	RSV	RSV	CBONU1	CBONU0	CBON9	CBON8	Value
0x25 Default	0	0	0	0	1	0	0	0	0x08

This setting determines how long the cell balancing outputs are turned ON during a cell balancing cycle.

See "Cell Balancing" on page 122 for more information on cell balancing operation.

4.1.19.1 0x25.[3:2] CBONU

The Cell Balance On-Time Unit selection bits 0x25.3 CBONU1 and 0x25.2 CBONU0 set the CBON time unit value. The following settings are available:

- 00 - µsec
- 01 - msec
- 10 - sec (default)
- 11 - min

4.1.19.2 0x24-25 CBON

The Cell Balance On-Time bits CBON9 - CBON0 set the 10-bit number of units value used to define the Cell Balance On-Time. The valid range is 0 - 1023.

The 12-bit Timer setting is split across two 8-bit registers at addresses:

- 0x24.[7:0]: Lower 8 bits - CBON
- 0x25.[1:0]: Upper 2 bits - CBON

The default CBON period is 2s. Multiply the 10-bit CBON number of units value by the CBONU unit value to calculate the time the CB pins are enabled in each cycle of Cell Balancing.

4.1.20 0x26-27 CBOFF Timer

The 12-bit Cell Balance Off-Time value is shared between two registers. The 2-bit unit selector for CBOFF (CBOFFU) is stored in 0x27.[3:2]. The upper 2 bits of the CBOFF value is stored in the lower 2 bits of register 0x27 and the lower 8 bits of the CBOFF value is stored in register 0x26. This is shown in Table 25. The upper 4 bits of register 0x27 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 25. CBOFF

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBOFF7	CBOFF6	CBOFF5	CBOFF4	CBOFF3	CBOFF2	CBOFF1	CBOFF0	Value
0x26 Default	0	0	0	0	0	0	1	0	0x02
Bit Name	RSV	RSV	RSV	RSV	CBOFFU1	CBOFFU0	CBOFF9	CBOFF8	Value
0x27 Default	0	0	0	0	1	0	0	0	0x08

This setting determines how long the cell balancing outputs are turned OFF following a cell balancing cycle. The CBOFF setting should be long enough to allow the ISL94202 to complete at least two measurement scans after the CB FETs have been turned off and all CB induced transients have settled out. If CBOFF is too short, internal decisions on which cells to balance can be made during a CBON period (or during post CB transients). This can lead to poor results. CBOFF also allows time for the CB FETs to cool.

See “Cell Balancing” on page 122 for more information on cell balancing operation.

4.1.20.1 CBOFFU

The Cell Balance Off-Time Unit selection bits 0x27.3 CBOFFU1 and 0x27.2 CBOFFU0 set the CBOFF time unit value. The following settings are available:

- 00 - µsec
- 01 - msec
- 10 - sec (default)
- 11 - min

4.1.20.2 CBOFF

The Cell Balance Off-Time bits CBOFF9 - CBOFF0 set the 10-bit number of units value used to define the Cell Balance Off time. The valid range is 0 - 1023.

The 12-bit Timer setting is split across two 8-bit registers at addresses:

- 0x26.[7:0]: Lower 8 bits - CBOFF
- 0x27.[1:0]: Upper 2 bits - CBOFF

The default CBOFF period is 2s. Multiply the 10-bit CBOFF number of units value by the CBOFFU unit value to calculate the time the CB pins are disabled following each cycle of Cell Balancing

4.1.21 0x28-29 CBUT

The Cell Balance Under-Temperature threshold setting is shared between two registers. The upper 4 bits of the CBUT setting are stored in the lower 4 bits of 0x29 while the remaining 8 bits of CBUT are stored in 0x28 as shown in Table 26 on page 54. The upper 4 bits of register 0x29 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 26. CBUT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBUT7	CBUT6	CBUT5	CBUT4	CBUT3	CBUT2	CBUT1	CBUT0	Value
0x28 Default	1	1	1	1	0	0	1	0	0xF2
Bit Name	RSV	RSV	RSV	RSV	CBUTB	CBUTA	CBUT9	CBUT8	Value
0x29 Default	0	0	0	0	1	0	1	1	0x0B

The ISL94202 is designed for use with an NTC thermistor.

If the voltage measured at either of the “Thermistor Pins (20-22)” on page 96 is greater than the CBUT threshold, the fault bit “0x83.1 CBUTF” on page 78 is set to 1. Given an NTC thermistor, this means that when the measured temperature at either thermistor input is less than the value represented by this register a fault is declared.

Given a CBUT fault, if bit “0x87.5 µCCBAL” on page 83 is set to 0 (default), cell balancing is disabled, otherwise an external MCU is responsible for ceasing cell balancing (see “MCU CB” on page 126).

For recovery from this fault see “0x2A-2B CBUTR” on page 54. The CBUTR setting must be less than the CBUT value.

The formula for converting from register digital value to voltage is:

$$CBUT = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~1.344V (-10°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CBUT \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86. Also see “0x4A.4 TGAIN” on page 68. For more information on cell balancing operation see “Cell Balancing” on page 122.

4.1.22 0x2A-2B CBUTR

The Cell Balancing Under-Temperature Recovery threshold setting is shared between two registers. The upper 4 bits of the CBUTR setting are stored in the lower 4 bits of 0x2B while the remaining 8 bits of CBUTR are stored in 0x2A as shown in Table 27. The upper 4 bits of register 0x2B are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 27. CBUTR

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBUTR7	CBUTR6	CBUTR5	CBUTR4	CBUTR3	CBUTR2	CBUTR1	CBUTR0	Value
0x2A Default	1	0	0	1	0	0	1	1	0x93
Bit Name	RSV	RSV	RSV	RSV	CBUTRB	CBUTRA	CBUTR9	CBUTR8	Value
0x2B Default	0	0	0	0	1	0	1	0	0x0A

The ISL94202 is designed for use with an NTC thermistor. The CBUTR setting must be less than the CBUT value.

If the voltage measured at both of the “Thermistor Pins (20-22)” on page 96 is less than the CBUTR value, and the device previously detected a Cell Balance Under-Temperature condition (“0x28-29 CBUT” on page 53), the fault bit “0x83.1 CBUTF” on page 78 is cleared to 0. Given an NTC thermistor, this means that when the measured temperature at either thermistor input is greater than the value represented by this register the previously existing fault is cleared.

When the CBUT fault is cleared, if bit "0x87.5 µCCBAL" on page 83 is set to 0 (default), cell balancing is re-enabled (subject to meeting all other conditions of cell balancing). Otherwise an external MCU is responsible for restarting cell balancing (see "MCU CB" on page 126).

The formula for converting from register digital value to voltage is:

$$CBUTR = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~1.19V (+5°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CBUTR \times 4095}{1.8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86. Also see 0x4A.4 TGAIN. For more information on cell balancing operation see "Cell Balancing" on page 122.

4.1.23 0x2C-2D CBOT

The Cell Balancing Over-Temperature threshold setting is shared between two registers. The upper 4 bits of the CBOT setting are stored in the lower 4 bits of 0x2D while the remaining 8 bits of CBOT are stored in 0x2C as shown in Table 28. The upper 4 bits of register 0x2D are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 28. CBOT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBOT7	CBOT6	CBOT5	CBOT4	CBOT3	CBOT2	CBOT1	CBOT0	Value
0x2C Default	1	0	1	1	0	1	1	0	0xB6
Bit Name	RSV	RSV	RSV	RSV	CBOTB	CBOTA	CBOT9	CBOT8	Value
0x2D Default	0	0	0	0	0	1	0	0	0x04

The ISL94202 is designed for use with an NTC thermistor.

If the voltage measured at either of the "Thermistor Pins (20-22)" on page 96 is less than the CBOT threshold, the fault bit "0x83.0 CBOTF" on page 78 is set to 1. Given an NTC thermistor, this means that when the measured temperature at either thermistor input is greater than the value represented by this register a fault is declared.

Given a CBOT fault, if bit "0x87.5 µCCBAL" on page 83 is set to 0 (default), cell balancing is disabled, otherwise an external MCU is responsible for ceasing cell balancing (see "MCU CB" on page 126).

For recovery from this fault see "0x2E-2F CBOTR" on page 56. The CBOTR setting must be greater than the CBOT value.

The formula for converting from register digital value to voltage is:

$$CBOT = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~0.53V (+55°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CBOT \times 4095}{1.8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86. Also see "0x4A.4 TGAIN" on page 68. For more information on cell balancing operation see "Cell Balancing" on page 122.

4.1.24 0x2E-2F CBOTR

The Cell Balancing Over-Temperature Recovery threshold setting is shared between two registers. The upper 4 bits of the CBOTR setting are stored in the lower 4 bits of 0x2F while the remaining 8 bits of CBOTR are stored in 0x2E as shown in Table 29. The upper 4 bits of register 0x2F are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 29. CBOTR

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CBOTR7	CBOTR6	CBOTR5	CBOTR4	CBOTR3	CBOTR2	CBOTR1	CBOTR0	Value
0x2E Default	0	0	1	1	1	1	1	0	0x3E
Bit Name	RSV	RSV	RSV	RSV	CBOTRB	CBOTRA	CBOTR9	CBOTR8	Value
0x2F Default	0	0	0	0	0	1	0	1	0x05

The ISL94202 is designed for use with an NTC thermistor. The CBOTR setting must be greater than the CBOT value.

If the voltage measured at both “Thermistor Pins (20-22)” on page 96 is greater than the CBOTR value, and the device previously detected a Cell Balance Over-Temperature condition, the fault bit “0x83.0 CBOTF” on page 78 is cleared to 0. Given an NTC thermistor, this means that when the measured temperature at both thermistor inputs is less than the value represented by this register the previously existing fault is cleared.

When the CBOT fault is cleared, if bit “0x87.5 µCCBAL” on page 83 is set to 0 (default), cell balancing is re-enabled (subject to meeting all other conditions of cell balancing), otherwise an external MCU is responsible for restarting cell balancing (see “MCU CB” on page 126).

The formula for converting from register digital value to voltage is:

$$CBOTR = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~0.59V (+50°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CBOTR \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86. Also see “0x4A.4 TGAIN” on page 68. For more information on cell balancing operation see “Cell Balancing” on page 122.

4.1.25 0x30-31 COT

The Charge Over-Temperature threshold setting is shared between two registers. The upper 4 bits of the COT setting are stored in the lower 4 bits of 0x31 while the remaining 8 bits of COT are stored in 0x30 as shown in Table 30. The upper 4 bits of register 0x31 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 30. COT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	COT7	COT6	COT5	COT4	COT3	COT2	COT1	COT0	Value
0x30 Default	1	0	1	1	0	1	1	0	0xB6
Bit Name	RSV	RSV	RSV	RSV	COTB	COTA	COT9	COT8	Value
0x31 Default	0	0	0	0	0	1	0	0	0x04

The ISL94202 is designed for use with an NTC thermistor.

If the voltage measured at either of the "Thermistor Pins (20-22)" on page 96 is less than the COT threshold, the fault bit "0x80.6 COTF" on page 71 is set to 1. Given an NTC thermistor, this means that when the measured temperature at either thermistor input is greater than the value represented by this register a fault is declared.

Given a COT fault, if bit "0x87.5 µCCBAL" on page 83 is set to 0 (default) then CFET/PCFET and cell balancing is disabled automatically, otherwise an external MCU is responsible for shutting off the CFET ("0x86.1 CFET" on page 81) and ceasing cell balancing (see "MCU CB" on page 126).

For recovery from this fault see "0x32-33 COTR" on page 57. The COTR setting must be greater than the COT value.

The formula for converting from register digital value to voltage is:

$$COT = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~0.53V (+55°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{COT \times 4095}{1.8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86. Also see "0x4A.4 TGAIN" on page 68.

4.1.26 0x32-33 COTR

The Charge Over-Temperature Recovery threshold setting is shared between two registers. The upper 4 bits of the COTR setting are stored in the lower 4 bits of 0x33 while the remaining 8 bits of COTR are stored in 0x32 as shown in Table 31. The upper 4 bits of register 0x33 are reserved, it should be ignored on read-back and set to 0000 when writing to the register.

Table 31. COTR

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	COTR7	COTR6	COTR5	COTR4	COTR3	COTR2	COTR1	COTR0	Value
0x32 Default	0	0	1	1	1	1	1	0	0x3E
Bit Name	RSV	RSV	RSV	RSV	COTRB	COTRA	COTR9	COTR8	Value
0x33 Default	0	0	0	0	0	1	0	1	0x05

The ISL94202 is designed for use with an NTC thermistor. The COTR setting must be greater than the COT value.

If the voltage measured at both "Thermistor Pins (20-22)" on page 96 is greater than the COTR value, and the device previously detected a Charge Over-Temperature condition, the fault bit "0x80.6 COTF" on page 71 is cleared to 0. Given an NTC thermistor, this means that when the measured temperature at both thermistor inputs is less than the value represented by this register the previously existing fault is cleared.

When the COT fault is cleared, if bit "0x87.5 µCCBAL" on page 83 is set to 0 (default), CFET/PCFET and cell balancing are re-enabled (subject to meeting all other conditions), otherwise an external MCU is responsible for enabling CFET ("0x86.1 CFET" on page 81) and restarting cell balancing (see "MCU CB" on page 126).

The formula for converting from register digital value to voltage is:

$$COTR = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~0.59V (+50°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{COTR \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86. Also see “0x4A.4 TGAIN” on page 68.

4.1.27 0x34-35 CUT

The Charge Under-Temperature threshold setting is shared between two registers. The upper 4 bits of the CUT setting are stored in the lower 4 bits of 0x35 while the remaining 8 bits of CUT are stored in 0x34 as shown in Table 32. The upper 4 bits of register 0x35 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 32. CUT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CUT7	CUT6	CUT5	CUT4	CUT3	CUT2	CUT1	CUT0	Value
0x34 Default	1	1	1	1	0	0	1	0	0xF2
Bit Name	RSV	RSV	RSV	RSV	CUTB	CUTA	CUT9	CUT8	Value
0x35 Default	0	0	0	0	1	0	1	1	0x0B

The ISL94202 is designed for use with an NTC thermistor.

If the voltage measured at either of the “Thermistor Pins (20-22)” on page 96 is greater than the CUT threshold, the fault bit “0x80.7 CUTF” on page 71 is set to 1. Given an NTC thermistor, this means that when the measured temperature at either thermistor input is less than the value represented by this register a fault is declared.

Given a CUT fault, if bit “0x87.5 µCCBAL” on page 83 is set to 0 (default), CFET/PCFET is shut off and cell balancing is disabled automatically, otherwise an external MCU is responsible for shutting off the power FET (“0x86.1 CFET” on page 81) and ceasing cell balancing (see “MCU CB” on page 126).

For recovery from this fault see “0x36-37 CUTR” on page 58. The CUTR setting must be less than the CUT value.

The formula for converting from register digital value to voltage is:

$$CUT = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~1.344V (-10°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CUT \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86. Also see “0x4A.4 TGAIN” on page 68.

4.1.28 0x36-37 CUTR

The Charge Under-Temperature Recovery threshold setting is shared between two registers. The upper 4 bits of the CUTR setting are stored in the lower 4 bits of 0x37 while the remaining 8 bits of CUTR are stored in 0x36 as shown in Table 33 on page 59. The upper 4 bits of register 0x37 are reserved, it should be ignored on read-back and set to 0000 when writing to the register.

Table 33. CUTR

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CUTR7	CUTR6	CUTR5	CUTR4	CUTR3	CUTR2	CUTR1	CUTR0	Value
0x36 Default	1	0	0	1	0	0	1	1	0x93
Bit Name	RSV	RSV	RSV	RSV	CUTRB	CUTRA	CUTR9	CUTR8	Value
0x37 Default	0	0	0	0	1	0	1	0	0x0A

The ISL94202 is designed for use with an NTC thermistor. The CUTR setting must be less than the CUT value.

If the voltage measured at both of the "Thermistor Pins (20-22)" on page 96 is less than the CUTR value, and the device previously detected a Cell Under-Temperature condition ("0x34-35 CUT" on page 58), the fault bit "0x80.7 CUTF" on page 71 is cleared to 0. Given an NTC thermistor, this means that when the measured temperature at both thermistor inputs is greater than the value represented by this register the previously existing fault is cleared.

When a CUT fault is cleared, if bit "0x87.5 µCCBAL" on page 83 is set to 0 (default), CFET/PCFET and cell balancing are re-enabled (subject to meeting all other conditions), otherwise an external MCU is responsible for enabling CFET ("0x86.1 CFET" on page 81) and restarting cell balancing (see "MCU CB" on page 126).

The formula for converting from register digital value to voltage is:

$$CUTR = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~1.19V (+5°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{CUTR \times 4095}{1.8}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86. Also see "0x4A.4 TGAIN" on page 68.

4.1.29 0x38-39 DOT

The Discharge Over-Temperature threshold Setting is shared between two registers. The upper 4 bits of the DOT setting are stored in the lower 4 bits of 0x39 while the remaining 8 bits of DOT are stored in 0x38 as shown in Table 34. The upper 4 bits of register 0x39 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 34. DOT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	DOT7	DOT6	DOT5	DOT4	DOT3	DOT2	DOT1	DOT0	Value
0x38 Default	1	0	1	1	0	1	1	0	0xB6
Bit Name	RSV	RSV	RSV	RSV	DOTB	DOTA	DOT9	DOT8	Value
0x39 Default	0	0	0	0	0	1	0	0	0x04

The ISL94202 is designed for use with an NTC thermistor.

If the voltage measured at either of the "Thermistor Pins (20-22)" on page 96 is less than the DOT threshold, the fault bit "0x80.4 DOTF" on page 72 is set to 1. Given an NTC thermistor, this means that when the measured temperature at either thermistor input is greater than the value represented by this register a fault is declared.

Given a DOT fault, if bit "0x87.5 µCCBAL" on page 83 is set to 0 (default), DFET and cell balancing are disabled automatically, otherwise an external MCU is responsible for shutting off DFET ("0x86.0 DFET" on page 82) and ceasing cell balancing (see "MCU CB" on page 126).

For recovery from this fault see “0x3A-3B DOTR” on page 60. The DOTR setting must be greater than the DOT value.

The formula for converting from register digital value to voltage is:

$$DOT = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~0.53V (+55°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{DOT \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86. Also see “0x4A.4 TGAIN” on page 68.

4.1.30 0x3A-3B DOTR

The Discharge Over-Temperature Recovery threshold setting is shared between two registers. The upper 4 bits of the DOTR setting are stored in the lower 4 bits of 0x3B while the remaining 8 bits of DOTR are stored in 0x3A as shown in Table 35. The upper 4 bits of register 0x3B are reserved, it should be ignored on read-back and set to 0000 when writing to the register.

Table 35. DOTR

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	DOTR7	DOTR6	DOTR5	DOTR4	DOTR3	DOTR2	DOTR1	DOTR0	Value
0x3A Default	0	0	1	1	1	1	1	0	0x3E
Bit Name	RSV	RSV	RSV	RSV	DOTRB	DOTRA	DOTR9	DOTR8	Value
0x3B Default	0	0	0	0	0	1	0	1	0x05

The ISL94202 is designed for use with an NTC thermistor. The DOTR setting must be greater than the DOT value.

If the voltage measured at both “Thermistor Pins (20-22)” on page 96 is greater than the DOTR value, and the device previously detected a Discharge Over-Temperature condition, the fault bit “0x80.4 DOTF” on page 72 is cleared to 0. Given an NTC thermistor, this means that when the measured temperature at both thermistor inputs is less than the value represented by this register, the previously existing fault is cleared.

When the DOT fault is cleared, if bit “0x87.5 µCCBAL” on page 83 is set to 0 (default), DFET and cell balancing are re-enabled (subject to meeting all other conditions), otherwise an external MCU is responsible for enabling DFET (“0x86.0 DFET” on page 82) and restarting cell balancing (see “MCU CB” on page 126).

The formula for converting from register digital value to voltage is:

$$DOTR = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~0.59V (+50°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{DOTR \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86. Also see “0x4A.4 TGAIN” on page 68.

4.1.31 0x3C-3D DUT

The Discharge Under-Temperature threshold setting is shared between two registers. The upper 4 bits of the DUT setting are stored in the lower 4 bits of 0x3D while the remaining 8 bits of DUT are stored in 0x3C as shown in Table 36. The upper 4 bits of register 0x3D are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 36. DUT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	DUT7	DUT6	DUT5	DUT4	DUT3	DUT2	DUT1	DUT0	Value
0x3C Default	1	1	1	1	0	0	1	0	0xF2
Bit Name	RSV	RSV	RSV	RSV	DUTB	DUTA	DUT9	DUT8	Value
0x3D Default	0	0	0	0	1	0	1	1	0x0B

The ISL94202 is designed for use with an NTC thermistor.

If the voltage measured at either of the “Thermistor Pins (20-22)” on page 96 is greater than the DUT threshold, the fault bit “0x80.5 DUTF” on page 72 is set to 1. Given an NTC thermistor, this means that when the measured temperature at either thermistor input is less than the value represented by this register a fault is declared.

When a DUT fault is cleared, if bit “0x87.5 µCCBAL” on page 83 is set to 0 (default), DFET is shut off and cell balancing is disabled automatically, otherwise an external MCU is responsible for shutting off the power FET (“0x86.0 DFET” on page 82) and ceasing cell balancing (see “MCU CB” on page 126).

For recovery from this fault see “0x3E-3F DUTR” on page 61. The DUTR setting must be less than the DUT value.

The formula for converting from register digital value to voltage is:

$$DUT = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~1.344V (-10°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{DUT \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86. Also see “0x4A.4 TGAIN” on page 68.

4.1.32 0x3E-3F DUTR

The Discharge Under-Temperature Recovery threshold setting is shared between two registers. The upper 4 bits of the DUTR setting are stored in the lower 4 bits of 0x3F while the remaining 8 bits of DUTR are stored in 0x3E as shown in Table 37 on page 62. The upper 4 bits of register 0x3F are reserved, it should be ignored on read-back and set to 0000 when writing to the register.

Table 37. DUTR

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	DUTR7	DUTR6	DUTR5	DUTR4	DUTR3	DUTR2	DUTR1	DUTR0	Value
0x3E Default	1	0	0	1	0	0	1	1	0x93
Bit Name	RSV	RSV	RSV	RSV	DUTRB	DUTRA	DUTR9	DUTR8	Value
0x3F Default	0	0	0	0	1	0	1	0	0x0A

The ISL94202 is designed for use with an NTC thermistor. The DUTR setting must be less than the DUT value.

If the voltage measured at both of the “Thermistor Pins (20-22)” on page 96 is less than the DUTR value, and the device previously detected a Discharge Under-Temperature condition (“0x3C-3D DUT” on page 61), the fault bit “0x80.5 DUTF” on page 72 is cleared to 0. Given an NTC thermistor, this means that when the measured temperature at both thermistor inputs is greater than the value represented by this register the previously existing fault is cleared.

Given a DUT fault, if bit “0x87.5 µCCBAL” on page 83 is set to 0 (default), DFET and cell balancing are re-enabled (subject to meeting all other conditions of cell balancing), otherwise an external MCU is responsible for enabling DFET (“0x86.0 DFET” on page 82) and restarting cell balancing. (see “MCU CB” on page 126)

The formula for converting from register digital value to voltage is:

$$DUTR = \frac{REGval \times 1.8}{4095}$$

The default results in a threshold setting of ~1.19V (+5°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{DUTR \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

4.1.33 0x40-41 IOT

The Internal Over-Temperature threshold Setting is shared between two registers. The upper 4 bits of the IOT setting are stored in the lower 4 bits of 0x41 while the remaining 8 bits of IOT are stored in 0x40 as shown in Table 38. The upper 4 bits of register 0x41 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 38. IOT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	IOT7	IOT6	IOT5	IOT4	IOT3	IOT2	IOT1	IOT0	Value
0x40 Default	0	1	1	0	0	1	0	0	0x64
Bit Name	RSV	RSV	RSV	RSV	IOTB	IOTA	IOT9	IOT8	Value
0x41 Default	0	0	0	0	0	1	1	0	0x06

If the voltage measured by the internal temperature senor is less than IOT threshold then the fault bit “0x81.0 IOTF” on page 75 is set to 1. When the temperature measured by the internal temperature senor is higher than the value represented by this register a fault is declared.

Given an IOT fault, if bit “0x87.5 µCCBAL” on page 83 is set to 0 (default) then all power FETS are shut off and cell balancing is disabled automatically, otherwise an external MCU is responsible for shutting off the power FETs

(“0x86.1 CFET” on page 81, “0x86.0 DFET” on page 82) and ceasing cell balancing (see “MCU CB” on page 126).

For recovery from this fault see“0x42-43 IOTR” on page 63. The IOTR setting must be less than the IOT value.

The formula for converting from register digital value to voltage (V) is:

$$IOT = \frac{REGval \times 1.8}{4095}$$

The formula for converting from voltage (V) to temperature (C) is:

$$ICTemp = \frac{IOT \times 1000}{1.8527} - 273.15$$

The default results in a threshold setting of ~0.719V (+115°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{IOT \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86. Also see “0x4A.4 TGAIN” on page 68.

4.1.34 0x42-43 IOTR

The Internal Over-Temperature Recovery threshold setting is shared between two registers. The upper 4 bits of the IOTR setting are stored in the lower 4 bits of 0x43 while the remaining 8 bits of IOTR are stored in 0x42 as shown in Table 39. The upper 4 bits of register 0x43 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 39. IOTR

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	IOTR7	IOTR6	IOTR5	IOTR4	IOTR3	IOTR2	IOTR1	IOTR0	Value
0x42 Default	0	0	0	1	0	0	0	0	0x10
Bit Name	RSV	RSV	RSV	RSV	IOTRB	IOTRA	IOTR9	IOTR8	Value
0x43 Default	0	0	0	0	0	1	1	0	0x06

The IOTR setting must be less than the IOT value.

If the internal temperature sensor voltage is less than the value in this register, the fault bit “0x81.0 IOTF” on page 75 is cleared to 0. When the measured temperature is less than the value represented by this register, the previously detected fault is cleared.

When a IOT fault is cleared, if bit “0x87.5 µCCBAL” on page 83 is set to 0 (default), both the Discharge & Charge Power FETs and cell balancing are re-enabled (subject to meeting all other conditions), otherwise an external MCU is responsible for enabling the FETs (“0x86.0 DFET” on page 82, “0x86.1 CFET” on page 81) and restarting cell balancing (see “MCU CB” on page 126).

The formula for converting from register digital value to voltage (V) is:

$$IOTR = \frac{REGval \times 1.8}{4095}$$

The formula for converting from voltage (V) to temperature (C) is:

$$ICTemp = \frac{IOTR \times 1000}{1.8527} - 273.15$$

The default results in a threshold setting of ~0.682V (+95°C; T_{GAIN} = 0, GAIN = 2, per Figure 39 on page 96).

To set the register decimal value to a desired threshold voltage use:

$$REGval = \frac{IOTR \times 4095}{1.8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86. Also see “0x4A.4 TGAIN” on page 68.

4.1.35 0x44-45 SLV

The Sleep Level Voltage threshold setting is shared between two registers. The upper 4 bits of the SLV setting are stored in the lower 4 bits of 0x45 while the remaining 8 bits of SLV are stored in 0x44 as shown in Table 40. The upper 4 bits of register 0x45 are reserved and should be ignored on read-back and set to 0000 when writing to the register.

Table 40. SLV

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	SLV7	SLV6	SLV5	SLV4	SLV3	SLV2	SLV1	SLV0	Value
0x44 Default	1	0	1	0	1	0	1	0	0xAA
Bit Name	RSV	RSV	RSV	RSV	SLVB	SLVA	SLV9	SLV8	Value
0x45 Default	0	0	0	0	0	1	1	0	0x06

If the voltage across any cell is below the SLV threshold for the time specified by “0x46-47 WDT & SLT” on page 64, the bit “0x83.6 IN_SLEEP” on page 78 is set to 1 and the device enters SLEEP Mode.

The formula for converting from register digital value to voltage is:

$$SLV = \frac{REGval \times 1.8 \times 8}{4095 \times 3}$$

The default results in a threshold setting of 2.0V.

To set the register decimal value to a desired threshold voltage use:

$$REGVal = \frac{SLV \times 3 \times 4095}{1.8 \times 8}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

4.1.36 0x46-47 WDT & SLT

The Watchdog Timer and Sleep Delay Timer values are shared between two registers. The WDT value is stored in 0x47.[7:3]. The upper 1-bit of the SLT value is stored in the lower 1 bit of the register (0x47.0) and the lower 8 bits of the SLT value is stored in register 0x46. The 2-bit unit selection for the SLT (SLTU) is stored in 0x47.[2:1]. This is shown in Table 41.

Table 41. WDT & SLT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	SLT7	SLT6	SLT5	SLT4	SLT3	SLT2	SLT1	SLT0	Value
0x46 Default	0	0	0	0	1	1	1	1	0x0F
Bit Name	WDT4	WDT3	WDT2	WDT1	WDT0	SLTU1	SLTU0	SLT8	Value
0x47 Default	1	1	1	1	1	1	0	0	0xFC

4.1.36.1 0x47.[7:3] WDT

The Watchdog Timer prevents an external MCU from initiating an action that it cannot undo through the I^2C port, which can result in poor or unexpected operation of the pack. The watchdog timer is normally inactive when the device is operating stand-alone.

When the pack is expected to have an MCU along with the ISL94202, the watchdog timer setting controls the maximum allowable time between communications from the external MCU to ISL94202 if any µC override bit has been set to 1.

The WDT is activated by setting any µC override bits:

- “0x87.6 µCFET” on page 82
- “0x87.5 µCCBAL” on page 83
- “0x87.4 µCLMON” on page 83
- “0x87.3 µCCMON” on page 83
- “0x87.2 µCSCAN” on page 84

If the watchdog timer is allowed to expire, the ISL94202 resets the serial interface, and pulses the $\overline{INT}$ output (“INT Pin (31)” on page 97) for 1µs at 1Hz to alert the MCU. If the $\overline{INT}$ is unsuccessful in restarting the communication interface, the part operates normally, except the power FETs and cell balance FETs are forced off on the next I^2C transaction. The ISL94202 remains in this condition until I^2C communications resume.

When I^2C communication resumes, the µCSCAN, µCCMON, µCLMON, µCFET, and EEEN bits are automatically reset (cleared) but the µCCBAL bit remains set if previously set. The power FETs and cell balance FETs turn on, if conditions allow.

Automatic system scans resume on the next I^2C communication.

To calculate the setting of the timer multiply the value of register bits 0x47.[7:3] by 1s. The default WDT value is 31s.

4.1.36.2 0x47.[2:1] SLTU

The Sleep Level Timer Unit selection bits 0x47.2 SLTU1 and 0x47.1 SLTU0 set the 2-bit SLT time unit value. The following settings are available:

- 00 - µsec
- 01 - msec
- 10 - sec (default)
- 11 - min

4.1.36.3 0x47.[0] - 0x46.[7:0] SLT

The Sleep Level Timer bits SLT8 - SLT0 set the 9-bit number of units value used to define a Sleep Voltage condition. The valid range is 0 - 511.

The 9-bit SLT setting is split across two 8-bit registers at addresses:

- 0x47.[0]: Upper 1 bit - SLT
- 0x46.[7:0]: lower 8 bits - SLT

The default Sleep Level Timer setting is 1s. Multiply the 9-bit SLT number of units value by the SLTU unit value to calculate the length of time a cell voltage must remain below the threshold “0x44-45 SLV” on page 64 before the device transitions to “SLEEP Mode” on page 121.

4.1.37 0x48 Mode Timers

The Mode Timer settings are stored at address 0x49. These settings govern the time between Mode transitions if no current flow is detected (see “0x82.2 CHING” on page 77 and “0x82.3 DCHING” on page 76). This register is split into two 4-bit values. The upper 4 bits (0x49.[7:4]) are the SLEEP Mode timer setting. The lower 4 bits (0x49.[3:0]) are the IDLE and DOZE Mode timer setting. This is shown in Table 42.

Table 42. MOD

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	MOD7	MOD6	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0	Value
0x48 Default	1	1	1	1	1	1	1	1	0xFF

One of these two timer settings must be non-zero, setting both to 0 is not supported. If both IDLE/DOZE and SLEEP timers are set to 0, the device immediately goes to sleep if there is no current flow detected. To recover from this condition, apply current to the device or hold the LDMON pin low (or CHMON pin high) and write non-zero values to the registers.

4.1.37.1 0x48.[3:0] IDLE/DOZE Timer

This setting controls how long the ISL94202 remains in NORMAL (or IDLE) Mode without detecting a “0x82.2 CHING” on page 77 or “0x82.3 DCHING” on page 76 condition before transitioning to IDLE (or DOZE) Mode. If a CHING or DCHING detection occurs, the device immediately transitions back to NORMAL Mode and the timer is reset to 0. Setting the IDLE/DOZE timer to 0 immediately forces the device into the IDLE (or DOZE) Mode when there is no current flow detected.

The timer is inactive if the bit “0x87.2 µCSCAN” on page 84 is set to 1, because the MCU is in charge of device operation.

The range of the IDLE and DOZE Mode timer is 0 - 15 minutes set with each LSB being 1 minute increments. The default time is 15 Minutes.

- 0x49.[3:0] - 1111 (default)

See “System Modes” on page 119 for more information on system Modes.

4.1.37.2 0x48.[7:4] SLEEP Timer

The SLEEP Timer setting controls how long the ISL94202 remains in DOZE Mode without detecting a “0x82.2 CHING” on page 77 or “0x82.3 DCHING” on page 76 condition before transitioning to SLEEP Mode. If a CHING or DCHING detection occurs, the device immediately transitions back to NORMAL Mode and the timer is reset to 0. Setting the SLEEP Timer to 0 immediately forces the device into SLEEP Mode if there is no current flow detected while in DOZE Mode. The device appears to have skipped directly from IDLE to SLEEP Mode to the observer.

The timer is inactive if the bit “0x87.2 µCSCAN” on page 84 is set to 1, because the MCU is in charge of device operation.

The range of the SLEEP Mode timer is 0 - 240 Minutes with each LSB being a 16 minute increment. The default setting is 240 minutes. If the SLEEP timer is set to 0s, the device transitions directly from IDLE to SLEEP Mode (if conditions for SLEEP are met) or NORMAL Mode (if SLEEP conditions are not met) completely bypassing DOZE Mode.

- 0x49.[7:4] - 1111 (default).

See “System Modes” on page 119 for more information on system Modes.

4.1.38 0x49 Cell Select

The Cell Select register as shown in Table 43 contains the cell configuration setting the device uses to determine where cells are present. Cells must be selected for measurement results to be compared to the various thresholds as appropriate. If a cell is present, the bit must be set to 1. This setting also determines which cell connections to test for “Open Wire” on page 126 and cell balancing determination.

Table 43. CELL

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Bit Name	CELL8	CELL7	CELL6	CELL5	CELL4	CELL3	CELL2	CELL1	Value
0x49 Default	1	0	0	0	0	0	1	1	0x83

ONLY the following combinations are supported:

- 1000 0011 - 3 Cells connected (default)
- 1100 0011 - 4 Cells connected
- 1100 0111 - 5 Cells connected
- 1110 0111 - 6 Cells connected
- 1110 1111 - 7 Cells connected
- 1111 1111 - 8 Cells connected

These values are mapped according to the external cell connections of VCn and CBn (“VCn Pins” on page 94 & “CBn Pins” on page 94 respectively) where bit CELLn corresponds to whether or not VCn/CBn is connected to a cell. See “Reduced Cell Count” on page 150 for configuring the VCn/CBn pins in applications with 3 - 8 cells.

4.1.39 0x4A Setup 0

Setup 0 is the first of two registers containing single bit settings that enable/disable specific operations or controls. RSV bits must be written as 0 and ignored on read back.

Table 44. Setup 0

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Byte
Name	CELLF PSD	RSV	XT2M	TGAIN	RSV (0)	PCFETE	DOWD	OWPSD	Value
0x4A Default	0	0	0	0	0	0	0	0	0x00

4.1.39.1 0x4A.7 CELLF PSD

The Cell Fail Pack Shutdown bit enables or disables the PSD pin function of the ISL94202 upon detecting a CELLF condition and setting flag “0x81.4 CELLF” on page 74.

Set this bit to 0 (default) to disable the CELLF connection to the PSD output pin.

Set this bit to 1 to activate the PSD output pin when a CELLF condition occurs.

See “0x22-23 CBMAXDV” on page 51, “0x81.4 CELLF” on page 74, and “PSD Pin (32)” on page 98 for more information.

4.1.39.2 0x4A.5 XT2M

The second External Temperature Monitor bit determines the function of the second thermistor input pin. This input can monitor either a second pack thermistor or a power FET temperature thermistor.

Set this bit to 0 (default) if the xT2 pin connects to a thermistor that monitors cell temperature, for normal operation.

Set this bit to 1 if the xT2 pin connects to a thermistor that monitors FET temperature. This setting blocks shut off of the cell balance outputs if the xT2 temperature exceeds cell balance temperature limits.

See “0x28-29 CBUT” on page 53, “0x2C-2D CBOT” on page 55, and “Thermistor Pins (20-22)” on page 96 for more information.

4.1.39.3 0x4A.4 TGAIN

The Temperature Gain bit controls the gain of the temperature measurement circuitry for input pins xT1 and xT2 and internal temperature monitoring.

Setting this bit to 0 (default) sets the gain of IOT, xT1, and xT2 voltage measurement to 2. **Note:** This is the preferred and strongly recommended choice as the device calibrations and specifications are tied to this setting. The temperature response is more linear and covers a wider temperature range before nearing the limits of the ADC reading.

Setting this bit to 1 sets the gain of IOT, xT1, and xT2 voltage measurement 1. This setting is not recommended for monitoring external thermistors or device internal temperature (IOT).

See “Thermistor Pins (20-22)” on page 96 and “0x40-41 IOT” on page 62 for more information.

4.1.39.4 0x4A.2 PCFETE

The Pre-Charge FET Enable bit controls whether or not the pre-charge FET is used when a cell has fallen below the LVCH threshold.

Set this bit to 0 (default) if the pre-charge FET is not used.

Set this bit to 1 to direct the ISL94202 to enable the pre-charge FET instead of the charge FET when any of the cell voltages are below the threshold “0x0E-0F V_{CELL} LVCL” on page 40.

See “Power FET Pins (42, 44, 45)” on page 107 and “PCFET Pin (44)” on page 108 for more information.

4.1.39.5 0x4A.1 DOWD

The Disable Open Wire Detection bit controls whether or not an open-wire detection is enabled and executed following detection of a “0x81.4 CELLF” on page 74 condition.

Set this bit to 0 (default) to enable an open-wire detection scan following a CELLF detection.

Set this bit to 1 to prevent and open-wire detection scan following a CELLF detection.

See “0x22-23 CBMAXDV” on page 51 and “Open Wire” on page 126 for more information.

4.1.39.6 0x4A.0 OWPSD

The Open Wire Pack Shutdown bit controls whether or not the PSD pin is asserted following an open-wire detection.

Set this bit to 0 (default) to prevent the ISL94202 from asserting the PSD pin following an open-wire detection.

Set this bit to 1 to force the ISL94202 to assert the PSD pin following an open-wire detection.

See “PSD Pin (32)” on page 98 and Open Wire for more information.

4.1.40 0x4B Setup 1

Setup 1 is the second of two registers containing single bit settings that enable/disable specific operations or controls. RSV bits must be written as 0 and ignored on read back.

Table 45. Setup 1

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	[0]	Byte
Name	CBDD	CBDC	DFODUV	CFODOV	UVLOPD	RSV	RSV	CB_EOC	Value
0x4B Default	0	1	0	0	0	0	0	0	0x40

4.1.40.1 0x4B.7 CBDD

The Cell Balance During Discharge bit controls whether or not cell balancing is performed during discharge. Status bit "0x82.3 DCHING" on page 76 must be 1 indicating a discharge current detection.

Set this bit to 0 (default) to disable cell balancing during discharge. In most cases cell balancing during discharge wastes system power and provides no positive benefits.

Set this bit to 1 to allow the ISL94202 to perform cell balancing during discharge.

See "Cell Balancing" on page 122 for more information. When both CBDD and CBDC are set to 0 automatic cell balancing is completely disabled.

4.1.40.2 0x4B.6 CBDC

The Cell Balance During Charge bit controls whether or not cell balancing is performed during charge. Status bit "0x82.2 CHING" on page 77 must be 1 indicating a charge current detection.

Set this bit to 0 to disable cell balancing during charge.

Set this bit to 1 (default) to allow the ISL94202 to perform automatic cell balancing during charge.

See "Cell Balancing" on page 122 for more information. When both CBDD and CBDC are set to 0 automatic cell balancing is completely disabled.

4.1.40.3 0x4B.5 DFODUV

The DFET On During Undervoltage bit controls whether or not DFET stays on during a cell under-voltage condition ("0x80.2 UVF" on page 72).

Set this bit 0 (default) in systems using separate (also referred to as parallel) discharge and charge paths. This enables the ISL94202 to automatically turn off DFET in a cell UV condition to prevent further discharge of the cells.

Set this bit 1 in systems using a single (also referred to as series) discharge and charge path. This enables the ISL94202 to keep DFET on in a cell UV condition if the device detects a charge current. Status bit "0x82.2 CHING" on page 77 must be 1 indicating a charge current detection, otherwise if discharge current is detected ("0x82.3 DCHING" on page 76) the cell UV forces the DFET off. This setting is intended to minimize DFET power dissipation through the body diode during cell UV when the pack is charging.

See "VCELL UV" on page 37 for more information.

4.1.40.4 0x4B.4 CFODOV

The CFET On During Overvoltage bit is used to control whether or not CFET stays on during a cell over-voltage condition ("0x80.0 OVF" on page 73).

Set this bit 0 (default) in systems using separate (also referred to as parallel) discharge and charge paths. This enables the ISL94202 to automatically turn off CFET in a cell OV condition to prevent further charge of the cells.

Set this bit 1 in systems using a single (also referred to as series) discharge and charge path. This enables the ISL94202 to keep CFET on in a cell OV condition if the device detects a discharge current. Status bit "0x82.3 DCHING" on page 76 must be a 1, indicating a discharge current detection, otherwise if charge current is detected ("0x82.2 CHING" on page 77) the cell OV forces the CFET off. This setting is intended to minimize CFET power dissipation through the body diode during cell OV when the pack is discharging.

See "V_{CELL} OV" on page 35 for more information.

4.1.40.5 0x4B.3 UVLOPD

The Undervoltage Lockout Powerdown bit controls whether or not the device powers down when detection of an undervoltage lockout condition ("0x80.3 UVLOF" on page 72) occurs.

The default setting of 0 means the device does not power down when detecting a UVLO condition.

Set UVLOPD to 1 to force the device to power down when detecting a UVLO condition. This selection combined with the V_{CELL} UVLO threshold is intended to prevent any further use of the pack. This is not intended as a method to conserve power until a charger is connected. If any cell is below "0x0A-0B V_{CELL} UVLO" on page 39, the device transitions back to power-down following wake-up from a charger connection.

See "System Modes" on page 119 and "Mode Exceptions" on page 122 for more information.

4.1.40.6 0x4B.0 CB_EOC

The Cell Balance During End-of-Charge bit controls whether cell balancing is performed following an V_{CELL} end-of-charge condition detection ("0x81.7 VEOC" on page 73).

The default of 0 disables cell balancing following an VEOC detection if there is no current flowing ("0x82.2 CHING" on page 77 or "0x82.3 DCHING" on page 76).

Set this bit to 1 to enable cell balancing after an VEOC detection regardless of current direction.

See "0x0C-0D V_{CELL} EOC" on page 40 and "Cell Balancing" on page 122 for more information.

4.2 0x80-89 Other Registers

These addresses apply to the EEPROM, the equivalent Configuration Register addresses are not to be accessed.

Page #	Register Address (Hex)	Register Name	Bit Function								Factory Default (Hex)	Type
			7	6	5	4	3	2	1	0		
Other Registers												
70	4C - 4F	Reserved	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	N/A	N/A
70	50 - 57	User EEPROM	User EEPROM								N/A	R/W
	58 - 5F	Reserved	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV

4.2.1 0x4C-4F RSV

These registers are reserved and should not be written to or read from.

4.2.2 0x50-57 User EEPROM

This is the user EEPROM area. There are no registers associated with this section of the EEPROM. See "Control/Data Registers" on page 138 for details on how to write to this area.

4.3 0x80-89 Operations Registers

The ISL94202 Operations Registers provide device/system status information. Some of these registers are writable and allow a level of device/system control. These registers do not map to any EEPROM location so they are not permanently programmable. During Power-On Reset (POR) these registers are set to default the values, which are subsequently updated by the ISL94202 following measurements and changes in status.

Some of these register bits enable MCU based systems to override the state machine and control the operation of the ISL94202.

Table 46. Operations Registers

Page #	Register Address (Hex)	Register Name	Bit Function 7	6	5	4	3	2	1	0	Factory Default (Hex)	Type
Operations Registers												
71	80	Status 0	CUTF	COTF	DUTF	DOTF	UVLOF	UVF	OVLOF	OVF	00	R
73	81	Status 1	VEOC	RSV	OPENF	CELLF	DSCF	DOCF	COCF	IOTF	00	R
75	82	Status 2	LVCHG	INT_ SCAN	ECC_ FAIL	ECC_ USED	DCHING	CHING	CH_ PRSNT	LD_ PRSNT	00	R
77	83	Status 3	RSV	SLEEP	DOZE	IDLE	CBUV	CBOV	CBUT	CBOT	00	R
78	84	CBFC	Cell Balance FET Control CBFC [8:1]								00	R/W
79	85	Control 0	RSV	ADC STRT	Current Gain CG1 - CG0		Analog Multiplexer Out AO [3:0]				00	R/W
80	86	Control 1	CLR_ LERR	LMON _EN	CLR_ CERR	CMON _EN	PSD	PCFET	CFET	DFET	00	RW
82	87	Control 2	RSV	µC FET	µC CBAL	µC LMON	µC CMON	µC SCAN	OW_ STRT	CBAL_ ON	00	RW
84	88	Control 3	RSV	RSV	RSV	RSV	PDWN	SLEEP	DOZE	IDLE	00	RW
85	89	EEPROM Enable	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EEEN	00	RW

4.3.1 0x80 Status 0 (R)

This status register is read only. The bits are set by the device as the specific threshold settings they are linked to are exceeded. They are cleared by the device if and when the condition that set them returns to within the related recovery threshold or hysteresis.

Table 47. Error Status Register 0

Address - Bits	0x80 - D[7]	0x80 - D[6]	0x80 - D[5]	0x80 - D[4]	0x80 - D[3]	0x80 - D[2]	0x80 - D[1]	0x80 - D[0]
Name	CUTF	COTF	DUTF	DOTF	UVLOF	UVF	OVLOF	OVF
Default	0	0	0	0	0	0	0	0

4.3.1.1 0x80.7 CUTF

The Charge Under-Temperature Fault bit is set following a Charge Under-Temperature condition detection. If the temperature of the external thermistor connected to “Thermistor Pins (20-22)” on page 96 drops below the “0x34-35 CUT” on page 58 temperature threshold, the CUTF bit is set to 1. An NTC thermistor is assumed, which means the voltage on the xTn pin is above the CUT threshold voltage.

If a CUTF condition detection occurs during charging (“0x82.2 CHING” on page 77 is set), the ISL94202 forces the CFET off. If the device detects discharge current (“0x82.3 DCHING” on page 76 is set), the “0x3C-3D DUT” on page 61 threshold determines FET status during under temperature conditions.

The ISL94202 clears the CUTF bit when it detects the temperature of the external thermistor has risen above the “0x36-37 CUTR” on page 58 threshold (the voltage has dropped below).

4.3.1.2 0x80.6 COTF

The Charge Over-Temperature Fault bit is set following a Charge Over-Temperature condition detection. If the temperature of the external thermistor connected to “Thermistor Pins (20-22)” on page 96 rises above the “0x30-31 COT” on page 56 temperature threshold, the COTF bit is set to 1. An NTC thermistor is assumed, which means the voltage on the xTn pin is below the COT threshold voltage.

If a COTF condition detection occurs during charging (“0x82.2 CHING” on page 77 is set), the ISL94202 forces the CFET off. If the device detects discharge current (“0x82.3 DCHING” on page 76 is set), the “0x38-39 DOT” on page 59 threshold determines FET status during over-temperature conditions.

The ISL94202 clears the COTF bit when it detects the temperature of the external thermistor has dropped below the "0x32-33 COTR" on page 57 threshold (the voltage has risen above).

4.3.1.3 0x80.5 DUTF

The Discharge Under-Temperature Fault bit is set following a Discharge Under-Temperature condition detection. If the temperature of the external thermistor connected to "Thermistor Pins (20-22)" on page 96 drops below the "0x3C-3D DUT" on page 61 temperature threshold, the DUT bit is set to 1. An NTC thermistor is assumed, which means the voltage on the xTn pin is above the DUT threshold voltage.

If a DUTF condition detection occurs during discharging ("0x82.3 DCHING" on page 76 is set), the ISL94202 forces the DFET off. If the device detects charge current ("0x82.2 CHING" on page 77 is set), the "0x34-35 CUT" on page 58 threshold determines FET status during under temperature conditions.

The ISL94202 clears the DUT bit when it detects the temperature of the external thermistor has risen above the "0x3E-3F DUTR" on page 61 threshold (the voltage has dropped below).

4.3.1.4 0x80.4 DOTF

The Discharge Over-Temperature Fault bit is set following a Discharge Over-Temperature condition detection. If the temperature of the external thermistor connected to "Thermistor Pins (20-22)" on page 96 rises above the "0x38-39 DOT" on page 59 temperature threshold, the DOT bit is set to 1. An NTC thermistor is assumed, which means the voltage on the xTn pin is below the DOT threshold voltage.

If a DOTF condition detection occurs during discharging ("0x82.3 DCHING" on page 76 is set), the ISL94202 forces the DFET off. If the device detects charge current ("0x82.2 CHING" on page 77 is set), the "0x30-31 COT" on page 56 threshold determines FET status during over-temperature conditions.

The ISL94202 clears the DOT bit when it detects the temperature of the external thermistor has dropped below the "0x3A-3B DOTR" on page 60 threshold (the voltage has risen above).

4.3.1.5 0x80.3 UVLOF

The Undervoltage Lockout Fault bit is set when the ISL94202 detects at least one cell voltage is below the threshold "0x0A-0B V_{CELL} UVLO" on page 39 for 5 consecutive sample cycles (measurements). This is an Undervoltage Lockout condition. When the UVLO bit is set, the "SD Pin (34)" on page 99 is driven low. If bit "0x4B.3 UVLOPD" on page 70 is set to 1, the device goes to the "Mode Exceptions" on page 122.

A UVLO condition overrides the control bit "0x87.6 µCFET" on page 82 and automatically forces the appropriate power FETs off.

The ISL94202 clears the UVLO bit only if it detects the cell voltages have risen above the recovery threshold "0x06-07 V_{CELL} UVR" on page 38. This requires all of the cell voltages to be above the UVR threshold, including when the device wakes from a UVLOPD induced Powerdown ("0x4B.3 UVLOPD" on page 70 is set to 1), otherwise it returns to Powerdown.

UVLO detection is disabled by setting the V_{CELL} UVLO threshold to 0V.

4.3.1.6 0x80.2 UVF

The Undervoltage Fault bit is set when at least one cell is below threshold "VCELL UV" on page 37 for the time period set by "0x12-13 V_{CELL} UV Timer" on page 42. This is an Undervoltage condition. If bit "0x87.6 µCFET" on page 82 is 0, the ISL94202 also shuts off DFET.

From the Undervoltage condition, if the cells recover to above the "0x06-07 V_{CELL} UVR" on page 38 threshold for a time exceeding V_{CELL} UVT plus three seconds, the ISL94202 pulses the LDMON output once every 256ms and looks for the absence of a load. The pulses are of programmable duration (0ms to 15ms) using bits "0x05.7:4 LDPW" on page 37. During the pulse period, a small current (~60µA) is output into the load. If there is no load, the LDMON voltage is higher than the recovery threshold of 0.6V. When the load has been removed and the cells are above the V_{CELL}UVR level, the ISL94202 clears the UV bit and, if µCFET = 0, turns on the discharge FET and resumes normal operation.

UV detection is disabled by setting the V_{CELL} UV threshold to 0V.

See "UV Detection & Response" on page 130 for more information.

4.3.1.7 0x80.1 OVLOF

The Overvoltage Lockout Fault bit is set when the ISL94202 detects at least one cell voltage is above the threshold "0x08-09 V_{CELL} OVLO" on page 38 for five consecutive sample cycles (measurements). This is an Overvoltage Lockout condition. When the OVLO bit is set the "CFET Pin (45)" on page 108 and "CBn Pins" on page 94 are turned off and the "PSD Pin (32)" on page 98 is driven high.

The ISL94202 clears the OVLO bit only if it detects the cell voltages have dropped below the recovery threshold "0x02-03 V_{CELL} OVR" on page 36.

The OVLO condition can be overridden by setting the OVLO threshold to 0x0FFF or by an external MCU setting the "0x87.2 µCSCAN" on page 84 bit to override the internal automatic scan, then turning on the CFET. However, if the MCU takes permanent control of the scan, it must take over the scan for all cells and all control functions, including comparisons of the cell voltage to OV and UV thresholds, managing time delays, and controlling all cell balance functions.

4.3.1.8 0x80.0 OVF

The Overvoltage Fault bit is set when at least one cell is above threshold "V_{CELL} OV" on page 35 for the time period set by "0x10-11 VC_{ELL} OV Timer" on page 41. This is an Overvoltage condition. If bit "0x87.6 µCFET" on page 82 is 0, the ISL94202 also shuts off CFET.

From the Overvoltage condition, if the cells recover to below the "0x02-03 V_{CELL} OVR" on page 36 threshold for a time exceeding V_{CELL} OVT, the ISL94202 clears the OV bit and, if µCFET = 0, turns on the charge FET and resumes normal operation.

OV detection is disabled by setting the V_{CELL} OV threshold to the maximum value (0x0FFF).

See "OV Detection/Response" on page 129 for more information.

4.3.2 0x81 - Status 1 (R)

This status register is read only. The bits are set by the device as the specific threshold settings they are linked to are exceeded. They are cleared by the device if and when the condition that set them returns to within the related recovery threshold or hysteresis. RSV bit should be ignored on register read.

Table 48. Error Status Register 1

Address - Bits	0x81 - D[7]	0x81 - D[6]	0x81 - D[5]	0x81 - D[4]	0x81 - D[3]	0x81 - D[2]	0x81 - D[1]	0x81 - D[0]
Name	VEOC	RSV	OWF	CELLF	DSCF	DOCF	COCF	IOTF
Default	0	0	0	0	0	0	0	0

4.3.2.1 0x81.7 VEOC

The Voltage End-of-Charge detection bit is set when any cell voltage is above the end-of-charge voltage threshold "0x0C-0D V_{CELL} EOC" on page 40. When this bit sets, the "EOC Pin (35)" on page 99 is pulled low. After this bit is set, it can only be cleared by the device when all cells are below the end-of-charge voltage threshold minus the hysteresis (~117mV, see "VEOCTH" on page 18). This is typically accomplished by enabling "0x4B.0 CB_EOC" on page 70.

When the CB_EOC bit is set, balancing occurs while an end-of-charge condition exists (VEOC bit = 1), regardless of current flow. This allows the ISL94202 to drain high voltage cells when charging is complete. This speeds the balancing of the pack, especially when there is a large capacity differential between cells. When the end-of-charge condition clears, the cell balance operation returns to normal programming.

VEOC detection does not shut off the CFET, disabling CFET at the end of charge is controlled by the threshold "V_{CELL} OV" on page 35.

See “VEOC” on page 130 and “Cell Balancing” on page 122.

4.3.2.2 0x81.5 OWF

The Open-Wire Fault bit is set when an open wire is detected on any of the cell voltage measurement pins. When detected, the OWF condition turns off the cell balance and power FETs, but only if bit “0x87.6 µCFET” on page 82 is 0. Setting the µCFET bit = 1 prevents the power FETs from turning off during a CELLF condition. When this bit is set, it can only be cleared if an open wire is not detected during a subsequent open-wire scan. The open-wire detection can be set to force the PSD pin high if bit “0x4A.0 OWPSD” on page 68 is set to 1. An open-wire test can be disabled by setting bit “0x4A.1 DOWD” on page 68 to 1.

See “Open Wire” on page 126 for details of operation and “0x14-15 OWT” on page 43 to set the duration of the open-wire test.

4.3.2.3 0x81.4 CELLF

The Cell Fail fault bit is set when the difference between the lowest voltage cell (“0x8A-8B CELMIN” on page 89) and highest voltage cell (“0x8C-8D CELMAX” on page 89) exceeds threshold “0x22-23 CBMAXDV” on page 51. When detected, the CELLF condition turns off the cell balance FETs and the power FETs, but only if bit “0x87.6 µCFET” on page 82 is 0. Setting the µCFET bit = 1 prevents the power FETs from turning off during a CELLF condition. The MCU is then responsible for the power FET control

When this bit is set, it is cleared only if the difference in cell voltage between the lowest voltage cell and highest voltage cell ceases to exceed the cell balance maximum differential voltage during a subsequent set of cell voltage measurements.

An CELLF detection can be set to force the PSD pin high if control bit “0x4A.7 CELLF PSD” on page 67 is set to 1.

The CELLF function can be disabled by setting the CBMAXDV value to 0x0FFF. In this case, the voltage differential can never exceed the limit. However, disabling the cell fail condition also disables open-wire detection because “Open Wire” on page 126 is triggered by a CELLF.

4.3.2.4 0x81.3 DSCF

The Discharge Short Circuit Fault bit is set when the discharge current induces a voltage across the current sense resistor that exceeds the voltage threshold “0x1B.[6:4] DSC” on page 48 for a time greater than the setting of “0x1B.[3:2] DSCTU” on page 48 and “0x1B.[1:0] - 0x1A.[7:0] DSCT” on page 49. When a discharge short-circuit condition is detected, bit “0x82.0 LD_PRSNT” on page 77 is set to 1 while the load remains attached (see “LDMON Pin (38)” on page 104).

The cell balance and power FETs turn off automatically in a short-circuit condition, regardless of the setting of the bit “0x87.6 µCFET” on page 82.

When the DSCF bit is set, it is cleared when the device detects that the load has been removed for two consecutive load monitoring scans if “0x87.4 µCLMON” on page 83 is 0 (see “DOC/DSC Recovery” on page 104). If the µCFET bit is 0, the device automatically re-enables the power FETs by setting the DFET and CFET (or PCFET) bits to 1 (assuming all other conditions are within normal ranges). If the µCFET bit is 1, the MCU must test for removal of the fault condition and turn on the power FETs. It does this by taking control of the load monitor circuit (set the µCLMON bit = 1) and periodically pulsing bit “0x86.6 LMON_EN” on page 80. When the MCU detects that LD_PRSNT = 0, it then must set the bit “0x86.7 CLR_LERR” on page 80 to 1 (to clear the error condition and reset the DOC or DSC bit) and sets the DFET and CFET (or PCFET) bits to 1 to turn on the power FETs.

4.3.2.5 0x81.2 DOCF

The Discharge Overcurrent Fault bit is set when the discharge current induces a voltage across the current sense resistor that exceeds the voltage threshold “0x17.[6:4] DOC” on page 44 for a time greater than the setting of “0x17.[3:2] DOCTU” on page 44 and “0x16-17 DOCT” on page 44. When a discharge overcurrent condition is detected, bit “0x82.0 LD_PRSNT” on page 77 is set to 1 while the load remains attached (see “LDMON Pin (38)” on page 104).

The cell balance and power FETs turn off automatically in an overcurrent condition if bit “0x87.6 µCFET” on page 82 = 0, otherwise the MCU must control the FETs.

When the DOCF bit is set, it is cleared when the device detects that the load has been removed for two consecutive load monitoring scans if “0x87.4 µCLMON” on page 83 is 0 (see “DOC/DSC Recovery” on page 104). If the µCFET bit is 0, the device automatically re-enables the power FETs by setting the DFET and CFET (or PCFET) bits to 1 (assuming all other conditions are within normal ranges). If the µCFET bit is 1, the MCU must test for removal of the fault condition and then turn on the power FETs. It does this by taking control of the load monitor circuit (set the µCLMON bit = 1) and periodically pulsing bit “0x86.6 LMON_EN” on page 80. When the MCU detects that LD_PRSNT = 0, it must set the bit “0x86.7 CLR_LERR” on page 80 to 1 (to clear the error condition and reset the DOC or DSC bit) and set the DFET and CFET (or PCFET) bits to 1 to turn on the power FETs.

4.3.2.6 0x81.1 COCF

The Charge Overcurrent Fault bit is set when the charge current induces a voltage across the current sense resistor that exceeds the voltage threshold “0x19.[6:4] COC” on page 46 for a time greater than the setting of “0x19.[3:2] COCTU” on page 46 and “0x18-19 COCT” on page 47. When a charge overcurrent condition is detected, bit “0x82.1 CH_PRSNT” on page 77 is set 1 while the charger remains attached (see “CHMON Pin (37)” on page 99).

The cell balance and power FETs turn off automatically in an overcurrent condition if bit “0x87.6 µCFET” on page 82 = 0, otherwise the MCU must control the FETs.

When the COCF bit is set, it is cleared when the device detects that the charger has been removed for two consecutive load monitoring scans if “0x87.3 µCCMON” on page 83 is 0 (see “COC Recovery” on page 100). If the µCFET bit is 0, the device automatically re-enables the power FETs by setting the DFET and CFET (or PCFET) bits to 1 (assuming all other conditions are within normal ranges). If the µCFET bit is 1, the MCU must test for removal of the fault condition and then turn on the power FETs. It does this by taking control of the charger monitor circuit (set the µCCMON bit = 1) and periodically pulsing bit “0x86.4 CMON_EN” on page 81. When the MCU detects that CH_PRSNT = 0, it must set the bit “0x86.5 CLR_CERR” on page 81 to 1 (to clear the error condition and reset the DOC or DSC bit) and set the DFET and CFET (or PCFET) bits to 1 to turn on the power FETs.

4.3.2.7 0x81.0 IOTF

The Internal Over-Temperature Fault bit is set to 1 if the internal temperature of the IC goes above the threshold “0x40-41 IOT” on page 62. When the ISL94202 sets the IOTF bit, it also stops/prevents cell balancing and turns off the power FETs. When IOTF is set, the device continues to prevent turn on of the FETs until the internal temperature drops below the recovery threshold “0x42-43 IOTR” on page 63.

Note: If the device wakes from Powerdown or SLEEP Mode with the internal temperature above IOTR it may also prevent turn on of the FETs.

4.3.3 0x82 - Status 2 (R)

This status register is read only. The bits are set by the device as the specific threshold settings they are linked to are exceeded. They are cleared by the device if and when the condition that set them returns to within the related recovery threshold or hysteresis.

Table 49. Error Status Register 2

Address - Bits	0x82 - D[7]	0x82 - D[6]	0x82 - D[5]	0x82 - D[4]	0x82 - D[3]	0x82 - D[2]	0x82 - D[1]	0x82 - D[0]
Name	LVCHG	INT_SCAN	ECC_FAIL	ECC_USED	DCHING	CHING	CH_PRSNT	LD_PRSNT
Default	0	0	0	0	0	0	0	0

4.3.3.1 0x82.7 LVCHG

The Low Voltage Charge bit is set if at least one cell voltage is below the threshold "0x0E-0F V_{CELL} LVCL" on page 40. If LVCHG is 1, the PCFET turns on instead of CFET as long as at least one cell is below the V_{CELL} LVCL setting.

When all cells are above the Low Voltage Charge threshold, the PCFET output turns off and the CFET output turns on (when appropriate).

See "0x4A.2 PCFETE" on page 68, "0x86.2 PCFET" on page 81, and "0x86.1 CFET" on page 81.

4.3.3.2 0x82.6 INT_SCAN

The Internal Scan bit is active low (0) for the duration of an internal measurement scan, otherwise it is 1. This bit allows a MCU to synchronize with the ISL94202 system scan when reading scan data such as voltages and temperatures. If the MCU attempts to read a data register while it is being written the result may be incorrect.

See "Wake Up" on page 115.

4.3.3.3 0x82.5,4 ECC_FAIL & ECC_USED

The ISL94202 contains an Error Checking/detection/Correction mechanism for EEPROM read operations. When reading a value from the EEPROM, the device checks the data value for an error. Two bits represent the status of the read operation, see Table 50.

If there are no errors, the EEPROM value is valid and the ECC_USED and ECC_FAIL bits are set to 0. If there is a 1-bit error, the ISL94202 corrects the error and sets the ECC_USED bit. This is a valid operation and the value read from the EEPROM is correct. During an EEPROM read, if there is an error consisting of two or more bits, the ISL94202 sets the ECC_FAIL bit (ECC_USED = 0). This read contains invalid data.

The error correction is also active during the initial power-on recall of the EEPROM values to the configuration registers. The circuit corrects for any 1-bit errors. 2-bit errors are not corrected and the contents of the configuration register maintain the previous value.

Internally, the power-on recall circuit uses the ECC_USED and ECC_FAIL bits to determine there is a proper recall before allowing the device operation to start. However, an external MCU cannot use these bits to detect the validity of the registers on power-up or determine the use of the error correction mechanism, because the bits automatically reset on the next valid read.

Table 50. ECC_FAIL & ECC_USED

0x82.5 ECC_FAIL	0x82.4 ECC_USED	Description
0	0	No Errors Detected.
0	1	1-bit error detected and corrected - Valid read.
1	0	2-bit or more error detected - NOT corrected - Invalid read.
1	1	Invalid.

See "Control/Data Registers" on page 138 and "I²C Interface" on page 141.

4.3.3.4 0x82.3 DCHING

The Discharging bit is set by the analog current direction detection circuit when the discharge current produces a voltage across the sense resistor greater than the minimum detection threshold voltage of ~100µV (typical, see "VDCTH" on page 15, not programmable) for more than 2ms.

For current direction detection, there is a 2ms digital delay for getting into or out of either direction condition (CHING or DCHING). This means that the current detection circuit needs to detect an uninterrupted flow of current out of the pack for more than 2ms to indicate a discharge condition (DCHING). Then, the current detector needs to identify that there is a charge current (CHING) or no current (both CHING and DCHING clear) for a continuous 2ms to remove the discharge condition.

The measured value for discharge (or charge) current is stored in registers “0x8E-8F IPACK” on page 90. The current reading should only be considered valid if this bit or “0x82.2 CHING” on page 77 is set, otherwise it should be discarded.

When set, this bit indicates current flowing out of the pack.

4.3.3.5 0x82.2 CHING

The Charging bit is set by the analog current direction detection circuit when the charge current produces a voltage across the sense resistor more negative than the minimum detection threshold voltage of -100µV (typical, see “VCCTH” on page 15, not programmable) for more than 2ms.

For current direction detection, there is a 2ms digital delay for getting into or out of either direction condition (CHING or DCHING). This means that the current detection circuit needs to detect an uninterrupted flow of current out of the pack for more than 2ms to indicate a discharge condition (DCHING). Then, the current detector needs to identify that there is a charge current (CHING) or no current (both CHING and DCHING clear) for a continuous 2ms to remove the discharge condition.

The measured value for charge (or discharge) current is stored in registers “0x8E-8F IPACK” on page 90. The current reading should only be considered valid if this bit or “0x82.3 DCHING” on page 76 is set, otherwise it should be discarded.

When set, this bit indicates current flowing into the pack.

4.3.3.6 0x82.1 CH_PRSNT

The Charger Present bit is set during a COC condition (see “0x18-19 COC & COCT” on page 46 and “0x81.1 COCF” on page 75) while the charger is still attached.

If the voltage on the “CHMON Pin (37)” on page 99 falls below the threshold (see “V_{CHMON}” on page 16) and “0x87.3 µCCMON” on page 83 = 0, the CH _PRSNT bit resets automatically. CH _PRSNT remains set as long as the voltage on the CHMON pin is above the threshold.

If the voltage on the CHMON pin drops below the threshold and µCCMON = 1, the bit is reset only upon a read of the “0x82 - Status 2 (R)” on page 75 by a MCU.

See “COC Recovery” on page 100.

A Charger Present detection wakes a device from Powerdown or SLEEP into NORMAL Mode.

4.3.3.7 0x82.0 LD_PRSNT

The Load Present bit is set during a DOC or DSC condition (see “0x16-17 DOC & DOCT” on page 43 and “0x1A-1B DSC & DSCT” on page 48 respectively) while the load is still attached.

If the voltage on the “LDMON Pin (38)” on page 104 pin rises above the threshold (see “V_{LDMON}” on page 16) and “0x87.3 µCCMON” on page 83 = 0, the bit resets automatically. LD_PRSNT remains set as long as the voltage on the LDMON pin is below the threshold.

If the voltage on the LDMON pin rises above the threshold and µCLMON = 1, the bit is reset only on a read of the “0x82 - Status 2 (R)” on page 75 by a MCU.

See “DOC/DSC Recovery” on page 104.

A Load Present detection wakes a device from SLEEP into NORMAL Mode. If the device is in Powerdown, a Load Present detection on wake up can prevent the power FETs from turning on.

4.3.4 0x83 - Status 3 (R)

The Status 3 register is read only. The bits are set by the device as the specific threshold settings they are linked to are exceeded. They are cleared by the device if/when the condition that set them returns to within the related recovery threshold or hysteresis. RSV bit should be ignored on register read.

Table 51. Error Status Register 3

Address - Bits	0x83 - D[7]	0x83 - D[6]	0x83 - D[5]	0x83 - D[4]	0x83 - D[3]	0x83 - D[2]	0x83 - D[1]	0x83 - D[0]
Name	RSV	IN_SLEEP	IN_DOZE	IN_IDLE	CBUV	CBOV	CBUTF	CBOTF
Default	0	0	0	0	0	0	0	0

4.3.4.1 0x83.6 IN_SLEEP

The In SLEEP Mode bit is set when the ISL94202 is in "SLEEP Mode" on page 121. The IN_SLEEP bit is cleared on initial power up, by the "CHMON Pin (37)" on page 99 going high or by the "LDMON Pin (38)" on page 104 going low.

If bits 0x83.[6:4] are all 0, the device is either in "NORMAL Mode" on page 120 or "Powerdown State" on page 120, the device does not respond in Powerdown and the "RGO Pin (36)" on page 99 is off.

4.3.4.2 0x83.5 IN_DOZE

The In DOZE Mode bit is set when the ISL94202 is in "DOZE Mode" on page 121.

If bits 0x83.[6:4] are all 0, the device is either in "NORMAL Mode" on page 120 or "Powerdown State" on page 120, the device does not respond in Powerdown and the "RGO Pin (36)" on page 99 is off.

4.3.4.3 0x83.4 IN_IDLE

The In IDLE Mode bit is set when the ISL94202 is in "IDLE Mode" on page 121.

If bits 0x83.[6:4] are all 0, the device is either in "NORMAL Mode" on page 120 or "Powerdown State" on page 120, the device does not respond in Powerdown and the "RGO Pin (36)" on page 99 is off.

4.3.4.4 0x83.3 CBUV

The Cell Balance Undervoltage bit is set during a Cell Balance Undervoltage condition, when all cell voltages are below threshold "0x1C-1D CBMIN" on page 49. At least one cell voltage must rise above the CBMIN threshold to recover from a Cell Balance Undervoltage condition, then the ISL94202 automatically clears the CBUV bit.

4.3.4.5 0x83.2 CBOV

The Cell Balance Overvoltage bit is set during a Cell Balance Overvoltage condition, when all cell voltages are above threshold "0x1E-1F CBMAX" on page 50. At least one cell voltage must drop below the CBMAX threshold to recover from a Cell Balance Overvoltage condition, then the ISL94202 automatically clears the CBOV bit.

4.3.4.6 0x83.1 CBUTF

The Cell Balance Under-Temperature Fault bit is set during a Cell Balance Under-Temperature condition. This occurs when the external temperature sensing thermistors indicate a battery pack temperature below the threshold defined by register "0x28-29 CBUT" on page 53. When the pack temperature rises above the threshold the ISL94202 automatically clears the CBUTF bit.

4.3.4.7 0x83.0 CBOTF

The Cell Balance Over-Temperature Fault bit is set during a Cell Balance Over-Temperature condition. This occurs when the external temperature sensing thermistors indicate a battery pack temperature above the threshold defined by register "0x2C-2D CBOT" on page 55. When the pack temperature drops below the threshold the ISL94202 automatically clears the CBOTF bit.

4.3.5 0x84 CBFC (R/W)

The Cell Balance FET Control register is located address 0x84. These bits enable MCU control of cell balancing only if the external MCU overrides the ISL94202 automatic cell balance operation ("0x87.5 µCCBAL" on page 83 = 1). Each CBxON bit (Table 52) controls the corresponding "CBn Pins" on page 94 cell balance FET drive output.

Table 52. CBFC

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	CB8ON	CB7ON	CB6ON	CB5ON	CB4ON	CB3ON	CB2ON	CB1ON
Default	0	0	0	0	0	0	0	0

- A value of 0 written to any bit in this register turns OFF the corresponding CBx pin cell balance output (default).
- A value of 1 written to any bit in this register turns ON the corresponding CBx pin cell balance output.

The following conditions apply (no faults):

- Cell Balance pin CBx = ON, if CBAL_ON = 1 and CBxON = 1 (see "0x87.0 CBAL_ON" on page 84)
- Cell Balance pin CBx = OFF, if CBAL_ON = 0 or CBxON = 0

If µCCBAL = 0, the ISL94202 performs cell balancing. These bits are also used during automatic cell balancing, but their state is not intended to indicate if/when a CB FET is on.

See "CBn Pins" on page 94 for more information on the cell balance FET drive pins and "Cell Balancing" on page 122 for more information on cell balancing operation.

4.3.6 0x85 Control 0 (R/W)

Control register 0 enables a MCU or test system to control the ADC conversion, current sense gain and the multiplexer if it overrides scan operation by setting bit "0x87.2 µCSCAN" on page 84 to 1. The RSV bit should be set to 0 on a write and ignored on register read.

Table 53. Control Register 0

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	RSV	ADCSTRT	CG1	CG0	AO3	AO2	AO1	AO0
Default	0	0	0	0	0	0	0	0

4.3.6.1 0x85.6 ADCSTRT

The ADC conversion start bit is used when an external MCU overrides measurement scan operation. When this bit is set to 1, an AD conversion is started. This bit automatically resets to 0 on execution and it does not indicate when the AD conversion is complete.

4.3.6.2 0x85.[5:4] CG

The Current Gain setting bits are used when an external MCU overrides measurement scan operation. These bits set the gain of the amplifier which measures the voltage across the current sense resistor ("CSI1-2 Pins (47, 48)" on page 111). Available settings are shown in Table 54.

Table 54. Current Gain Settings

CG1	CG0	Current gain
0	0	x50
0	1	x5
1	0	x500
1	1	x500

If the MCU overrides measurement scan operation, the selected gain must be used in the current calculation ("0x8E-8F IPACK" on page 90).

See "Current Monitoring/Response" on page 132 for more information.

4.3.6.3 0x85.[3:0] AO

The Analog Output selection bits are used when an external MCU overrides measurement scan operation. The AO bits select (Table 55) which ISL94202 voltage sense pins are output from the internal analog MUX. The result is stored in registers “0xAA-AB - ADCV” on page 93 by the ADC when internal scan operation has been overridden.

Table 55. Analog MUX Control

AO3	AO2	AO1	AO0	Output
0	0	0	0	OFF (Hi-Z)
0	0	0	1	VC1
0	0	1	0	VC2
0	0	1	1	VC3
0	1	0	0	VC4
0	1	0	1	VC5
0	1	1	0	VC6
0	1	1	1	VC7
1	0	0	0	VC8
1	0	0	1	Pack Current
1	0	1	0	VBAT/16
1	0	1	1	RGO/2
1	1	0	0	xT1
1	1	0	1	xT2
1	1	1	0	iT
1	1	1	1	OFF (Hi-Z)

4.3.7 0x86 Control 1 (R/W)

Control register 0 enables a MCU or test system to control Load/Charger detection, power FET operation, and the PSD pin if it overrides automatic device operation by setting bits “0x87.6 µCFET” on page 82, “0x87.4 µCLMON” on page 83, and/or “0x87.3 µCCMON” on page 83 to 1.

Table 56. Control Register 1

Address - Bits	0x86 - D[7]	0x86 - D[6]	0x86 - D[5]	0x86 - D[4]	0x86 - D[3]	0x86 - D[2]	0x86 - D[1]	0x86 - D[0]
Name	CLR_LERR	LMON_EN	CLR_CERR	CMON_EN	PSD	PCFET	CFET	DFET
Default	0	0	0	0	0	0	0	0

4.3.7.1 0x86.7 CLR_LERR

The Clear Load Error bit resets the bit “0x82.0 LD_PRSNT” on page 77 if the MCU has taken control of the load monitor function by setting bit “0x87.4 µCLMON” on page 83 to 1.

- Writing a 1 to CLR_LERR resets the LD_PRSNT bit. CLR_LERR automatically resets and is only active when µCLMON = 1.

See “LDMON Pin (38)” on page 104 for more information.

4.3.7.2 0x86.6 LMON_EN

The Load Monitor Enable bit is used by the MCU to turn the load monitor circuit ON or OFF if it has taken control of the monitor function by setting bit “0x87.4 µCLMON” on page 83 to 1.

- Writing a 0 to this bit turns OFF the load monitor circuit (default).

- Writing a 1 to this bit turns ON the load monitor circuit.

After writing a 1 to this bit, the LDMON recovery circuit is pulsed once and the status of the bit “0x82.0 LD_PRSNT” on page 77 is updated. LMON_EN automatically clears.

See “LDMON Pin (38)” on page 104 for more information.

4.3.7.3 0x86.5 CLR_CERR

The Clear Charger Error bit resets the bit “0x82.1 CH_PRSNT” on page 77 if the MCU has taken control of the charger monitor function by setting bit “0x87.3 µCCMON” on page 83 to 1.

Writing a 1 to CLR_CERR resets the CH_PRSNT bit. This bit automatically resets and is only active when µCCMON = 1.

See “CHMON Pin (37)” on page 99 for more information.

4.3.7.4 0x86.4 CMON_EN

The Charger Monitor Enable bit is used by the MCU to turn the charger monitor circuit ON or OFF if it has taken control of the monitor function by setting bit “0x87.3 µCCMON” on page 83 to 1.

- Writing a 0 to this bit turns OFF the charger monitor circuit (default).
- Writing a 1 to this bit turns ON the charger monitor circuit.

After writing a 1 to this bit, the CHMON recovery circuit is pulsed once and the status of the bit “0x82.1 CH_PRSNT” on page 77 is updated. CMON_EN automatically clears.

See “CHMON Pin (37)” on page 99 for more information.

4.3.7.5 0x86.3 PSD

The pack shutdown bit is used by the MCU to assert (set high) the “PSD Pin (32)” on page 98. This output can be used to drive external circuitry to blow a fuse. The ISL94202 digital pins operate relative to the “RGO Pin (36)” on page 99, which provides ~2.5V maximum logic High.

- Write a 0 to his register to set the PSD pin low (default).
- Write a 1 to this register to set the PSD pin high.

This bit is also set in conditions where PSD is asserted automatically by the ISL94202 if enabled by the following bits; “0x4A.7 CELLF PSD” on page 67, “0x4A.0 OWPSD” on page 68 and “0x08-09 V_{CELL} OVLO” on page 38.

Follow the links for more information.

4.3.7.6 0x86.2 PCFET

The Pre-Charge FET bit is used by the MCU to turn on or off the “PCFET Pin (44)” on page 108.

- Writing a 0 to this bit turns PCFET OFF (default).
- Writing a 1 to this bit turns PCFET ON.

This bit is set to 0 automatically by the ISL94202 in COC, DOC, or DSC conditions, unless the automatic response is disabled by the bit “0x87.6 µCFET” on page 82. If automatic FET control is disabled, a DSC condition still forces the power FETs off because a MCU cannot override the DSC response.

Figure 37 on page 82 shows the timing between set/clear of this bit and the PCFET pin. See “0x18-19 COC & COCT” on page 46, “0x16-17 DOC & DOCT” on page 43, and “0x1A-1B DSC & DSCT” on page 48 for more information.

4.3.7.7 0x86.1 CFET

The Charge FET bit is used by the MCU to turn on or off the “CFET Pin (45)” on page 108.

- Writing a 0 to this bit turns CFET OFF (default).
- Writing a 1 to this bit turns CFET ON.

This bit is set to 0 automatically by the ISL94202 in a COC or DSC condition, unless the automatic response is disabled by the bit “0x87.6 µCFET” on page 82. If automatic FET control is disabled, a DSC condition still forces the power FETs off because a MCU cannot override DSC response.

Figure 37 on page 82 shows the timing relationship between set/clear of this bit and the CFET pin. See “0x18-19 COC & COCT” on page 46 and “0x1A-1B DSC & DSCT” on page 48 for more information.

4.3.7.8 0x86.0 DFET

The Discharge FET bit is used by the MCU to turn on or off the “DFET Pin (42)” on page 108.

- Writing a 0 to this bit turns DFET OFF (default).
- Writing a 1 to this bit turns DFET ON.

This bit is set to 0 automatically by the ISL94202 in a DOC or DSC condition, unless the automatic response is disabled by the bit “0x87.6 µCFET” on page 82. If automatic FET control is disabled, a DSC condition still forces the power FETs off because a MCU cannot override DSC response.

Figure 37 shows the timing relationship between set/clear of this bit and the DFET pin. See “0x16-17 DOC & DOCT” on page 43 and “0x1A-1B DSC & DSCT” on page 48 for more information.

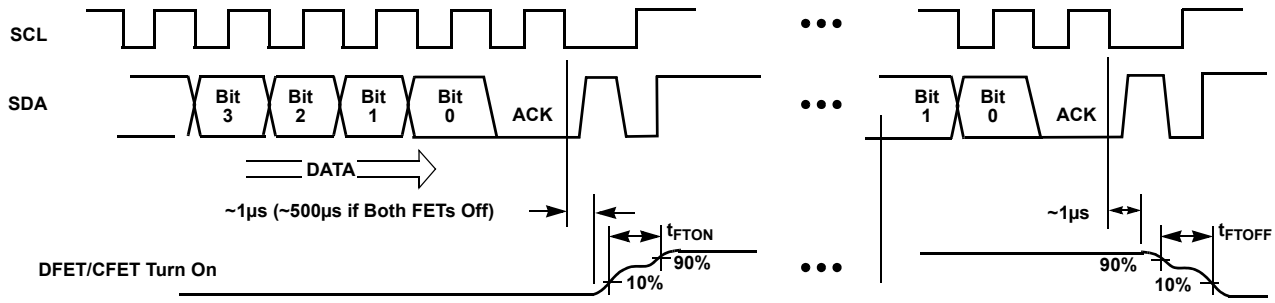


Figure 37. I²C FET Control Timing

4.3.8 0x87 - Control 2 (R/W)

Control register 2 enables a MCU or test system to override most of the ISL94202 autonomous operations.

The RSV bit should be set to 0 on a write and ignored on register read.

Table 57. Control Register 2

Address - Bits	0x87 - D[7]	0x87 - D[6]	0x87 - D[5]	0x87 - D[4]	0x87 - D[3]	0x87 - D[2]	0x87 - D[1]	0x87 - D[0]
Name	RSV	µCFET	µCCBAL	µCLMON	µCCMON	µCSCAN	OW_STRT	CBAL_ON
Default	0	0	0	0	0	0	0	0

4.3.8.1 0x87.6 µCFET

The MCU FET control bit overrides automatic FET control by the ISL94202. When the MCU sets this bit it is responsible for enabling/disabling the FETs when necessary under most conditions. The exceptions are Short-Circuit Current, Open-Wire, Internal Over-Temperature, OVLO and UVLO faults, plus SLEEP, and FETSOFF (“FETSOFF Pin (33)” on page 98) conditions override the µCFET control bit and automatically force the appropriate power FETs off.

- Writing a 0 to bit µCFET means automatic FET control is operational (default).
- Writing a 1 to bit µCFET means the FETs are controlled by an external MCU.

For more information on the relationship of the µCFET setting and automatic FET control response scenarios also see:

Cell Voltages

- “0x00-01 CDPW & V_{CELL} OV” on page 35 and “0x02-03 V_{CELL} OVR” on page 36
- “0x04-05 LDPW & V_{CELL} UV” on page 37 and “0x06-07 V_{CELL} UVR” on page 38
- “0x08-09 V_{CELL} OVLO” on page 38 and “0x80.1 OVLOF” on page 73
- “0x0A-0B V_{CELL} UVLO” on page 39 and “0x80.3 UVLOF” on page 72
- “0x0E-0F V_{CELL} LVCL” on page 40 and “0x82.7 LVCHG” on page 76

Pack Current

- “0x16-17 DOC & DOCT” on page 43 and “0x81.2 DOCF” on page 74
- “0x18-19 COC & COCT” on page 46 and “0x81.1 COCF” on page 75
- “0x1A-1B DSC & DSCT” on page 48 and “0x81.3 DSCF” on page 74

Temperature

- “0x30-31 COT” on page 56, “0x32-33 COTR” on page 57, and “0x80.6 COTF” on page 71
- “0x34-35 CUT” on page 58, “0x36-37 CUTR” on page 58, and “0x80.7 CUTF” on page 71
- “0x38-39 DOT” on page 59, “0x3A-3B DOTR” on page 60, and “0x80.4 DOTF” on page 72
- “0x3C-3D DUT” on page 61, “0x3E-3F DUTR” on page 61, and “0x80.5 DUTF” on page 72
- “0x40-41 IOT” on page 62, “0x42-43 IOTR” on page 63, and “0x81.0 IOTF” on page 75

Open Wire

- “0x14-15 OWT” on page 43 and “0x81.5 OWF” on page 74

4.3.8.2 0x87.5 µCCBAL

The MCU Cell Balancing bit overrides automatic CB FET control by the ISL94202. When the MCU sets this bit it is responsible for enabling/disabling the CB FETs. See “0x85 Control 0 (R/W)” on page 79 and “0x49 Cell Select” on page 67.

- Writing a 0 to this bit means automatic cell balancing by the ISL94202 is enabled (default).
- Writing a 1 to this bit means automatic cell balancing by the ISL94202 is disabled.

For more information on automatic and MCU enabled cell balancing, see section “Cell Balancing” on page 122.

4.3.8.3 0x87.4 µCLMON

The MCU Load Monitoring bit overrides automatic load monitoring control by the ISL94202.

- Writing a 0 to this bit means automatic load monitoring by the ISL94202 is enabled (default).
- Writing a 1 to this bit means automatic load monitoring by the ISL94202 is disabled. The MCU must trigger load detection using “0x86.6 LMON_EN” on page 80.

For more information on operations dependent on load monitoring, see “LDMON Pin (38)” on page 104, “OV Detection/Response” on page 129, “UV Detection & Response” on page 130, and “Current Monitoring/Response” on page 132.

4.3.8.4 0x87.3 µCCMON

The MCU Charger Monitoring bit overrides automatic charger monitoring control by the ISL94202.

- Writing a 0 to this bit means automatic charger monitoring by the ISL94202 is enabled (default).
- Writing a 1 to this bit means automatic charger monitoring by the ISL94202 is disabled. The MCU must trigger load detection using “0x86.4 CMON_EN” on page 81.

For more information on operations dependent on charger monitoring, see “CHMON Pin (37)” on page 99, “OV Detection/Response” on page 129, “UV Detection & Response” on page 130, and “Current Monitoring/Response” on page 132.

4.3.8.5 0x87.2 µCSCAN

The MCU System Scan bit overrides automatic system measurement scans that are normally based on the device "System Modes" on page 119. This bit is reset if the "0x47.[7:3] WDT" on page 65 expires, system scans only resume on receipt of the next I^2C transaction.

- Writing a 0 to this bit means the ISL94202 automatically performs the system scan based on the device Mode (default).
- Writing a 1 to this bit means the ISL94202 does not perform the system scans automatically. The MCU must trigger the measurements normally executed by the automatic system scans. See "0x85 Control 0 (R/W)" on page 79.

See "System Scans" on page 116 for more information.

4.3.8.6 0x87.1 OW_STRT

The Open Wire Start bit triggers an open-wire scan. This bit automatically resets when completing the open-wire scan. This bit is only active if "0x4A.1 DOWD" on page 68 is 1 or µCSCAN is 1.

- Writing a 0 to this bit does nothing, but reading a 0 means no open-wire scan is being performed (default).
- Writing a 1 to this bit initiates an open-wire scan.

For more information, see "Open Wire" on page 126.

4.3.8.7 0x87.0 CBAL_ON

The Cell Balance on bit turns on selected cell balance pins if the MCU Cell Balancing bit (µCCBAL) is set to 1. This bit is only operational if the µCCBAL bit is 1.

- Writing a 0 to this bit disables all CBn outputs (default).
- Writing a 1 to this bit enables CBn outputs previously set to 1 in register "0x84 CBFC (R/W)" on page 78 and disables the outputs set to 0.

For more information, see "MCU CB" on page 126.

4.3.9 0x88 - Control 3

Control register 3 enables a MCU or test system to override the ISL94202 automatic mode transitions and select a specific mode. When set, the device remains in the selected Mode as automatic mode transitions are blocked. Setting more than one of these bits simultaneously to 1 is not supported. These bits are not intended to indicate device Mode status, see "0x83 - Status 3 (R)" on page 77. The device does not include a bit to indicate "Powerdown State" on page 120 because register access is not possible in Powerdown.

Table 58. Control Register 3

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	RSV	RSV	RSV	RSV	PDWN	SLEEP	DOZE	IDLE
Default	0	0	0	0	0	0	0	0

The RSV bits should be set to 0 on a write and ignored on register read.

4.3.9.1 0x88.3 PDWN

The Powerdown bit is used by the MCU to force the ISL94202 into the "Mode Exceptions" on page 122. This bit can be used to place the pack in the lowest current state for prolonged storage at the end of battery pack test. The device can only be brought out of Powerdown by a charger connection detection ("Charger Detection" on page 102) as no communications are possible. On wake-up from Powerdown the device loads settings to the registers backed by EEPROM while the other registers are set to default including this bit.

- Writing a 0 (default) to this bit is not possible if the device is in "Powerdown State" on page 120, only a CHMON detection ("CHMON Pin (37)" on page 99) wakes the device from Powerdown.

- Writing a 1 to this bit puts the device in the Powerdown State.
- Reading a 0 from this bit shows the device is not in the Powerdown State, although any response from the device indicates it is not in Powerdown.

For more information, see "System Modes" on page 119.

4.3.9.2 0x88.2 SLEEP

The SLEEP bit is used by a MCU to force the ISL94202 into "SLEEP Mode" on page 121.

- Writing a 1 to this bit puts the device in SLEEP Mode.
- Overwriting a 1 with a 0 (default) on this bit enables normal ISL94202 Mode operation.
- Reading a 0 from this bit shows the device is not forced into SLEEP Mode by command from the MCU.

For more information, see "System Modes" on page 119.

4.3.9.3 0x88.1 DOZE

The DOZE bit is used by a MCU to force the ISL94202 into "DOZE Mode" on page 121.

- Writing a 1 to this bit puts the device in DOZE Mode.
- Overwriting a 1 with a 0 (default) on this bit enables normal ISL94202 Mode operation.
- Reading a 0 from this bit shows the device is not forced into DOZE Mode by command from the MCU.

For more information, see "System Modes" on page 119.

4.3.9.4 0x88.0 IDLE

The IDLE bit is used by a MCU to force the ISL94202 into "IDLE Mode" on page 121.

- Writing a 1 to this bit puts the device in IDLE Mode.
- Overwriting a 1 with a 0 (default) on this bit enables normal ISL94202 Mode operation.
- Reading a 0 from this bit shows the device is not forced into IDLE Mode by command from the MCU.

For more information, see "System Modes" on page 119.

4.3.10 0x89 - EEPROM Enable

This register contains the bit used for reading from and programming the ISL94202 EEPROM.

The RSV bits should be set to 0 on a write and ignored on register read.

Table 59. EEPROM Enable

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EEEN
Default	0	0	0	0	0	0	0	0

4.3.10.1 0x89.0 EEEN

The EEPROM Enable bit determines read/write access to either the control registers or the EEPROM.

- Set EEEN = 0 (default) by writing 0x00 to register 0x89 to access the control registers.
- Set EEEN = 1 by writing 0x01 to register 0x89 to access the ISL94202 EEPROM.

Reading from and writing to control/status registers and reading from EEPROM can be performed using a byte operation (read/write 1 byte) or page operation (read/write 4 bytes).

Writing to EEPROM must be performed using a byte operation, and all 4 bytes in the page must be written. For more information, see "Byte Write" on page 143 and "EEPROM Write" on page 148.

For more information on programming the EEPROM, see "Control/Data Registers" on page 138.

4.4 0x8A-AB Data Registers

The ISL94202 has a 14-bit ADC for voltage measurements. The outputs of most measurements are stored as 12-bits spanning two 8-bit registers to represent the digitized result. When two registers are used, the portion of the result is described in the register map name such as MSB or LSB.

Table 60. Data Registers

Page #	Register Address (Hex)	Register Name	Bit Function 7	6	5	4	3	2	1	0	Factory Default (Hex)	Type
Data Registers												
89	8A	CELMIN LSB	Minimum Cell Voltage CELMIN [7:0]								N/A	R
	8B	CELMIN MSB	RSV	RSV	RSV	RSV	Minimum Cell Voltage CELMIN [B:8]				N/A	R
89	8C	CELMAX LSB	Maximum Cell Voltage CELMAX [7:0]								N/A	R
	8D	CELMAX MSB	RSV	RSV	RSV	RSV	Maximum Cell Voltage CELMAX [B:8]				N/A	R
90	8E	IPACK LSB	Pack Current IPACK [7:0]								N/A	R
	8F	IPACK MSB	RSV	RSV	RSV	RSV	Pack Current IPACK [B:8]				N/A	R
90	90	VCELL1 LSB	Cell 1 Voltage VCELL1 [7:0]								N/A	R
	91	VCELL1 MSB	RSV	RSV	RSV	RSV	Cell 1 Voltage VCELL1 [B:8]				N/A	R
91	92	VCELL2 LSB	Cell 2 Voltage VCELL2 [7:0]								N/A	R
	93	VCELL2 MSB	RSV	RSV	RSV	RSV	Cell 2 Voltage VCELL2 [B:8]				N/A	R
91	94	VCELL3 LSB	Cell 3 Voltage VCELL3 [7:0]								N/A	R
	95	VCELL3 MSB	RSV	RSV	RSV	RSV	Cell 3 Voltage VCELL3 [B:8]				N/A	R
91	96	VCELL4 LSB	Cell 4 Voltage VCELL4 [7:0]								N/A	R
	97	VCELL4 MSB	RSV	RSV	RSV	RSV	Cell 4 Voltage VCELL4 [B:8]				N/A	R
91	98	VCELL5 LSB	Cell 5 Voltage VCELL5 [7:0]								N/A	R
	99	VCELL5 MSB	RSV	RSV	RSV	RSV	Cell 5 Voltage VCELL5 [B:8]				N/A	R
91	9A	VCELL6 LSB	Cell 6 Voltage VCELL6 [7:0]								N/A	R
	9B	VCELL6 MSB	RSV	RSV	RSV	RSV	Cell 6 Voltage VCELL6 [B:8]				N/A	R
91	9C	VCELL7 LSB	Cell 7 Voltage VCELL7 [7:0]								N/A	R
	9D	VCELL7 MSB	RSV	RSV	RSV	RSV	Cell 7 Voltage VCELL7 [B:8]				N/A	R
91	9E	VCELL8 LSB	Cell 8 Voltage VCELL8 [7:0]								N/A	R
	9F	VCELL8 MSB	RSV	RSV	RSV	RSV	Cell 8 Voltage VCELL8 [B:8]				N/A	R
91	A0	ITEMP LSB	Internal Temperature IT [7:0]								N/A	R
	A1	ITEMP MSB	RSV	RSV	RSV	RSV	Internal Temperature IT [B:8]				N/A	R
91	A2	XT1 LSB	External Temperature 1 XT1 [7:0]								N/A	R
	A3	XT1 MSB	RSV	RSV	RSV	RSV	External Temperature 1 XT1 [B:8]				N/A	R
92	A4	XT2 LSB	External Temperature 2 XT2 [7:0]								N/A	R
	A5	XT2 MSB	RSV	RSV	RSV	RSV	External Temperature 2 XT2 [B:8]				N/A	R
92	A6	VBATT LSB	Pack Voltage VBATT [7:0]								N/A	R
	A7	VBATT MSB	RSV	RSV	RSV	RSV	Pack Voltage VBATT [B:8]				N/A	R
92	A8	VRGO LSB	RGO Voltage VRGO [7:0]								N/A	R
	A9	VRGO MSB	RSV	RSV	RSV	RSV	RGO Voltage VRGO [B:8]				N/A	R
93	AA	ADC LSB	14-bit ADC Voltage ADC [7:0]								N/A	R
	AB	ADC MSB	RSV	RSV	14-bit ADC Voltage ADC [D:8]						N/A	R
	AC - AF	Reserved (RSV)	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	N/A	N/A

The ranges and step-sizes listed for measurement registers are the ideal values to be used for calculation purposes. The usable measurement range is also limited by the recommended operating conditions and by non-idealities of the measurement channel. Measurement result registers may or may not reach the maximum or minimum for input voltages within the ideal voltage range listed.

Formulas used for conversion between voltages and register values include constants. The following section explains the origin of these constants. Not all of these parameters are included in every conversion, see the specific register description for the correct method of conversion for each.

4.4.1 Conversion Constants

The ISL94202 has an internal 14-bit ADC and a precision 1.8V voltage reference for measurement of all of the system voltages. The full-scale ADC reading is limited to this 1.8V reference voltage.

Each voltage to be measured is level shifted to the input of the ADC. Given a 1.8V full-scale range, most of these voltages must be divided to remain within this range.

Given a maximum cell voltage of 4.8V and the 1.8V ADC full-scale voltage, cell voltages must be scaled by 1.8/4.8 or 3/8 to use the entire input range of the ADC.

The following are used in the next two subsections as examples of a cell voltage reading conversion from Analog to Digital and Digital to Analog.

- $\mathbf{V_{cell}}$ = 3.85V = The actual cell voltage.
- $\mathbf{V_{ref}}$ = 1.8V = The ADC reference.
- $\mathbf{V_{scale}}$ = (3/8) = The ADC reference voltage divided by the full scale voltage (4.8V).
- $\mathbf{V_{shift}}$ = Level shifted voltage fed to the ADC.
- **Ratio** = Ratio of the Level shifted voltage to the ADC reference voltage.
- $\mathbf{HexValue_{10}}$ = Digitized final ADC output value.

4.4.1.1 Threshold Setting

The first example covers the conversion from an analog voltage ($\mathbf{V_{cell}}$) to its corresponding digital value as if setting a voltage threshold register.

1. Voltage Division

First scale the input voltage by multiplying it by the ratio of 3/8.

$$V_{shift} = V_{cell} \times \frac{3}{8}$$

$$1.44375 = 3.85 \times \frac{3}{8}$$

2. Ratio of voltage to V_{ref}

Calculate the ratio of the measured voltage to V_{ref}.

$$Ratio = \frac{V_{shift}}{V_{ref}}$$

$$0.8020834 = \frac{1.44375}{1.8}$$

3. Ratio to 12-bit value

Finally convert this ratio to a 12-bit decimal value by multiplying it by the 12-bit maximum value.

$$HexValue_{10} = Ratio \times (2^{12} - 1)$$

$$3285 = 0.8020834 \times 4095$$

4.4.1.2 ADC Reading

The second example covers the conversion from a digital value to a voltage as if reading a voltage measurement result from a data register.

1. 12-bit value to Ratio

Take the digitized value and divide it by the maximum digital value possible (rounding has occurred below and was required due to the quantization error inherent to all ADCs).

$$Ratio = \frac{HexValue_{10}}{(2^{12} - 1)}$$

$$0.8020834 = \frac{3285}{4095}$$

2. Voltage derived from V_{ref} and Ratio

Use this value to derive the scaled voltage from the reference voltage.

$$V_{shift} = Ratio \times V_{ref}$$

$$1.44375 = 0.8020834 \times 1.8$$

3. Reverse Level Shifted voltage

Divide by the scaled ADC input level by the value of the scaler (or multiply by its inverse).

$$V_{cell} = \frac{Vshift}{\left(\frac{3}{8}\right)}$$

$$3.85 = 1.44375 \times \frac{8}{3}$$

4.4.1.3 Cell Voltage Formula

Putting the information in the above steps together gives the final formulas for conversion between Analog and Digital values for Cell voltages.

To calculate a register threshold from a desired voltage setting use:

$$HexValue_{10} = \frac{V_{meas} \times 3 \times 4095}{1.8 \times 8}$$

To calculate a voltage from a measured value or threshold setting use:

$$V_{meas} = \frac{HexValue_{10} \times 1.8 \times 8}{4095 \times 3}$$

4.4.2 0x8A-8B CELMIN

The V_{CELL} Minimum registers store the lowest measured cell voltage from the last cell voltage system scan. The data is split between two registers. The upper 4 bits of the CELMIN result are stored in the lower 4 bits of 0x8B while the remaining 8 bits are stored in 0x8A as shown in Table 61. The upper 4 bits of register 0x8B are reserved and should be ignored on read.

Table 61. CELMIN

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x8A	CELMIN7	CELMIN6	CELMIN5	CELMIN4	CELMIN3	CELMIN2	CELMIN1	CELMIN0
0x8B	RSV	RSV	RSV	RSV	CELMINB	CELMINA	CELMIN9	CELMIN8

The formula to convert the register decimal value to voltage is:

$$Cell_v = \frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

For more information on cell measurements, see “VCn Pins” on page 94.

4.4.3 0x8C-8D CELMAX

The V_{CELL} Maximum registers store the highest measured cell voltage from the last cell voltage system scan. The data is split between two registers. The upper 4 bits of the CELMAX result are stored in the lower 4 bits of 0x8D while the remaining 8 bits are stored in 0x8C as shown in Table 62. The upper 4 bits of register 0x8D are reserved and should be ignored on read.

Table 62. CELMAX

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x8C	CELMAX7	CELMAX6	CELMAX5	CELMAX4	CELMAX3	CELMAX2	CELMAX1	CELMAX0
0x8D	RSV	RSV	RSV	RSV	CELMAXB	CELMAXA	CELMAX9	CELMAX8

The formula to convert the register decimal value to voltage is:

$$Cell_v = \frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

For more information on cell measurements, see “VCn Pins” on page 94.

4.4.4 0x8E-8F IPACK

The Pack current measurement result registers store the voltage measured across the current sense resistor from the last system scan. The data is split between two registers. The upper 4 bits of the IPACK result are stored in the lower 4 bits of 0x8F while the remaining 8 bits are stored in 0x8E as shown in Table 63. The upper 4 bits of register 0x8F are reserved and should be ignored on read.

Table 63. IPACK

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x8E	IPACK7	IPACK6	IPACK5	IPACK4	IPACK3	IPACK2	IPACK1	IPACK0
0x8F	RSV	RSV	RSV	RSV	IPACKB	IPACKA	IPACK9	IPACK8

The value in this register is only valid if either “0x82.2 CHING” on page 77 or “0x82.3 DCHING” on page 76 bit is set. If neither of these bits are set, the value in this register is invalid and must be ignored.

The formula to convert the register decimal value to current is:

$$Current_A = \frac{HEXvalue_{10} \times 1.8}{4095 \times Gain \times R_{sense}}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86 and “0x85.[5:4] CG” on page 79.

For more information on IPACK measurements, see “CSI1-2 Pins (47, 48)” on page 111.

4.4.5 0x90-9F VCELL1-8

The V_{CELL} registers store the cell voltage measurement result from the last cell voltage system scan. The data is split between two registers. The upper 4 bits of the V_{CELL} result are stored in the lower 4 bits of 0x9x while the remaining 8 bits are stored in 0x9(x-1) as shown in Table 64. The full set of V_{CELL} registers are listed in Table 2. The upper 4 bits of register 0x9x are reserved and should be ignored on read.

Table 64. VCELLx

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x90	$V_{CELL1}7$	$V_{CELL1}6$	$V_{CELL1}5$	$V_{CELL1}4$	$V_{CELL1}3$	$V_{CELL1}2$	$V_{CELL1}1$	$V_{CELL1}0$
0x91	RSV	RSV	RSV	RSV	$V_{CELL1}B$	$V_{CELL1}A$	$V_{CELL1}9$	$V_{CELL1}8$
-	-	-	-	-	-	-	-	-
0x9E	$V_{CELL8}7$	$V_{CELL8}6$	$V_{CELL8}5$	$V_{CELL8}4$	$V_{CELL8}3$	$V_{CELL8}2$	$V_{CELL8}1$	$V_{CELL8}0$
0x9F	RSV	RSV	RSV	RSV	$V_{CELL8}B$	$V_{CELL8}A$	$V_{CELL8}9$	$V_{CELL8}8$

The cell must be selected (set to 1) in register “0x49 Cell Select” on page 67 for the V_{CELL} data register(s) to update during system scans. If the cell is not enabled, it is not measured and the value in the register is invalid.

The formula to convert the register decimal value to cell voltage is:

$$Cell_V = \frac{HEXvalue_{10} \times 1.8 \times 8}{4095 \times 3}$$

The equation constants are detailed in “0x8A-AB Data Registers” on page 86.

For more information on cell measurements, see “VCn Pins” on page 94.

4.4.6 0xA0-A1 ITEMP

The I_{TEMP} registers store the internal temperature voltage measurement result from the last system scan. The data is split between two registers. The upper 4 bits of the I_{TEMP} result are stored in the lower 4 bits of 0xA1 while the remaining 8 bits are stored in 0xA0 as shown in Table 65. The upper 4 bits of register 0xA1 are reserved and should be ignored on read.

Table 65. ITEMP

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0xA0	IT7	IT6	IT5	IT4	IT3	IT2	IT1	IT0
0xA1	RSV	RSV	RSV	RSV	ITB	ITA	IT9	IT8

The I_{TEMP} voltage is not scaled so the 3/8 factor is not part of the formula to convert the register decimal value to voltage as the following shows:

$$Temp_V = \frac{HEXvalue_{10} \times 1.8}{4095}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

The formula for converting from voltage (V) to temperature (C) is:

$$ITemp = \frac{(Temp_V) \times 1000}{1.8527} - 273.15$$

4.4.7 0xA2-A5 XT1-2

The External Temperature 1 and 2 registers store the voltage measurement results from the last system scan at the device "Thermistor Pins (20-22)" on page 96. The data for each of the two pins is split between two pairs of registers. The upper 4 bits of the xT1 (xT2) result are stored in the lower 4 bits of 0xA3 (0xA5) while the remaining 8 bits are stored in 0xA2 (0xA4) as shown in Table 65. The upper 4 bits of registers 0xA3 and 0xA5 are reserved and should be ignored on read.

Table 66. EXT1

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0xA2	XT17	XT16	XT15	XT14	XT13	XT12	XT11	XT10
0xA3	RSV	RSV	RSV	RSV	XT1B	XT1A	XT19	XT18
0xA4	XT27	XT26	XT25	XT24	XT23	XT22	XT21	XT20
0xA5	RSV	RSV	RSV	RSV	XT2B	XT2A	XT29	XT28

The formula to convert the register decimal value to voltage is:

$$Temp_V = \frac{HEXvalue_{10} \times 1.8}{4095}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

The conversion from voltage to temperature is a function of the thermistor and external circuitry used. For more information on external temperature measurement, see "Thermistor Pins (20-22)" on page 96.

4.4.8 0xA6-A7 VBATT

The V_{BATT} registers store the voltage measurement results from the last system scan. The data is split between two registers. The upper 4 bits of the V_{BATT} result are stored in the lower 4 bits of 0xA7 while the remaining 8 bits are stored in 0xA6 as shown in Table 67. The upper 4 bits of register 0xA7 are reserved and should be ignored on read.

Table 67. VBATT

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0xA6	VBATT7	VBATT6	VBATT5	VBATT4	VBATT3	VBATT2	VBATT1	VBATT0
0xA7	RSV	RSV	RSV	RSV	VBATTB	VBATTA	VBATT9	VBATT8

The V_{BATT} voltage presented to the ADC for measurement is divided by 32 between the "VBATT Pin (48)" on page 113 and VSS. The formula to convert the register decimal value to voltage is:

$$VBATT_V = \frac{HEXvalue_{10} \times 1.8 \times 32}{4095}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

4.4.9 0xA8-A9 VRGO

The V_{RGO} registers store the voltage measurement results from the last system scan. The data is split between two registers. The upper 4 bits of the V_{RGO} result are stored in the lower 4 bits of 0xA9 while the remaining 8 bits are stored in 0xA8 as shown in Table 67. The upper 4 bits of register 0xA9 are reserved and should be ignored on read.

Table 68. VRGO

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0xA8	VRGO7	VRGO6	VRGO5	VRGO4	VRGO3	VRGO2	VRGO1	VRGO0
0xA9	RSV	RSV	RSV	RSV	VRGOB	VRGOA	VRGO9	VRGO8

The V_{RGO} voltage presented to the ADC for measurement is divided by 2 between the "RGO Pin (36)" on page 99 and VSS. The formula to convert the register decimal value to voltage is:

$$VBATT_V = \frac{HEXvalue_{10} \times 1.8 \times 2}{4095}$$

The equation constants are detailed in "0x8A-AB Data Registers" on page 86.

4.4.10 0xAA-AB - ADCV

The 14-bit ADC Voltage register contains a 2's complement calibrated voltage output from the device ADC. In NORMAL Mode this reading is not usable because it cannot be associated with a specific monitored voltage. If a MCU takes control of scan operation then this reading becomes useful.

The data is split between two registers. The upper 6 bits of the ADCV result are stored in the lower 6-bits of 0xAB while the remaining 8 bits are stored in 0xAA as shown in Table 69. The upper 2 bits of register 0xAB are reserved and should be ignored on read.

Table 69. ADCV

Bit	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0xAA	ADCV7	ADCV6	ADCV5	ADCV4	ADCV3	ADCV2	ADCV1	ADCV0
0xAB	RSV	RSV	ADCVD	ADCVC	ADCVB	ADCVA	ADCV9	ADCV8

To use this register a MCU must take control of the system scan ("0x87.2 µCSCAN" on page 84), use register "0x85.[3:0] AO" on page 80, set the internal multiplexer to select the desired channel, and finally set the bit "0x85.6 ADCSTRT" on page 79 to trigger the ADC. The conversion result is found in this register.

The following are the formulas for converting from the register digital value to voltage:

$$HEXvalue_{10} \geq 8191 \rightarrow ADC_V = \frac{(HEXvalue_{10} - 16384) \times 1.8}{8191}$$

$$HEXvalue_{10} < 8191 \rightarrow ADC_V = \frac{HEXvalue_{10} \times 1.8}{8191}$$

5. Pin Function

5.1 VCn Pins

Pins VC0 - VC8 are the voltage sense inputs of the ISL94202, which are used by the device in pairs to sense the differential voltage across each cell. Positive pin VC_n and negative pin VC_{n-1} are connected to the ADC through a multiplexer. Each voltage sense input uses an external RC filter to minimize noise and protect against EMI and voltage transients. The filters carry the loop currents produced by EMI and should be placed as close to the battery connector as possible. Connect the ground terminals of the capacitors directly to a solid ground plane. Place any vias in line to the signal inputs so that the inductance of these forms a low pass filter with the grounded capacitors.

The filtered battery cell voltages internally connect to the cell voltage monitoring system. The monitoring system contains a multiplexer to select a specific input, and an analog-to-digital converter.

These pins should be connected to their respective cells as shown in Figure 38 on page 95 through a 1kΩ resistor, with a 47nF capacitor at the VC_n pin to the VSS ground plane ("VSS Pin (18, 28, 29)" on page 95).

Renesas recommends that capacitors connected to cells are fail safe or fail open types.

See "Reduced Cell Count" on page 150 for configuring the VC pins in applications with less than 8 cells.

5.2 CBn Pins

The Cell Balance pins, CB1 - CB8, are the cell balance driver outputs of the ISL94202. A combination of NMOS and PMOS FETs are driven by these pins to enable external cell balancing operation. The ISL94202 cell balancing outputs are current sources/sinks that are switched on and off to balance a cell. The cell balance FETs are driven by a current source (Cells 1-5) or sink (Cells 6-8) of 25µA, the simplified diagram is shown in Figure 38.

Cell balancing requires four external components; A cell balance FET, a gate-source resistor (180-330kΩ), an 10kΩ isolation resistor and a cell balance current setting resistor (R_2) in series with the FET drain.

Use the equation below to calculate the cell balance current:

$$I_{CB} = \frac{V_{CELL}}{(R_2 + R_{DSON})}$$

Set the gate-source resistor so the voltage does not exceed 7V. A Zener across the gate-source of the FET can be used to protect less robust FETs and the CBn pin from EOS in more severe environments.

The gate isolation resistor between the CBn pin and the balance FET gate serves primarily to protect the FET and the CBn pin. It limits the current spike that occurs during FET turn on, which is a function of the gate capacitance.

The CB pins can be controlled either externally from a MCU or by the ISL94202 automatically (default). Setting bit "0x87.5 µCCBAL" on page 83 to 1 gives the MCU control of the CB pins.

For more information, see "Cell Balancing" on page 122.

See "Reduced Cell Count" on page 150 for configuring the CB pins in applications with less than 8 cells.

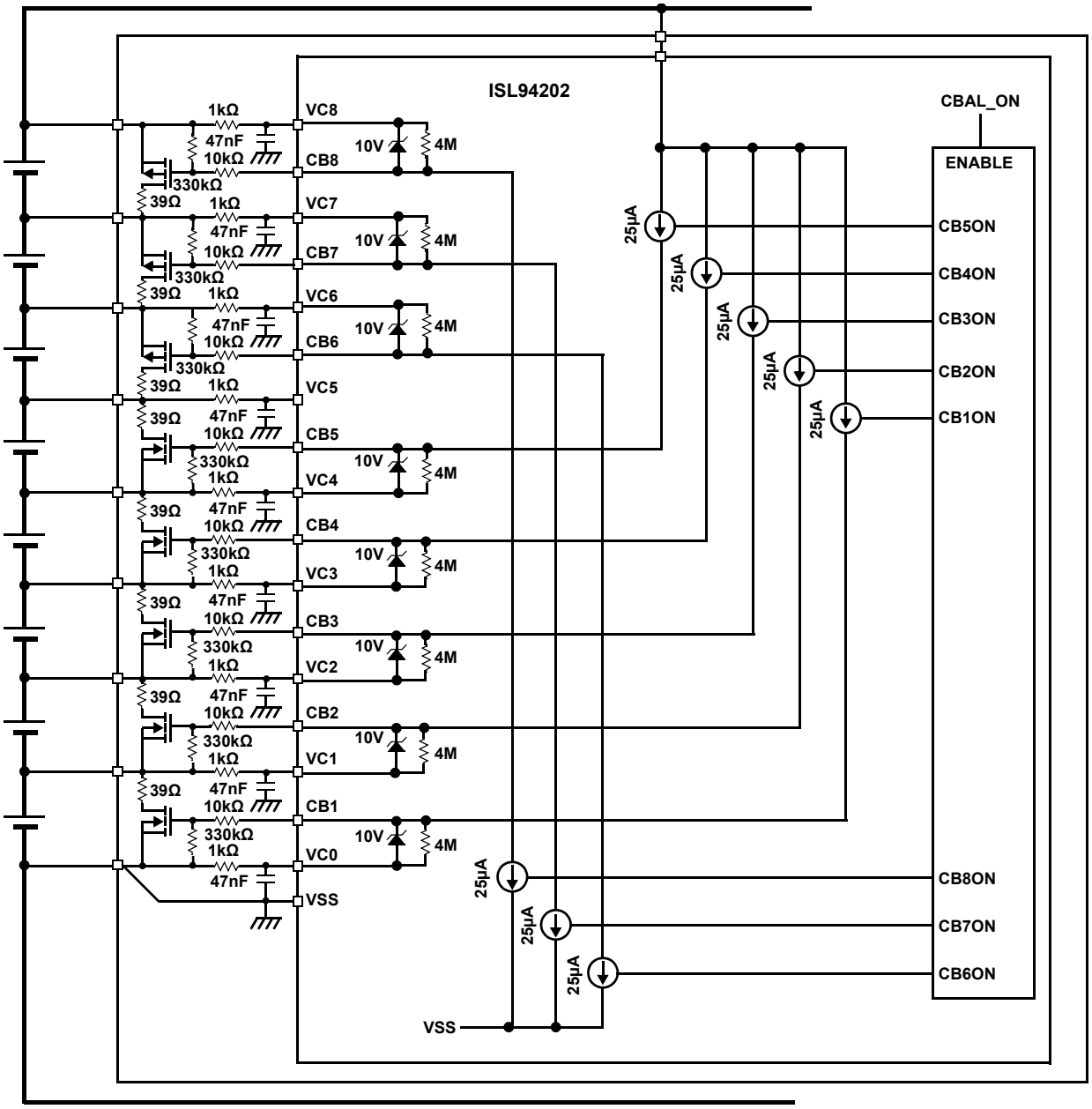


Figure 38. VCn/CBn and CB Drive Circuitry

Note: The internal 10V Zener is selected based on the device ESD diodes. It is not intended to limit the VGS of the external CB FET. It is an internal device that helps protect the pins from ESD/Latch-up/Hot plug, although the primary purpose is ESD protection.

5.3 VSS Pin (18, 28, 29)

VSS is the ISL94202 analog ground pin. It must have a solid connection to the ground plane(s). The digital and analog ground planes should connect together as close to the VSS pin Via as possible. The Exposed Pad (EPAD) on the bottom of the ISL94202 must also be tied to analog ground. Multiple Vias are recommended for good thermal conductivity.

5.4 VREF Pin (19)

The ISL94202 Reference Voltage pin is connected to the internal 1.8V reference used by the ADC. This pin should not be loaded as this could cause significant ADC error. The VREF pin should be connected to a 1µF capacitor connected to Analog GND.

There is a 6k resistor internal to the ISL94202 between the VREF Buffer and the ADC Reference input. The VREF pin is connected to this node so that the external cap completes the LPF for the ADC Ref input. A 0.5µA current pulled out of the VREF pin causes an error of 3mV on this node. This induces measurement errors on all ADC measurements. **WARNING:** Any noise on this node directly couples into the ADC and its measurements. With the exception of the external capacitor other connections to this pin are not recommended.

5.5 Thermistor Pins (20-22)

The ISL94202 monitors the internal temperature of the device ("0xA0-A1 ITEMP" on page 91) plus two external NTC thermistors ("0xA2-A5 XT1-2" on page 91). Three device pins are used for connections to external temperature measurement circuits; xT1, xT2, and TEMPO.

Pin xT1 (20) is dedicated to monitoring the battery pack temperature. Charge and discharge temperature faults are linked to the voltage at this pin. See "0x28-29 CBUT" on page 53 through "0x3E-3F DUTR" on page 61.

Pin xT2 (21) is configurable, it can monitor either pack temperature (default setting of "0x4A.5 XT2M" on page 68 to 0) or the temperature of the FETs by setting the bit XT2M to 1.

The TEMPO pin (22) supplies the bias voltage to the thermistors during measurement, it achieves this using an internal PMOS switch between RGO and TEMPO pins. The switch to the TEMPO pin is only turned on while temperature measurements are being taken to save power. Typical value is 2.45V (see "VTEMPO" on page 18).

When the MCU is in control of the scan ("0x87.2 µCSCAN" on page 84), the TEMPO pin is turned on when the analog MUX ("0x85.[3:0] AO" on page 80) for the ADC is set to read xT1 or xT2.

The temperature voltages have two selectable gain settings ("0x4A.4 TGAIN" on page 68) applied to both pins. Setting the TGain bit = 0 (default) sets the gain to 2x, providing for a full scale input voltage = 0.9V. The device is calibrated at the default temperature gain setting of 2x, this is the preferred setting because it produces a more linear temperature response. Using TGain = 1 sets the gain to 1 and is not recommended. The external voltage reading as a function of temperature in the default configurations given in Figure 39 are shown in Table 70.

Table 70. xT Pin Voltage vs Temperature and Configuration

TGain = 0			
TEMP (°C)	R_{Therm} (Ω)	$R_{Parallel}$ (Ω)	xTn (V)
-40	195652	9514	0.7396
0	27219	7313	0.6112
25	10000	5000	0.4537
50	4161	2938	0.2887
80	1669	1430	0.1495

TGain = 1		
TEMP (°C)	R_{Therm} (Ω)	xTn (V)
-40	195652	1.7233
0	27219	0.6078
25	10000	0.2649
50	4161	0.1176
80	1669	0.0486

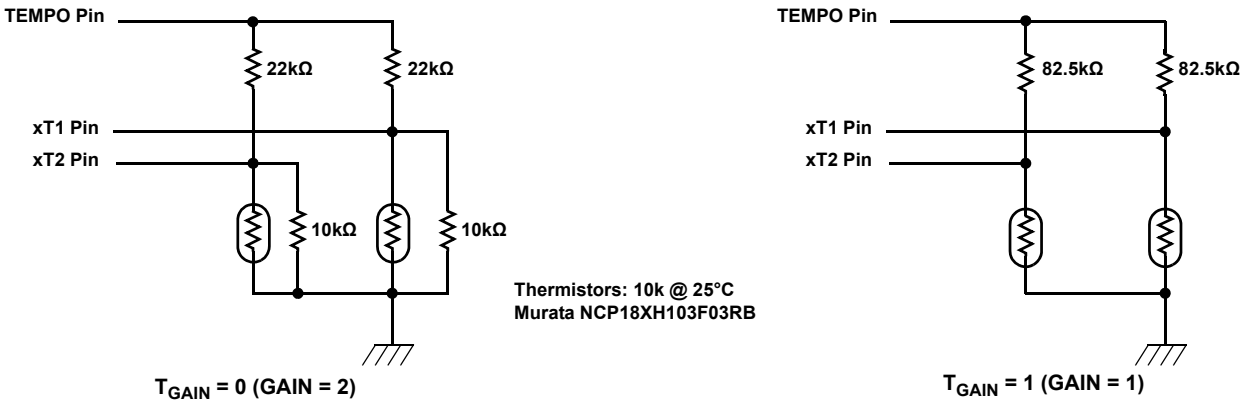


Figure 39. External Temperature Circuits

5.6 ADDR Pin (24)

The serial address pin is logically tied to the LSB of the ISL94202 7-bit device “I2C Address” on page 141.

If the address pin is tied to “RGO Pin (36)” on page 99, the LSB of the ISL94202 7-bit address is a 1, giving a 7-bit device address of b0101001.

If the address pin is tied to digital GND, the LSB of the ISL94202 7-bit address is a 0, giving a 7-bit device address of b0101000.

Appending the 8th bit of the address, the read or write bit, provides the address matrix shown in Table 79 on page 141.

This pin should not float, either tie it to RGO or digital GND (no resistor is needed).

5.7 SCL Pin (25)

The serial clock pin is the I2C clock pin driven by the master for I2C communications. A pull up to RGO of between 4.7kΩ to 10kΩ is recommended.

Note: The I2C pins should not be driven externally while the device is in the Powerdown State, this can back-feed into the RGO pin and partially power the device logic into an unknown state.

5.8 SDAI/O Pins (26, 27)

The ISL94202 uses a standard I2C interface though it separates the input and output data interfaces onto two pins. Input data is clocked in on SDAI (from MCU to ISL94202), and output data is clocked out on SDAO (from ISL94202 to MCU). These pins should be tied together to form a standard I2C SDA signal. A pull up to RGO of 4.7kΩ to 10kΩ is recommended.

Note: The I2C pins should not be driven externally while the device is in the Powerdown State, this can back-feed into the RGO pin and partially power the device logic into an unknown state.

5.9 $\overline{\text{INT}}$ Pin (31)

The Interrupt pin is a CMOS type push-pull output that is active low and is used when there is a MCU connected to the ISL94202. This pin is only active if one or more of the MCU override bits are set to 1.

The MCU override bits are:

- µCFET - “0x87.6 µCFET” on page 82
- µCCBAL - “0x87.5 µCCBAL” on page 83
- µCLMON - “0x87.4 µCLMON” on page 83
- µCCMON - “0x87.3 µCCMON” on page 83
- µCSCAN - “0x87.2 µCSCAN” on page 84

If there is no communication within the watchdog timeout period (see “0x47.[7:3] WDT” on page 65), $\overline{\text{INT}}$ is asserted. If a timeout occurs, all CB outputs and power FETs are turned off (see “CBn Pins” on page 94 and “Power FET Pins (42, 44, 45)” on page 107).

The device pulses the $\overline{\text{INT}}$ pin low for 1µs at a rate of 1Hz until the MCU responds. While the MCU does not respond, the part operates normally except no FETs (CB or power) are allowed to turn on. The device remains in this condition until an I2C transaction occurs.

When I2C communications resumes, bits µCLMON, µCCMON, µCSCAN, µCFET, and EEEN (“0x89.0 EEEN” on page 85) are cleared. µCCBAL remains set. The system scans resume on the next I2C transaction.

The CB outputs and power FETs turn back on, if conditions allow.

If the $\overline{\text{INT}}$ pin is unused, it can float as no connections are required.

5.10 PSD Pin (32)

The Pack Shutdown pin is an output indicator that the pack has encountered a fatal error. This pin goes active high when any cell voltage reaches the threshold “0x08-09 V_{CELL} OVLO” on page 38.

The PSD pin can optionally be configured to operate in two other fail conditions; Cell Fail (“0x4A.7 CELLF PSD” on page 67) and Open-Wire Fail (“0x4A.0 OWPSD” on page 68).

The PSD output remains active as long as the fault conditions exist, it is not latched. A momentary fault condition results in a PSD pulse. A continuous fault condition results in a continuous output. This pin is intended to be used with external circuitry to blow a fuse or as an interrupt to a MCU. If the PSD pin is unused, it can float as no connections are required.

5.11 FETSOFF Pin (33)

The FETs Off pin is an active high input that allows an external MCU to turn off both the cell balance outputs and the power FETs. This pin should be pulled up to RGO to turn the FETs off. The FETSOFF input is typically used when an external MCU is in control of the system scan and FETs. It provides a second method to quickly shut all FETs off in addition to writing to the FET control registers.

The logic circuitry of the FETSOFF input is composed of stacked 5V devices to tolerate a 5V MCU. There is an ESD diode to VRGO that turns on if the pin is pulled high enough above the RGO voltage (Therefore, the Abs Max of RGO + 0.5V). Given the 10k external resistor and a 200Ω internal resistance, if the resistors are pulled up to 5.5V, there is 3V across the resistors and ESD diode. If we assume all of the voltage is across the resistors, the current is <300µA.

For more information on MCU control, see:

- µCFET - “0x87.6 µCFET” on page 82
- µCCBAL - “0x87.5 µCCBAL” on page 83
- µCLMON - “0x87.4 µCLMON” on page 83
- µCCMON - “0x87.3 µCCMON” on page 83
- µCSCAN - “0x87.2 µCSCAN” on page 84

Figure 40 shows the timing relationship between the FETSOFF pin state and the C/DFET pins.

If the FETSOFF pin is unused, it should be connected to VSS with a 120kΩ resistor.

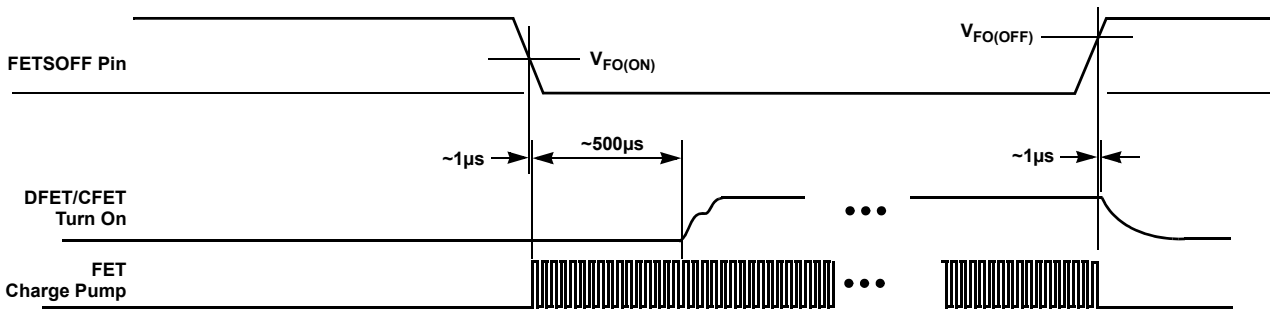


Figure 40. FETSOFF FET Control Timing

5.12 $\overline{SD}$ Pin (34)

The Shutdown pin is an output that indicates the ISL94202 detected any of the following fault conditions:

- Undervoltage - “VCELL UV” on page 37
- Discharge overcurrent - “0x16-17 DOC & DOCT” on page 43
- Discharge short-circuit - “0x1A-1B DSC & DSCT” on page 48
- Discharge over-temperature - “0x38-39 DOT” on page 59
- Discharge under-temperature - “0x3C-3D DUT” on page 61
- Internal over-temperature - “0x40-41 IOT” on page 62
- Charge overcurrent - “0x18-19 COC & COCT” on page 46

The pin also indicates if the FETS are off and the device is in SLEEP Mode. The $\overline{SD}$ pin is an open-drain output and should be pulled up to RGO with a high value resistor (1MΩ). If the $\overline{SD}$ pin is unused, it can float as no connections are required.

5.13 $\overline{EOC}$ Pin (35)

The End of Charge pin is an output which indicates that the ISL94202 has detected a fully charged condition. This is defined as any cell voltage exceeding the VEOC threshold (“0x0C-0D V_{CELL} EOC” on page 40) setting. The EOC pin output is open drain, the pin should be pulled up to RGO with a high value resistor (1MΩ).

If the $\overline{EOC}$ pin is unused, it can float as no connections are required.

5.14 RGO Pin (36)

The RGO pin is an external connection to the internal device digital voltage reference. It is intended to enable connection to the external decoupling capacitor and logic pull-ups. It has very limited external drive capability and no current sink capability. It is not intended to be driven externally.

RGO is always on, except when the device is in the Powerdown State.

5.15 CHMON Pin (37)

The Charge Monitor pin tests for a charger connection. In a series path configuration the CHMON pin connects through a resistor (499Ω) to the input of the positive charger connection as shown in Figure 41 on page 100 (commonly referred to as PACK+). This node may include the DFET source. In a split path configuration the CHMON pin connects through a resistor (499Ω) to the input of the positive charger connection as shown in Figure 42 on page 100 (commonly referred to as CHRG+). VGS diodes are omitted from the figures for clarity. This pin should not be tied to the LDMON pin and it should not share a resistor with LDMON.

The charge monitoring mechanism is different depending on what state the device is in. Two states exist for the charge monitoring mechanism.

The first state is recovery, which uses the CHMON recovery circuit described in “COC Recovery” on page 100 to recover from a COC condition (see “0x18-19 COC & COCT” on page 46).

The second state is wake-up, which functions to wake the device up when detecting a charger if the device is in “SLEEP Mode” on page 121 or “Mode Exceptions” on page 122. See “Charger Detection” on page 102.

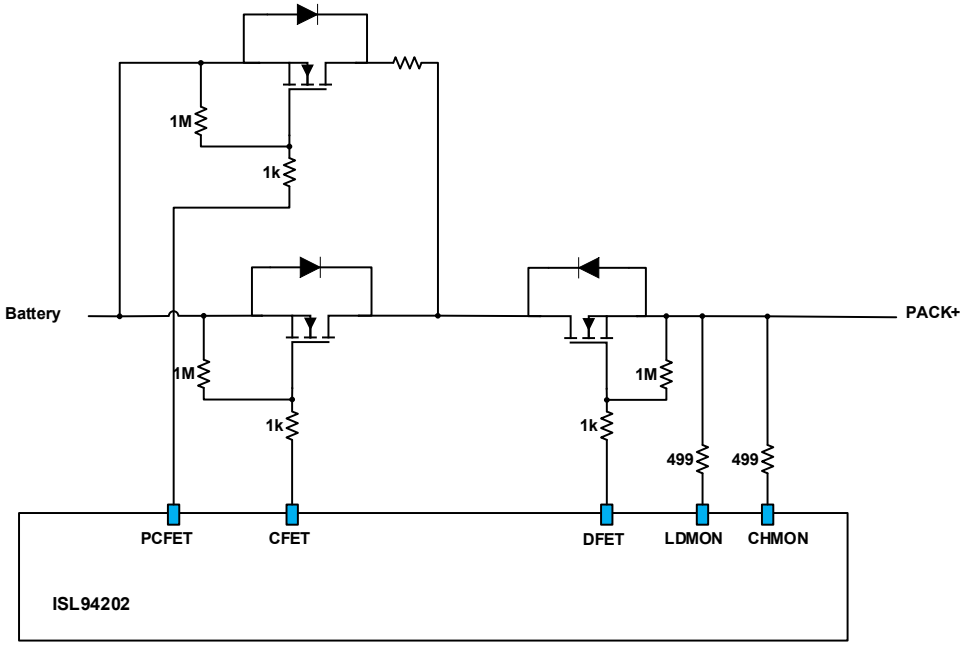


Figure 41. Series Path

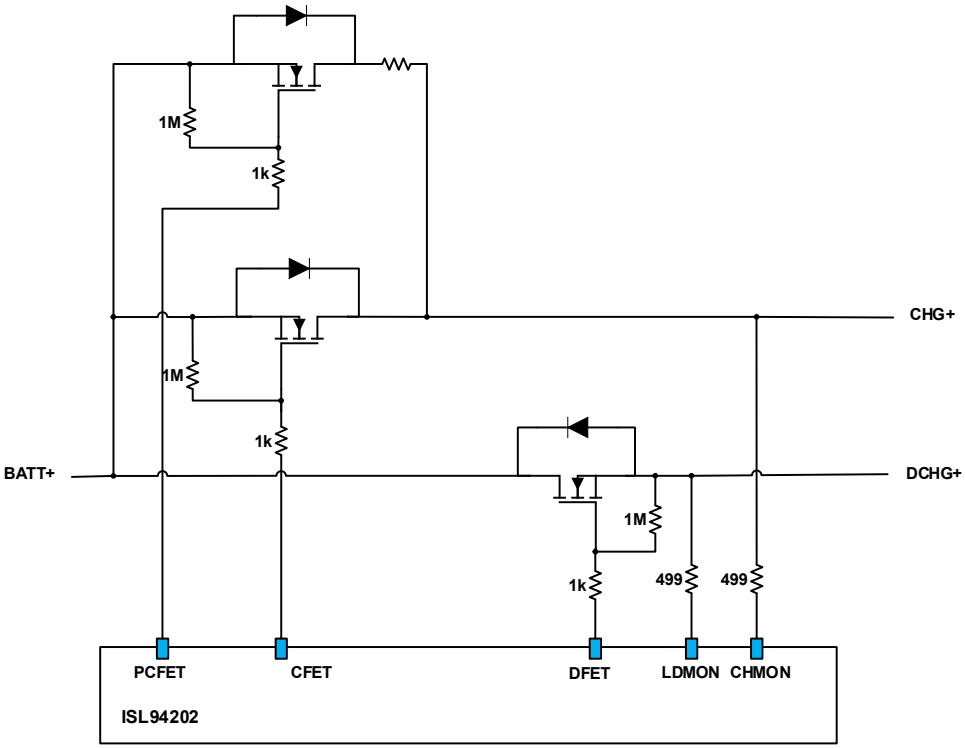


Figure 42. Parallel Path

5.15.1 COC Recovery

For a description of charge overcurrent and the recovery thresholds, see "0x19.[6:4] COC" on page 46 and "COCR" on page 47 respectively.

The COC (charge overcurrent) recovery circuit in Figure 43 shows a simplified view of the ISL94202 charge detection function.

For a charger to be detected (“0x82.1 CH_PRSNT” on page 77 = 1), the voltage at CHMON must be >9V. When the voltage at CHMON exceeds the threshold, the current is high enough (>~25µA) for the voltage of D1 and D2 to exceed the threshold of the comparator.

The bit CH_PRSNT clears (= 0) if the voltage at CHMON drops below 9V. When the voltage at CHMON is below the threshold, insufficient current flows to fully turn on diodes D1 and D2. This means the voltage at the positive input of the comparator drops below the band-gap voltage reference.

5.15.1.1 Automatic CHMON

After detecting a COC condition and “0x87.3 µCCMON” on page 83 is set to 0, the ISL94202 automatically enters recovery and periodically turns on the CHMON recovery circuit. The length of this pulse is set in register “0x01.7:4 CDPW” on page 36.

When a charger is not detected (“0x82.1 CH_PRSNT” on page 77 is 0), the device resets the COC bit (“0x81.1 COCF” on page 75) and returns to normal operation. If µCFET bit (“0x87.6 µCFET” on page 82) is 0, the FETs are automatically re-enabled (subject to all other safe operating conditions being met). If µCFET bit is 1, the MCU is responsible for re-enabling the FETs.

5.15.1.2 MCU CHMON

After detecting a COC condition and “0x87.3 µCCMON” on page 83 is set to 1, the MCU must perform recovery for the ISL94202 to return to normal operation.

The recommended recovery sequence is:

1. Write 1 to CMON_EN (“0x86.4 CMON_EN” on page 81).
2. Wait at least CDPW time (“0x01.7:4 CDPW” on page 36).
3. Read CH_PRSNT (“0x82.1 CH_PRSNT” on page 77).
4. If CH_PRSNT = 1, go back to Step 1. If CH_PRSNT = 0, set CLR_CERR bit (“0x86.5 CLR_CERR” on page 81) to 1 to clear the overcurrent condition fault bit. If µCFET bit (“0x87.6 µCFET” on page 82) is 0, the FETs are automatically re-enabled (subject to all other safe operating conditions being met). If µCFET bit is 1, the MCU is responsible for re-enabling the FETs.

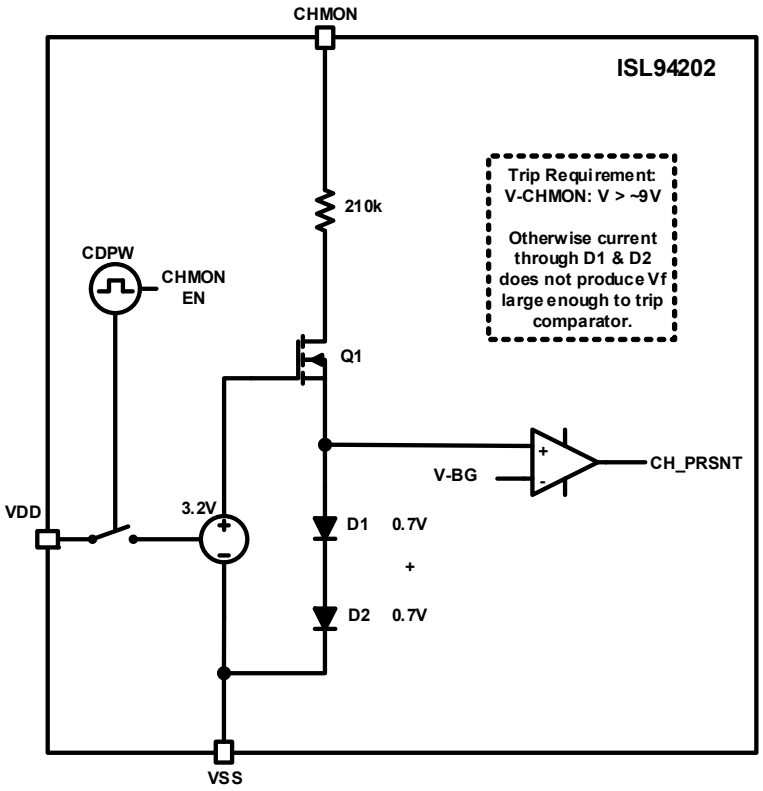


Figure 43. CHMON Recovery

5.15.2 Charger Detection

If the ISL94202 is in the "Powerdown State" on page 120, a charger connection must be used to wake the device up. If in "SLEEP Mode" on page 121, a charger or load connection can be used to wake the device up.

When entering SLEEP Mode (via "0x44-45 SLV" on page 64, "0x48.[3:0] IDLE/DOZE Timer" on page 66, or "0x88.2 SLEEP" on page 85), the ISL94202 keeps the wake-up circuit disabled for ~50ms. During this 50ms, the ISL94202 is in SLEEP Mode. After a ~50ms delay, the ISL94202 enables the "Load Detection" on page 105 and charger detection circuits. If a detection is made, the device exits SLEEP to NORMAL Mode. If after the 50ms period there is no load or charger detection, the wakeup circuit stays enabled and the device remains in SLEEP Mode (Figure 46). The circuit does not draw significant current (Figure 44).

Note: A load connection to CHMON while in SLEEP Mode also wakes the device.

It is important to be aware of the timing and voltage levels. If an application has a particularly large capacitive load with a slow discharge rate, there is a possibility that the voltage seen at the CHMON pin is large enough to prevent SLEEP as the voltage can trigger a false charger detection. Conversely, if the voltage at CHMON drops to ~0V to quickly (<50ms), this also stops the device from entering SLEEP as the ISL94202 detects a load connection. See Figure 45.

The charger detection voltage is >~9V (See "0x82.1 CH_PRSNT" on page 77).

The load detection voltage is <~0.7V (See "0x82.0 LD_PRSNT" on page 77).

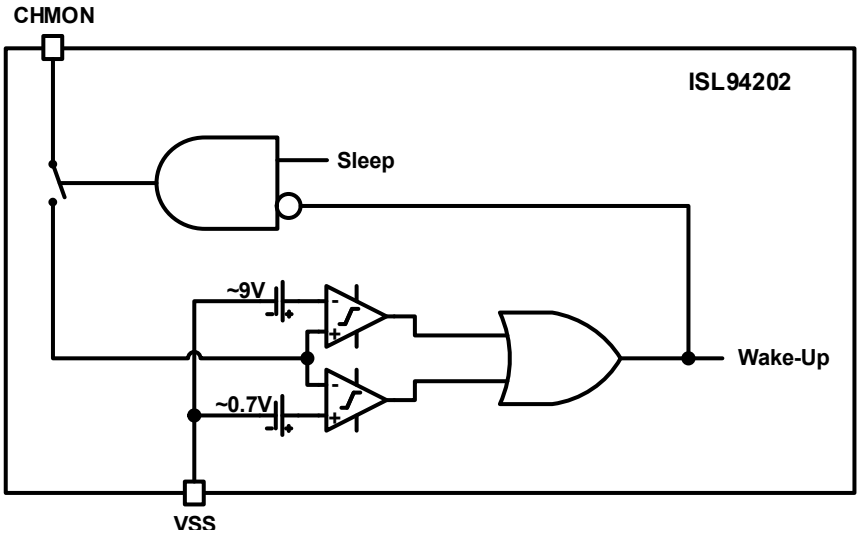


Figure 44. CHMON Wake Up

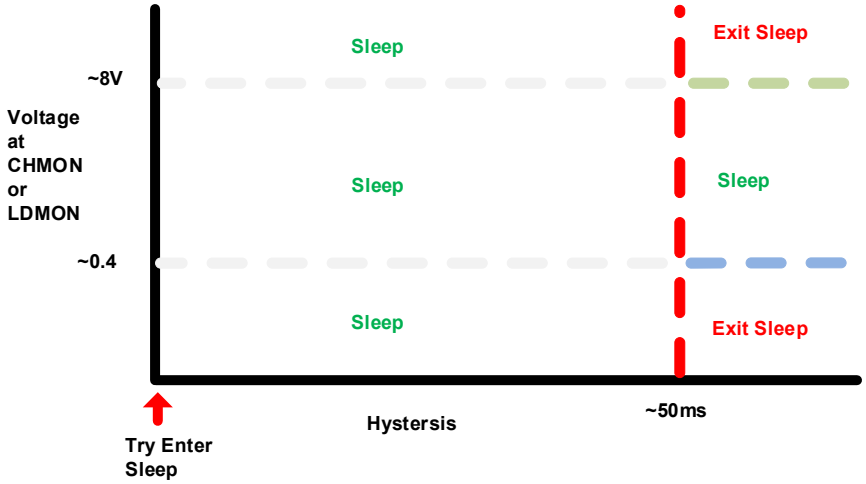


Figure 45. SLEEP Qualification

It is important to note that if the voltage after the ~50ms delay (shown in Figure 45) seen at either CHMON or LDMON is not between ~0.4V and ~8V, the device does not stay in SLEEP Mode. If there is a large load capacitance, it may be necessary to partially discharge this capacitor before the device sleeps. See the following section for operation relating to load detection.

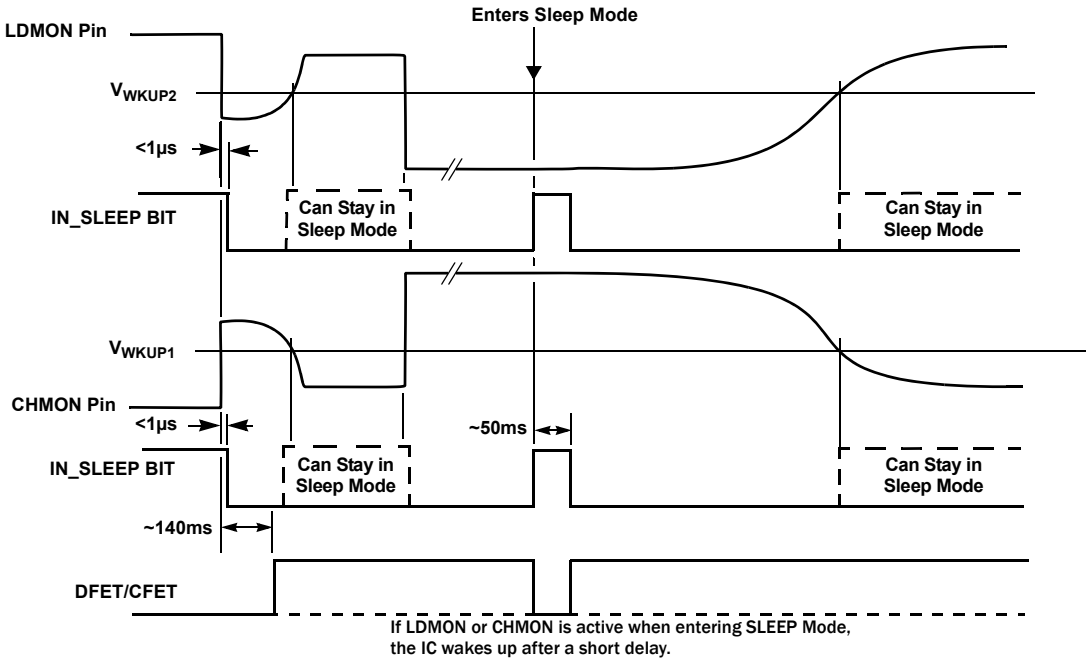


Figure 46. Wake-Up Timing (from SLEEP)

5.16 LDMON Pin (38)

The load monitor pin is designed to detect a connected load. In either a series (Figure 41) or split (Figure 42) path configuration the LDMON pin connects through a resistor (499Ω) to the positive output of the discharge path (commonly referred to as PACK+). This node may include the DFET source. This pin should not be tied to the CHMON pin and it should not share a resistor with CHMON.

The load monitoring mechanism is different depending on what state the device is in. Two states exist for load monitoring mechanism.

The first state is recovery, which uses the LDMON recovery circuit described in "DOC/DSC Recovery" on page 104 to recover from a DOC or DSC condition (see "0x16-17 DOC & DOCT" on page 43 or "0x1A-1B DSC & DSCT" on page 48, respectively). This method also applies to recovery from a cell voltage UV.

The second state is wake-up, which functions to wake the device up when detecting a load (Figure 46) if the device is in "SLEEP Mode" on page 121. See "Load Detection" on page 105.

Load detection does not bring a device out of the Powerdown State, but a detection of a charger and a load in Powerdown can result in the device waking into NORMAL Mode with the power FETs off. The load must be removed to recover, then the FETs are enabled.

5.16.1 DOC/DSC Recovery

The schematic in Figure 47 shows a simplified view of the Discharge Overcurrent and Discharge Short-Circuit (DOC & DSC) recovery circuit used to detect if a load was removed or is still attached.

For a load to be detected, the voltage at LDMON must be <0.4V. The ISL94202 forces ~62µA out of the LDMON pin, if an impedance of less than ~6.4kΩ is present between PACK+ and PACK-, the LDMON comparator detects and signals a load is present by setting LD_PRSNT = 1.

When the load is removed (impedance > ~6.4kΩ), the LDMON pin rises towards PACK+ and a load is not detected (LD_PRSNT = 0).

For a description of discharge overcurrent and recovery thresholds, see "0x17.[6:4] DOC" on page 44 and "DOCR" on page 45, respectively. For a description of discharge short-circuit and recovery thresholds, see "0x1B.[6:4] DSC" on page 48 and "DSCR" on page 49, respectively.

5.16.1.1 Automatic LDMON

After detecting a DOC or DSC condition, with “0x87.4 µCLMON” on page 83 set to 0, the ISL94202 automatically enters overcurrent recovery. This periodically enables LDMON load detection. The detection pulse width is set in register “0x05.7:4 LDPW” on page 37.

When a load is not detected (“0x82.0 LD_PRSNT” on page 77 is 0), the device resets the DOC and/or DSC bit (“0x81.2 DOCF” on page 74 & “0x81.3 DSCF” on page 74, respectively) and returns to normal operation. If the µCFET bit (“0x87.6 µCFET” on page 82) is 0, the FETs are automatically re-enabled (subject to all other safe operating conditions being met). If the µCFET bit is 1, the MCU is responsible for re-enabling the FETs, see the next section for details.

5.16.1.2 MCU LDMON

After detecting a DOC or DSC condition, with “0x87.4 µCLMON” on page 83 set to 1, the MCU must perform recovery for the ISL94202 to return to normal operation.

The following is the recommended recovery sequence:

1. Write 1 to “0x86.6 LMON_EN” on page 80.
2. Wait at least LDPW time (“0x05.7:4 LDPW” on page 37).
3. Read “0x82.0 LD_PRSNT” on page 77.
4. If LD_PRSNT = 1, go back to Step 1.

If LD_PRSNT = 0, set bit “0x86.7 CLR_LERR” on page 80 to 1 to clear the DOC & DSC fault bits. If the µCFET bit (“0x87.6 µCFET” on page 82) is 0, the FETs are automatically re-enabled (subject to all other safe operating conditions being met). If the µCFET bit is 1, the MCU is responsible for re-enabling the FETs.

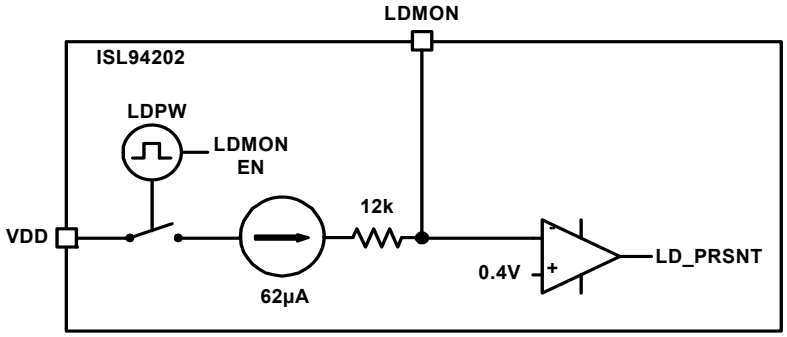


Figure 47. LDMON Recovery

5.16.2 Load Detection

If the device is in “SLEEP Mode” on page 121, a load connection can be used to wake the device up. A load connection does not wake the device from Powerdown, a charger connection is required.

When entering SLEEP Mode (using “0x44-45 SLV” on page 64, “0x48.[3:0] IDLE/DOZE Timer” on page 66, or “0x88.2 SLEEP” on page 85), the ISL94202 keeps the wake-up circuit disabled for ~50ms. During this 50ms, the ISL94202 is in SLEEP Mode. After a ~50ms delay, the ISL94202 enables the load detection and “Charger Detection” on page 102 circuits, if a detection is made, the device exits SLEEP to NORMAL Mode. If after the 50ms period there is no load or charger detection, the wakeup circuit stays enabled and the device remains in SLEEP Mode. The circuit does not draw significant current. See Figure 48.

Note: A charger connection to LDMON while in SLEEP Mode also wakes the device.

It is important to be aware of the timing and voltage levels. If an application has a particularly large capacitive load with a slow discharge rate, there is a possibility that the voltage seen at the CHMON pin is large enough to stop the device from sleeping as the ISL94202 detects a charger. Conversely, if the voltage at CHMON drops to ~0V to

quickly (<50ms), this also stops the device from entering SLEEP as the ISL94202 detects a load connection. See Figure 45.

The charger detection voltage is >~9V (See “Electrical Specifications” on page 13).

The load detection voltage is <~0.7V(See “Electrical Specifications” on page 13).

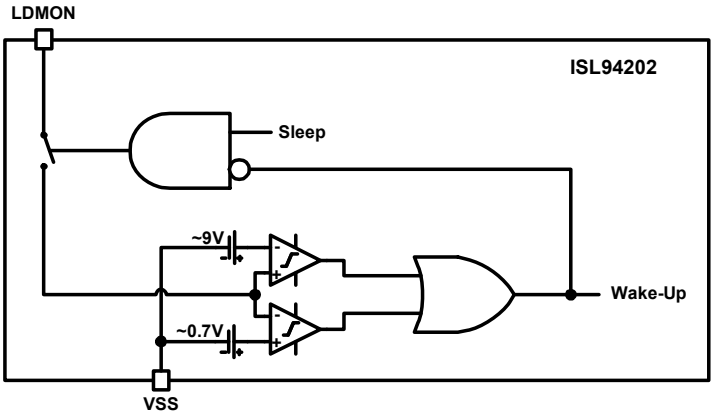


Figure 48. LDMON Wake Up

5.17 Cn Pins (39-41)

The ISL94202 includes an internal charge pump that uses two external capacitors connected to these three pins. The charge pump drives the power FETs (“Power FET Pins (42, 44, 45)” on page 107).

The ISL94202 is configured to drive high-side power FETs, these are located at the positive rail of the battery stack. A voltage higher than the battery pack must be provided to drive the NMOS power FET gates above their sources. The ISL94202 implements a charge pump to create this voltage. A charge pump is a switched capacitor circuit (the Cn Pins provide a way of connecting these capacitors externally). The charge pump of the ISL94202 can provide a voltage of approximately 2*VBATT (“CSI1-2 Pins (47, 48)” on page 111) in low cell count systems, but this is limited to ~VBATT+16V. For example, turn on and turn off times are given in Table 71.

In most applications 4.7nF is an acceptable charge pump capacitor value; however, Renesas recommends that the capacitors connected to these pins are 10-20 times the sum of the gate capacitance of the power FETs to be driven. Below is a diagram of how the Charge pump capacitors connect to the device pins.

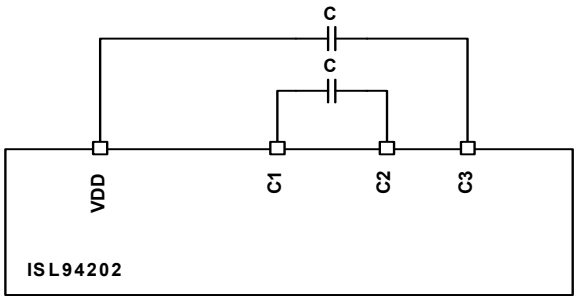


Figure 49. Charge Pump Capacitors (Cn pins)

5.18 VDD Pin (43)

The VDD pin is the supply voltage pin that provides the power connection for the ISL94202. This pin should be connected to the top of the pack through a low pass filter consisting of a <10Ω resistor and a 4.7µF capacitor to analog ground (“VSS Pin (18, 28, 29)” on page 95). In noisy environments the VDD pin filter time constant should match that of the VBATT pin, but with a smaller R and bigger C (~1µF) on VDD. If the voltage between VBATT and VDD is mismatched, the device measurement accuracy can be adversely affected in the presence of noise.

In low cell count systems it may be necessary to use a diode OR circuit if the pack voltage can drop below the POR threshold of the ISL94202. In this case, the device is unable to turn on the power FETs. The solution is to

connect one Schottky diode to route supply current from the top of the pack and a second one from the power FET common drain connections. The second diode supplies current when a charger is attached allowing the device to power up and enable the FETs, see Figure 50. Schottky diodes are necessary to keep VDD and VBAT pin voltages closely matched. VGS protection diodes omitted for clarity.

Route the PCB trace feeding the VDD pin from the top of the pack separately from other connections (VBATT and VC8) including the high current path feeding the power FETs.

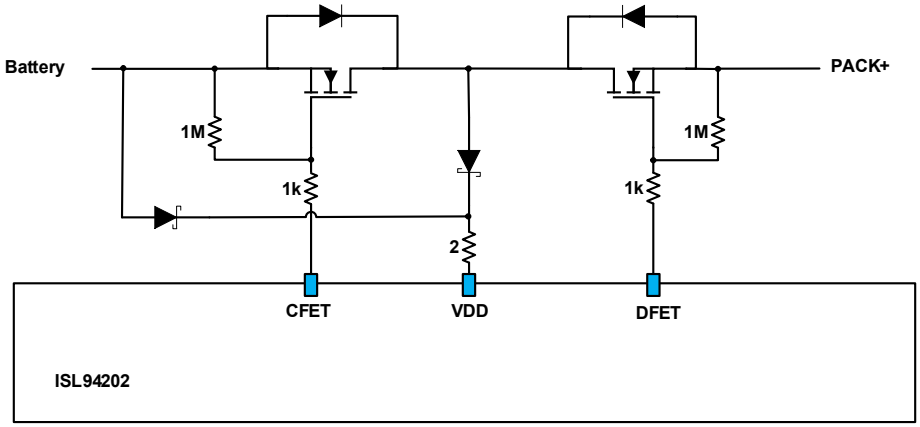


Figure 50. VDD Diode OR

5.19 Power FET Pins (42, 44, 45)

The Charge FET, Pre-Charge FET, and Discharge FET pins are driven above VBATT ("VBATT Pin (48)" on page 113) through an internal switch by the charge pump when enabled. These pins are analog outputs used to drive the power FETs only, they should not be driven by an external source and are should not be used to drive other loads. The power FETs can be arranged in either series (Figure 41) or parallel (Figure 42) configuration.

Charge pumps are charge transfer circuits that inherently cannot provide high drive current as their drive capability is a function of the charge pump capacitors ("Cn Pins (39-41)" on page 106), FET gate isolation resistor, and FET gate capacitance.

When any of the power FET pins ("DFET Pin (42)" on page 108, "CFET Pin (45)" on page 108, and "PCFET Pin (44)" on page 108) are turned on, the FET pin is connected to and driven by the charge pump voltage. Typical power FET gate control characteristics are listed in Table 71.

When the CFET or PCFET pins are turned off, the pin is internally connected to a current sink pulse of ~13mA for 300µs then allowed to float (high-Z). The current is routed from the CFET/PCFET pin and dumped out of the VBATT pin.

When the DFET is turned off, the DFET pin is internally connected to a current sink pulse of ~15mA for 300µs then allowed to float (high-Z). The current is routed from the DFET pin and dumped out of the "LDMON Pin (38)" on page 104.

Table 71. Power FET Gate Control

Parameter	Conditions	Typical
Power FET Gate Turn-On Current	DFET, CFET, PCFET Charge pump caps = 4.7nF	32kHz 5mA, pulses, 50% duty cycle
Power FET Gate Turn-On Time	10% to 90% of final voltage V_{DD} = 28V;	
	DFET, CFET = IRF1404	160µs
	PCFET = FDD8451	160µs
Power FET Gate Turn-Off Current	CFET, DFET, PCFET	13mA (CFET, PCFET) 15mA (DFET)
Power FET Gate Turn-Off Pulse Width	Pulse duration	300µs

Table 71. Power FET Gate Control (Continued)

Parameter	Conditions	Typical
Power FET Gate Fall Time	90% to 10% of final voltage V_{DD} = 28V;	
	DFET: IRF1404	6µs
	CFET: IRF1404	6µs
	PCFET: FDD8451	2µs

5.19.1 DFET Pin (42)

The Discharge FET pin is the voltage driver output designed to drive the discharge FET gate. Renesas recommends placing a 1kΩ isolation resistor between this pin and the DFET gate. Reducing this resistor value decreases the turn-on/off time of the power FETs, increasing the resistor slows down the turn-on/off of the power FETs.

Note: Care should be taken in selecting this value as turning off the FETs too quickly can cause them to be damaged by transients due to inductive kick back. Turning them off too slowly can lead to overheating of the power FETs.

Typical applications use single Zener diodes to clamp the VGS of the power FETS to within their operating range. In higher current applications with the potential for extreme transients, use back-to-back Zener protection diodes to limit the FET gate-to-source voltage and transient induced currents at the DFET pin. In either case, connect a large value resistor (~1MΩ) between the gate and source of the DFET. The resistor prevents the FET from turning on while in “SLEEP Mode” on page 121 or “Mode Exceptions” on page 122.

The most common conditions for DFET being enabled or disabled are shown in Tables 72 and 73.

When the MCU does FET control (“0x87.6 µCFET” on page 82 = 1), the DFET pin is controlled using bit “0x86.0 DFET” on page 82.

See Figures 41 and 42 for DFET connection information.

5.19.2 CFET Pin (45)

The Charge FET pin is the voltage driver output designed to drive the charge FET gate. Renesas recommends placing a1kΩ isolation resistor between this pin and the CFET gate. Reducing this resistor value decreases the turn-on/off time of the power FETs, increasing the resistor slows down the turn-on/off of the power FETs.

Note: Care should be taken in selecting this value as turning off the FETs too quickly can cause them to be damaged by transients due to inductive kick back. Turning them off too slowly may lead to overheating of the power FETs.

Typical applications use single Zener diodes to clamp the VGS of the power FETS to within their operating range. In higher current applications with the potential for extreme transients, use back-to-back Zener protection diodes to limit the FET gate-to-source voltage and transient induced currents at the CFET pin. The back-to-back diode also increases the device hot-plug voltage tolerance. In either case, connect a large value resistor (~1MΩ) between the gate and source of the CFET. The resistor prevents the FET from turning on while in “SLEEP Mode” on page 121 or “Mode Exceptions” on page 122.

The most common conditions for CFET being enabled or disabled are shown in Tables 72 and 73.

When the MCU does FET control (“0x87.6 µCFET” on page 82 = 1), the CFET pin is controlled using bit “0x86.1 CFET” on page 81.

See Figures 41 and 42 for CFET connection information.

5.19.3 PCFET Pin (44)

The Pre-Charge FET pin is the voltage driver output designed to drive the pre-charge FET gate. Renesas recommends placing a 1kΩ isolation resistor between this pin and the PCFET gate. A gate-to-source protection Zener diode should be used to protect the FET from EOS (electrical over-stress) and the PCFET pin from

transients. Connect a large value resistor (~1MΩ) between the gate and source of the PCFET. The resistor prevents the FET from turning on while in "SLEEP Mode" on page 121 or "Mode Exceptions" on page 122.

The most common conditions for PCFET being enabled or turned off are shown in Table 72 and Table 73.

When the MCU does FET control ("0x87.6 µCFET" on page 82 = 1), the PCFET pin is controlled using "0x86.2 PCFET" on page 81 and enabled using "0x4A.2 PCFETE" on page 68.

The PCFET pin exists to enable pre-charge of a pack near the lowest chargeable voltage, when the cell voltages have depleted to a point whereby a normal charge current causes stress on the cells. The ISL94202 enables this function by allowing you to place a FET with a series resistor that limits charge current in parallel with the CFET. With this configuration, if any cell voltage is found to be lower than the threshold Low Voltage Charge Level ("0x0E-0F V_{CELL} LVCL" on page 40), the PCFET output is turned on instead of CFET. The PCFET remains on until all cell voltages rise above the low voltage charge level at which time the ISL94202 automatically (assuming µCFET = 0) turns off the PCFET and turns on the CFET output.

The PCFET is optional and if unused the pin should be floated. To disable the PCFET function of the device, both of the following should be performed:

1. Set the Low Voltage Charge Level to 0V.
2. Set bit "0x4A.2 PCFETE" on page 68 to 0.

See Figures 41 and 42 for PCFET connection information.

5.19.4 Automatic FET Control

Automatic FET control is achieved by a state machine. This enables the ISL94202 to control the power FETs based on user programmed settings, thresholds and device measurements. Fully automatic FET control is active while "0x87.6 µCFET" on page 82 is clear (default).

Table 72 shows the automatic FET control matrix implemented by the ISL94202. See "0x0E-0F V_{CELL} LVCL" on page 40 and "0x4A.2 PCFETE" on page 68 for conditions specific to the PCFET.

Table 72. Automatic FET Control

Fault Condition	PCFET	CFET	DFET
"0x80.2 UVF" on page 72 = 1 and "0x4B.5 DFODUV" on page 69 = 0	EN	EN	OFF
"0x80.2 UVF" on page 72 = 1 and "0x4B.5 DFODUV" on page 69 = 1 and CHING 1	EN	EN	EN
"0x80.3 UVLOF" on page 72 = 1 with "0x4B.3 UVLOPD" on page 70 = 0	EN	EN	OFF
"0x80.3 UVLOF" on page 72 = 1 with "0x4B.3 UVLOPD" on page 70 = 1	OFF	OFF	OFF
"0x80.0 OVF" on page 73 = 1 and "0x4B.4 CFODOV" on page 69 = 0	OFF	OFF	EN
"0x80.0 OVF" on page 73 = 1 and "0x4B.4 CFODOV" on page 69 = 1 and DCHING 1	EN	EN	EN
"0x80.1 OVLOF" on page 73 = 1 (also shuts off "CBn Pins" on page 94)	OFF	OFF	EN
"0x81.1 COCF" on page 75 = 1	OFF	OFF	EN
"0x81.2 DOCF" on page 74 = 1	EN	EN	OFF
"0x81.3 DSCF" on page 74 = 1	OFF	OFF	OFF
"0x83.6 IN_SLEEP" on page 78 = 1	OFF	OFF	OFF
"Mode Exceptions" on page 122 (independent of other settings)	OFF	OFF	OFF
"0x82.7 LVCHG" on page 76 = 1 with "0x4A.2 PCFETE" on page 68 = 0	OFF	EN	EN
"0x82.7 LVCHG" on page 76 = 1 with "0x4A.2 PCFETE" on page 68 = 1	EN	OFF	EN
"FETSOFF Pin (33)" on page 98 = 1 (also shuts off "CBn Pins" on page 94)	OFF	OFF	OFF
"0x81.7 VEOC" on page 73 = 1 (also sets "EOC Pin (35)" on page 99)	EN	EN	EN
"0x81.0 IOTF" on page 75 = 1	OFF	OFF	OFF
"0x80.5 DUTF" on page 72 = 1, CHING or DCHING = 1 (See Note 11)	OFF	OFF	OFF

Table 72. Automatic FET Control

Fault Condition	PCFET	CFET	DFET
"0x80.4 DOTF" on page 72 = 1, CHING or DCHING = 1 (See Note 11)	OFF	OFF	OFF
"0x80.7 CUTF" on page 71 = 1, CHING = 1	OFF	OFF	EN
"0x80.7 CUTF" on page 71 = 1, DCHING = 1 (See Note 11)	EN	EN	EN
"0x80.6 COTF" on page 71 = 1, CHING = 1	OFF	OFF	EN
"0x80.6 COTF" on page 71 = 1, DCHING = 1 (See Note 11)	EN	EN	EN
"0x81.4 CELLF" on page 74 = 1 and/or "0x81.5 OWF" on page 74 = 1	OFF	OFF	OFF

Note:
11. Device assumes series connected FETs and the allowed cell charge temperature range is inside of the allowed discharge temperature range. This has no impact on the parallel configuration.

See "0x82.2 CHING" on page 77 and "0x82.3 DCHING" on page 76 for more information.

5.19.5 MCU FET Control

MCU FET control is achieved by setting bit "0x87.6 µCFET" on page 82 to 1. In this mode the MCU can turn the FETs ON or OFF under all conditions with the following exceptions:

- If there is a discharge short-circuit fault condition ("0x81.3 DSCF" on page 74), the ISL94202 turns the FETs off. The external MCU is responsible for clearing the fault and turning the FETs back on. The FETs can only be turned back on when the short-circuit condition clears, see "DSCR" on page 49.
- If there is an internal over-temperature condition ("0x81.0 IOTF" on page 75), the ISL94202 turns the FETs off. The external MCU is responsible for turning the FETs back on. The FETs can only be turned back on when the internal over-temperature condition clears, see "0x42-43 IOTR" on page 63.
- If there is an overvoltage lockout condition ("0x80.1 OVLOF" on page 73), the ISL94202 turns the charge and precharge FETs off. The external MCU is responsible for turning the FETs back on. The FETs can only be turned back on once the OVLO condition clears, see "0x02-03 V_{CELL} OVR" on page 36. This assumes that the "PSD Pin (32)" on page 98 has not been configured to blow a fuse to disable the pack.
- If there is an open-wire condition ("Open Wire" on page 126), the ISL94202 turns the power FETs off. The external MCU is responsible for turning the FETs back on. The FETs can only be turned back on when the open-wire condition clears. This assumes that the "PSD Pin (32)" on page 98 has not been configured to blow a fuse to disable the pack, see "0x4A.0 OWPSD" on page 68.
- If the FETSOFF input pin ("FETSOFF Pin (33)" on page 98) is pulled high, the power FETs turn off and remain off. The external MCU is responsible for turning the FETs on when the FETSOFF input pin is pulled low.
- On wake-up from "SLEEP Mode" on page 121 the MCU is responsible for turning on the power FETs.
- On wake-up from "Mode Exceptions" on page 122 the ISL94202 returns to automatic operation, the MCU is responsible for regaining control because all µC bits have been cleared.
- The MCU can also control the FETs by setting bit "0x87.2 µCSCAN" on page 84 to 1. However, this also stops the scan, requiring the MCU to manage scan operation. While the µCSCAN bit is set to 1, the only operations controlled by the ISL94202 are:
  - Discharge short-circuit FET control. The external MCU cannot override the turn off of the FETs during short-circuit.
  - FETSOFF external control. The FETSOFF pin has priority on control of the FETs, even when the MCU is managing the scan.

Table 73 shows the FET control matrix implemented by the ISL94202 if the MCU takes control of the power FETS by setting "0x87.6 µCFET" on page 82 to 1. See "0x0E-0F V_{CELL} LVCL" on page 40 and "0x4A.2 PCFETE" on page 68 for conditions specific to the PCFET.

Table 73. MCU FET Control

Condition	PCFET	CFET	DFET
"0x80.2 UVF" on page 72 = 1	µC Control	µC Control	µC Control
"0x80.3 UVLOF" on page 72 = 1	µC Control	µC Control	µC Control
"0x80.0 OVF" on page 73 = 1	µC Control	µC Control	µC Control
"0x80.1 OVLOF" on page 73 = 1	OFF	OFF	µC Control
"0x81.1 COCF" on page 75 = 1	µC Control	µC Control	µC Control
"0x81.2 DOCF" on page 74 = 1	µC Control	µC Control	µC Control
"0x81.3 DSCF" on page 74 = 1	OFF	OFF	OFF
"SLEEP Mode" on page 121 = 1	OFF	OFF	OFF
"Mode Exceptions" on page 122 (independent of other settings)	OFF	OFF	OFF
"0x82.7 LVCHG" on page 76 = 1	µC Control	µC Control	µC Control
"FETSOFF Pin (33)" on page 98 = 1	OFF	OFF	OFF
"0x81.7 VEOC" on page 73 = 1	µC Control	µC Control	µC Control
"0x81.0 IOTF" on page 75 = 1	OFF	OFF	OFF
"0x80.5 DUTF" on page 72 = 1	µC Control	µC Control	µC Control
"0x80.4 DOTF" on page 72 = 1	µC Control	µC Control	µC Control
"0x80.7 CUTF" on page 71 = 1	µC Control	µC Control	µC Control
"0x80.6 COTF" on page 71 = 1	µC Control	µC Control	µC Control
"0x81.4 CELLF" on page 74 = 1	µC Control	µC Control	µC Control
"0x81.5 OWF" on page 74 = 1	µC Control	µC Control	µC Control

5.20 CSI1-2 Pins (47, 48)

The Current Sense pins are the inputs to the ISL94202 current sense circuitry. This circuitry includes current direction detection, overcurrent monitoring, and current sense functions as shown in Figure 51 on page 112. The device requires an external resistor in series with the load/charge current to produce a measurable voltage.

The current monitoring circuit includes comparators for short-circuit and overcurrent detection along with current direction detection. This circuit is always on except in SLEEP and Powerdown Modes. The Current Monitoring blocks compare the voltage across the sense resistor to three thresholds. These are Discharge Short-Circuit ("0x1A-1B DSC & DSCT" on page 48), Discharge Overcurrent ("0x16-17 DOC & DOCT" on page 43), and Charge Overcurrent ("0x18-19 COC & COCT" on page 46). If the measured voltage exceeds the set threshold for the selected time duration, the ISL94202 acts to protect the system according to the device settings.

The DOC, COC, and DSC settings with their corresponding sense resistor and trip currents are given in Tables 15, 17,and 19 respectively.

The current direction detection block in Figure 51 controls the setting of the Charging ("0x82.2 CHING" on page 77) and Discharging ("0x82.3 DCHING" on page 76) register bits. There is a 2ms digital delay to set either direction bit. This means that the current direction detection circuit needs to detect an uninterrupted flow of current out of the pack for more than 2ms to indicate a discharge condition. Conversely, the current direction detection circuit needs to detect an uninterrupted flow of current into the pack for more than 2ms to indicate a charge condition. Finally, the current direction detection circuit needs to detect no current flow for 2ms to clear both charge and discharge conditions.

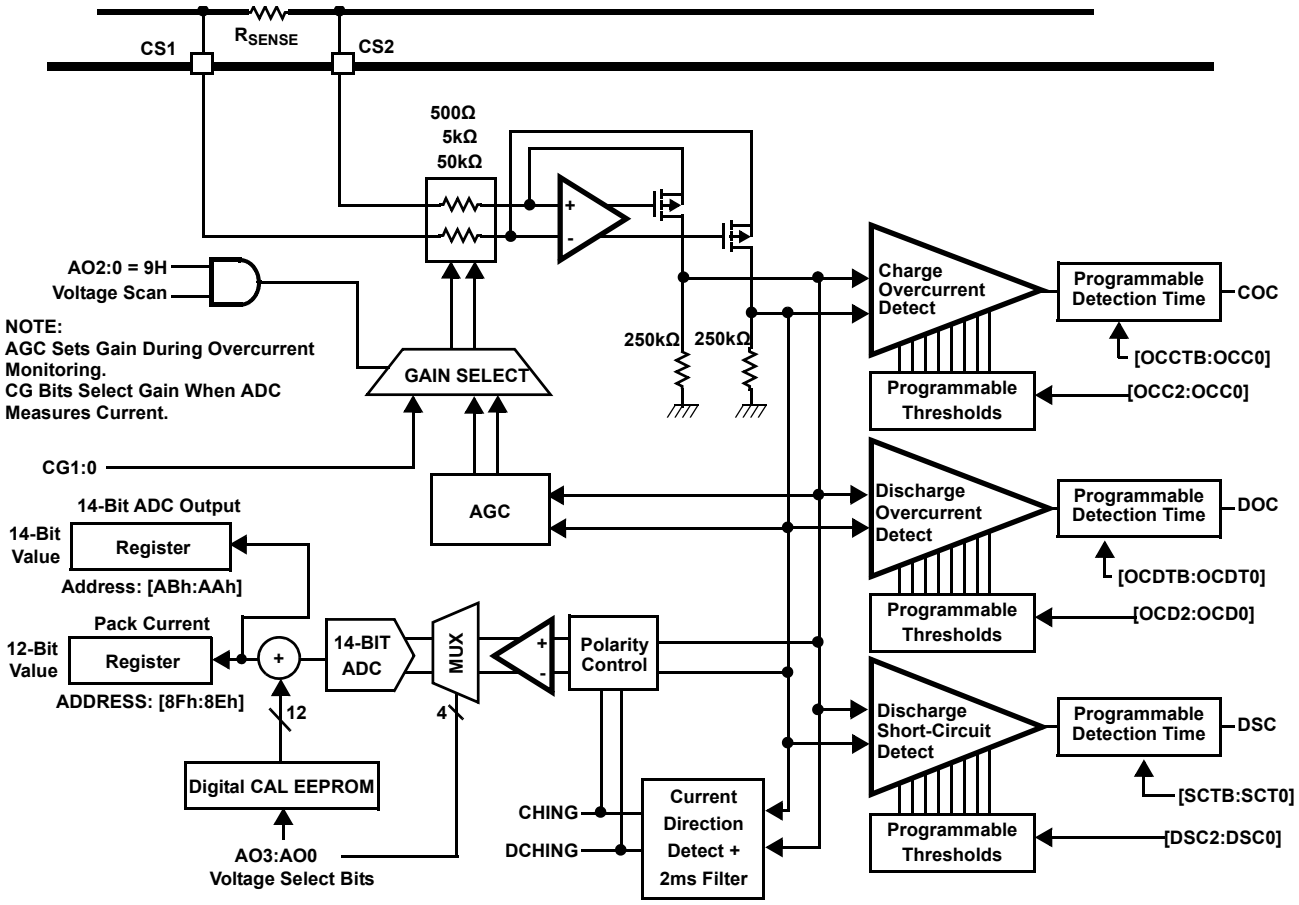


Figure 51. Current Sense

The measured current value in register "0x8E-8F IPACK" on page 90 is only valid if one of these bits is set.

The current sense circuit includes programmable gains (x5, x50, and x500) and a connection through the multiplexer to the ADC. The current-sense amplifier gain is set by the [CG1:CG0] bits ("0x85.[5:4] CG" on page 79). The result of the voltage measurement across the current-sense resistor is saved to the IPACK register. Current measurement ranges are given in Table 74 on page 112.

The recommended external current sense circuit is shown in Figure 52 on page 113.

Table 74. Maximum Current Measurement Range

Gain Setting	Voltage Range (mV)	Current Range (RSENSE = 1mΩ) (A)
5x	-250 to 250	-250 to 250
50x	-25 to 25	-25 to 25A
500x	-2.5 to 2.5	-2.5 to 2.5

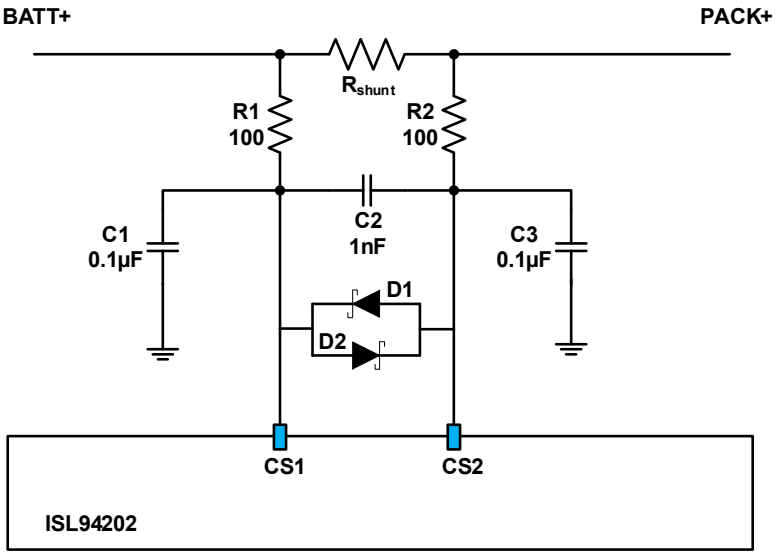


Figure 52. Current Sense Circuit

R_{shunt}: This is the current sense resistor used for measuring current and detecting overcurrent conditions. The maximum value is determined by the DSC Threshold (Table 19), while the minimum value is a function of the lowest currents in the normal operating range of the intended application.

R_1, C_1, R_2, C_3: These components form low pass filters on the current sense inputs. They improve measurement accuracy by filtering common mode noise and protect the pins against transients. Capacitors should tolerate at least 2x the fully charged pack voltage.

D_1, D_2: Schottky diodes protect the current sense pins from differential voltages beyond the tolerance level of the device.

R_1, R_2, C_2: These components form a low pass filter for differential mode noise.

5.21 VBATT Pin (48)

The VBATT pin powers the measurement input level shifter circuitry and is also used to monitor the voltage of the battery pack. The voltage is internally divided by 32 and connected to the ADC through an Analog MUX. This pin should be connected to the top of the pack through a low pass filter consisting of a 100Ω resistor and a 470nF capacitor to VSS ("VSS Pin (18, 28, 29)" on page 95).

In noisy environments, the VDD pin filter time constant should match that of the VBATT pin, but with a smaller R and bigger C (~1uF) on VDD. If the voltage between VBATT and VDD is mismatched, the device measurement accuracy can be adversely affected, particularly in the presence of noise.

Route the PCB trace connecting this pin to the battery pack separately from the high current path feeding the power FETs, VDD, and VC8.

6. System Operation

The ISL94202 is intended to be a stand-alone battery pack monitor; therefore, it provides monitor and protection functions without requiring an external MCU. The device provides configurable functions and behaviors that are tailored to the application. It operates power control FETs on the high side with a built-in charge pump for driving N-channel FETs. The current-sense function is also on the high side. To extend battery life, power is minimized in all areas with parts of the circuit powered down a majority of the time.

6.1 Power Up

When the ISL94202 is first connected to a battery pack, it is unknown which pins connect first or in what order. When the "VDD Pin (43)" on page 106 and "VSS Pin (18, 28, 29)" on page 95 connect, the device enters the Powerdown state. It remains in this state until a charger is connected. The device also powers up if the "CHMON Pin (37)" on page 99 is connected to the top of the pack through an outside resistor to enable PCB test. It is possible that the pack powers up automatically when the battery stack is connected due to momentary conduction through the power FET G-S and G-D capacitors.

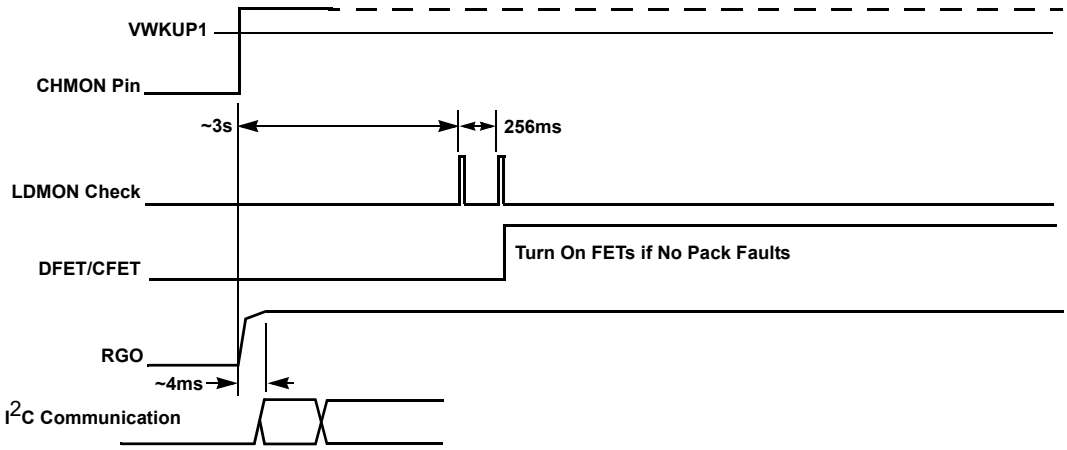


Figure 53. Power-Up Timing (from Power-Up/Shutdown)

When the charger connects (or CHMON connects), the internal power supply turns on. This powers up all internal supplies and starts the state machine. If some cells are not connected, the state machine recognizes this, either the monitored cell voltage reads zero when the register "0x49 Cell Select" on page 67 indicates that there should be a cell at that pin or through the open-wire test (see "Open Wire" on page 126). If the cell voltages do not read correctly, the ISL94202 remains in the POR loop until conditions are valid for power-up. It is for this reason that the factory default for the device is three cells. When manufacturing the application board, Cells 1, 2, and 8 must be connected to power up. If other cells are connected it is OK, but for the other cells to be monitored, the Cell Select register needs to be changed.

If the inputs all read good during this sequence (Figures 53 and 55), the state machine enters the normal monitor state. In the normal state, if all cell voltages read good and there are no overcurrent or temperature issues and there is no load, the FETs turn on. To determine if there is a load, the device does a load check. This operation waits for about 3s and then must see no load for two successive load monitor cycles (256ms apart).

During the POR operation, the configuration registers are all reset to default conditions from values saved in the EEPROM. See "System Registers" on page 32.

When the pack voltage drops, the ISL94202 remains on if the V_{DD} voltage remains above 1V and the VRGO voltage is above 2.25V. If a longer battery stack voltage drop occurs, the device returns to a Powerdown condition if V_{DD} drops below a POR threshold of ~3V when V_{RGO} is below 2.25V (see Figures 54 and 55).

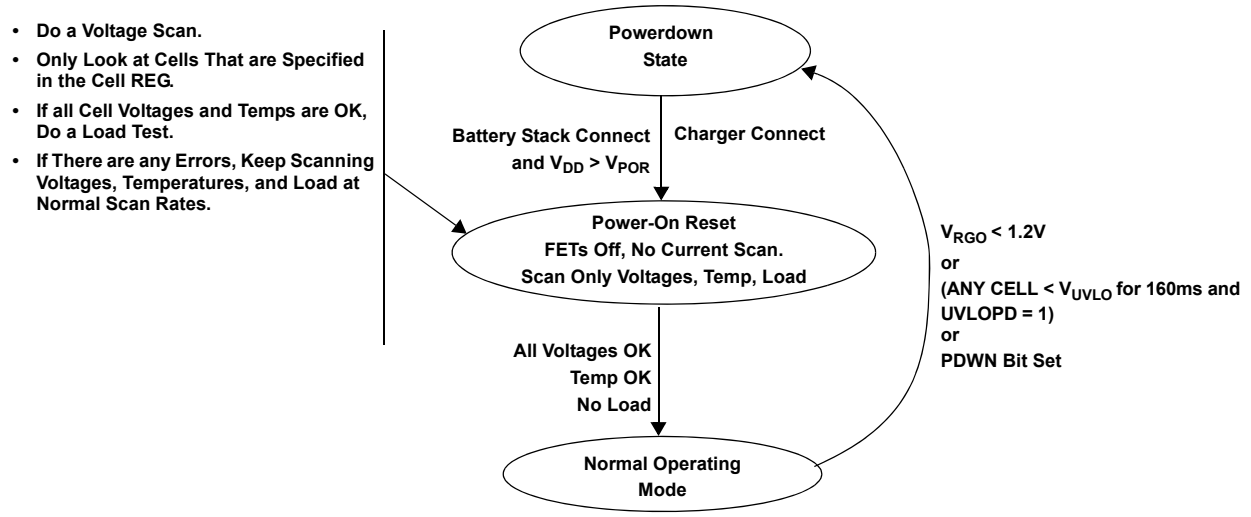


Figure 54. Power-On Reset State Machine

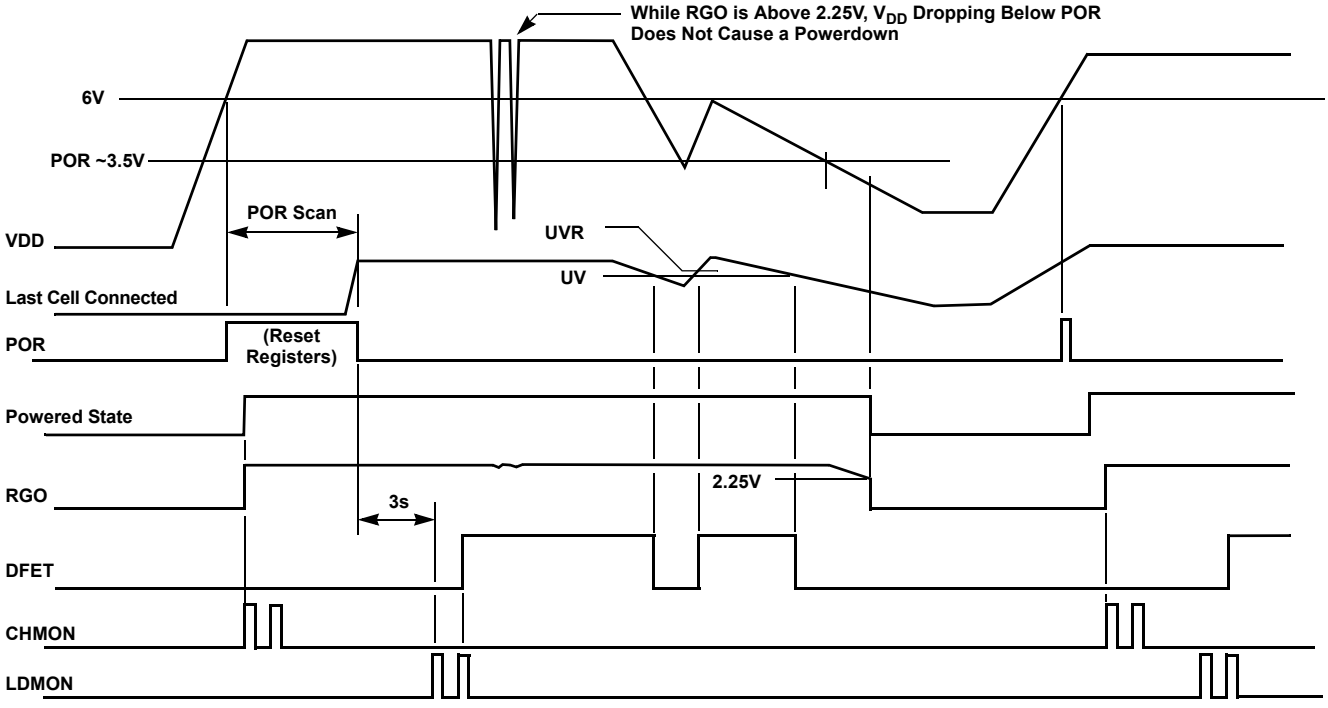


Figure 55. Power-Up/Powerdown Low Voltage Waveforms

6.2 Wake Up

When in "SLEEP Mode" on page 121, the ISL94202 monitors the "CHMON Pin (37)" on page 99 for a charger connection and the "LDMON Pin (38)" on page 104 for a load connection. A detection by either monitor wakes the device into "NORMAL Mode" on page 120.

A "Charger Detection" on page 102 occurs if the CHMON pin is pulled high, this happens when the charger is connected and the FETs are off. A charger detection is the only method to wake a device from the "Powerdown State" on page 120.

A "Load Detection" on page 105 occurs if the LDMON pin is pulled low when a load is attached to the pack and the FETs are off.

The first measurement scan starts 1.5ms after exiting SLEEP Mode. The type of scan is the special 4th cycle scan ("Automatic V, I, & T Scan" on page 117). The wake-up circuit does not draw significant continuous current from the battery.

6.3 System Scans

The ISL94202 executes two different automatic system scans, the "Automatic V & I Scan" on page 117 shown in Figure 57 and "Automatic V, I, & T Scan" on page 117 as shown in Figure 58. The V & I scan measures the cell voltages and pack current then compares them against the fault thresholds. The V, I, & T scan is executed every 4th scan, it includes the actions of the V & I scan plus additional voltages as indicated.

These system scans are applicable only when the device is in control of the scan, that is "0x87.2 µCSCAN" on page 84 is 0. The Open-Wire check is performed every 32nd scan if a "0x81.4 CELLF" on page 74 condition is flagged. The ISL94202 captures cell voltages using the circuit represented by the block diagram in Figure 56. When the µSCAN bit is 1, the external MCU must manually trigger measurements using register "0x85 Control 0 (R/W)" on page 79. This section covers automatic scan (µSCAN bit is 0), see "MCU Scan" on page 118 for the µSCAN = 1 case.

Following measurement (Figure 56), the cell voltages are stored in data registers and compared against the cell voltage thresholds "V_{CELL} OV" on page 35, "0x08-09 V_{CELL} OVLO" on page 38, "VCELL UV" on page 37, and "0x0A-0B V_{CELL} UVLO" on page 39. Violations of any of these threshold voltages set the related fault bit as indicated in the register descriptions.

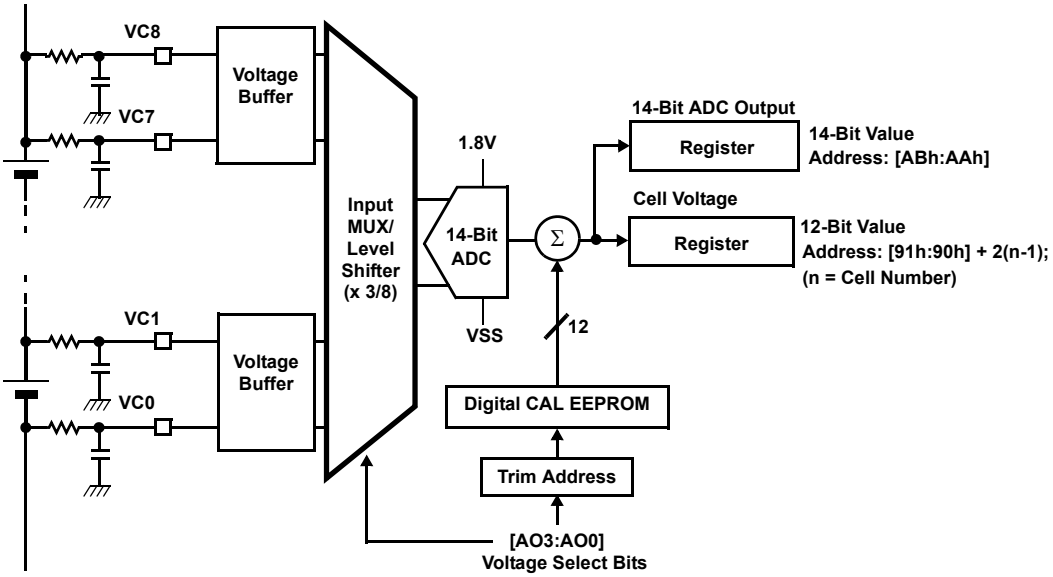


Figure 56. Cell Voltage Capture

Pack current is measured next and the results are stored in the data register "0x8E-8F IPACK" on page 90. The measured value is not compared to the current thresholds, comparators are used for pack current fault detection. Threshold violations of any of these thresholds set the related fault bit as indicated in the register descriptions. The current protection circuits are described in "Current Monitoring/Response" on page 132.

On every 4th scan temperature measurements are executed and stored in data registers then compared against the external temperature thresholds "0x30-31 COT" on page 56, "0x34-35 CUT" on page 58, "0x38-39 DOT" on page 59, and "0x3C-3D DUT" on page 61. Violations of any of these threshold voltages set the related fault bit as indicated in the register descriptions.

The 4th scan also includes measurement of "RGO Pin (36)" on page 99 and "VBATT Pin (48)" on page 113.

During manufacture, calibration values are stored in the device EEPROM for each voltage reading. When there is a new conversion for a particular voltage, the calibration is applied to the conversion.

Scan rates vary depending on the system Mode:

- "NORMAL Mode" on page 120; scan rate is once every 32ms.
- "IDLE Mode" on page 121; scan rate is once every 256ms.
- "SLEEP Mode" on page 121; scan rate is once every 512ms.

The transition between Modes is governed solely by the time since a charge current detection ("0x82.2 CHING" on page 77) or discharge current detection ("0x82.3 DCHING" on page 76). These times are user programmable, see "0x48.[3:0] IDLE/DOZE Timer" on page 66 and "0x48.[7:4] SLEEP Timer" on page 66 for more information.

FETs turn off immediately if there is an error, but they do not turn on until the end of the voltage scan that follows the removal of the fault condition. An exception to this is when a device wakes up due to a load detection ("Load Detection" on page 105). In this case, the FETs turn on immediately on wake-up, then a scan begins.

6.3.1 Automatic V & I Scan

The V & I Scan shown in Figure 57 shows the measurement sequence performed on every 3 of 4 scan intervals. It also includes the portion of time dedicated to performing digital comparisons for fault detection and response.

Cell voltages enabled by register "0x49 Cell Select" on page 67 are measured sequentially, followed by the pack current. After each measurement scan, the ISL94202 performs an offset adjustment and stores the results in the data registers. After the values are stored, the state machine executes compare operations that determine if the pack is operating within limits. Current thresholds are constantly compared and are not gated by this sequence.

The Open-Wire check is performed only every 32nd scan if "0x81.4 CELLF" on page 74 condition exists.

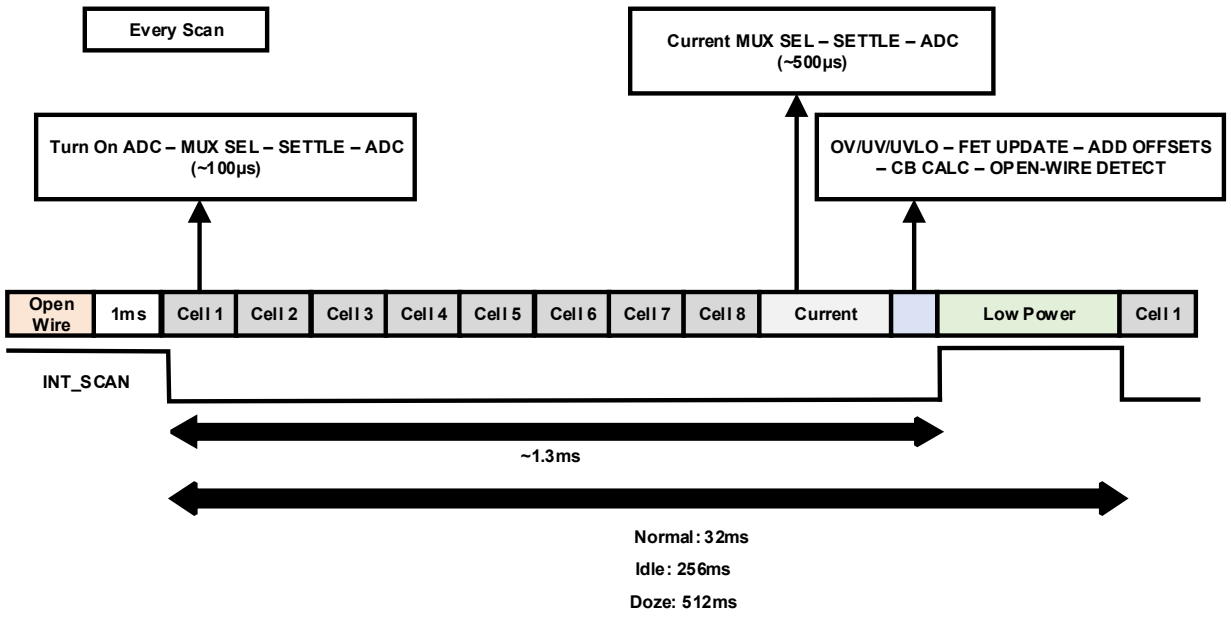


Figure 57. System Scan V & I

6.3.2 Automatic V, I, & T Scan

The V, I, & T Scan pictured in Figure 58 shows the measurements performed at every 4th scan interval, including the first scan on device power-on and/or wake-up. It also includes the portion of time dedicated to performing digital comparisons for fault detection and response.

Cell voltages enabled by register "0x49 Cell Select" on page 67 are measured sequentially, followed by the pack current. This longer scan also includes VBATT, VRGO, and external and internal temperature measurements. After the values are stored, the state machine executes compare operations that determine if the pack is operating within limits. Current thresholds are constantly compared and are not gated by this sequence.

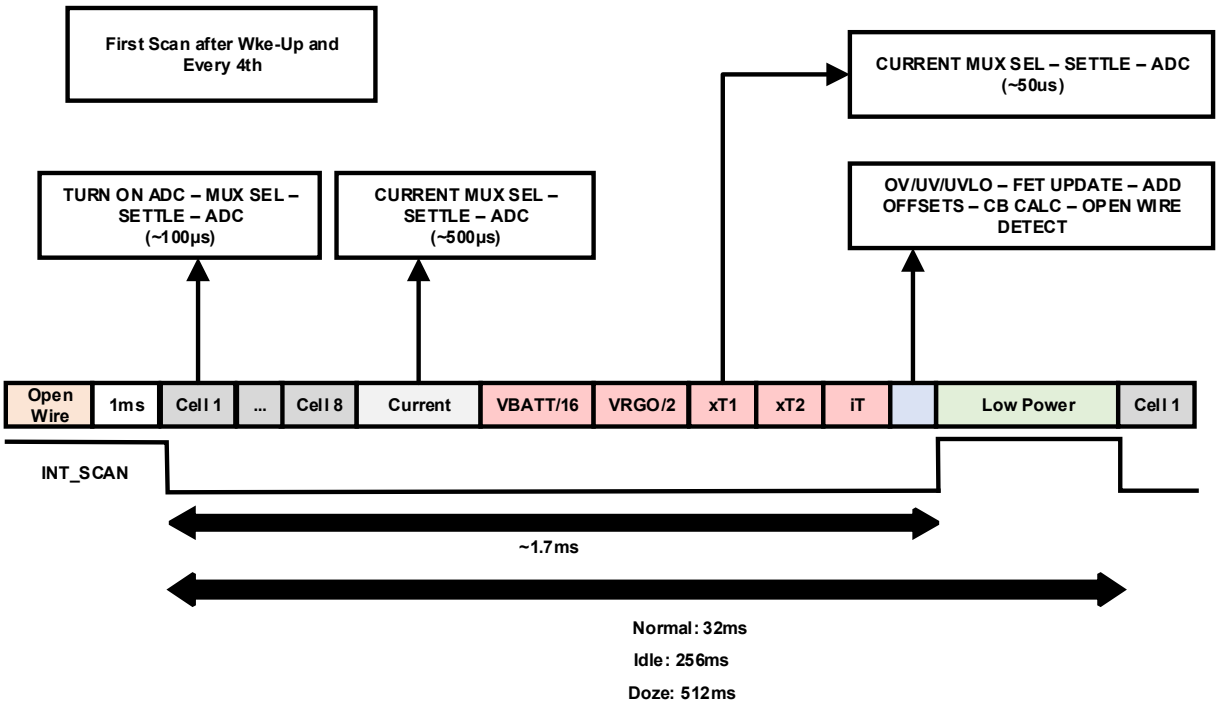


Figure 58. System Scan V, I, & T

The automatic scan timing of the external temperature sensors is detailed in Figure 59.

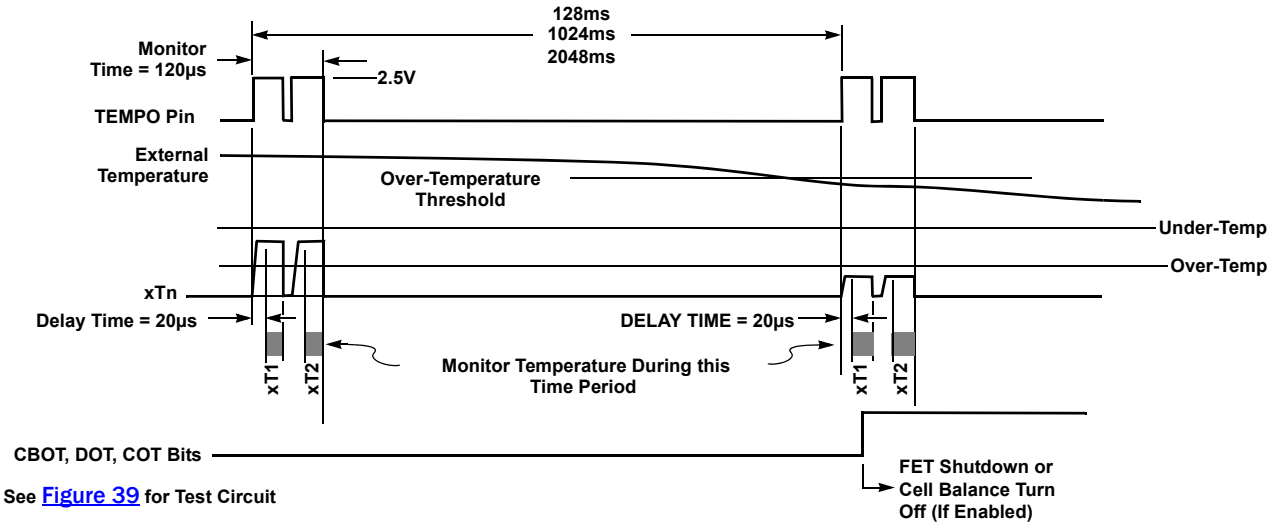


Figure 59. Automatic Temperature Scan

6.3.3 MCU Scan

When the MCU performs the system scan, a specific sequence should be followed for any voltage measurement. If the device is made to perform a measurement, the ISL94202 does not automatically react to any out of bounds conditions for voltage, external temperature, or overcurrent conditions. The exception is a discharge short-circuit current condition ("0x81.3 DSCF" on page 74).

An external MCU can trigger a measurement and read the result of any of the internally monitored voltages independently of the normal voltage scan. The MCU must first set the bit "0x87.2 µCSCAN" on page 84 to 1 to take control. This stops the internal scan and starts the watchdog timer ("0x47.[7:3] WDT" on page 65). If the MCU maintains this state, communication must continue and the MCU must manage all voltage and current pack

control operations and implement the cell balance algorithms. However, when the µCSCAN is cleared (µCSCAN = 0), by the MCU or the WDT the ISL94202 resumes automatic scans.

After setting the µCSCAN bit, the MCU must write to register bits “0x85.[3:0] AO” on page 80 to select the desired input to measure. Next set the bit “0x85.6 ADCSTRT” on page 79 to start an ADC conversion. When the conversion is complete, the results are read from the ADC registers (“0xAA-AB - ADCV” on page 93). The result is a 14-bit value. The ADC conversion takes ~100µs, the MCU can poll the I^2C connection waiting for an ACK to indicate that the ADC conversion is complete.

If the µCSCAN bit is set when the ISL94202 internal scan is scheduled, the internal scan pauses until the µCSCAN bit is cleared and the internal scan continues immediately.

Reading an ADC value from the MCU requires the sequence and time shown in Table 75 to complete:

Table 75. MCU Measurement of Voltages

Step	Operation	Number I^2C Cycles	Time at 400kHz I^2C CLK (ea.) (µs)	Time (Cumulative) (µs)
1	Set “0x87.2 µCSCAN” on page 84 bit	29	72.5	72.5
2	Select MUX channel (“0x85.[3:0] AO” on page 80), then start the ADC (“0x85.6 ADCSTRT” on page 79 = 1)	29	72.5	145
3	Wait for ADC complete	N/A	110	255
4	Read register “0xAA-AB - ADCV” on page 93	(0xAB) 29 (0xAA) 29	(0xAB) 72.5 (0xAA) 72.5	(0xAB) 327.5 (0xAA) 410
5	Clear µCSCAN bit	29	100	472.5

To take multiple readings of the same value for averaging, repeat Steps 2 through 4 as many times as desired. However, if this is a continuous operation, care must be taken to monitor other pack functions or to pause long enough for the ISL94202 internal operations to collect data to control the pack. A burst of five measurements takes ~1.8ms.

6.4 System Modes

To minimize power consumption, most circuits are kept off when not being used and items are sampled at intervals. There are five power states in the device as shown in Figure 60 on page 120. Powerdown is a static non-operational state, the other states are also referred to as Modes because they are functional.

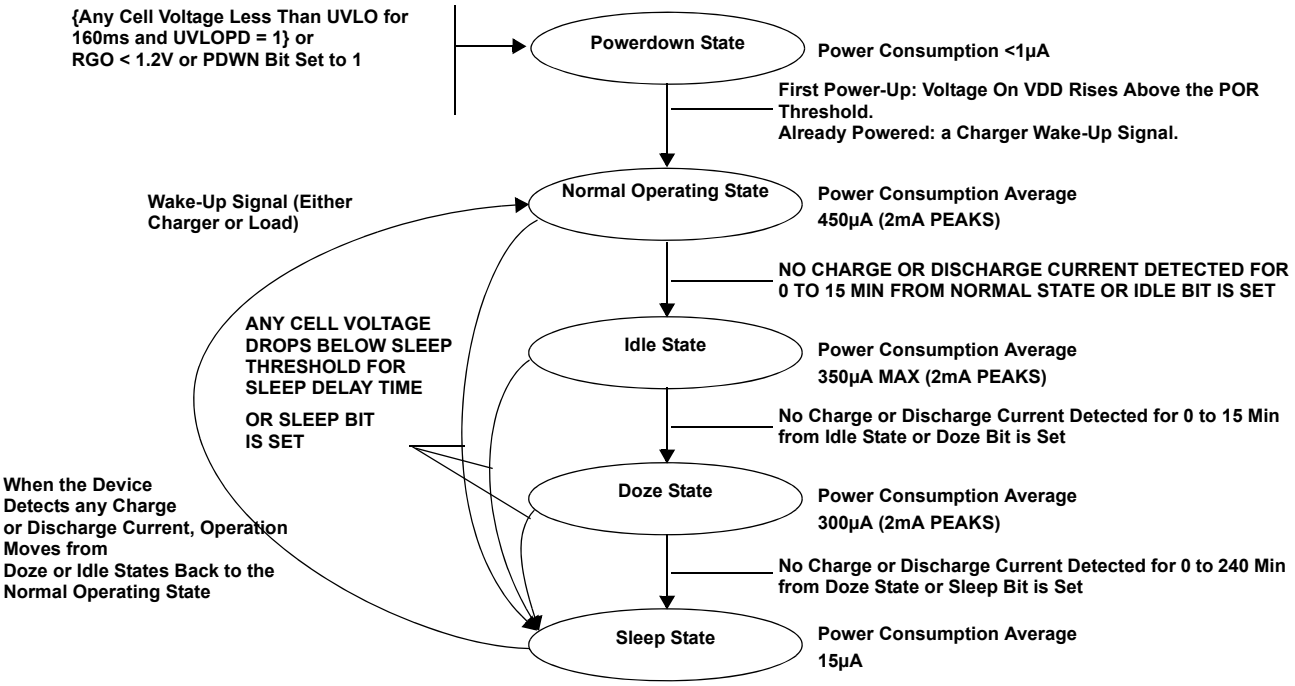


Figure 60. ISL94202 Mode transitions.

6.4.1 Powerdown State

The ISL94202 is designed to tolerate an unknown connection sequence. Often when the device is first connected to a battery pack it is unknown which pins connect first or in what order. After the "VDD Pin (43)" on page 106 and "VSS Pin (18, 28, 29)" on page 95 pins connect, the device enters the Powerdown state. It remains in this state until a charger is connected. The device also powers up if the "CHMON Pin (37)" on page 99 is connected to the top of the pack through an outside resistor to enable PCB test. It is possible that the pack powers up automatically when the battery stack is connected due to momentary conduction through the power FET G-S and G-D capacitors.

The device also enters the Powerdown State when the voltage on the pack is too low for proper operation. This occurs when:

- V_{DD} is less than the POR threshold and RGO < 2.25V. This condition can occur in low cell count packs, or low voltage storage components are used, or if cells discharge over a long period of time.
- V_{DD} is less than 1V and RGO > 2.25V. This condition can occur during a short-circuit with minimum capacity cells. VDD drops out, but the RGO cap maintains the logic supply.
- Any cell voltage is less than the "0x0A-0B V_{CELL} UVLO" on page 39 threshold for more than ~160ms (and "0x4B.3 UVLOPD" on page 70 = 1).
- Commanded by an external MCU (set "0x88.3 PDWN" on page 84). The device no longer communicates following this command. It is most often used at the end of Pack production test in preparation for storage.

Recovering out of any low-power state brings the ISL94202 into the NORMAL Mode. The only way to recover from a this state (transition to NORMAL Mode) is through a charger connection "CHMON Pin (37)" on page 99.

6.4.2 NORMAL Mode

This is the Normal monitoring/scan Mode for the ISL94202. In this Mode, the device monitors for overcurrent continuously and scans the voltages every 32ms. If balancing is required, the device activates external balancing components. All necessary circuits are on and unnecessary circuits are off.

During the scan, the ISL94202 draws more current as it activates the input level shifter, the ADC, and data processing. Between scans, circuits turn off to minimize power consumption.

The device remains in the Mode as long as charge (“0x82.2 CHING” on page 77) or discharge (“0x82.3 DCHING” on page 76) current is detected.

6.4.3 IDLE Mode

If there is no current flowing for 0 to 15 minutes (set by “0x48.[3:0] IDLE/DOZE Timer” on page 66), the device enters the IDLE Mode. The transition between NORMAL Mode to IDLE Mode is governed by the time since CHING (“0x82.2 CHING” on page 77) or DCHING (“0x82.3 DCHING” on page 76 bits were set, in other words, the time since last detecting a charge or discharge current. If there is no current flowing for this time, the device enters the IDLE Mode. In this Mode, voltage scanning slows to once every 256ms. The FETs and the LDO remain on. In this Mode, the device consumes less current, because there is more time between scans.

When the ISL94202 detects any charge or discharge current, the device exits the IDLE Mode and returns to the NORMAL Mode of operation.

The device does not automatically enter the IDLE Mode if “0x87.2 µCSCAN” on page 84 is set to 1, because the MCU is in charge of performing the scan and controlling the operation.

Setting “0x88.0 IDLE” on page 85 to 1 forces the device to enter IDLE Mode, regardless of current flow. When an MCU sets the IDLE bit, the device remains in IDLE Mode, regardless of the timer or the current. Setting the Mode control bits to 0 allows the device to control the Mode.

The device transitions back to NORMAL Mode if a charge (“0x82.2 CHING” on page 77) or discharge (“0x82.3 DCHING” on page 76) current is detected.

6.4.4 DOZE Mode

If there is no current flowing for 0 to 15 minutes (also set by “0x48.[3:0] IDLE/DOZE Timer” on page 66), the device enters the DOZE Mode. The transition from IDLE to DOZE Mode is governed by the time since CHING (“0x82.2 CHING” on page 77) or DCHING (“0x82.3 DCHING” on page 76) bits were set, in other words, the time since last detecting a charge or discharge current. If there is no current flowing for the set time the device enters the DOZE Mode, where cell voltage sampling occurs every 512ms. The power FETs and the LDO remain on. In this Mode, the device consumes less current than in IDLE Mode, because there is more time between scans.

When the ISL94202 detects any charge or discharge current, the device exits DOZE Mode and returns to the NORMAL Mode.

The device does not automatically enter the DOZE Mode if “0x87.2 µCSCAN” on page 84 is set to 1, because the MCU is in charge of performing the scan and controlling the operation.

Setting “0x88.1 DOZE” on page 85 to 1 forces the device to enter the DOZE Mode, regardless of the current flow. When a MCU sets the DOZE bit, the device remains in DOZE Mode regardless of the timer or the current. Setting the Mode control bits to 0 allows the device to control the Mode.

Setting the IDLE/DOZE timer to 0 immediately forces the device from NORMAL into the DOZE Mode when there is no current. To transition back to NORMAL Mode, either “0x82.2 CHING” on page 77 or “0x82.3 DCHING” on page 76 bits must be set due to a charge or discharge current detection.

If the SLEEP timer (“0x48.[7:4] SLEEP Timer” on page 66) is set to 0, the device transitions from DOZE to SLEEP Mode immediately and it may appear as if it skipped DOZE Mode.

6.4.5 SLEEP Mode

The ISL94202 enters the SLEEP Mode when the voltage on the cells drops below the Sleep Level Voltage threshold (“0x44-45 SLV” on page 64) for the time specified by the Sleep Level Timer (“0x47.[0] - 0x46.[7:0] SLT” on page 66). To prevent the device from entering SLEEP Mode by a low voltage on the cells, the SLV register can be set to 0. If “0x87.6 µCFET” on page 82 = 1, the SLV setting is ignored and cannot place the device into SLEEP.

The ISL94202 also transitions to SLEEP from DOZE Mode if there has been no detected current for more than the duration of the sleep mode timer (“0x48.[7:4] SLEEP Timer” on page 66). In this case, the device remains in DOZE Mode until there has been no current for 0 to 240 minutes (with 16 minute steps). The Mode transition is governed by the time since “0x82.2 CHING” on page 77 or “0x82.3 DCHING” on page 76 bits were set, in other

words, the time since last detecting a charge or discharge current. If there is no current flowing for this time, the device transitions to SLEEP Mode from DOZE Mode.

Setting "0x88.2 SLEEP" on page 85 to 1 forces the device to enter the SLEEP Mode, regardless of the current flow. When a MCU sets the SLEEP bit, the device remains in SLEEP Mode regardless of the timer or the current. Setting the Mode control bits to 0 allows the device to control the Mode.

If both IDLE/DOZE and SLEEP timers are set to 0, the device immediately goes to SLEEP when there is no charge or discharge current detected. To wake the device, a charger ("CHMON Pin (37)" on page 99) or load ("LDMON Pin (38)" on page 104) must be attached and non-zero values must be written to the timer register ("0x48.[3:0] IDLE/DOZE Timer" on page 66).

While the ISL94202 is in SLEEP, registers "0x8A-8B CELMIN" on page 89 and "0x8C-8D CELMAX" on page 89 read 0x000 and 0x0FFF, respectively. When waking up, these registers are restored to their previous reading (last reading before entering SLEEP) within 538µs.

While in the SLEEP Mode, everything is off (including the power FETs) except for the 2.5V regulator and the wake-up circuits. To wake and transition back to NORMAL Mode, either a "LDMON Pin (38)" on page 104 connection to a load or "CHMON Pin (37)" on page 99 connection to a charger detection must be made.

The part resumes system scans ~1.5ms after waking from SLEEP. The first scan to performed is the V, I, and T scan shown in Figure 58 on page 118.

6.4.6 Mode Exceptions

There is one exception to the normal sequence of Mode management. When the MCU sets "0x87.2 µCSCAN" on page 84 bit to 1, the internal scan stops. This means that the device no longer looks for the conditions required for SLEEP. The external MCU needs to manage the Modes of operation. Forcing the device into different Modes can be achieved by using the following bits:

- "0x88.0 IDLE" on page 85.
- "0x88.1 DOZE" on page 85.
- "0x88.2 SLEEP" on page 85.
- "0x88.3 PDWN" on page 84.

Possible forced transitions (using the bits above and an external MCU) are shown in Table 76.

Table 76. Forced Mode Transitions

		TO				
		PDOWN	**NORM**	**IDLE**	**DOZE**	**SLEEP**
FROM	**PDOWN**	N/A	NO*	NO	NO	NO
	NORM	YES	N/A	YES	YES	YES
	IDLE	YES	NO	N/A	YES	YES
	DOZE	YES	NO	YES	N/A	YES
	SLEEP	NO	NO	NO	NO	N/A

Note: A transition from Powerdown to NORMAL Mode is only possible through detection of a charger connection ("CHMON Pin (37)" on page 99). The detection of a charger or load forces the device into NORMAL Mode from any other Mode, with the exception of Powerdown.

6.5 Cell Balancing

External cell balancing is supported by the ISL94202. The "CBn Pins" on page 94 are the cell balance FET driver outputs while the cell balance current level is controlled by placing resistors in series with the cell balance FETs.

There are two choices of operation for cell balancing, use the ISL94202 automatic cell balancing algorithm or the option of MCU controlled cell balancing.

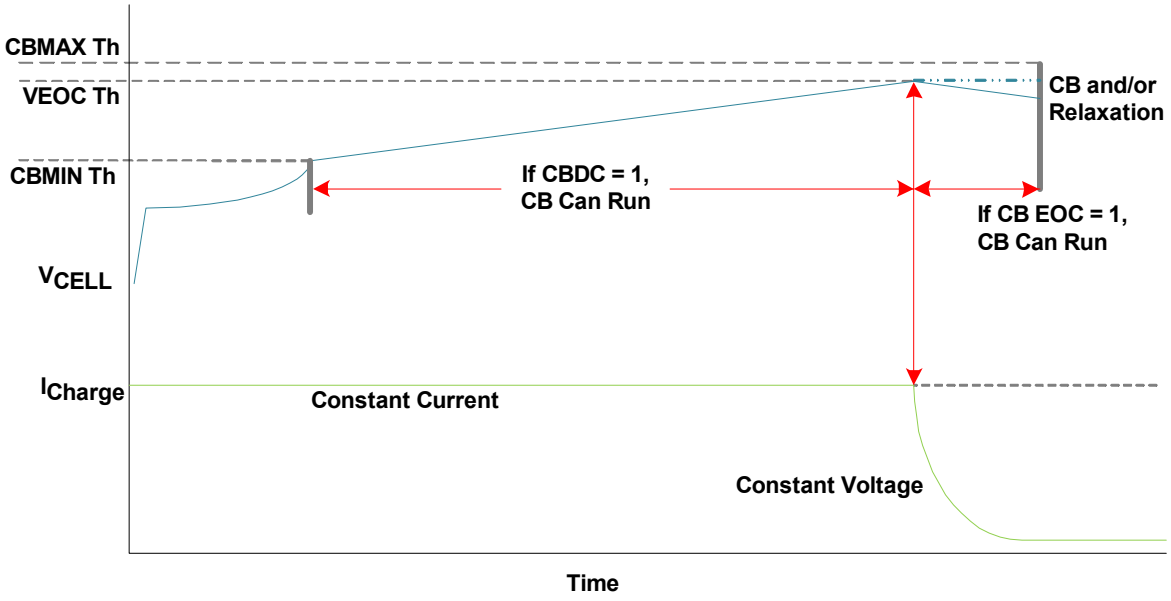


Figure 61. Cell Balance (Charging)

6.5.1 Automatic CB

At the same rate as the scan of the cell voltages, if cell balancing is enabled, the system checks for proper cell balance conditions. The ISL94202 prevents cell balancing if proper temperature, current, and voltage conditions are not met. The cells only balance during a CBON ("0x24-25 CBON Timer" on page 52) time period. When the CBOFF ("0x26-27 CBOFF Timer" on page 53) timer is running, the cell balance is off. Three additional bits determine whether the balancing happens only during charge, only during discharge, during both charge and discharge, during the end-of-charge condition, or not at any time. Figure 61 shows the relationship between the cell balancing thresholds and enable bits during an example charge cycle.

- The cell balance circuit depends on the 14-bit ADC converter built into the device and the results of the cell voltage scan (after calibration).
- The ADC converter loads a set of registers with each cell voltage during every cell voltage measurement.
- At the end of the cell voltage measurement scan, the ISL94202 updates the minimum ("0x8A-8B CELMIN" on page 89) and maximum ("0x8C-8D CELMAX" on page 89) cell voltage data registers.
- After calculating the CELMIN and CELMAX values, all of the cell voltages are compared with the CELMIN value. When any of the cells exceed CELMIN by CBMINDV ("0x20-21 CBMINDV" on page 50), a flag is set in register CBFC indicating that cell n needs balancing (CBnON bit n in register "0x84 CBFC (R/W)" on page 78 is set to 1).
- If any of the cells exceed the lowest cell by CBMAXDV ("0x22-23 CBMAXDV" on page 51), a fault is set indicating that a Cell voltage Failure occurred ("0x81.4 CELLF" on page 74). When the CELLF flag indicates that there is too great a cell-to-cell differential, cell balancing is turned off.
- If CELMAX is below the CBMIN threshold ("0x1C-1D CBMIN" on page 49), status bit "0x83.3 CBUV" on page 78 is set and there is no cell balancing. Cell balance does not start again until the CELMAX value rises above (CBMIN + 117mV). When this happens, the ISL94202 clears the CBUV bit.
- If the CELMIN voltage is greater than the CBMAX voltage ("0x1E-1F CBMAX" on page 50), "0x83.2 CBOV" on page 78 is set and there is no cell balancing. Cell balancing does not start again until the CELMIN value drops below (CBMAX - 117mV). When this happens, the ISL94202 clears the CBOV bit.
- The "0x49 Cell Select" on page 67 register, backed up in EEPROM, identifies the number of cells that are supposed to be present so only the cells present are used for the cell balance operation.
  Note: This register is also used in the cell voltage scan and open-wire detect operation.

- There are no limits to the number of cells that can be balanced at any one time, because the balancing current is external to the device.
- The cell balance block updates at the start of the cell balance on period (“0x24-25 CBON Timer” on page 52) to determine if balancing is needed and that the right cells are being balanced. The cells selected at this time are balanced for the duration of the cell balance period. This cell balance duration is CBON + CBOFF (“0x26-27 CBOFF Timer” on page 53).
- The cell balance is disabled if any external temperature is out of a programmed range set by “0x28-29 CBUT” on page 53 and “0x2C-2D CBOT” on page 55.
- Control bit “0x4B.7 CBDD” on page 69 enables and disables cell balancing when a discharge current is detected (“0x82.3 DCHING” on page 76).
- Control bit “0x4B.6 CBDC” on page 69 enables and disables cell balancing when a charge current is detected (“0x82.2 CHING” on page 77).
- Control bit “0x4B.0 CB_EOC” on page 70 enables and disables cell balancing when an end-of-charge condition is detected. If the CB_EOC bit is 0, it does not matter what the EOC pin does, balance is enabled. If the CB_EOC bit is 1, the EOC pin must also be 1 (and the other conditions are also correct) for balance to be enabled (see “0x81.7 VEOC” on page 73).
- The cell balance operation can be disabled by clearing all of the following bits:
  - “0x4B.7 CBDD” on page 69
  - “0x4B.6 CBDC” on page 69
  - “0x4B.0 CB_EOC” on page 70
- Any combination of the CBDD, CBDC, and CB_EOC bits can be used to enable or disable balancing in one, two, or all three of the possible cell balance conditions (charging, discharging and end-of-charge, see Figure 62 and Table 77).
- Cell balancing is disabled by asserting the “FETSOFF Pin (33)” on page 98.
- The cell balance outputs are on only while the “0x24-25 CBON Timer” on page 52 is counting down. The cell balance outputs are all off while the “0x26-27 CBOFF Timer” on page 53 is counting down. Both of these are 12-bit timers.

Cell balancing is synchronous with the cell voltage measurements, meaning cell balancing starts following the voltage scan measurements that determined the cells to be balanced. However, if the CBON period exceeds the 32ms NORMAL scan cycle, measurements are still taken during cell balancing regardless of whether a cell is being balanced or not. To avoid erroneous cell measurements inhibiting proper cell balancing, the cell balance off time (“0x26-27 CBOFF Timer” on page 53) should be large enough to allow a voltage scan to read the settled cell voltages before making any cell balancing decisions. Therefore, the cell balance off time should be at least larger than the scan interval time plus and settling time needed for the cell voltages to stabilize following the last CBON time.

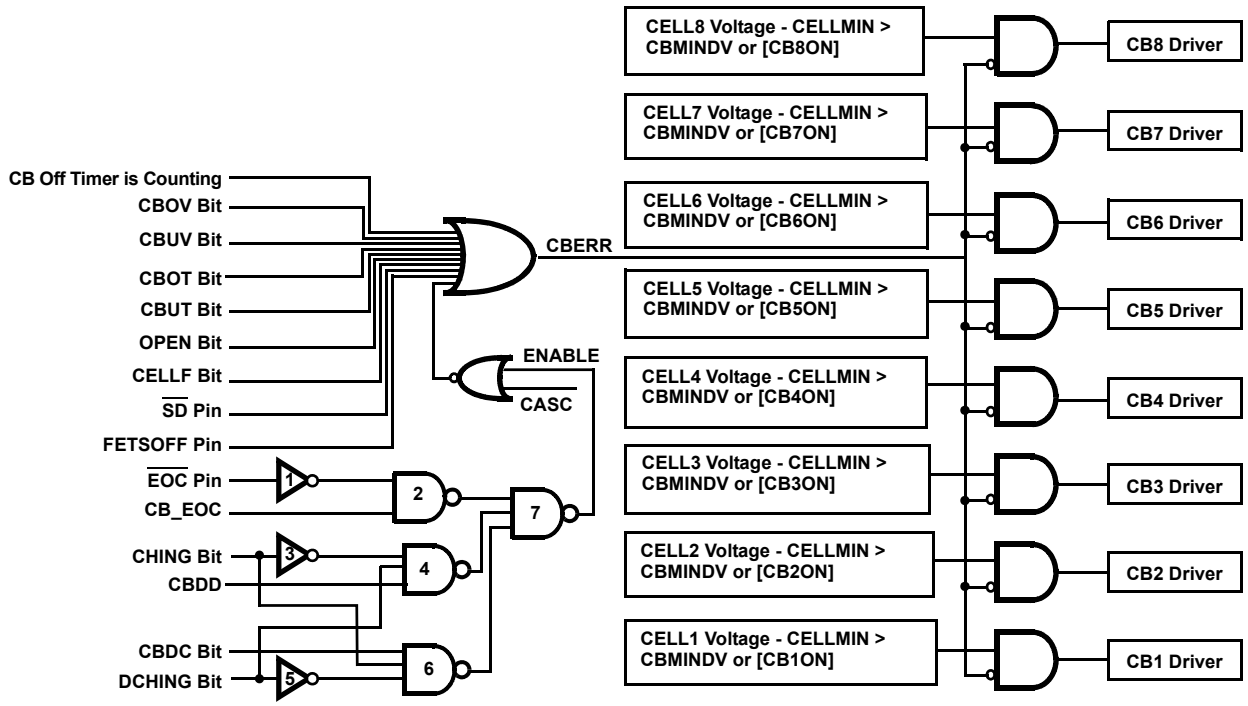


Figure 62. Cell Balance Operation

Table 77. Cell Balance Truth Table

CB_EOC Bit	EOC Pin	CBDC	CHING	CBDD	DCHING	Enable
0	x	0	0	0	0	0
1	1	0	0	0	0	0
0	x	0	0	0	1	0
1	1	0	0	0	1	0
0	x	0	0	1	0	0
1	1	0	0	1	0	0
0	x	0	0	1	1	1
1	1	0	0	1	1	1
0	x	0	1	0	0	0
1	1	0	1	0	0	0
0	x	0	1	0	1	0
1	1	0	1	0	1	0
0	x	0	1	1	0	0
1	1	0	1	1	0	0
0	x	0	1	1	1	0
1	1	0	1	1	1	0
0	x	1	0	0	0	0
1	1	1	0	0	0	0
0	x	1	0	0	1	0
1	1	1	0	0	1	0
0	x	1	0	1	0	0
1	1	1	0	1	0	0

Table 77. Cell Balance Truth Table (Continued)

CB_EOC Bit	EOC Pin	CBDC	CHING	CBDD	DCHING	Enable
0	x	1	0	1	1	1
1	1	1	0	1	1	1
0	x	1	1	0	0	1
1	1	1	1	0	0	1
0	x	1	1	0	1	0
1	1	1	1	0	1	0
0	x	1	1	1	0	1
1	1	1	1	1	0	1
0	x	1	1	1	1	0
1	1	1	1	1	1	0
1	0	x	x	x	x	1

6.5.2 MCU CB

To control the cell balance FETs, the external MCU first needs to set “0x87.5 µCCBAL” on page 83 bit to disable automatic cell balance operation.

To turn on the cell balance FETs, the MCU needs to enable each individual cell balance FET output using the cell balance control register (“0x84 CBFC (R/W)” on page 78). In this register, each bit corresponds to a specific cell balance output.

With the cell balance outputs selected/enabled, the MCU sets “0x87.0 CBAL_ON” on page 84 to turn on the cell balance output control circuit. To turn the cell balance outputs off, the CBAL_ON bit should be cleared.

If the external MCU is performing the system scan, cell voltages should not be measured until the cell balance output FETs are turned off and there has been enough time for the cell voltages to settle. Only then should cell voltages be measured and read for use in determining the next cells to be balanced.

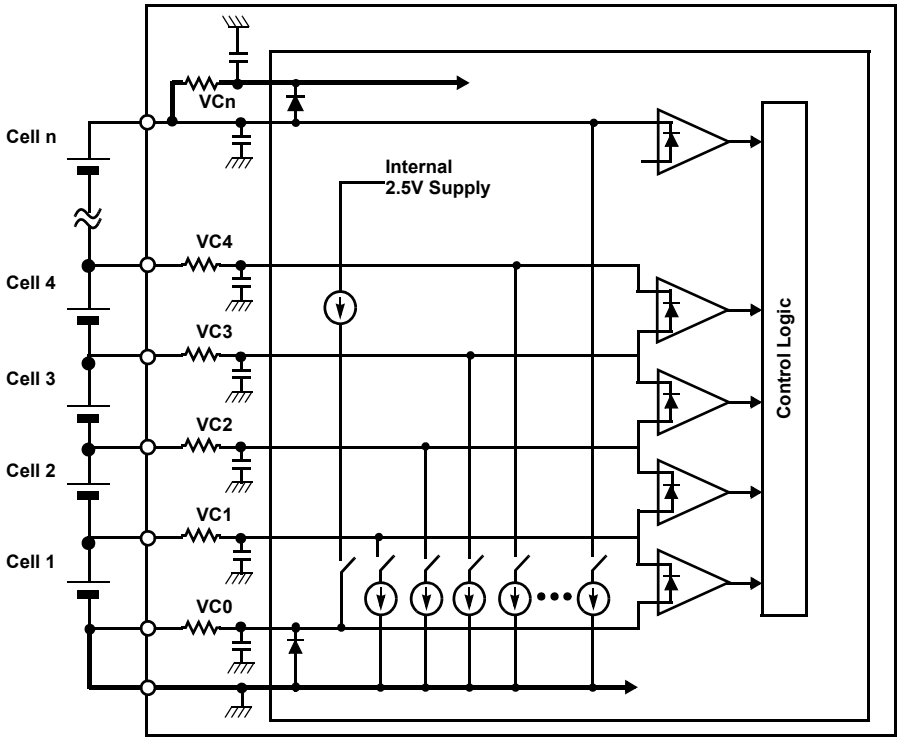
6.6 Open Wire

An Open-Wire condition occurs when the series connection between a VCn measurement pin and the cell to be measured is broken. A CELLF condition (see “Cell Fail” on page 129) detection is required to trigger an Open-Wire test. The test is performed on the first scan following the CELLF condition detection and then once every 32 scans while the CELLF condition remains. A CELLF condition is the first indication that an Open-Wire condition may be present.

Bit “0x4A.1 DOWD” on page 68 is used to enable or disable the Open-Wire test.

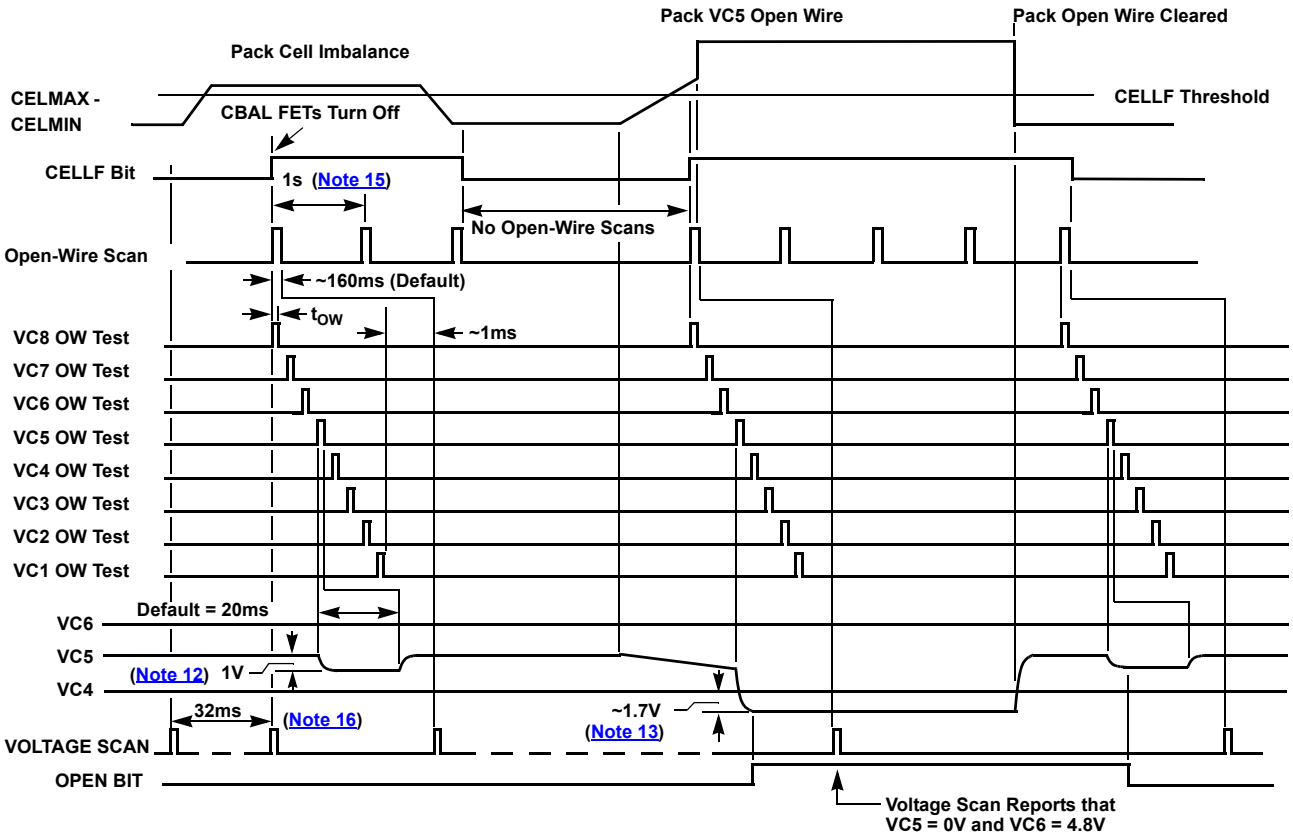
The Open-Wire detection mechanism pulls (or pushes) 1mA of current sequentially on each VC_n input (“VCn Pins” on page 94) for a period of time specified by register “0x14-15 OWT” on page 43. The pulse is programmable between 1µs and 512ms, the default time is 1ms. During this test, comparators test the voltage at the VC_n pin relative to its adjacent cells (VC_{n-1} & VC_{n+1}). In the absence of a cell and with an external 4.7nF capacitor a 1mA input current changes the voltage at VC_n to the open-wire threshold (relative to adjacent cell) within 30µs (signaling a Open-Wire condition). If the cell is present, the voltage change on the VC_n input is negligible.

Each VC_n input has a comparator that detects if the voltage on an input drops more than 0.3V below the voltage of VC_{n-1} with exceptions to VC_0 & VC_1. For VC_1, the comparator looks to see if the voltage drops 0.4V below VC_0. For VC_0, the circuit looks to see if the voltage exceeds 1.25V.



Note: The open-wire test is run only if the device detects the CELLF condition and then once every 32 voltage scans while a CELLF condition exists. Each current source is turned on sequentially.

Figure 63. Open-Wire Detection



Notes:

12. Voltage drop = 1mA * 1kΩ = 1V.
13. Voltage = V_F of CB5 Balance FET body diode + (1mA * 1kΩ).
14. OWPSD bit = 0.
15. This time is 8s in IDLE and 16s in DOZE.
16. This 32ms scan rate increases to 256ms in IDLE and 512ms in DOZE.

Figure 64. Open-Wire Test Timing

With the Open-Wire pulse current setting of 1mA, input resistors of 1kΩ create a voltage drop of 1V. This voltage drop combined with the body diode clamp of the cell balance FET, provides the -1.4V drop to trip an open-wire detection. For this reason and for the increased protection, Renesas recommends not using smaller input series resistors. For example, with a 100Ω input resistor the voltage across the input resistor drops only 0.1V. This would not allow the input open-wire detection hardware to trigger (although the digital detection of an open wire still works, the hardware detection automatically turns off the open-wire current).

Input resistors larger than 1kΩ may be desired to increase the input filtering. This is enabled with an increase in the detection time (by changing the OWT value, see “0x14-15 OWT” on page 43.) However, increasing the input resistors affects measurement accuracy. The ISL94202 has up to 2µA variation in the input measurement current. This amounts to about 2mV measurement error with 1k resistors (this error has been factory calibrated out). However, 10kΩ resistors can result in up to 20mV measurement errors. To increase the input filtering, the preferred method is to increase the size of the capacitors.

Depending on the selection of the input filter components, the internal open-wire comparators may not detect an open-wire condition. This might happen if the input resistor is small. In this case, the body diode of the cell balance FET may clamp the input before it reaches the open-wire detection threshold. To overcome this limitation and provide a redundant open-wire detection, at the end of the open-wire scan all input voltages are converted to digital values. If any digital value equals 0V (minimum) or 4.8V (maximum), the device sets the OPEN error flag (see “0x81.5 OWF” on page 74) indicating an open-wire failure.

When an open-wire condition occurs and the Open-Wire Pack Shutdown bit (“0x4A.0 OWPSD” on page 68) is equal to 0, the ISL94202 turns off all (CB and Power) FETs, but does not set the PSD output. While in this

condition, the device continues to operate normally in all other ways (for example, the cells are scanned and the current monitored. As time passes, the device drops into lower power Modes).

When an open-wire condition occurs and OWPSD bit is equal to 1, the Open Wire Fault (“0x81.5 OWF” on page 74) is set, the ISL94202 turns off all (CB and Power) FETs, and asserts the “PSD Pin (32)” on page 98.

The device can automatically recover from an open-wire condition because the open-wire test is still functional, unless the OWPSD bit equals 1 and the PSD pin blows a fuse in the pack. If the open-wire test finds that the open wire has been cleared, then Open-Wire Fault is reset to 0 and other tests determine whether conditions allow the power FETs to turn back on.

The open-wire test hardware has two limitations. First, it depends on the CELLF indicator (“0x81.4 CELLF” on page 74). If the Cell Balance Maximum Voltage Delta (“0x22-23 CBMAXDV” on page 51) value is set too high (FFFh for example), the device may never detect a CELLF condition. The second limitation is that the open-wire test does not happen immediately. A scan must detect a CELLF condition, then the open-wire test occurs on the next scan, 32ms (NORMAL Mode) to 512ms (DOZE Mode) later.

6.7 Cell Fail

The Cell Fail (“0x81.4 CELLF” on page 74) condition indicates that the difference between the highest voltage cell and the lowest voltage cell exceeds a programmed threshold (“0x22-23 CBMAXDV” on page 51). When detected, the CELLF condition turns off the cell balance and power FETs, but only if “0x87.6 µCFET” on page 82 = 0. Setting µCFET = 1 prevents the power FETs from turning off during a CELLF condition. The MCU is then responsible for the power FET control.

Setting control bit “0x4A.7 CELLF PSD” on page 67 to 1 enables the PSD activation when the ISL94202 detects a Cell Fail condition. When “0x81.4 CELLF” on page 74 = 1 and CELLF_PSD = 1, the power FETs and cell balance FETs turn off, and the PSD output (“PSD Pin (32)” on page 98) goes active. You can use the PSD pin output through additional circuitry to deactivate the pack by blowing a fuse. The PSD pin alone is not capable of blowing a fuse.

The CELLF function can be disabled by setting the CBMAXDV value to 0xFFF. In this case, the voltage differential can never exceed the limit. However, disabling the cell fail condition also disables the open-wire detection (see “Open Wire” on page 126).

6.8 OV Detection/Response

The device needs to monitor the voltage on each battery cell (“VCn Pins” on page 94). If the voltage of any cell exceeds the cell overvoltage threshold (“V_{CELL} OV” on page 35) for a time exceeding cell overvoltage timer (“0x10-11 VC_{ELL} OV Timer” on page 41), the device sets the Overvoltage Fault bit (“0x80.0 OVF” on page 73). Then, if “0x87.6 µCFET” on page 82 = 0, the ISL94202 turns the charge FET OFF by setting “0x86.1 CFET” on page 81 to 0. When the OV fault is set, the pack has entered Overcharge Protection Mode. The status of the discharge FET remains unaffected.

The charge FET remains off until the voltage on the overcharged cell drops below “0x02-03 V_{CELL} OVR” on page 36 for the time period set by “0x10-11 VC_{ELL} OV Timer” on page 41. **Note:** The time taken to recover is equal to the time taken to enter the condition because the same timer setting is used. The detection timer and recovery timer are asynchronous to the voltage threshold. As a result, a setting of 1s can result in a delay time of 1s to 2s, depending on when the OV/OVR is detected.

The device further continues to monitor the battery cell voltages and is released from Overcharge Protection Mode when $[V_{Cn} - V_{C(n-1)}] < V_{OVR}$ for more than the overcharge delay time, for all cells.

When the device is released from Overcharge Protection Mode, the charge FET is automatically switched on (if µCFET = 0). When the device returns from Overcharge Protection Mode, the status of the discharge FET remains unaffected.

There is also an overvoltage lockout (“0x08-09 V_{CELL} OVLO” on page 38). When this level is reached, an OVLO bit (“0x80.1 OVLOF” on page 73) is set, the PSD output is asserted, and the charge FET or precharge FET is

immediately turned off. You can use the PSD pin output through additional circuitry to deactivate the pack by blowing a fuse. The PSD pin alone is not capable of blowing a fuse.

If the µCFET bit is 1 during an OV condition, the MCU must control both turn off and turn on of the charge and precharge power FETs. This does not apply to the OVLO condition.

If there is discharge current flowing out of the pack, the device includes an option to turn the charge FET back on in an overvoltage condition. This option is set by bit "0x4B.4 CFODOV" on page 69 (CFET ON During Overvoltage). Then, if the discharge current stops and there is still an overcharge condition on the cell, the device again disables the charge FET.

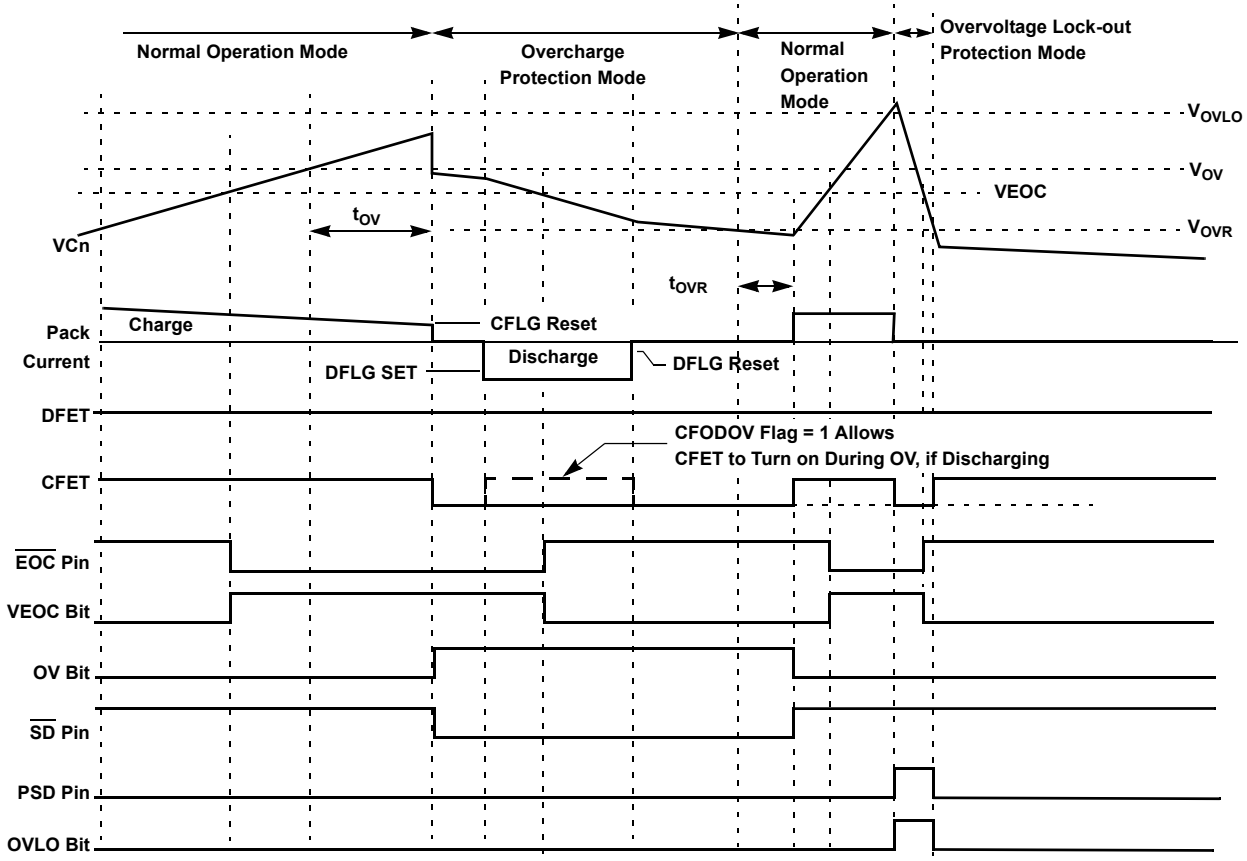


Figure 65. OV Detection/Response

6.8.1 VEOC

During charge, if the voltage on any cell exceeds an Voltage End-Of-Charge threshold ("0x0C-0D V_{CELL} EOC" on page 40), the VEOC bit ("0x81.7 VEOC" on page 73) is set and the $\overline{EOC}$ output ("EOC Pin (35)" on page 99) is pulled low. The VEOC bit and the $\overline{EOC}$ output resume normal conditions when the voltage on all cells drops back below the [V_{CELL} EOC - 117mV] threshold.

VEOC detection does not shut off the CFET, disabling CFET at the end of charge is controlled by the threshold "V_{CELL} OV" on page 35.

6.9 UV Detection & Response

If the voltage of any cell falls below the cell undervoltage threshold ("VCELL UV" on page 37) for a time exceeding cell overvoltage timer ("0x12-13 V_{CELL} UV Timer" on page 42), the device sets the Undervoltage Fault bit ("0x80.2 UVF" on page 72). Then, if "0x87.6 µCFET" on page 82 = 0, the ISL94202 turns the discharge FET OFF by setting "0x86.0 DFET" on page 82 to 0. When the UV fault is set, the pack has entered Undercharge Protection mode. The status of the charge FET remains unaffected.

While any cell voltage is less than a low voltage charge threshold ("0x0E-0F V_{CELL} LVCL" on page 40) and if the PCFETE bit ("0x4A.2 PCFETE" on page 68) is set, the PCFET output is turned on instead of the CFET output during charging. This enables a precharge condition to limit the charge current to undervoltage cells.

From the undervoltage condition, if the cells recover to above "0x06-07 V_{CELL} UVR" on page 38 for a time exceeding "0x12-13 V_{CELL} UV Timer" on page 42 plus three seconds, the ISL94202 pulses the LDMON output once every 256ms and looks for the absence of a load (see "LDMON Pin (38)" on page 104). The pulses are of programmable duration (0ms to 15ms) using the [LPW3:LPW0] bits. During the pulse period, a small current (~60µA) is output into the load. If there is no load, the LDMON voltage is higher than the recovery threshold of 0.6V. When the load has been removed and the cells are above the undervoltage recovery level, the ISL94202 clears the UV bit and, if µCFET = 0, turns on the discharge FET and resumes normal operation.

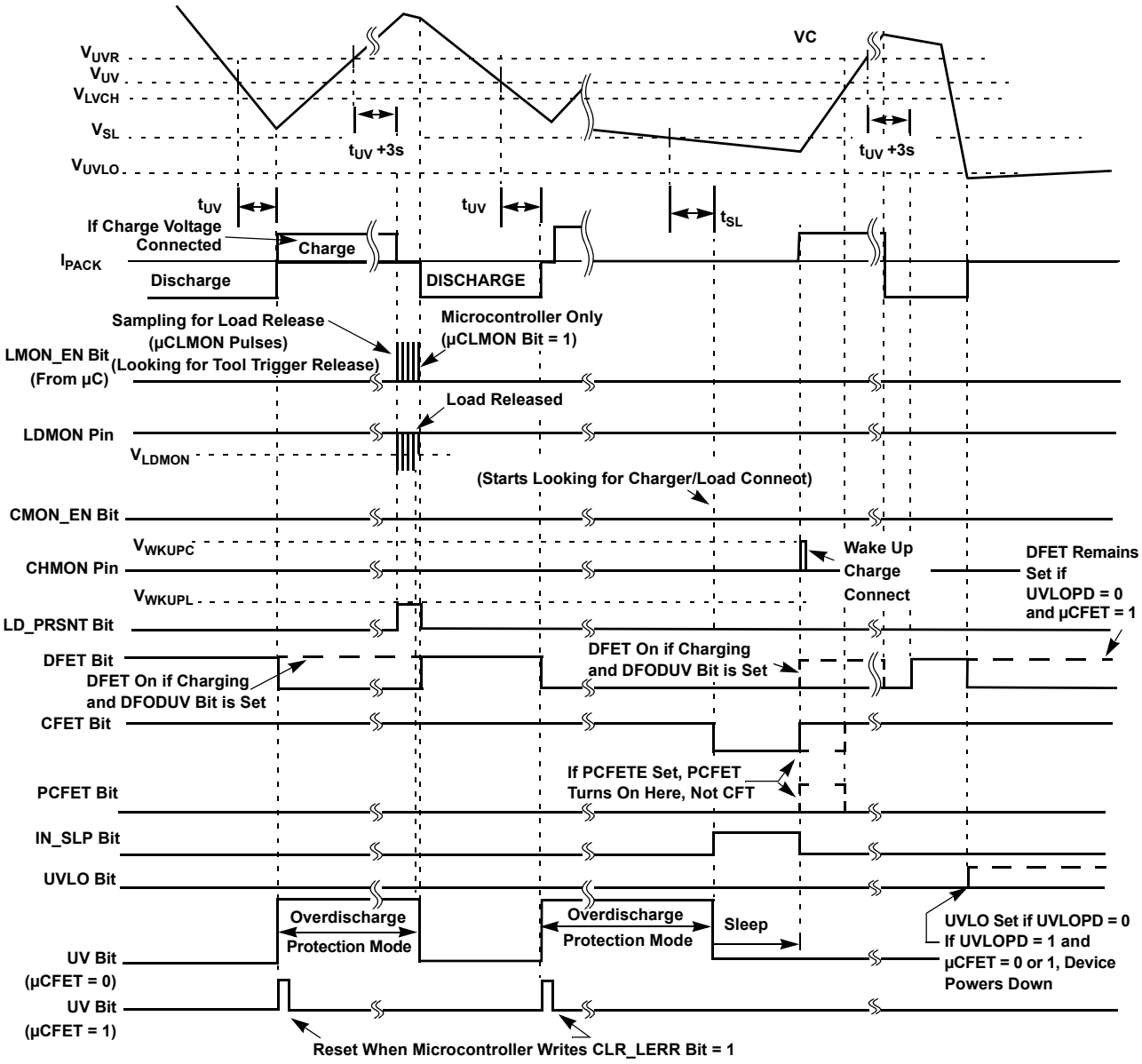


Figure 66. UV detection/response

The V_{CELL} UV detection and recovery timer is asynchronous to the voltage threshold. As a result, a setting of 1s can result in a delay time of 1s to 2s (and a recovery time of 3s to 4s), depending on when the UV/UVR is detected.

If any of the cells drop below a sleep threshold ("0x44-45 SLV" on page 64) for a period of time ("0x47.[2:1] SLTU" on page 65), the ISL94202 turns off both FETs (DFET and CFET = 0) and puts the pack into SLEEP Mode by

setting the Sleep bit ("0x83.6 IN_SLEEP" on page 78) to 1. If the µCFET bit is set, the device does not go to sleep.

There is also an undervoltage lockout condition. This is detected by comparing the cell voltages to a programmable UVLO threshold ("0x0A-0B V_{CELL} UVLO" on page 39). When any cell voltage drops below the UVLO threshold and remains below the threshold for five voltage scan periods (~160ms), the UVLO bit ("0x80.3 UVLOF" on page 72) is set and the $\overline{SD}$ output pin goes active. If UVLOPD = 0 and µCFET = 0, the DFET is also turned off. If UVLOPD = 1 ("0x4B.3 UVLOPD" on page 70), the ISL94202 goes into a "Powerdown State" on page 120.

If the µCFET bit is set to 1, the MCU must both turn off and turn on the discharge power FETs and control the sleep and power-down conditions.

The device includes an option to turn the discharge FET back on in an undervoltage condition, if there is a charge current flowing into the pack ("0x82.2 CHING" on page 77). This option is set by the "0x4B.5 DFODUV" on page 69 (DFET ON During Undervoltage) control bit. Then, if the charge current stops and there is still an undervoltage condition on the cell, the device again disables the discharge FET.

6.10 Current Monitoring/Response

The current monitor is an analog detection circuit that tracks the charge current, discharge current, and current direction. The current monitor circuit is on all the time, except in SLEEP and Power-Down Modes ("System Modes" on page 119). The power FETs are off in these two states.

The current monitor compares the voltage across the sense resistor to several different thresholds. These are discharge short-circuit ("0x1A-1B DSC & DSCT" on page 48), discharge overcurrent ("0x16-17 DOC & DOCT" on page 43), and charge overcurrent ("0x18-19 COC & COCT" on page 46). If the measured voltage exceeds the specified limit for a specified duration of time, the ISL94202 acts to protect the system.

The current monitor also tracks the direction of the current. This is a low-level detection and indicates the presence of a charge or discharge current. If either condition is detected, the ISL94202 sets an appropriate flag ("0x82.2 CHING" on page 77 and "0x82.3 DCHING" on page 76). The current-sense element is on the high-side of the battery pack.

The current-sense circuit has a gain x5, x50, or x500. The sense amplifier allows a very wide range of currents to be monitored. The gain settings allow a sense resistor in the range of 0.3mΩ to 5mΩ. A diagram of the current-sense circuit is shown in Figure 67 on page 133.

There are two parts of the current-sense circuit. The first part is a digital current monitor circuit. This circuit allows the current to be tracked by an external MCU or computer. The current-sense amplifier gain in this current measurement is set by "0x85.[5:4] CG" on page 79. The 14-bit offset adjusted ADC result of the conversion of the voltage across the current-sense resistor is saved to register "0xAA-AB - ADCV" on page 93, as well as a 12-bit value ("0x8E-8F IPACK" on page 90) that is used for threshold comparisons. The offset adjustment is based on a factory calibration value saved in EEPROM.

The digital readouts cover the input voltage ranges shown in Table 78.

Table 78. Maximum Current Measurement Range

Gain Setting	Voltage Range (mV)	Current Range (RSENSE = 1mΩ)
5x	-250 to 250	-250A to 250A
50x	-25 to 25	-25A to 25A
500x	-2.5 to 2.5	-2.5A to 2.5A

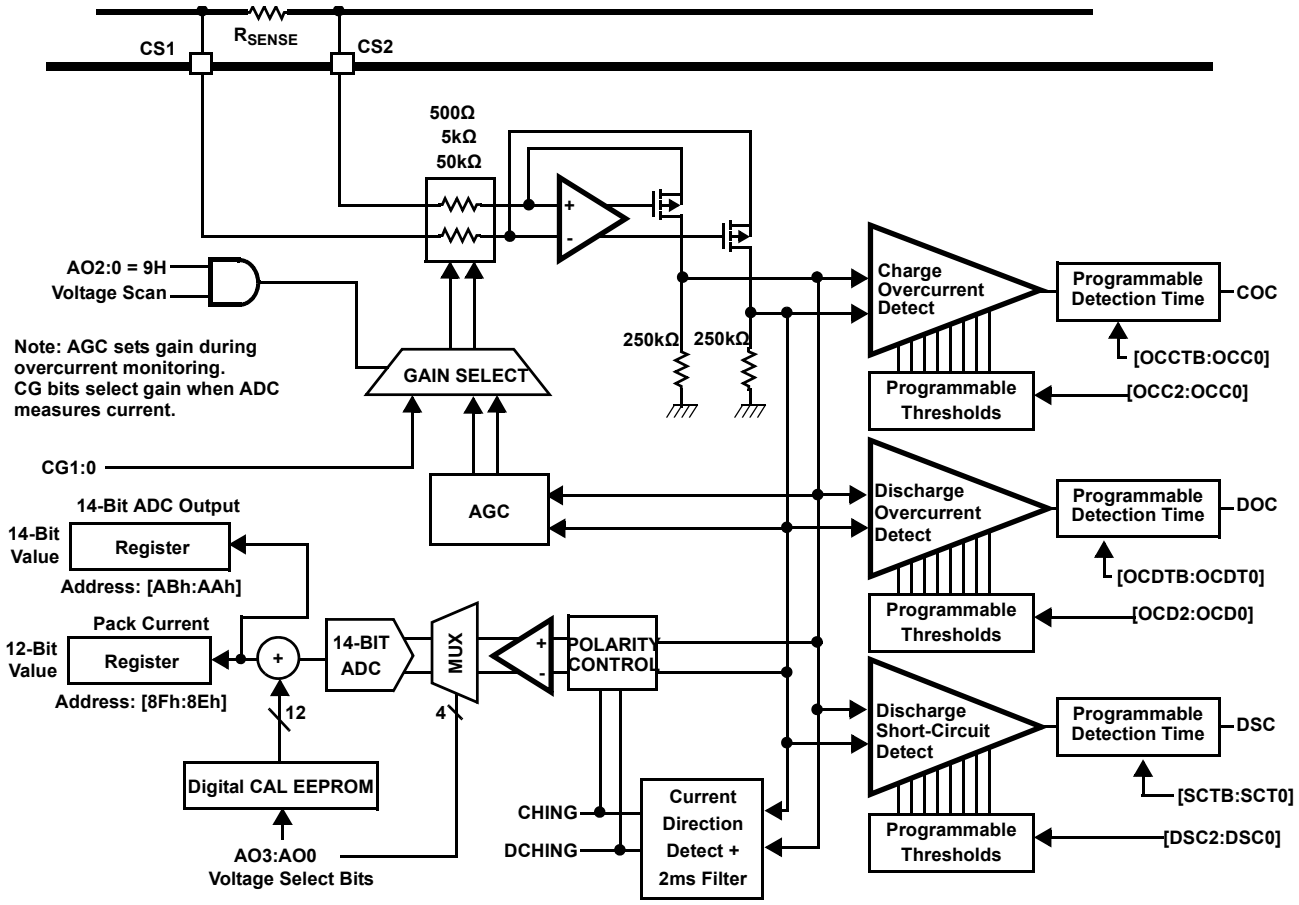


Figure 67. Current sense block diagram

The second part is the analog current direction, overcurrent, and short-circuit detect mechanisms. This circuit is on all the time. During the operation of the overcurrent detection circuit, the sense amplifier gain is automatically controlled.

For current direction detection, there is a 2ms digital delay for getting into or out of either direction condition, which means that the charge current detection circuit needs to detect an uninterrupted flow of current out of the pack for more than 2ms to indicate a discharge condition. Then, the current detector needs to identify that there is a charge current or no current for a continuous 2ms to remove the discharge condition.

The overcurrent and short-circuit detection thresholds are programmable values stored in the EEPROM. The charge and discharge overcurrent conditions and the discharge short-circuit condition need to be continuous for a period of time before an overcurrent condition is detected.

For more information on the relevant settings, review the following sections:

- Discharge Overcurrent - “0x16-17 DOC & DOCT” on page 43 & “DOCR” on page 45.
- Charge Overcurrent - “0x18-19 COC & COCT” on page 46 & “COCR” on page 47.
- Discharge Short Circuit - “0x1A-1B DSC & DSCT” on page 48 & “DSCR” on page 49.
- Current Direction - “0x82.2 CHING” on page 77 & “0x82.3 DCHING” on page 76.

6.10.1 Overcurrent and Short-Circuit Detection

The ISL94202 continually monitors current by mirroring the current across a current-sense resistor (between the CS1 and CS2 pins) to a resistor to ground.

- A discharge overcurrent condition exists when the voltage across the external sense resistor exceeds the discharge overcurrent threshold (set by the discharge overcurrent threshold bits) for an overcurrent time delay, set by the discharge overcurrent timeout bits (“0x16-17 DOC & DOCT” on page 43). This condition sets the fault

bit "0x81.2 DOCF" on page 74 high. The bit "0x82.0 LD_PRSNT" on page 77 is also set high at this time. If the µCFET bit is 0, the power FETs turn off automatically. If the µCFET bit is 1, the external MCU must control the power FETs ("0x87.6 µCFET" on page 82).

- A charge overcurrent condition exists when the voltage across the external sense resistor exceeds the charge overcurrent threshold (set by the charge overcurrent threshold bits) for an overcurrent time delay, set by the discharge overcurrent timeout bits ("0x18-19 COC & COCT" on page 46). This condition sets the fault bit "0x81.1 COCF" on page 75 high. The bit "0x82.1 CH_PRSNT" on page 77 is also set high at this time. If the µCFET bit is 0, the power FETs turn off automatically. If the µCFET bit is 1, the external MCU must control the power FETs.
- A discharge short-circuit condition exists when the voltage across the external sense resistor exceeds the discharge short-circuit threshold (set by the discharge short-circuit threshold bits) for an overcurrent time delay, set by the discharge short-circuit timeout bits ("0x1A-1B DSC & DSCT" on page 48). This condition sets the fault bit "0x81.3 DSCF" on page 74 high. The bit "0x82.0 LD_PRSNT" on page 77 is also set high at this time. The power FETs turn off automatically in a shortcircuit condition, regardless of the condition of the µCFET bit.

6.10.1.1 DOC and DSC Response

When the ISL94202 enters the discharge overcurrent protection or short-circuit protection mode, the ISL94202 begins a load monitor state. In the load monitor state, the ISL94202 waits three seconds and then periodically checks the load by turning on the "LDMON Pin (38)" on page 104 output for 0 to 15ms every 256ms. Program the pulse duration with the bits "0x05.7:4 LDPW" on page 37.

When turned on, the recovery circuit outputs a small current (~60µA) to flow from the device and into the load. With a load present, the voltage on the LDMON pin is low and the LD_PRSNT bit remains set to 1. When the load rises to a sufficiently high resistance, the voltage on the LDMON pin rises above the LDMON threshold and the LD_PRSNT bit is reset. When the load has been released for a sufficiently long period of time (two successive load sample periods), the ISL94202 recognizes that the conditions are OK and resets the bit "0x81.2 DOCF" on page 74 or bit "0x81.3 DSCF" on page 74. If the µCFET bit is 0, the device automatically re-enables the power FETs by setting the DFET and CFET (or PCFET) bits to 1 (assuming all other conditions are within normal ranges). If the µCFET bit is 1, the MCU must turn on the power FETs.

An external MCU can override the automatic load monitoring of the device. It does this by taking control of the load monitor circuit (set the bit "0x87.4 µCLMON" on page 83 = 1) and periodically pulsing the bit "0x86.6 LMON_EN" on page 80. When the MCU detects that LD_PRSNT = 0, it sets the bit "0x86.7 CLR_LERR" on page 80 to 1 (to clear the error condition and reset the DOC or DSC bit) and sets the DFET and CFET (or PCFET) bits to 1 to turn on the power FETs.

6.10.1.2 COC Response

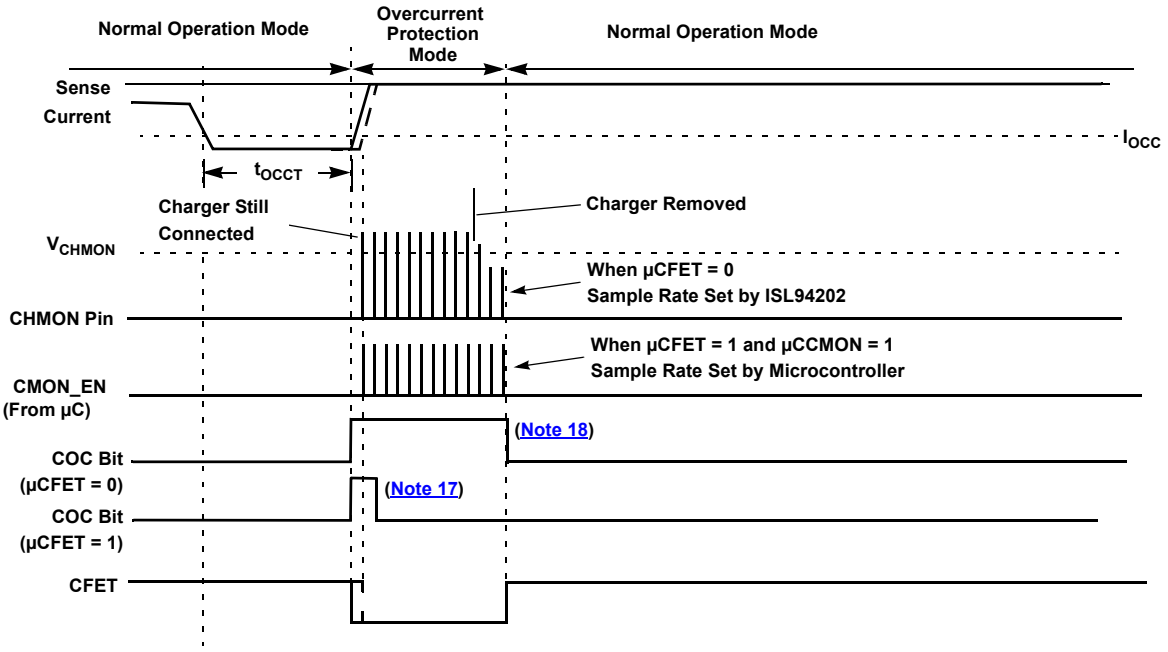
When the ISL94202 enters the Charge Overcurrent Protection mode, the ISL94202 begins a charger monitor state. In the charger monitor state, the ISL94202 periodically checks the charger connection by turning on the "CHMON Pin (37)" on page 99 output for 0ms to 15ms every 256ms. Program the pulse duration with the bits "0x01.7:4 CDPW" on page 36.

When turned on, the recovery circuit checks the voltage on the CHMON pin. With a charger present, the voltage on the CHMON pin is high (>9V) and the CH_PRSNT bit remains set to 1. When the charger connection is removed, the voltage on the CHMON pin falls below the CHMON threshold and the CH_PRSNT bit is reset. When the charger has been released for a sufficiently long period of time (two successive sample periods), the ISL94202 recognizes that the conditions are OK and clears the bit "0x81.1 COCF" on page 75.

If the µCFET bit is 0, the device automatically re-enables the power FETs by setting the DFET and CFET (or PCFET) bits to 1 (assuming all other conditions are within normal ranges). If the µCFET bit is 1, the MCU must turn on the power FETs.

An external MCU can override the automatic charger monitoring of the device. It does this by taking control of the load monitor circuit (set the bit "0x87.3 µCCMON" on page 83 = 1) and periodically pulsing the bit "0x86.4 CMON_EN" on page 81. When the MCU detects that CH_PRSNT = 0, it sets the bit "0x86.5 CLR_CERR" on

page 81 to 1 (to clear the error condition and reset the COC bit) and sets the DFET and CFET (or PCFET) bits to 1 to turn on the power FETs.



Notes:

17. When µCFET = 1, COC bit is reset when the CLR_CERR is set to 1.
18. When µCFET = 0, COC is reset by the ISL94202 when the condition is released.

Figure 68. COC Protection Mode

6.11 Temperature Monitoring/Response

As part of the normal voltage scan, the ISL94202 monitors both the temperature of the device (“0xA0-A1 ITEMP” on page 91) and the temperature of two external temperature sensors (see “Thermistor Pins (20-22)” on page 96). External Temperature 2 can be used to monitor the temperature of the FETs, instead of the cells, by setting the bit “0x4A.5 XT2M” on page 68 to 1.

The temperature voltages have two selectable gain settings (“0x4A.4 TGAIN” on page 68) applied to both pins. Setting the TGain bit = 0 (default) sets the gain to 2x, providing for a full scale input voltage = 0.9V. The device is calibrated at the default temperature gain setting of 2x, this is the preferred setting because it produces a more linear temperature response.

The temperature management state machine is detailed in Figure 69 on page 137.

6.11.1 Charging Temperature

There are four relevant temperature thresholds in effect when the ISL94202 detects a charge current (“0x82.2 CHING” on page 77). These thresholds consist of two out of bounds levels and their complementary recovery levels.

- When the external temperature on xT1 or xT2 exceeds threshold Charge Over-Temperature (“0x30-31 COT” on page 56), fault bit “0x80.6 COTF” on page 71 is set to 1 and the CFET (“CFET Pin (45)” on page 108) is turned off. If “0x87.6 µCFET” on page 82 = 1, an external MCU must turn off the CFET.
- When the external temperature on xT1 and xT2 falls back below threshold Charge Over-Temperature Recovery (“0x32-33 COTR” on page 57) following a COTF condition previously detected, the fault bit COTF clears and the CFET is turned on (if all other safe operating conditions are met). If µCFET = 1, an external MCU must turn on the CFET.

- When the external temperature on xT1 or xT2 falls below threshold Charge Under-Temperature (“0x34-35 CUT” on page 58), fault bit “0x80.7 CUTF” on page 71 is set to 1 and the CFET is turned off. If µCFET = 1, an external MCU must turn off the CFET.
- When the external temperature on xT1 and xT2 rises back above threshold Charge Under-Temperature Recovery (“0x36-37 CUTR” on page 58) following a CUTF condition previously detected, the fault bit CUTF clears and the CFET is turned on (if all other safe operating conditions are met). If µCFET = 1, an external MCU must turn on the CFET.

If “0x4A.2 PCFETE” on page 68 = 1, PCFET (“PCFET Pin (44)” on page 108) follows the state of the CFET pin.

6.11.2 Discharging Temperature

There are four relevant temperature thresholds in effect when the ISL94202 detects a discharge current (“0x82.3 DCHING” on page 76). These thresholds consist of two out of bounds levels and their complementary recovery levels.

- When the external temperature on xT1 or xT2 exceeds threshold Discharge Over-Temperature (“0x38-39 DOT” on page 59), fault bit “0x80.4 DOTF” on page 72 is set to 1 and the DFET (“DFET Pin (42)” on page 108) is turned off. If “0x87.6 µCFET” on page 82 = 1, an external MCU must turn off the DFET.
- When the external temperature on xT1 and xT2 falls back below threshold Discharge Over-Temperature Recovery (“0x3A-3B DOTR” on page 60) following a DOTF condition previously detected, the fault bit DOTF clears and the DFET is turned on (if all other safe operating conditions are met). If µCFET = 1, an external MCU must turn on the DFET.
- When the external temperature on xT1 or xT2 falls below threshold Discharge Under-Temperature (“0x3C-3D DUT” on page 61), fault bit “0x80.5 DUTF” on page 72 is set to 1 and the DFET is turned off. If µCFET = 1, an external MCU must turn off the DFET.
- When the external temperature on xT1 and xT2 rises back above threshold Discharge Under-Temperature Recovery (“0x3E-3F DUTR” on page 61) following a DUTF condition previously detected, the fault bit DUTF clears and the DFET is turned on (if all other safe operating conditions are met). If µCFET = 1, an external MCU must turn on the DFET.

6.11.3 Internal Temperature

There are two internal temperature thresholds independent of current direction. These thresholds consist of an out of bounds level and its complementary recovery level.

- Internal over-temperature (“0x40-41 IOT” on page 62) - When the internal temperature exceeds this threshold, bit “0x81.0 IOTF” on page 75 is set to 1 and all power FETs are turned off regardless of the state of “0x87.6 µCFET” on page 82.
- Internal over-temperature recovery (“0x42-43 IOTR” on page 63) - When the internal temperature falls below this threshold, bit “0x81.0 IOTF” on page 75 is automatically cleared to 0 and all power FETs are allowed to turn back on. If “0x87.6 µCFET” on page 82 = 1, an external MCU must turn on any FETs.

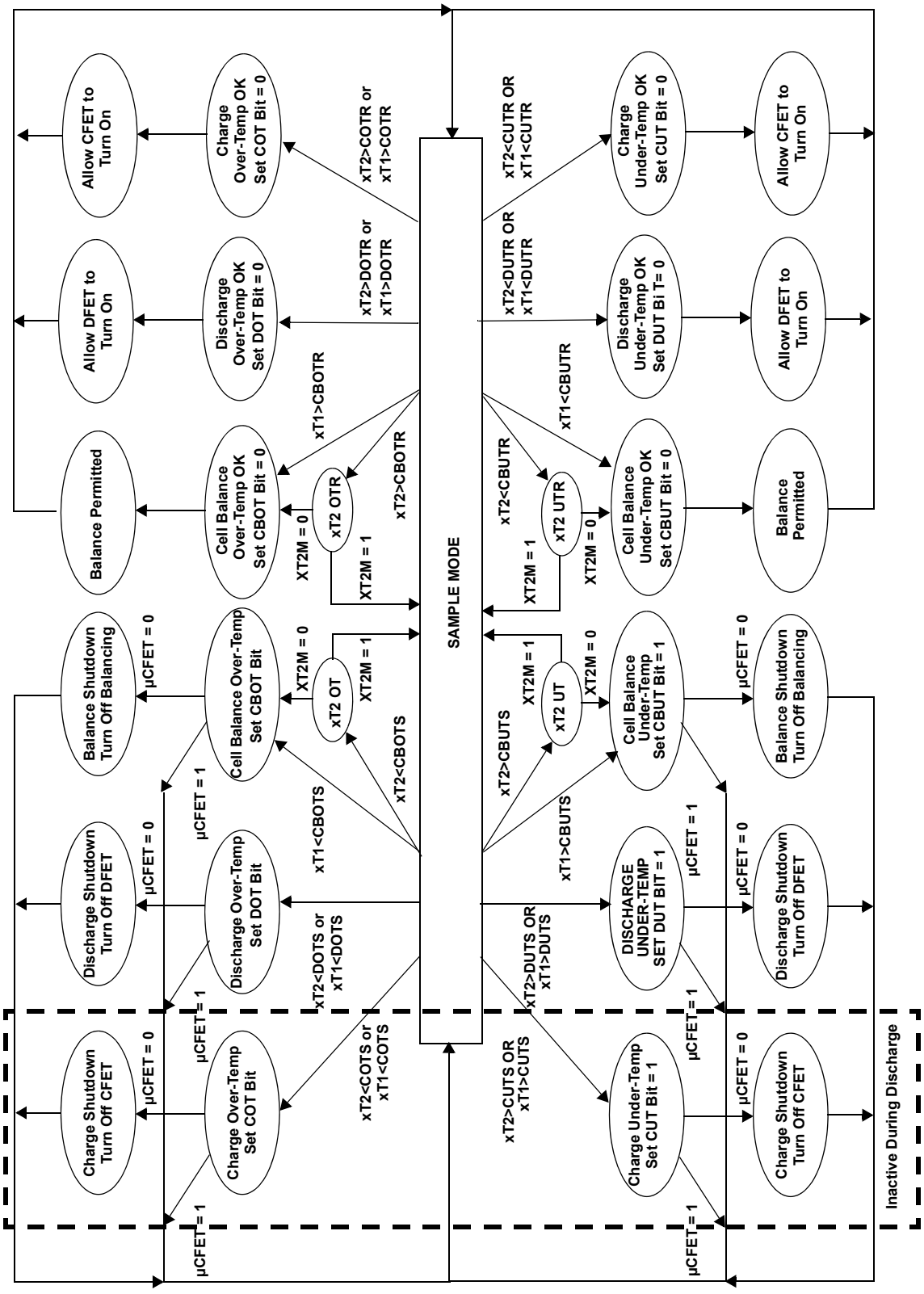


Figure 69. Temperature Management State Machine

6.12 Operational Options

The ISL94202 is a flexible and configurable device. It is capable of operating as a complete standalone Battery Management System (BMS), as MCU dependent battery front end or a combination of both.

6.12.1 Control/Data Registers

Operation and control of ISL94202 is accomplished through three groups of registers. The first group is the EEPROM and the Configuration Registers that are backed up by the EEPROM (Table 2 on page 32). The second group, the Operations Registers (Table 46 on page 71), contain status, and control registers to support an optional MCU. The last group, the Data Registers, contains the measurement results (Table 60 on page 86).

The EEPROM is customer programmable non-volatile memory that contains all configuration data necessary for standalone operation. EEPROM contents are copied to the configuration registers upon power-up/Power-On Reset (POR). The ISL94202 operates based on the settings in these configuration registers, not from the EEPROM itself. The configuration registers are volatile (contents lost in "Powerdown State" on page 120) and are used by the ISL94202 internally during operation. The EEPROM and configuration registers share the same register address 0x00 - 0x57 with access determined by control bit "0x89.0 EEEN" on page 85. This control bit is not backed up by EEPROM, so on POR the device starts up assuming standalone operation.

When EEEN = 1, access to register address 0x00 - 0x57 writes to and reads from EEPROM. When EEEN = 0, access to register address 0x00 - 0x57 writes to and reads from configuration registers.

EEEN does not reset automatically (care must be taken when setting this bit to 1 to ensure that it is reset to 0 when interaction with the EEPROM is finished).

Changes to the EEPROM does not effect device operation or the configuration registers until the devices resets.

Changes to the configuration registers do not effect the EEPROM but take effect on device operation immediately.

Figure 70 shows the register sets and their relationships in the ISL94202.

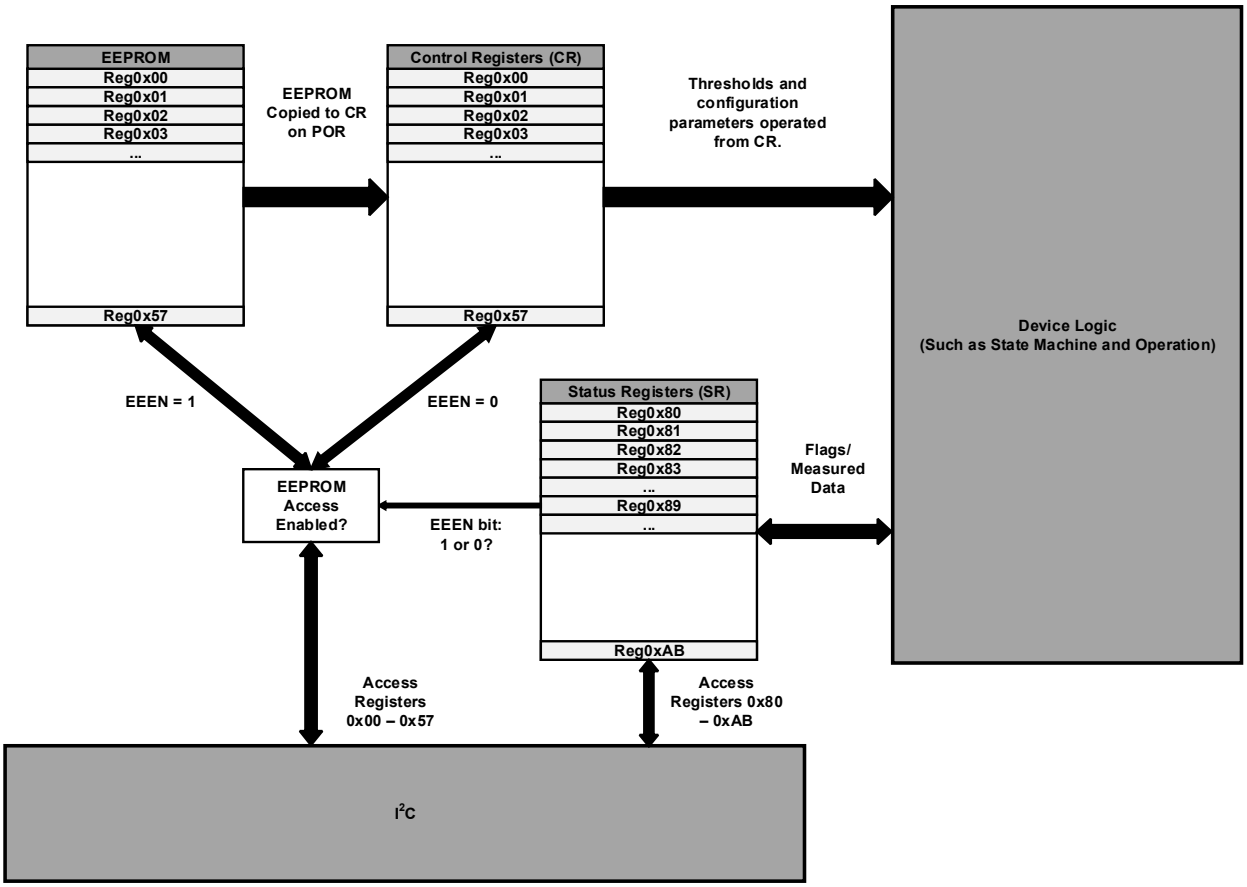


Figure 70. Register Groups

6.12.1.1 EEPROM

The ISL94202 contains an EEPROM array for storing the device configuration parameters, the device calibration values, and some user data registers. Access to the EEPROM is through the I^2C port of the device. Memory is organized in memory maps as described in:

- "Register List" on page 32
- "EEPROM Page/Register Summary" on page 145
- "Page/Register Summary" on page 145

When the device powers up, the ISL94202 transfers the contents of the configuration EEPROM memory areas to the device Configuration Registers ("0x00-0x4B Configuration Registers" on page 32). The user EEPROM has no associated registers. An external MCU can read the contents of the Configuration Registers or the contents of the EEPROM. Prior to reading the EEPROM, set the EEEN bit to 1 ("EEPROM Access" on page 147). This enables access to the EEPROM area. If EEEN is 0, a read or write occurs in the Configuration Register area.

The content of the Configuration Registers determines the operation of the device.

Reading from the registers can be done using a byte or page read. See:

- "Current Address Read" on page 146
- "Random Read" on page 146
- "Sequential Read" on page 146

Reading from the EEPROM should be done using a byte read only, if reading the first byte of a 4-byte page (such as 0x00, 0x04, and 0x08), repeat the read transaction twice (see "EEPROM Read" on page 148).

You are advised not to use page transfers when reading or writing to EEPROM. Only single byte I^2C transactions should be used. In addition, Write transactions should be separated with a 30ms delay to enable each byte write operation to complete.

- "EEPROM Access" on page 147
- "EEPROM Write" on page 148

The EEPROM contains an error detection and correction mechanism. When reading a value from the EEPROM, the device checks the data value for an error.

If there are no errors, the EEPROM value is valid and the ECC_USED and ECC_FAIL bits are set to 0. If there is a 1-bit error, the ISL94202 corrects the error and sets the ECC_USED bit. This is a valid operation and value read from the EEPROM is correct. During an EEPROM read if there is an error consisting of two or more bits, the ISL94202 sets the ECC_FAIL bit (ECC_USED = 0). This read contains invalid data.

The error correction is also active during the initial power-on recall of the EEPROM values to the Configuration Registers. The circuit corrects for any one-bit errors. Two-bit errors are not corrected and the contents of the Configuration Registers maintain the previous value.

Internally, the power-on recall circuit uses the ECC_USED and ECC_FAIL bits to determine there is a proper recall before allowing the device operation to start. However, an external MCU cannot use these bits to detect the validity of the Configuration Registers on power-up or determine the use of the error correction mechanism, because the bits automatically reset on the next valid read.

6.12.2 Standalone

The ISL94202 is designed to be a standalone battery pack monitor. It provides monitor and protection functions using state machines without requiring an external MCU. The device operates using negative control, it always turns on and functions unless there is a fault condition preventing it.

The part operates power control FETs on the high side with a built-in charge pump for driving N-channel FETs. The current-sense function is also on the high side.

To extend battery life, power is minimized in all areas with parts of the circuit automatically powered down a majority of the time.

The ISL94202 includes:

- 14-bit ADC converter, with calibrated voltage measurements saved as 12-bit results in data registers
- Automatic scan of the cell voltages; overvoltage, undervoltage, and sleep voltage monitoring
- Selectable overcurrent detection settings
- Eight discharge overcurrent thresholds
- Eight charge overcurrent thresholds
- Eight short-circuit thresholds
- 12-bit programmable discharge overcurrent delay time
- 12-bit programmable charge overcurrent delay time
- 12-bit programmable short-circuit delay time
- Current-sense monitor with gain
- Second external temperature sensor for use in monitoring the pack or power FET temperatures
- EEPROM for storing operating parameters
- Automatic Charger and Load detection

6.12.3 MCU Control

The ISL94202 can be used as a complete Battery Front End (BFE), which means all internal circuitry can be operated and controlled by an external MCU. This configuration would typically leverage a small, inexpensive MCU with an I^2C port to control the logic of the ISL94202. For example, the MCU would contain the state machine while using the ISL94202 as a tool to access pack information and drive circuitry.

By using the override bits found in register “0x87 - Control 2 (R/W)” on page 82 you can enable the MCU override of the default functionality of the ISL94202.

The only exceptions to this are under the following faults:

- “0x80.1 OVLOF” on page 73
- “0x81.3 DSCF” on page 74
- “0x81.0 IOTF” on page 75
- “0x83.6 IN_SLEEP” on page 78
- “Mode Exceptions” on page 122
- “FETSOFF Pin (33)” on page 98

During these conditions, power FETs have a set behavior, see “MCU FET Control” on page 110.

6.12.4 Mixed Control

The Mixed Control is an implementation of the ISL94202 that provides the most system redundancy, although an increase in design effort is required to implement. By combining the use of the override bits (using an external MCU) with autonomous functionality of the ISL94202, you can pick and chose which functions you would like autonomous and which you would like control over from an external MCU.

To implement a design of this nature you must have a thorough understanding of the ISL94202 datasheet, specifically “System Registers” on page 32, “0x87 - Control 2 (R/W)” on page 82, “System Operation” on page 114, and the “Communication Interface” on page 141.

7. Communication Interface

The ISL94202 uses an I²C interface for you to configure operation and monitor input and output parameters. Serial communication is functional anytime the chip is not being reset or in "Powerdown State" on page 120.

The ISL94202 supports sequential read, which can start at any register address. If the master continues to send clock cycles or a presence bit is sent after reading one byte, the device indexes to the next byte and returns the byte value. This continues until the stop bit is received.

Register read/write access is executed using a byte operation (read/write 1 byte) or page operation (read/write 4 bytes).

- The ISL94202 uses a standard I²C interface, except the design separates the SDA input and output (SDAI and SDAO)
- Separate SDAI and SDAO lines can be tied together and operate as a typical I²C bus
- Interface speed is 400kHz, maximum

7.1 I²C Interface

The ISL94202 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL94202 operates as the slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first. Therefore, the first address bit sent is Bit 7.

7.1.1 I²C Address

The ISL94202 can be used with any I²C host device. Each device must have its own unique serial address to distinguish it from other devices on the bus. The device address is set by connecting the "ADDR Pin (24)" on page 97 to either the "RGO Pin (36)" on page 99 or the "VSS Pin (18, 28, 29)" on page 95). The available addresses are listed in Table 79.

Table 79. ADDR matrix

ADDR state	Read/Write	Binary Address	Hex Address
High	Read	b0101 0010	0x52
	Write	b0101 0011	0x53
Low	Read	b0101 0000	0x50
	Write	b0101 0001	0x51

The last bit of the Slave Address byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a 1, a Read operation is selected. A 0 selects a Write operation.

7.1.2 Clock/Data Timing

Data states on the SDA line can change only while SCL is LOW. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (Figure 72 on page 142). At power-up, the SDA pin is an input.

7.1.3 Start Condition

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (Figure 72). A START condition is ignored during the power-up sequence.

7.1.4 Stop Condition

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (Figure 72). A STOP condition at the end of a Read operation, or at the end of a Write operation returns the I^2C state machine to its initial state where it waits for the next START.

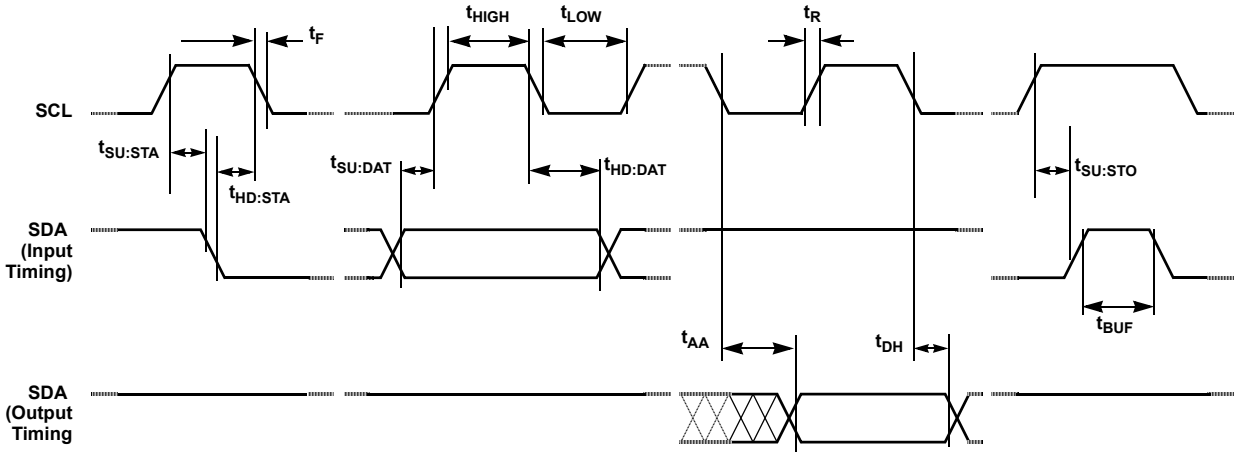


Figure 71. I^2C Timing

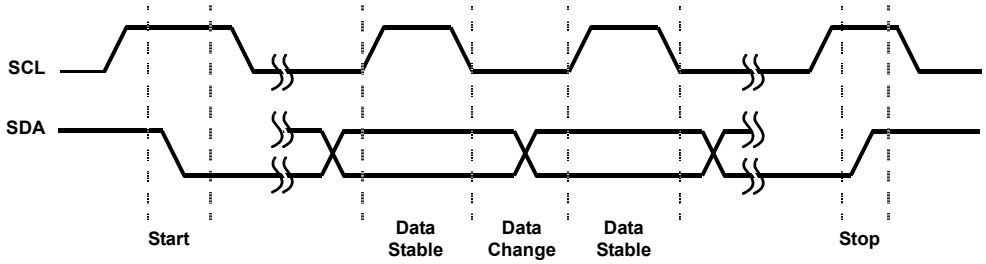


Figure 72. Valid Data Changes, Start, and Stop Conditions

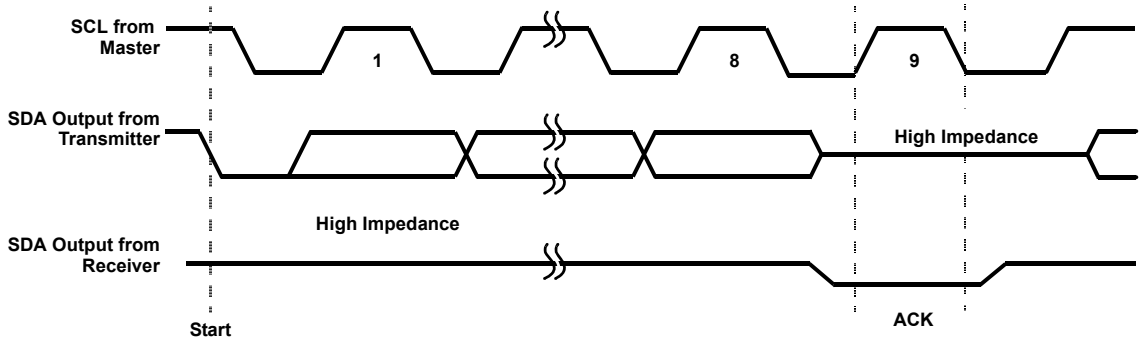


Figure 73. Acknowledge Response from Receiver

7.1.5 Acknowledge

An Acknowledge (ACK) is a software convention that indicates a successful data transfer. The transmitting device, either master or slave, releases the SDA line after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (Figure 73).

The device responds with an ACK after recognition of a START condition followed by a valid Slave Address byte. If a write operation is selected, the device responds with an acknowledge after the receipt of each subsequent eight bits. The device acknowledges all incoming data and address bytes, except for the slave byte when the contents do not match the device internal slave address. Attempting to write to a protected block of memory suppresses the acknowledge bit.

In the read mode, the device transmits eight bits of data, releases the SDA line, then monitors the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device continues to transmit data. The device terminates further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

7.1.6 Write Operation

A Write operation requires a START condition, followed by a Slave Address byte, a Register Address byte, a Data byte, and a STOP condition. The slave device responds with an ACK after successfully receiving each of the three bytes.

7.1.6.1 Byte Write

For a byte write operation, the device requires the Slave Address Byte and a Word Address Byte, which gives the master access to any one of the words in the array. After receipt of the Word Address Byte, the device responds with an acknowledge and awaits the next eight bits of data. After receiving the eight bits of the Data Byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle. During this internal write cycle, the device inputs are disabled, so the device does not respond to any requests from the master. The SDA output is at high impedance.

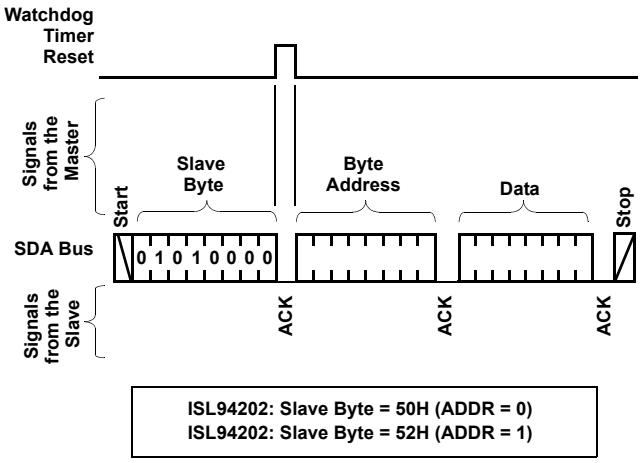


Figure 74. Byte Write Sequence

A write to a protected block of memory suppresses the acknowledge bit.

When writing to the EEPROM, write to all addresses of a page without an intermediate read operation, but do not use a page write operation to write to the EEPROM. Each page is four bytes long, starting at Address 0.

7.1.6.2 Page Write

Do not use a page write operation to write to the EEPROM. A page write operation is initiated in the same manner as the byte write operation; however, instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the device responds with an acknowledge and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it rolls over and goes back to 0 on the same page. This means that the master can write four bytes to the page starting at any location on that page. If the master begins writing at Location 2 and loads four bytes, the first two bytes are written to Locations 2 and 3 and the last two bytes are written to Locations 0 and 1. Afterwards, the address counter would point to Location 2 of the page that was just written. If the master supplies more than four bytes of data, new data overwrites the previous data, one byte at a time. See Figures 75 and 76.

Do not write to addresses 58H through 7FH or locations higher than address ABH, because these addresses access registers that are reserved. Writing to these locations can result in unexpected device operation.

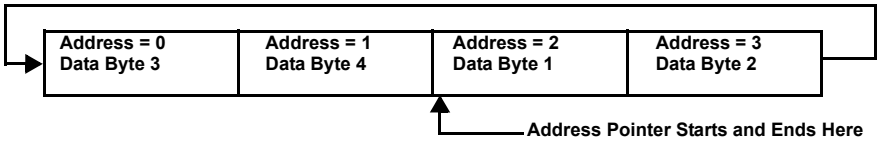


Figure 75. Writing 4 Bytes to A 4-Byte Page Starting at Location 2

Register and page groupings for the EEPROM backed Configuration Registers are summarized in Table 80 on page 145, the groupings for the Operations Registers are summarized in Table 81 on page 145. The value represented by the x in the column headers is determined by the value of the ADDR in the row being evaluated.

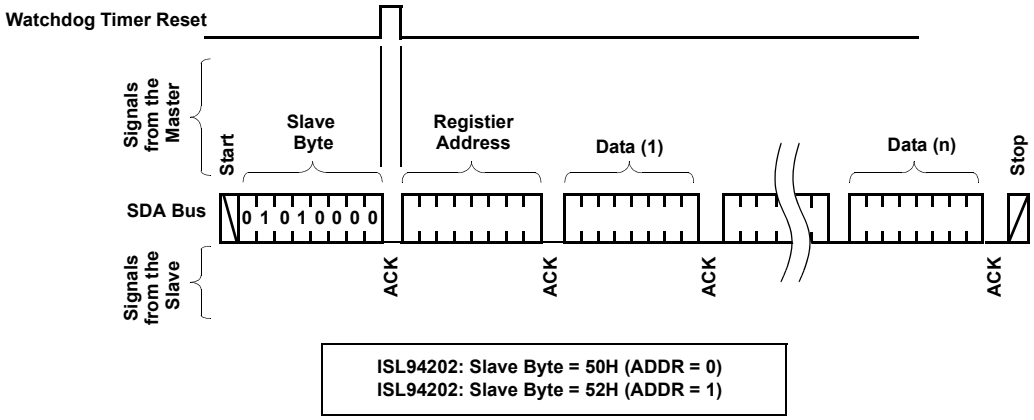


Figure 76. Page Write Sequence

Table 80. EEPROM Page/Register Summary

EEPROM (Configured as 32 4-Byte Pages)							
Page	**ADDR**	**0x**	**1x**	**2x**	**3x**	**4x**	**5x**
0	0	Overvoltage Level	Overvoltage Delay Timer	Minimum CB Delta	Charge Over-Temperature Level	Internal Over-Temperature Level	User EEPROM
	1						
	2	Overvoltage recovery	Undervoltage Delay Timer	Maximum CB Delta	Charge Over-Temp Recovery	Internal Over-Temperature Recovery	
	3						
1	4	Undervoltage Level	Open Wire Timing	Cell Balance On time	Charge Under-Temperature Level	Sleep Voltage	
	5						
	6	Undervoltage Recovery	Discharge Overcurrent Timeout Settings, Discharge Setting	Cell Balance Off Time	Charge Under-Temperature Recovery	Sleep Delay Timer/ Watchdog Timer	
	7						
2	8	OVLO Threshold	Charge overcurrent Timeout Settings, Charge overcurrent Setting	Minimum CB Temperature Level	Discharge Over-Temperature Level	Sleep Mode Timer	Reserved
	9					CELLS Config	
	A	UVLO Threshold	Short-Circuit Timeout Settings/ Recovery Settings, Short-Circuit Setting	Minimum CB Temperature Recovery	Discharge Over-Temperature Recovery	Features 1	
	B					Features 2	
3	C	EOC Voltage Level	Minimum CB Volts	Maximum CB Temperature Level	Discharge Under-Temperature Level	Reserved	
	D						
	E	Low Voltage Charge Level	Maximum CB Volts	Maximum CB Temperature Recovery	Discharge Under-Temperature Recovery		
	F						

Table 81. Page/Register Summary

Registers				
Page	**ADDR**	**8x**	**9x**	**Ax**
0	0	Status1	CELL1 Voltage	iT Voltage
	1	Status2		
	2	Status3	CELL2 Voltage	xT1 Voltage
	3	Status4		
1	4	Cell Balance	CELL3 Voltage	xT2 Voltage
	5	Analog Out		
	6	FET Cntl/Override Control Bits	CELL4 Voltage	VBATT/16 Voltage
	7	Override Control Bits		
2	8	Force Ops	CELL5 Voltage	VRGO/2 Voltage
	9	EE Write Enable		
	A	CELLMIN Voltage	CELL6 Voltage	14-bit ADC Voltage
	B			
3	C	CELLMAX Voltage	CELL7 Voltage	Reserved
	D			
	E	ISense Voltage	CELL8 Voltage	
	F			

7.1.7 Read Operation

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to 1. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

7.1.7.1 Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power-up, the address of the address counter is undefined, requiring a read or write operation for initialization. See Figure 77.

On receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition.

It should be noted that the ninth clock cycle of the read operation is not a don't care. To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

7.1.7.2 Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a dummy write operation. The master issues the start condition and the Slave Address Byte, receives an acknowledge, then issues the Word Address Bytes. After acknowledging receipts of the Word Address Bytes, the master immediately issues another start condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition (see Figure 78 on page 147)

7.1.7.3 Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first Data Byte is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition

The data output is sequential, with the data from address n followed by the data from address n+1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter rolls over to address 0000H and the device continues to output data for each acknowledge received. See Figure 79 on page 147 for the acknowledge and data transfer sequence.

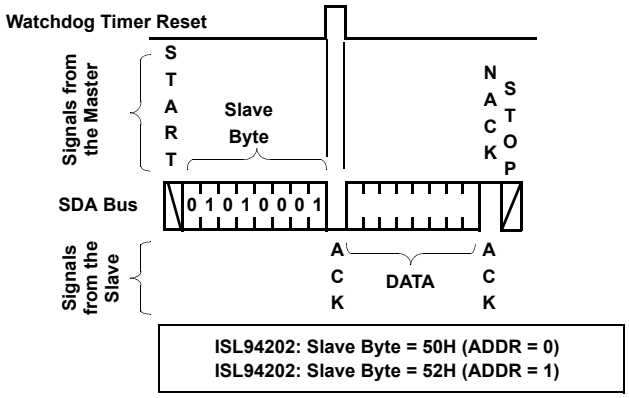


Figure 77. Current Address Read Sequence

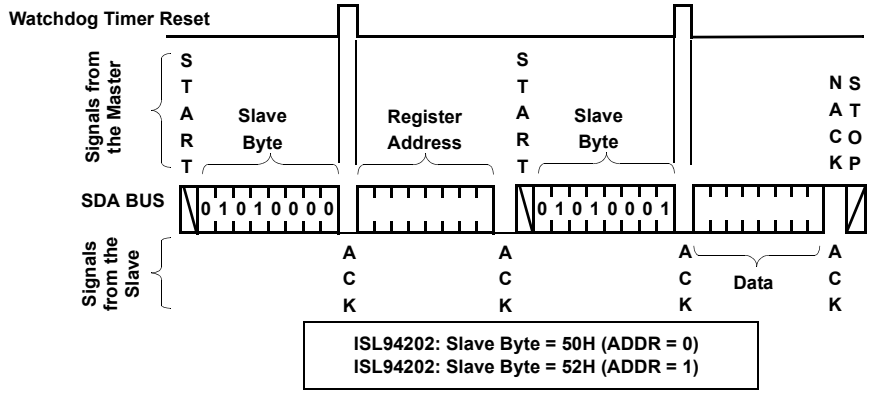


Figure 78. Random Read Sequence

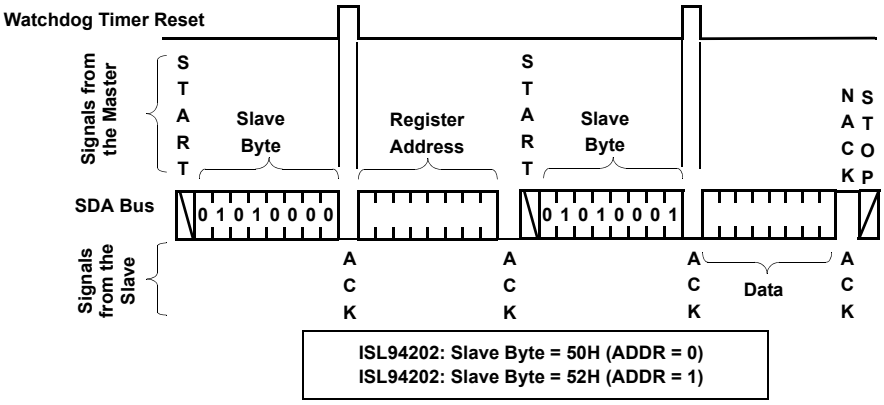


Figure 79. Sequential Read Sequence

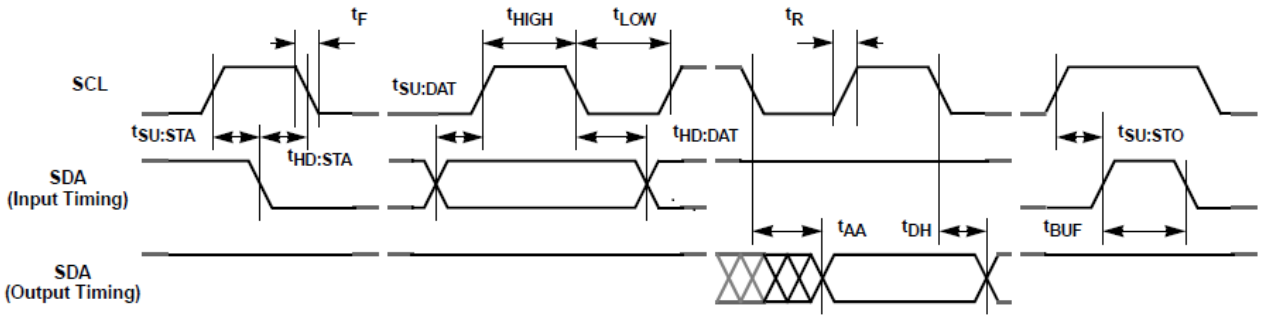


Figure 80. I²C Timing

7.1.8 EEPROM Access

You are advised not to use page transfers when reading or writing to EEPROM. Only single byte I²C transactions should be used. In addition, Write transactions should be separated with a 30ms delay to enable each byte write operation to complete.

The entire EEPROM is write protected on initial power-up and during normal operation. An enable byte allows writing to various areas of the memory array.

The enable byte is encoded, so that a value of 0 in the EEPROM Enable register ("0x89.0 EEEN" on page 85) enables access to the shadow memory (registers), a value of 1 allows access to the EEPROM.

After a read or write of the EEPROM, the MCU should reset the EEPROM Enable register value back to zero to prevent inadvertent writes to the EEPROM and to turn off the EEPROM block to reduce current consumption. If the MCU fails to reset the EEPROM bit and communications to the chip stops, the Watchdog timer ("0x47.[7:3] WDT" on page 65) resets the EEPROM select bit.

7.1.9 EEPROM Read

The ISL94202 has a special requirement when reading the EEPROM. An EEPROM read operation from the first byte of a four byte page (locations 0H, 4H, 8H, etc.) initiates a recall of the EEPROM page. This recall takes more than 200µs, so the first byte may not be ready in time for a standard I^2C response. In some applications, it may be necessary to read this first byte of every page two times.

7.1.10 EEPROM Write

Renesas provides an EEPROM Programming GUI and User Manual available for download from our website, see the ISL94202 device page.

The ISL94202 also has specific requirements when writing the EEPROM. An EEPROM write operation to the first byte of a four byte page (such as 0H, 4H, and 8H locations) initiates a recall of the EEPROM page. This recall takes more than 200µs, so the first byte may not be ready in time for a standard I^2C write. In some applications it may be necessary to write this first byte of every page two times. These duplicate writes should be separated with a 30ms delay and followed with a 30ms delay. Again, only single byte transactions should be used with a 30ms delay between each write operation.

To write the ISL94202 EEPROM, there are a number of steps that must be followed. Prior to writing to the ISL94202 EEPROM ensure:

- The device is in NORMAL or IDLE mode
- No faults are present
- No load or charger is connected

The following subsections detail how EEPROM programming should be executed.

7.1.10.1 Prepare the ISL94202

The first step is to set the ISL94202 Mode ("System Modes" on page 119). Force the ISL94202 into IDLE Mode by setting register "0x88.0 IDLE" on page 85 to 0x01. This setting prevents the device from transitioning to lower modes based on the timer selections ("0x48 Mode Timers" on page 66). This setting cannot prevent a mode transition due to a fault.

The ISL94202 EEPROM cannot be programmed if the device is in SLEEP Mode or the Powerdown State, nor can IDLE Mode be forced using Register 0x88 if the device is in SLEEP Mode or Powerdown. You must take steps to transition the device to NORMAL Mode; a CHMON or LDMON detection is required ("Wake Up" on page 115).

After forcing IDLE Mode, automatic scans are disabled by setting Register "0x87 - Control 2 (R/W)" on page 82 to 0x04. Disabling automatic scans prevents faults detected during measurement scans caused by any programming induced glitches from forcing the device into SLEEP Mode or Powerdown. Mode transition during EEPROM programming must be avoided.

The next step is to set the Sleep Voltage Threshold Registers "0x44-45 SLV" on page 64 to 0x00 (0V). This setting prevents a low cell voltage from causing the device to transition to SLEEP Mode. Because measurement scans were disabled in the previous paragraph, this step is redundant.

7.1.10.2 Program EEPROM

EEPROM programming can begin now that the ISL94202 is in a known state. Set register “0x89 - EEPROM Enable” on page 85 to 0x01 to enable access to the EEPROM instead of the Configuration Registers. This description is a simplification, as with any EEPROM actual programming requires multiple steps. This setting enables a state machine that handles EEPROM programming for the user.

When writing to the EEPROM there are two important guidelines to follow:

- Only single byte writes are permitted, do not attempt multi-byte transfers
- Wait 30ms between each EEPROM write

7.1.10.3 Verify EEPROM

After the Program EEPROM step, read the EEPROM back to verify it was programmed correctly. Following verification, pass or fail, the device register changes made in “Prepare the ISL94202” on page 148 should be returned to normal (not to be confused with NORMAL mode):

1. Set “0x89 - EEPROM Enable” on page 85 to 0x00 to switch from EEPROM to Register access
2. Set “0x87 - Control 2 (R/W)” on page 82 to 0x00 to put the device back into automatic mode
3. Set “0x44-45 SLV” on page 64 back to desired values

Renesas highly recommends writing the Configuration Registers with the same values as the EEPROM after a successful Write EEPROM. Only a POR transfers the EEPROM settings to the Configuration Registers. This can also be accomplished by forcing Powerdown then waking the device.

7.2 Synchronizing MCU Operations with Internal Scan

Internal scans occur every 32ms in NORMAL Mode, 256ms in IDLE Mode, and 512ms in DOZE Mode. The internal scan normally takes about 1.3ms, with every fourth scan taking about 1.7ms. While the percentage of time taken by the scan is small, it is long enough that random communications from the MCU can coincide with the internal scan. When the two operations happen at the same time, errors can occur in the returned values.

To avoid errors in the returned values, the goal is to synchronize external I^2C transactions so that they only occur during the device Low Power State (NOT Powerdown State, see Figure 58 on page 118). To assist in the synchronization, the MCU can use the INT_SCAN bit. This bit is 0 during the internal scan and 1 during the Low Power State.

The MCU software should look for the INT_SCAN bit to go from a 0 to a 1 to allow the maximum time to complete read or write operations. This ensures that the results reported to the MCU are from a single scan and changes made do not interfere with state machine detection and timing.

Alternately, the MCU can stop and restart scan with bit “0x87.2 µCSCAN” on page 84.

8. Reduced Cell Count

Suggested connections for pack configurations varying from three cells to eight cells are shown in Figure 81.

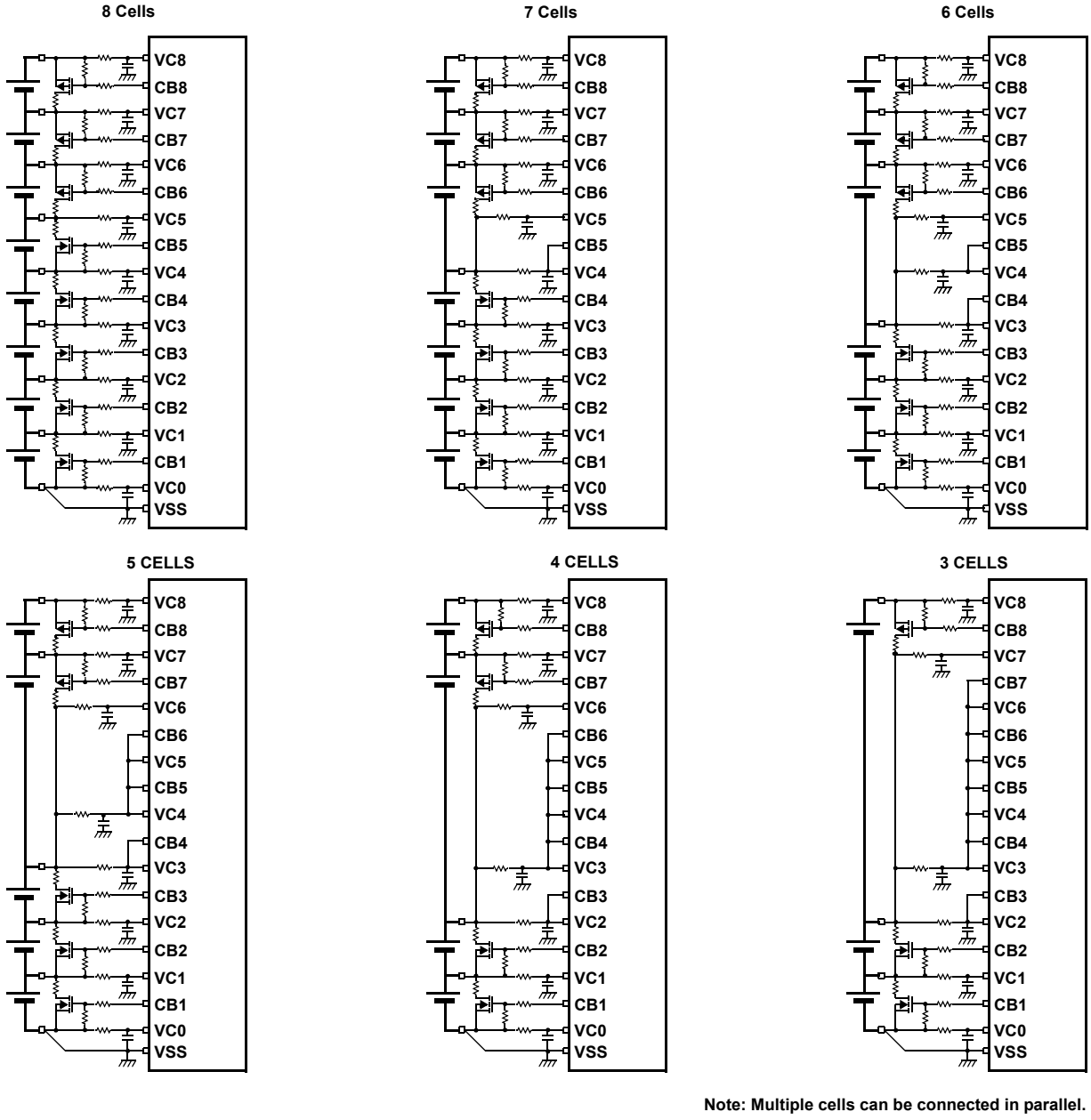


Figure 81. Battery Connection Options

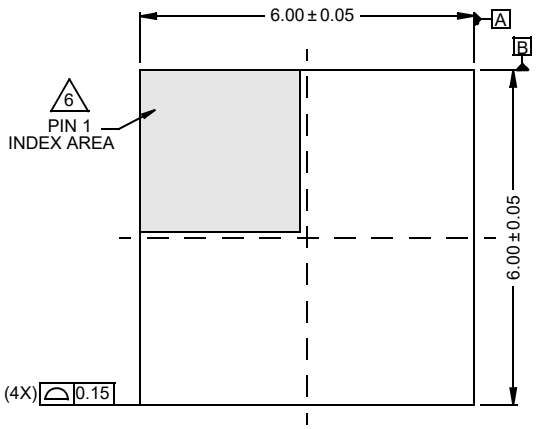
9. Revision History

Rev.	Date	Description
3.00	Oct.14.19	Applied new formatting. Complete rewrite of ISL94202 datasheet. No specification changes.
2.00	Mar.7.17	Updated entire datasheet to new standards. Updated Applications section on page 1 Added Table #1.1 on page 4.
1.00	Dec.12.16	Ordering Information table on page 4, updated Note 1 to include tape and reel options and quantities. ESD Rating on page 8, Human Body Model (Tested per JESD22-A114F) changed from: 2kV to: 1.5kV
0.00	Oct.24.16	Initial Release.

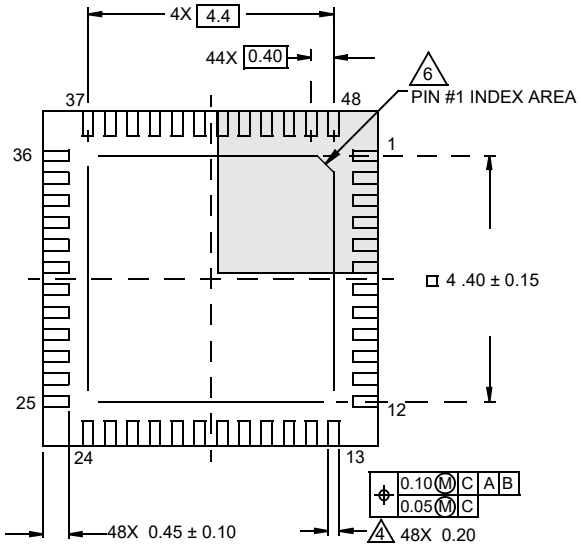
10. Package Outline Drawing

For the most recent package outline drawing, see L48.6x6.

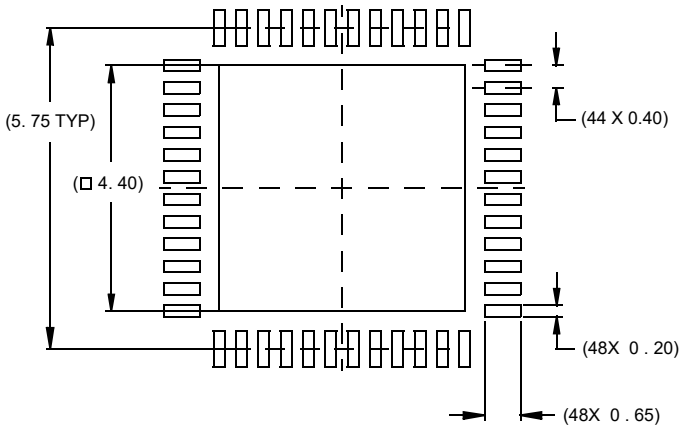
L48.6x6
48 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 7/14



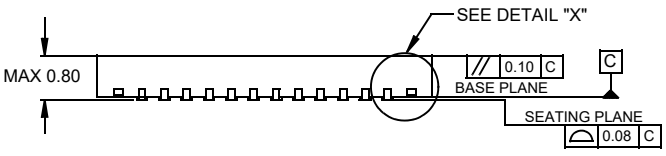
TOP VIEW



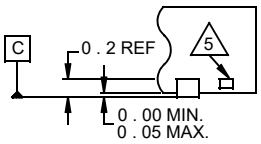
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Notice

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