THE DATASHEET OF

MC44C401LAC

MC44C401L
Rev. 0.5, 07/2004

MC44C401L
MTS Stereo Encoder

The MC44C401L Multi-Channel Television Sound (MTS) Stereo Encoder is the industry's first, single-chip, CMOS implementation of a Broadcast Television Systems Committee (BTSC)-compatible stereo encoder.

The MC44C401L MTS Stereo Encoder is designed for use in set-top boxes, VCRs, DVD players/recorders, game stations, and other applications that are required to output high-quality stereo sound through a single RF coaxial cable.

The digital audio processing used in the MC44C401L preserves the full fidelity of surround sound and other audio coding schemes while ensuring overall system performance is not impacted by copy protection technologies.

The MC44C401L is engineered to process right and left analog audio signals and baseband composite video to generate a stereophonic composite signal in accordance with BTSC system standards. The MC44C401L is designed to output this signal to a Motorola RF modulator, which in turn produces a stereo encoded RF channel for use with any BTSC stereo television receiver.

Contents

1 Features

- Integrated A/D input and D/A output circuitry
- CEX™ digital audio processing encodes and transports stereo signals
- Surround sound and Macrovision™ compatible

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- Extended low frequency response (The MC44C401L frequency response extends below 25 Hz)
- Simple passive interface to Motorola's MC44BC374 (UHF/VHF) and MC44BC375 (VHF) modulators
- Preservation of original surround sound fidelity
- System performance not impacted by copy protection technologies
- Enables lower system component count, smaller board size, and significantly lower overall system cost
- Eliminates manual alignment of filters, phase controls, and composite signal amplitude

2 Reference Documentation

"Multichannel Television Sound Transmission and Audio Processing Requirements for the BTSC System", FCC OET Bulletin No. 60, February 1986.

3 Block Diagrams

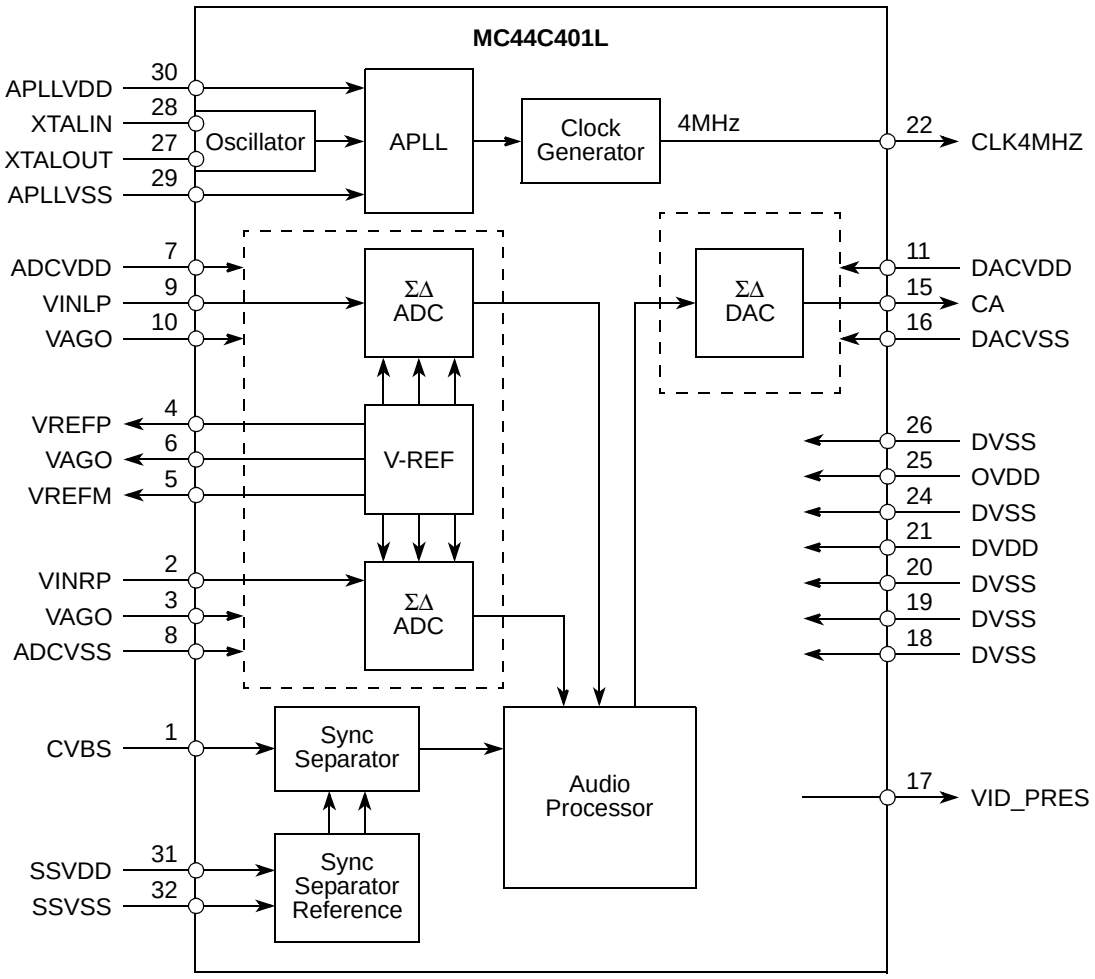


Figure 1. MC44C401L Block Diagram

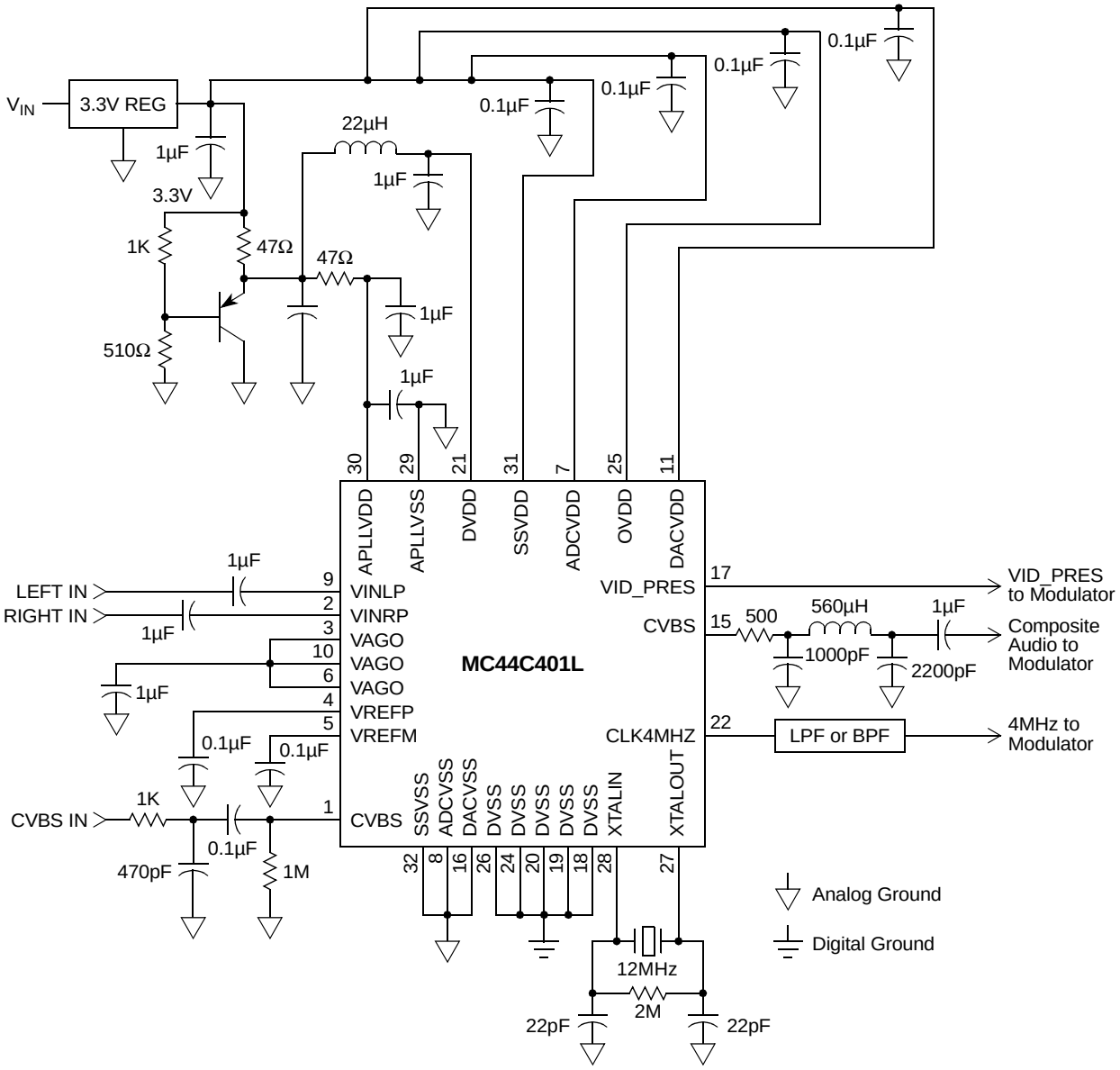


Figure 2. MC44C401L Recommended Usage

4 I/O Description

4.1 Signal List

The Stereo Modulator I/O signals are described in Table 1.

Table 1. MC44C401L Signal Descriptions

Signal	Pin #	Description
Analog		
VINL	9	Left channel input voltage
VREFP	4	ADC ref. input voltage
VAGO	3,6,10	Analog virtual ground
VREFM	5	ADC ref. input voltage
VINR	2	Right channel input voltage
CVBS	1	Composite video input
Digital		
CA	15	Composite Audio Output
VID_PRES	17	Video present flag, 0 = no video, hi-z = video present valid after 100 lines of valid video
NC	23,14, 13,12	No Connect
Clocks		
XTALIN	28	Crystal input
XTALOUT	27	Crystal output
CLK4MHZ[1]	22	4 MHz clock for Audio/Video modulator IC
Power Supply		
APLLVDD	30	APLL analog supply voltage, 1.8 V
APLLVSS	29	APLL analog ground
SSVDD	31	Sync Separator analog supply voltage, 3.3 V
SSVSS	32	Sync Separator analog ground
ADCVDD	7	ADC analog supply voltage, 3.3 V
ADCVSS	8	ADC analog ground

Table 1. MC44C401L Signal Descriptions (continued)

Signal	Pin #	Description
DACVDD	11	DAC I/O supply voltage, 3.3 V
DACVSS	16	DAC I/O ground
DVDD	21	Digital Logic supply voltage, 1.8 V
DVSS	18, 19, 20, 24, 26	Digital Logic/I/O ground
OVDD	25	I/O supply voltage, 3.3 V

1 Use a 4MHz LPF or BPF on this clock signal to the modulator

5 Electrical Specifications

5.1 DC Characteristics

Table 2. MC44C401L DC Characteristics (Preliminary)

PIN	Symbol	Parameter	Min	Typ	Max	Unit
DVDD	-	1.8 V Digital Logic	1.62	1.80	1.98	V
DVDD	-	1.8 V Digital Logic		18.0	22.0	mA
OVDD	-	3.3 V Digital Output	2.97	3.30	3.63	V
OVDD	-	3.3 V Digital Output		2.0	8.0	mA
DACVDD	-	3.3 V DAC Supply	2.97	3.30	3.63	V
DACVDD	-	3.3 V DAC Supply		7.0	9.0	mA
ADCVDD	-	3.3 V ADC Supply	2.97	3.30	3.63	V
ADCVDD	-	3.3 V ADC Supply		7.0	9.0	mA
SSVDD	-	3.3 V Sync. Sep Supply	2.97	3.3	3.63	V
SSVDD	-	3.3 V Sync. Sep Supply		2.0		mA
APLLVDD	-	1.8 V APLL Supply	1.62	1.8	1.98	V
APLLVDD	-	1.8 V APLL Supply		3.0		mA
VREFP	-	Voltage Ref. Bypass plus		2.0		V
VREFM	-	Voltage Ref. Bypass minus		1.0		V
VAGO	-	Voltage Ref. Ground		1.5		V
VINX	V_{il}	Signal Input	VREFM		VREFP	V
VINX	V_{ih}	Signal Input	VREFM		VREFP	V
CVBS		Video input (See Figure 2)		1		V_{pp}

Table 2. MC44C401L DC Characteristics (continued)(Preliminary)

PIN	Symbol	Parameter	Min	Typ	Max	Unit
CLK4MHZ	V_{ol}	4 MHz Clock Output @ I =.6 mA	2.97			V
CLK4MHZ	V_{oh}	4 MHz Clock Output @ I =.6 mA			3.63	V
CA	V_{ol}[1]	Composite Audio Output		2.2		V_{pp}

1 V_{ol} is measured at I_{load}= 6 mA (see test circuit Figure 2)

5.2 AC Characteristics

Table 3. MC44C401L AC Characteristics (Preliminary) (See Figure 2)

SIGNALS	Symbol	Parameter[1]	Min	Typ	Max	Unit
LEFT/RIGHT IN		Input Level			1.0	V_{pp}
LEFT/RIGHT IN		Input Impedance		250		kΩ
COMPOSITE		Composite Output Level[2]		2.2		V_{pp}
COMPOSITE		SNR[3]	65	75		dB
COMPOSITE		THD<superscript>2		0.1	0.3	%
COMPOSITE		-1 db Bandwidth	20		14000	Hz
CVBS IN		Video Level	0.5		2.0	V_{pp}
CVBS	Zin	Video Input Impedance		1000		W
		Stereo Separation 500Hz - 5KHz[4]		35		dB
		Stereo Separation 100Hz - 10KHz<superscript>4	30	35		dB

1 See Figure 2 for test setup

2 Test conditions 1 kHz 0 dB

3 Measured in 20 Hz to 13.5 kHz bandwidth

4 Measured -10 dB input level

6 Package Data

6.1 MC44C401L Package

The MC44C401L pin-outs (32TQFP package) are shown in Figure 3.

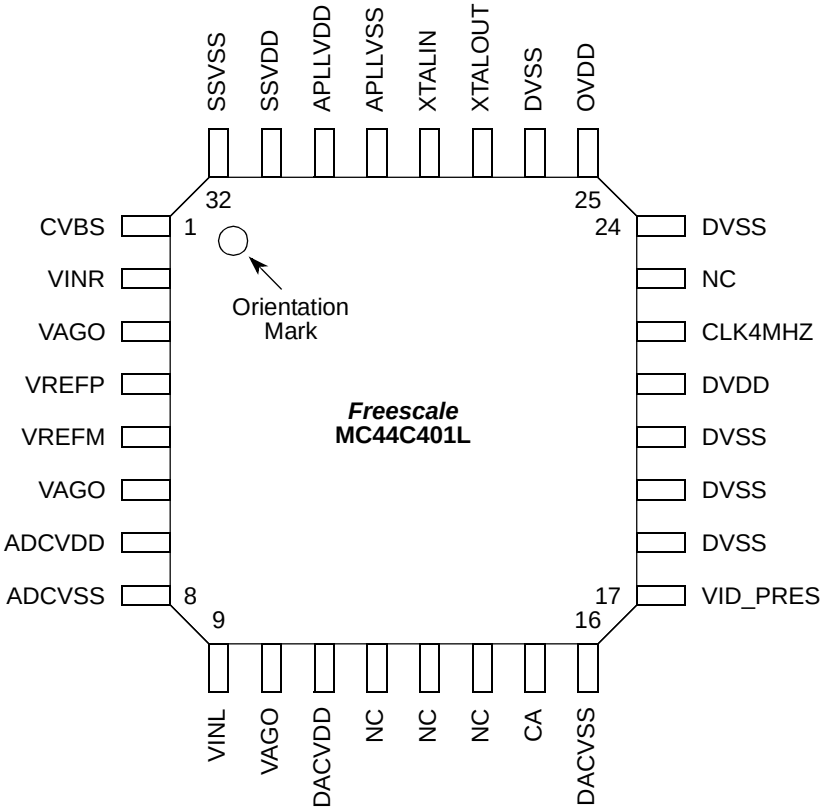
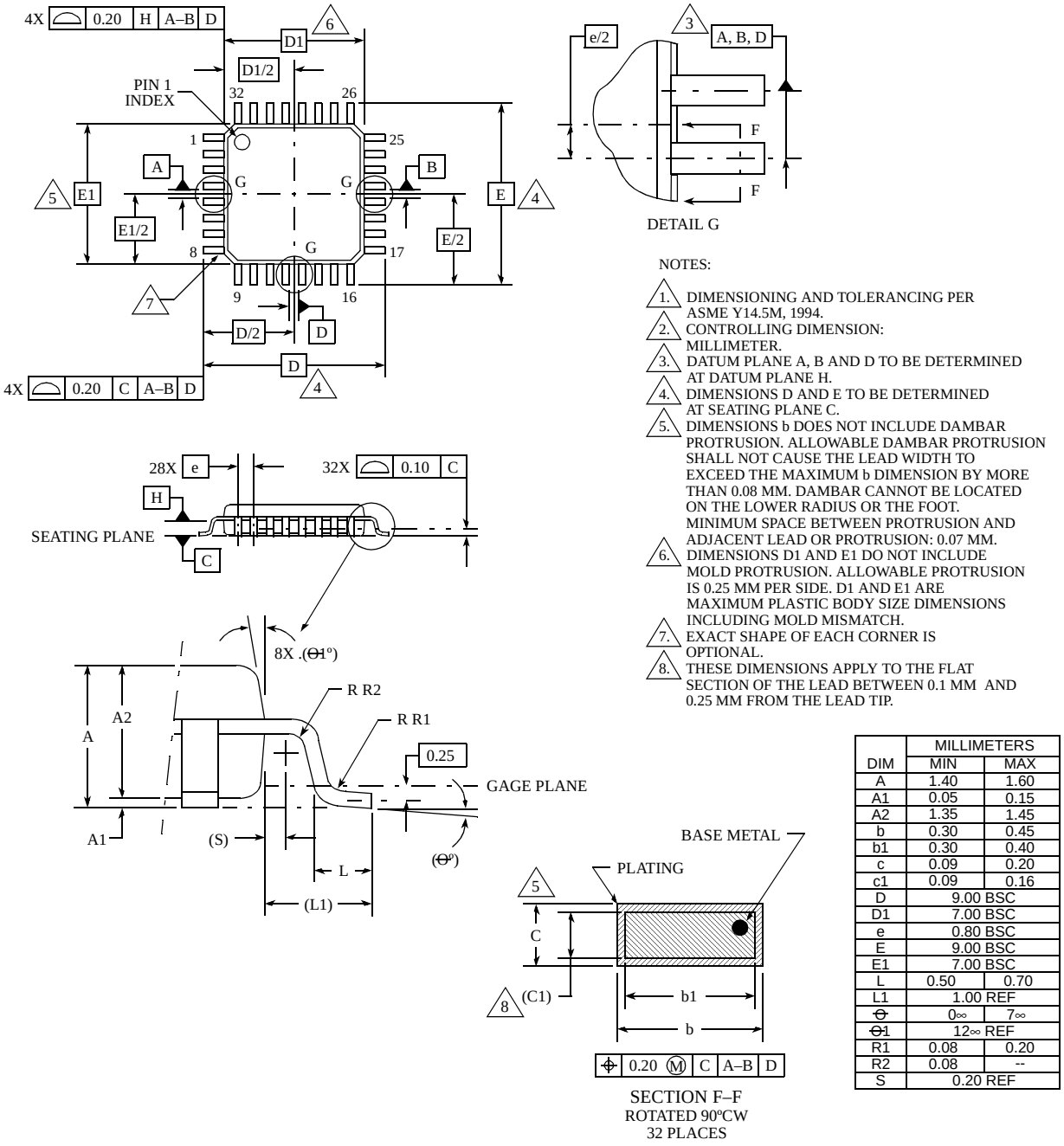


Figure 3. MC44C401L 32LQFP Package

6.2 Mechanical Data



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
Θ	0∞	7∞
Θ1	12∞ REF	
R1	0.08	0.20
R2	0.08	--
S	0.20 REF	

Figure 4.

7 Functional Description

The following sections provide brief descriptions of the MC44C401L modules.

7.1 Phase Locked Loop (APLL)

The APLL, shown in Figure 5, locks to the reference frequency of 12 MHz and generates the master clock.

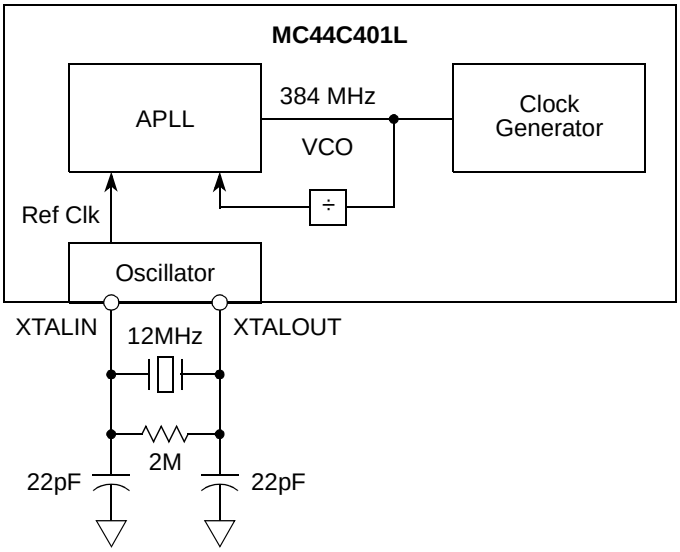


Figure 5. APLL and Clock Generator

7.2 Sync Separator

The Sync Separator, shown in Figure 6, extracts the composite sync from the incoming composite video signal.

The composite sync is used by the Audio Processor to generate the 15.734 kHz pilot tone and the 31.468 kHz carrier to modulate the Left-Right channel. The nominal output level of composite video signal sources is 1 V_{pp} on 75 Ω and the sync amplitude is 0.3 V.

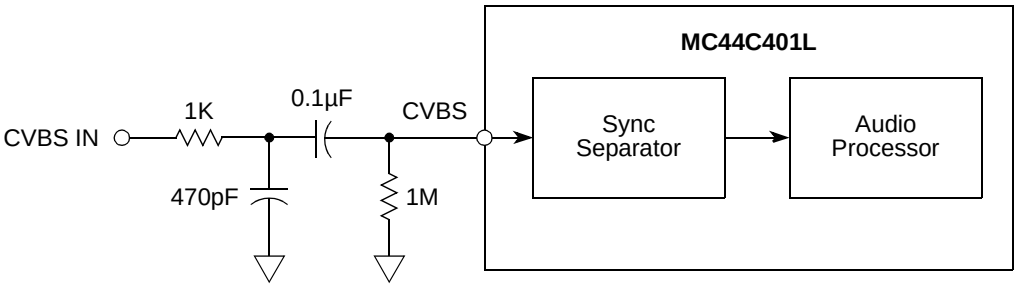
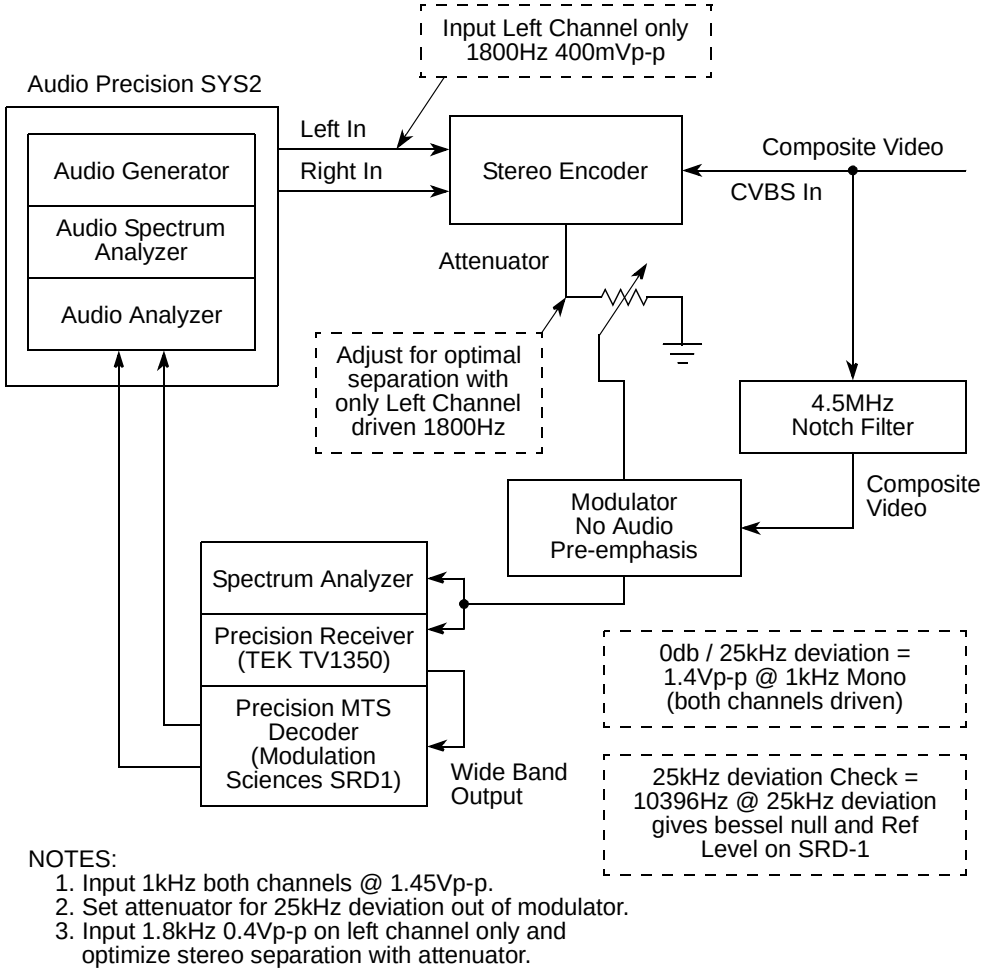


Figure 6. Sync Separator



NOTES:
1. Input 1kHz both channels @ 1.45Vp-p.
2. Set attenuator for 25kHz deviation out of modulator.
3. Input 1.8kHz 0.4Vp-p on left channel only and optimize stereo separation with attenuator.

Figure 7. MC44C401L Level Setup

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