THE DATASHEET OF

VSC8502XML-03

VSC8502 Datasheet
Dual Port 10/100/1000BASE-T PHY with RGMII/GMII/MII MAC Interface

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1 Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.2

Revision 4.2 of this datasheet was published in February 2019. In revision 4.2, references to VeriPHY registers were deleted. For functional details of the VeriPHY suite and the operating instructions, see the ENT-AN0125 PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics application note.

1.2 Revision 4.1

Revision 4.1 of this datasheet was published in April 2018. The following is a summary of the changes implemented in revision 4.1 of this document.

- Proprietary and confidential footer removed to accurately reflect document availability.
- Media recovered clock outputs information was updated. For more information, see Media Recovered Clock Outputs, page 13.
- LED behavior information was updated to better reflect device functionality. For more information, see LED Behavior, page 17.
- Fast link failure information was updated. For more information, see Fast Link Failure Indication, page 18.
- Voltage regulator graphics were updated to use consistent pin naming conventions. For more information, see On-Chip Voltage Regulators, page 22.
- Configuration procedure steps were clarified. For more information, see Configuration, page 23.
- The delay time for the software reset bit of the Mode Control register was corrected. For more information, see Table 14, page 26.
- Extended PHY Control 1 register information was corrected. For more information see Table 35, page 36.
- Timeout values for ActiPHY link status timeout control registers were corrected. For more information, see Table 39, page 38.
- “Sticky bit” designations were added where applicable for various control registers.
- The default value for the disable carrier extension bit of the ActiPHY Control register was corrected to 1. For more information, see Table 46, page 43.
- EEE Control register information was updated. For more information, see EEE Control, page 47.
- Reference Clock AC Specifications were added. For more information, see Reference Clock, page 59.
- I/O domain information was added to pins where applicable. For more information, see Pins by Function, page 68.
- The GTX_CLK_0 and GTX_CLK_1 pin names were changed to GTX_CLK_0/TXC_0 and GTX_CLK_1/TXC_1. There was no change to functionality. For more information, see Table 92, page 71.
- Additional design considerations were added. For more information, see Design Considerations, page 76.

1.3 Revision 4.0

Revision 4.0 of this datasheet was published in October 2014. The following is a summary of the changes implemented in the document.

- Voltage regulator block diagrams were updated.
- Output voltage specifications were updated.
- Power consumption specifications were updated.
- Recovered clock specifications were updated.
- GMII electrical specifications were added.
- Uncompensated and compensated RGMII electrical specifications were updated.
- PHY latency specifications were added.

- Design considerations were added.

1.4 Revision 2.2

Revision 2.2 of this datasheet was published in August 2014. The following is a summary of the changes implemented in the document.

- Bit descriptions for the Extended PHY Control 1 register were updated.
- Bit descriptions for the Extended Mode Control register were updated.
- Electrical specifications for the pins referenced to VDDMAC0, VDDMAC1, VDDIO, and VDDMDIO were updated.
- Electrical specifications for internal pull-up and pull-down resistors were added.
- Power consumption specifications were added in place of current consumption.
- Thermal diode description and specifications were updated.
- ESD (electrostatic discharge) was added. For human body model (HBM), it is a Class 2 rating for all pins except the REF_FILT pin, which is ±1500 V. For charged device model (CDM), it is ±500 V.
- Moisture sensitivity level (MSL) is level 4.

1.5 Revision 2.1

Revision 2.1 of this datasheet was published in April 2014. The following is a summary of the changes implemented in the document.

- Functional descriptions for Wake-On-LAN were added.
- JTAG instruction codes for IEEE compliance were updated.
- Device configuration information was added.
- Bit descriptions for the Recovered Clock 1 control register were updated.
- Electrical specifications for current consumption were updated.

1.6 Revision 2.0

Revision 2.0 of this datasheet was published in November 2013. This was the first publication of the document.

2 Product Overview

The VSC8502 device is designed for space-constrained 10/100/1000BASE-T applications. It features integrated, line-side termination to conserve board space, lower EMI, and improved system performance. To further reduce system complexity, component count, and system cost, the VSC8502 device can operate from a single 3.3 V supply using integrated voltage regulators. Additionally, integrated RGMII timing compensation eliminates the need for on-board delay lines.

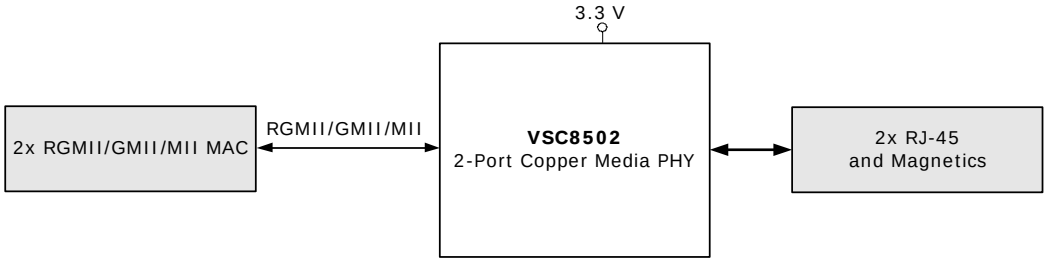
Microsemi's EcoEthernet™ v2.0 technology supports IEEE 802.3az Energy Efficient Ethernet (EEE) and power saving features to reduce power based on link state and cable reach. It optimizes power consumption in all link operating speeds and features Wake-on-LAN (WOL) power management using magic packets.

Fast link failure indication for high availability networks identifies the onset of a link failure in less than 1 ms typical to go beyond the IEEE 802.3 standard requirement of 750 ms ±10 ms (link master).

Synchronous Ethernet and Ring Resiliency™ are supported. The device includes recovered clock output for Synchronous Ethernet applications. Programmable clock squelch control is included to inhibit undesirable clocks from propagating and to help prevent timing loops. Ring Resiliency allows a PHY port to switch between master and slave timing references with no link drop in 1000BASE-T mode.

The following illustration shows a high-level, general view of a typical VSC8502 application.

Figure 1 • **Copper Transceiver Application Diagram**



2.1 Key Features

This section lists the main features and benefits of the VSC8502 device.

2.1.1 Superior PHY and Interface Technology

- Two integrated 10/100/1000BASE-T Ethernet copper transceiver (IEEE 802.3ab compliant) with VeriPHY® cable diagnostics software
- Patented line driver with low EMI voltage mode architecture and integrated line-side termination resistors
- Wake-on-LAN using magic packets
- HP Auto-MDIX and manual MDI/MDIX support
- RGMII/GMII MAC interface
- Jumbo frame support up to 16 kilobytes with programmable synchronization FIFOs

2.1.2 Synchronous Ethernet Support

- Recovered clock output with programmable clock squelch control and fast link failure indication (<1 ms typical) for G.8261 Synchronous Ethernet applications
- 1000BASE-T Ring Resiliency feature to switch between master and slave timing without dropping link
- Clock output squelch to inhibit clocks during auto-negotiation and no link status

2.1.3 Best in Class Power Consumption

- EcoEthernet™ v2.0 green energy efficiency with ActiPHY™, PerfectReach™, and IEEE 802.3az Energy Efficient Ethernet (EEE)

- Fully optimized power consumption for all link speeds
- Clause 45 registers to support Energy Efficient Ethernet and IEEE 802.3bf

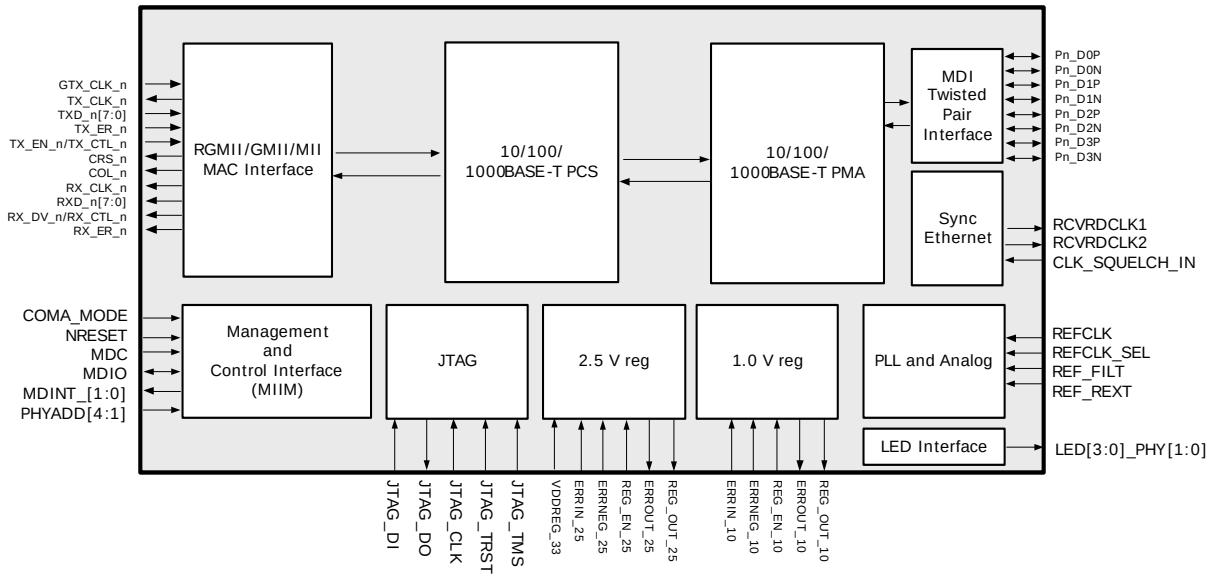
2.1.4 Key Specifications

- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, and 1000BASE-T) specifications
- Supports GMII
- Supports RGMII version 1.3 and 2.5 V and 3.3 V CMOS for RGMII version 2.0
- Devices support operating temperatures of –40 °C ambient to 125 °C junction or 0 °C ambient to 125 °C junction
- Optionally reports if a link partner is requesting inline Power over Ethernet (PoE and PoE+)
- Available in 12 mm x 12 mm, 135-pin multi-row QFN package

2.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC8502 device.

Figure 2 • **Block Diagram**



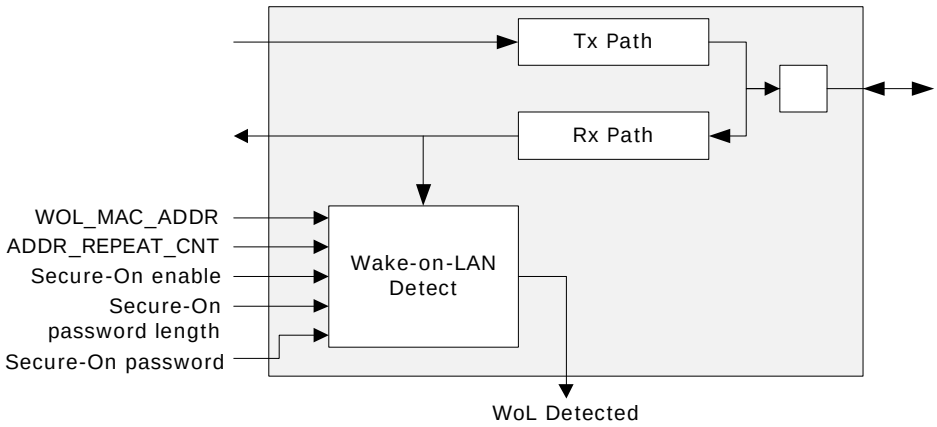
3 Functional Descriptions

This section describes the functional aspects of the VSC8502 device, including available configurations, operational features, and testing functionality. It also defines the device setup parameters that configure the device for a particular application.

3.1 Wake-On-LAN and SecureOn

The VSC8502 device supports Wake-on-LAN, an Ethernet networking standard to awaken hosts by using a “magic packet” that is decoded to ascertain the source, and then assert an interrupt pin or an LED. The VSC8502 device also supports SecureOn to secure Wake-on-LAN against unauthorized access. The following illustration shows an overview of the Wake-on-LAN functionality.

Figure 3 • **Wake-on-LAN Functionality**



Wake-on-LAN detection is available in 10BASE-T, 100BASE-TX, and 1000BASE-T modes. It is enabled by setting the interrupt mask register (25.6) and its status is read in the interrupt status register (26.6). Wake-on-LAN and SecureOn are configured for each port using register 27E2. The MAC address for each port is saved in its local register space (21E2, 22E2, and 23E2).

3.2 Operating Modes

The following table lists the operating modes of the VSC8502 device.

Table 1 • **Operating Modes**

Operating Mode	Supported Media
RGMII-Cat5	10/100/1000BASE-T
GMII-Cat5	10/100/1000BASE-T

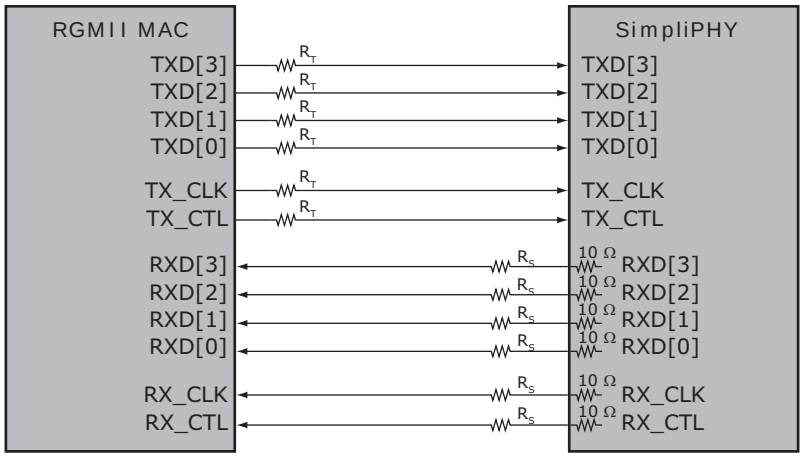
3.3 MAC Interface

The VSC8502 device supports RGMII versions 1.3 and 2.0 and GMII/MII MAC interfaces at 2.5 V and 3.3 V operating voltages.

3.3.1 RGMII MAC Interface Mode

The VSC8502 device supports RGMII versions 1.3 and 2.0 (2.5 V). The RGMII interface supports all three speeds (10 Mbps, 100 Mbps, and 1000 Mbps) and is used as an interface to an RGMII-compatible MAC.

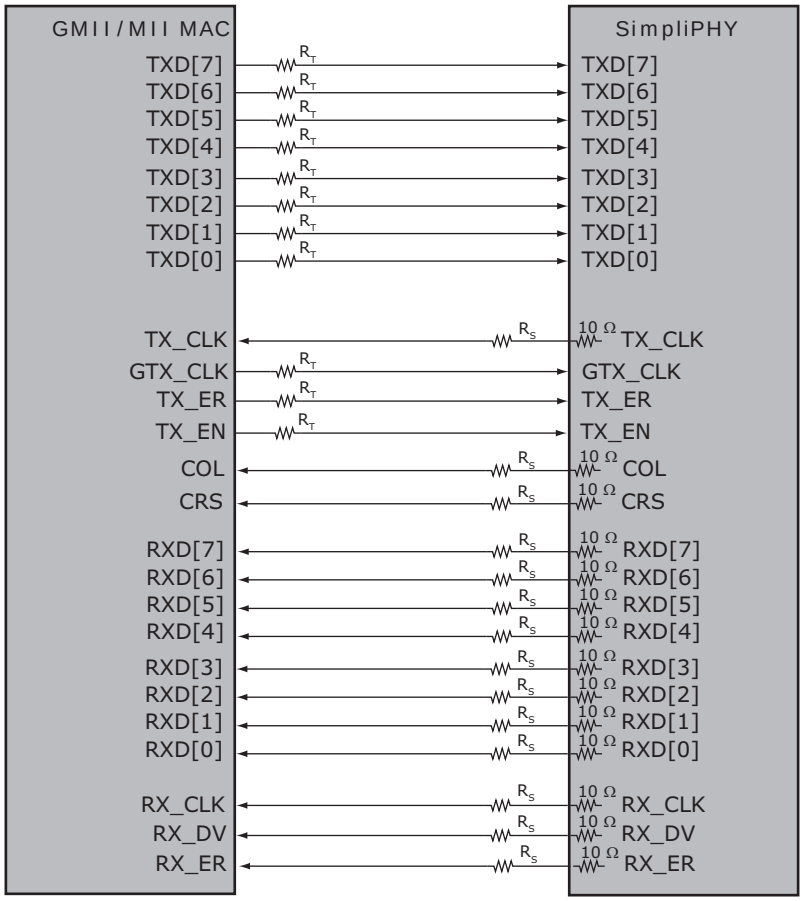
Figure 4 • **RGMII MAC Interface**



3.3.2 GMII/MII Interface Mode

The GMII/MII interface supports all three speeds (10 Mbps, 100 Mbps, and 1000 Mbps), and is used as an interface to a GMII/MII-compatible MAC.

Figure 5 • **GMII/MII MAC Interface**



3.4 PHY Addressing

The VSC8502 device includes four external PHY address pins, PHYADD[4:1], to allow control of multiple PHY devices on a system board sharing a common management bus.

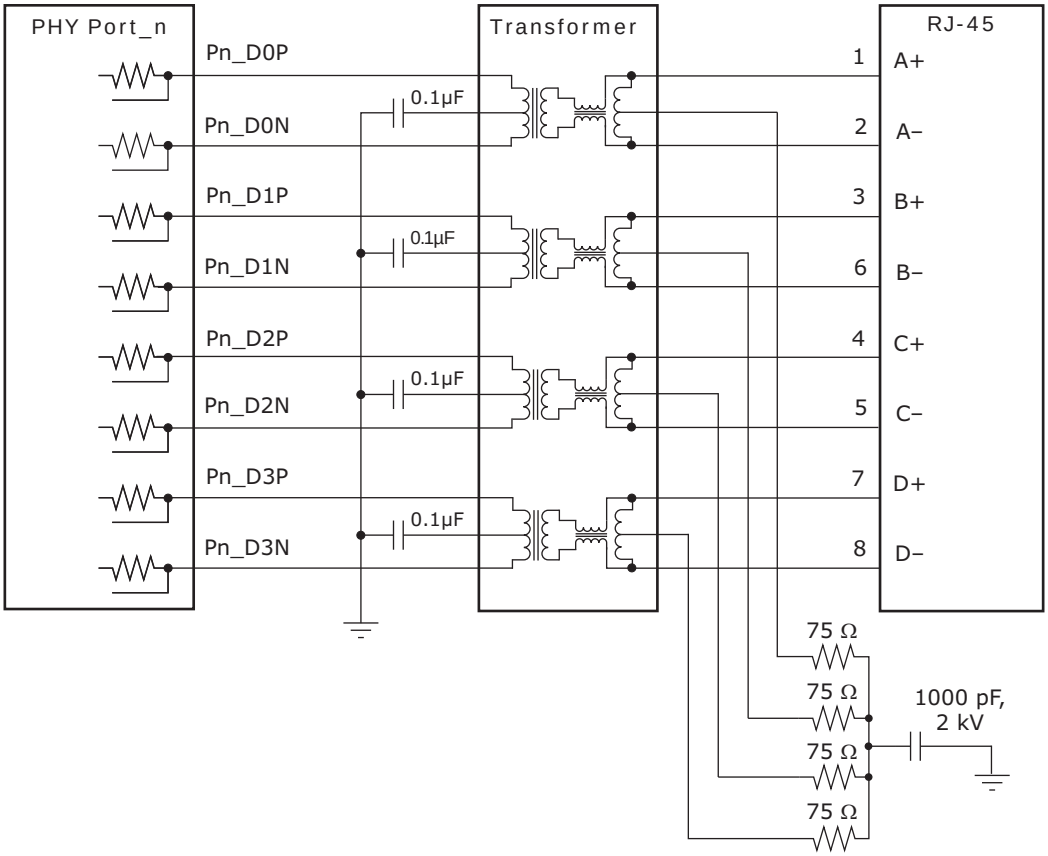
3.5 Cat5 Twisted Pair Media Interface

The twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az-2010 standard for Energy Efficient Ethernet.

3.5.1 Voltage Mode Line Driver

The VSC8502 device uses a patented voltage mode line driver that allows it to fully integrate the series termination resistors, which are required to connect the PHY's Cat5 interface to an external 1:1 transformer. Also, the interface does not require the user to place an external voltage on the center tap of the magnetic. The following illustration shows the connections.

Figure 6 • **Cat5 Media Interface**



3.5.2 Cat5 Auto-Negotiation and Parallel Detection

The VSC8502 device supports twisted pair auto-negotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az-2010. The auto-negotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-TX. Auto-negotiation also enables a connected MAC to communicate with its link partner MAC through the VSC8502 device using optional next pages to set attributes that may not otherwise be defined by the IEEE standard.

If the Category 5 (Cat5) link partner does not support auto-negotiation, the VSC8502 device automatically uses parallel detection to select the appropriate link speed.

Auto-negotiation is disabled by clearing register 0, bit 12. When auto-negotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode.

Note: While 10BASE-T and 100BASE-TX do not require auto-negotiation, IEEE 802.3-2008 Clause 40 has defined 1000BASE-T to require auto-negotiation.

3.5.3 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8502 device includes a robust automatic crossover detection feature for all three speeds on the twisted pair interface (10BASE-T, 100BASE-T, and 1000BASE T). Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs — a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Note: The VSC8502 device can be configured to perform HP Auto-MDIX, even when auto-negotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To use the feature, also set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table, which shows that twisted pair A (of four twisted pairs A, B, C, and D) is connected to the RJ45 connector 1,2 in normal MDI mode.

Table 2 • **Supported MDI Pair Combinations**

RJ45 Connections				
1, 2	**3, 6**	**4, 5**	**7, 8**	**Mode**
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

3.5.4 Manual MDI/MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

3.5.5 Link Speed Downshift

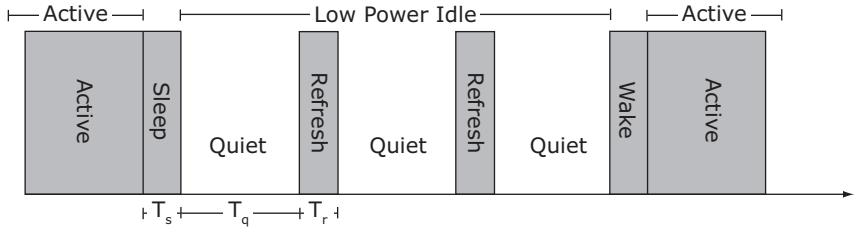
For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8502 device provides an automatic link speed downshift option. When enabled, the device automatically changes its 1000BASE-T auto-negotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state when a subsequent link partner with 1000BASE-T support is connected. This feature is useful in setting up in networks using older cable installations that include only pairs A and B, and not pairs C and D.

To configure and monitor link speed downshifting, set register 20E1, bits 4:1. For more information, see Table 46, page 43.

3.5.6 Energy Efficient Ethernet

The VSC8502 device supports the IEEE 802.3az-2010 Energy Efficient Ethernet standard to provide a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low power idles (LPI) to achieve this objective.

Figure 7 • **Low Power Idle Operation**



Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization. The VSC8502 device uses LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T modes of operation.

In addition, the IEEE 802.3az-2010 standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V peak-to-peak to approximately 3.3 V peak-to-peak. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T compliant PHYs over 100 m Cat5 cable or better.

To configure the VSC8502 device in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional energy efficient Ethernet features are controlled through Clause 45 registers. For more information, see Clause 45 Registers to Support Energy Efficient Ethernet and 802.3bf, page 53.

3.5.7 Ring Resiliency

Ring resiliency changes the timing reference between the master and slave PHYs without altering the master/slave configuration in 1000BASE-T mode. The master PHY transmitter sends data based on the local clock and initiates timing recovery in the receiver. The slave PHY instructs nodes to switch the local timing reference to the recovered clock from other PHYs in the box, freezes timing recovery, and locks clock frequency for the transmitter. The master PHY makes a smooth transition to transmission from local clock to recovered clock after timing lock is achieved.

Ring resiliency can be used in synchronous Ethernet systems because the local clocks in each node are synchronized to a grandmaster clock.

Note: For ring resiliency to successfully exchange master/slave timing over 1000BASE-T, the link partner must also support ring resiliency.

3.6 Reference Clock

The device reference clock supports a single-ended, CMOS logic level drive clock signal with both 25 MHz and 125 MHz frequency.

The REFCLK_SEL pin configures the reference clock frequency. The following table shows the functionality and associated reference clock frequency.

Table 3 • **REFCLK Frequency Selection**

REFCLK_SEL	Frequency
0	125 MHz
1	25 MHz

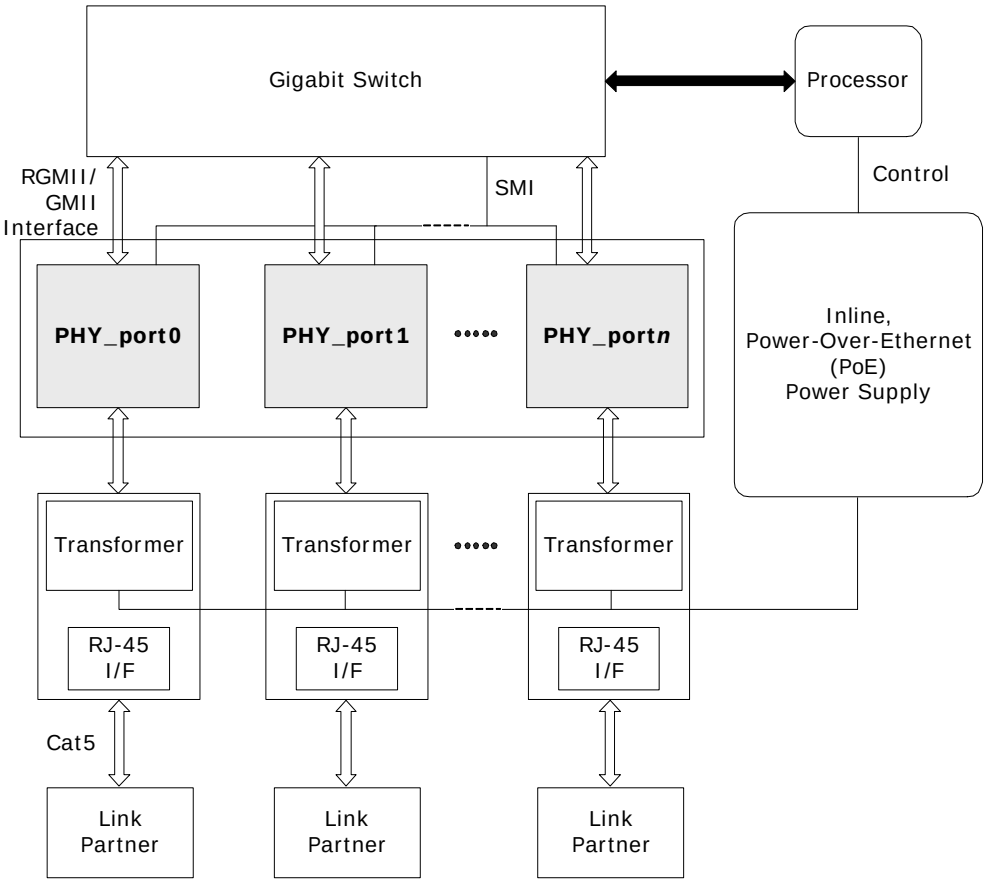
3.7 Ethernet Inline-Powered Devices

The VSC8502 device can detect legacy inline-powered devices in Ethernet network applications. Inline-powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline-powered device to remain

active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptable power source.

For more information about legacy inline-powered device detection, visit the Cisco Web site at www.cisco.com. The following illustration shows an example of an inline-powered Ethernet switch application.

Figure 8 • **Inline-Powered Ethernet Switch Diagram**



The following procedure describes the process that an Ethernet switch must perform to process inline-power requests made by a link partner that is, in turn, capable of receiving inline-power:

1. Enable the inline-powered device detection mode on each VSC8502 PHY using its serial management interface. Set register bit 23E1.10 to 1.
2. Ensure that the auto-negotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special fast link pulse signal to the link partner. Reading register bit 23E1.9:8 returns 00 during the search for devices that require power over Ethernet (PoE).
3. The VSC8502 PHY monitors its inputs for the fast link pulse signal looped back by the link partner. A link partner capable of receiving PoE loops back the fast link pulses when the link partner is in a powered down state. This is reported when register bit 23E1.9:8 reads back 01. It can also be verified as an inline-power detection interrupt by reading register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read. When a link partner device does not loop back the fast link pulse after a specific time, register bit 23E1.9:8 automatically resets to 10.
4. If the VSC8502 PHY reports that the link partner requires PoE, the Ethernet switch must enable inline-power on this port, independent of the PHY.
5. The PHY automatically disables inline-powered device detection when the register bits 23E1.9:8 automatically reset to 10, and then automatically changes to its normal auto-negotiation process. A link is then autonegotiated and established when the link status bit is set (register bit 1.2 is set to 1).

6. In the event of a link failure (indicated when register bit 1.2 reads 0), it is recommended that the inline-power be disabled to the inline-powered device independent of the PHY. The VSC8502 PHY disables its normal auto-negotiation process and re-enables its inline-powered device detection mode.

3.8 IEEE 802.3af Power Over Ethernet Support

The VSC8502 device is compatible with designs that are intended for use in systems that supply power to data terminal equipment (DTE) by means of the MDI or twisted pair cable, as described in IEEE 802.3af Clause 33.

3.9 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the VSC8502 device also includes an ActiPHY power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY wakes up at a programmable interval and attempts to wake up the link partner PHY by sending a burst of fast link pulse over copper media.

The ActiPHY power management mode is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

The following operating states are possible when ActiPHY mode is enabled:

- Low power state
- Link partner wake-up state
- Normal operating state (link-up state)

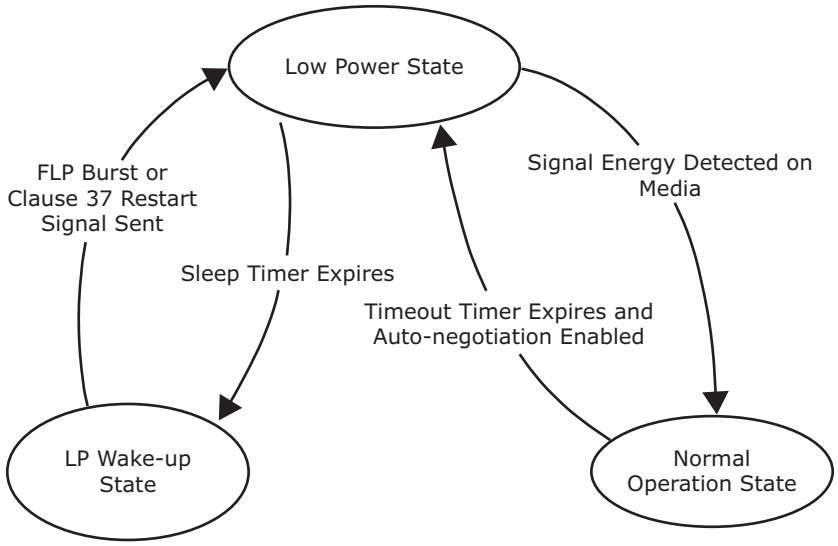
The VSC8502 device switches between the low power state and link partner wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When auto-negotiation is enabled in the PHY, the ActiPHY state machine operates as described.

When auto-negotiation is disabled and the link is forced to use 10BASE-T or 100BASE-TX modes while the PHY is in its low power state, the PHY continues to transition between the low power and link partner wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. When auto-negotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 9 • **ActiPHY State Diagram**



3.9.1 Low Power State

In the low power state, all major digital blocks are powered down. However, the SMI interface (MDC, MDIO, and MDINT) functionality is provided.

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Auto-negotiation-capable link partner
- Another PHY in enhanced ActiPHY link partner wake-up state

In the absence of signal energy on the media pins, the PHY periodically transitions from low-power state to link partner wake-up state, based on the programmable sleep timer (register bits 20E1.14:13). The actual sleep time duration is randomized from –80 ms to 60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

3.9.2 Link Partner Wake-Up State

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete fast link pulse bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

In this state, SMI interface (MDC, MDIO, and MDINT) functionality is provided.

After sending signal energy on the relevant media, the PHY returns to the low power state.

3.9.3 Normal Operating State

In the normal operating state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

3.10 Media Recovered Clock Outputs

For Synchronous Ethernet applications, the VSC8502 includes two recovered clock output pins, RCVRDCLK1 and RCVRDCLK2, controlled by register 23G and 24G, respectively. The recovered clock pins are synchronized to the clock of the active media link.

To enable recovered clock output, set register 23G or 24G bit 15 to 1. By default, the recovered clock output pins are disabled and held low, including when NRESET is asserted. Register 23G and 24G also control the PHY port for clock output, the clock source, the clock frequency (either 25 MHz, 31.25 MHz, or 125 MHz), and squelch conditions.

Note: When EEE is enabled on a link, the use of the recovered clock output is not recommended due to long holdovers occurring during EEE quiet/refresh cycles.

3.10.1 Clock Output Squelch

Under certain conditions, the PHY outputs a clock based on the REFCLK pin, such as when there is no link present or during auto-negotiation. To prevent an undesirable clock from appearing on the recovered clock pins, the VSC8502 device squelches, or inhibits, the clock output based on any of the following criteria:

- No link is detected (the link status register 1, bit 2 = 0).
- The link is found to be unstable using the fast link failure detection feature. The FASTLINK-FAIL pin is asserted high when enabled.
- The active link is in 10BASE-T or in 1000BASE-T master mode. These modes produce unreliable recovered clock sources.
- CLK_SQUELCH_IN is enabled to squelch the clock.

Use registers 23G or 24G, bits 5:4 to configure the clock squelch criteria. These registers can also disable the squelch feature. The CLK_SQUELCH_IN pin controls the squelching of the clock. The recovered clock output is squelched when the CLK_SQUELCH_IN pin is high. This pin should not be left floating.

3.11 Serial Management Interface

The VSC8502 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.

Energy efficient Ethernet control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14. For more information, see Table 25, page 31 and Table 60, page 53.

The SMI is a synchronous serial interface with input data to the VSC8502 device on the MDIO pin that is clocked on the rising edge of the MDC pin. The output data is sent on the MDIO pin on the rising edge of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2-kΩ pull-up resistor is required on the MDIO pin.

3.11.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional, arbitrary-length preamble. Before the first frame can be sent, at least two clock pulses on MDC must be provided with the MDIO signal at logic one to initialize the SMI state machine. The following illustrations show the SMI frame format for read and write operations.

Figure 10 • **SMI Read Frame**

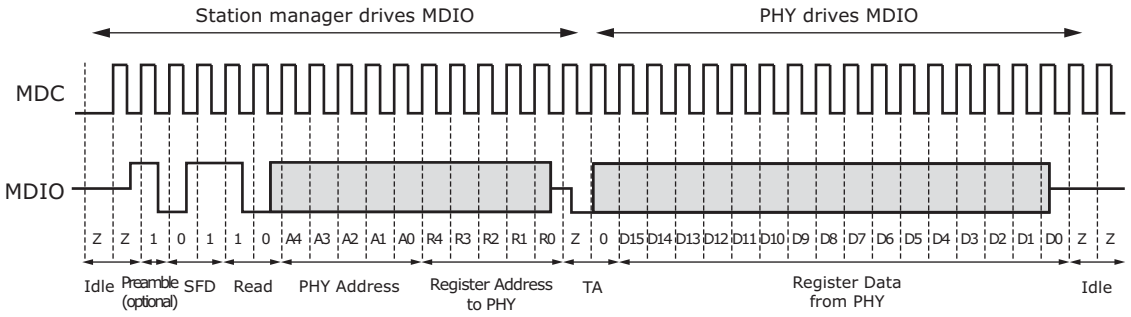
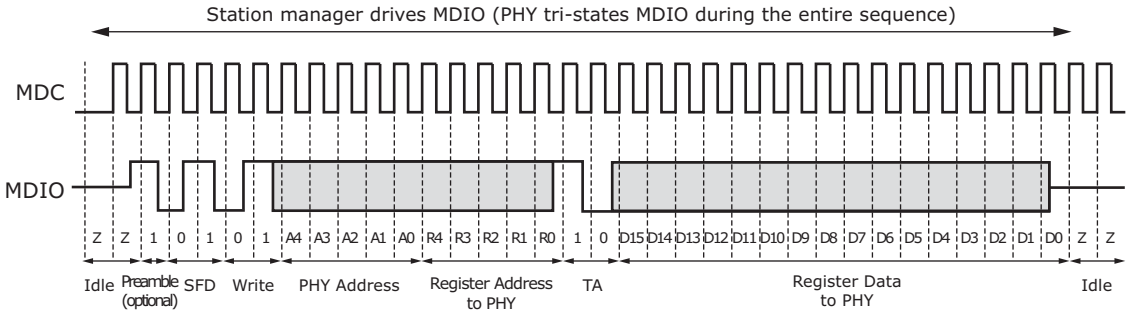


Figure 11 • **SMI Write Frame**



The following list defines the terms used in the SMI read and write timing diagrams.

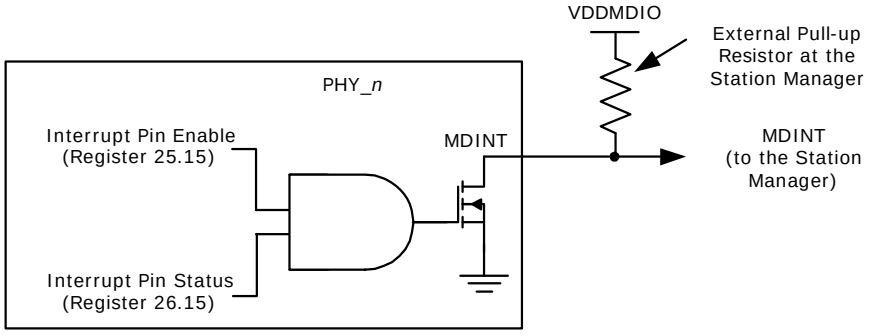
- **Idle** During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode does not contain any transitions on MDIO, the number of bits is undefined during idle.
- **Preamble** By default, preambles are not expected or required. The preamble is a string of ones. If it exists, the preamble must be at least 1 bit; otherwise, it can be of an arbitrary length.
- **Start of Frame Delimiter (SFD)** A pattern of 01 indicates the start of frame. If the pattern is not 01, all following bits are ignored until the next preamble pattern is detected.
- **Read or Write Opcode** A pattern of 10 indicates a read. A 01 pattern indicates a write. If the bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.
- **PHY Address** The particular VSC8502 device responds to a message frame only when the received PHY address matches its physical address. The physical address is 5 bits long (4:0).
- **Register Address** The next five bits are the register address.
- **Turnaround** The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turnaround (TA) bits. During read operations, the VSC8502 device drives the second TA bit, a logical 0.
- **Data** The 16-bits read from or written to the device are considered the data or data stream. When data is read from a PHY, it is valid at the output from one rising edge of MDC to the next rising edge of MDC. When data is written to the PHY, it must be valid around the rising edge of MDC.
- **Idle** The sequence is repeated.

3.11.2 SMI Interrupt

The SMI includes two output interrupt signals, MDINT_0 and MDINT_1, for signaling the station manager when certain events occur in the VSC8502 device.

When a PHY generates an interrupt, the MDINT_0/1 pins are asserted by driving low if the interrupt pin enable bit (MII register 25.15) is set. The MDINT pins are configured for open-drain (active-low) operation. Tie the pin to a pull-up resistor to VDDMDIO. The following illustration shows the configuration.

Figure 12 • **MDINT Configured as an Open-Drain (Active-Low) Pin**



3.12 LED Interface

The LED interface supports the following configurations: direct drive, basic serial LED mode, and enhanced serial LED mode. The polarity of the LED outputs is programmable and can be changed using register 17E2, bits 13:10. The default polarity is active low.

Direct drive mode provides four LED signals per port, LED0 through LED3. The mode and function of each LED signal can be configured independently. When serial LED mode is enabled, the direct drive pins not used by the serial LED interface remain available.

In basic serial LED mode, all signals that can be displayed on LEDs are sent as LED_Data and LED_CLK for external processing.

In enhanced serial LED mode, up to four LED signals per port can be sent as LED_Data, LED_CLK, LED_LD, and LED_Pulse. The following sections provide detailed information about the various LED modes.

Note: LED number is listed using the convention, LED<LED#>_<Port#>.

The following table shows the bit 9 settings for register 14G that are used to control the LED behavior for all the LEDs in the VSC8502 device.

Table 4 • **LED Drive State**

Setting	Active	Not Active
14G.9 = 1 (default)	Ground	Tristate
14G.9 = 0 (alternate setting)	Ground	V_{DD}

3.12.1 LED Modes

Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. The default LED state is active low and can be changed by modifying the value in register 17E2, bits 13:10. The blink/pulse stretch is dependent on the LED behavior setting in register 30.

The following table provides a summary of the LED modes and functions. The modes listed are equivalent to the setting used in register 29 to configure each LED pin.

Table 5 • **LED Mode and Function Summary**

Mode	Function Name	LED State and Description
0	Link/Activity	1: No link in any speed on any media interface. 0: Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1: No link in 1000BASE-T. 0: Valid 1000BASE-T. Blink or pulse-stretch = Valid 1000BASE-T link with activity present.
2	Link100/Activity	1: No link in 100BASE-TX. 0: Valid 100BASE-TX. Blink or pulse-stretch = Valid 100BASE-TX link with activity present.
3	Link10/Activity	1: No link in 10BASE-T. 0: Valid 10BASE-T link. Blink or pulse-stretch = Valid 10BASE-T link with activity present.
4	Link100/1000/Activity	1: No link in 100BASE-TX or 1000BASE-T. 0: Valid 100BASE-TX or 1000BASE-T link. Blink or pulse-stretch = Valid 100BASE-TX or 1000BASE-T link with activity present.

Table 5 • **LED Mode and Function Summary *(continued)***

Mode	Function Name	LED State and Description
5	Link10/1000/Activity	1: No link in 10BASE-T or 1000BASE-T. 0: Valid 10BASE-T or 1000BASE-T link. Blink or pulse-stretch = Valid 10BASE-T or 1000BASE-T link with activity present.
6	Link10/100/Activity	1: No link in 10BASE-T or 100BASE-TX. 0: Valid 10BASE-T or 100BASE-TX link. Blink or pulse-stretch = Valid 10BASE-T or 100BASE-TX link with activity present.
7	Reserved	Reserved.
8	Duplex/Collision	1: Link established in half-duplex mode, or no link established. 0: Link established in full-duplex mode. Blink or pulse-stretch = Link established in half-duplex mode but collisions are present.
9	Collision	1: No collision detected. Blink or pulse-stretch = Collision detected.
10	Activity	1: No activity present. Blink or pulse-stretch = Activity present (becomes TX activity present when register bit 30.14 is set to 1).
11	Reserved	Reserved.
12	Autonegotiation Fault	1: No auto-negotiation fault present. 0: Auto-negotiation fault occurred.
13	Serial Mode	Serial stream. See Basic Serial LED Mode, page 15. Only relevant on PHY port 0. Reserved in others.
14	Force LED Off	1: De-asserts the LED(1).
15	Force LED On	0: Asserts the LED(1).

1. Setting this mode suppresses LED blinking after reset.

3.12.2 Basic Serial LED Mode

The VSC8502 device can be configured so that access to all its LED signals is available through two pins. This option is enabled by setting LED0 on PHY0 to serial LED mode in register 29, bits 3:0 to 0xD. When serial LED mode is enabled, the LED0_PHY0 pin becomes the serial data pin, and the LED1_PHY0 pin becomes the serial clock pin. All other LED pins can still be configured normally. The serial LED mode clocks the LED status bits on the rising edge of the serial clock.

The LED behavior settings can also be used in serial LED mode. The controls are used on a per-PHY basis, where the LED combine and LED blink or pulse-stretch setting of LED0_n for each PHY is used to control the behavior of each bit of the serial LED stream for each corresponding PHY. To configure LED behavior, set device register 30.

The following table shows the serial output bitstream of each LED signal.

Table 6 • **LED Serial Bitstream Order**

Output	PHY0	PHY1
Link/activity	1	13
Link1000/activity	2	14
Link100/activity	3	15
Link10/activity	4	16

Table 6 • **LED Serial Bitstream Order *(continued)***

Output	PHY0	PHY1
Reserved	5	17
Duplex/collision	6	18
Collision	7	19
Activity	8	20
Reserved	9	21
Tx activity	10	22
Rx activity	11	23
Autonegotiation fault	12	24

3.12.3 Enhanced Serial LED Mode

The VSC8502 device can be configured to output up to four LED signals per port on a serial stream that can be de-serialized externally to drive LEDs on the system board. In enhanced serial LED mode, the port 0 and port 1 LED output pins serve the following functions:

- LED0: LED_DATA
- LED1: LED_CLK
- LED2: LED_LD
- LED3: LED_PULSE

The serial LED_DATA is shifted out on the falling edge of LED_CLK and is latched in the external serial-to-parallel converter on the rising edge of LED_CLK. The falling edge of LED_LD signal can be used to shift the data from the shift register in the converter to the parallel output drive register. When a separate parallel output drive register is not used in the external serial-to-parallel converter, the LEDs will blink at a high frequency as the data bits are being shifted through, which may be undesirable. LED pin functionality is controlled by setting register 25G, bits 7:1.

The LED_PULSE signal provides a 5 kHz pulse stream whose duty cycle can be modulated to turn on/off LEDs at a high rate. This signal can be tied to the output enable signal of the serial-to-parallel converter to provide the LED dimming functionality to save energy. The LED_PULSE duty cycle is controlled by setting register 25G, bits 15:8.

3.12.4 Extended LED Modes

In addition to the LED modes in register 29, there are also additional LED modes that are enabled on the LED0 pin whenever the corresponding register 19E1, bits 15 to 12 are set to 1. Each of these bits enables an extended mode shown in the following table. For example, LED0 = mode 17 means that register 19E1 bit 12 = 1 and register 29 bits 3 to 0 = 0001.

The following table provides a summary of the extended LED modes and functions.

Table 7 • **Extended LED Mode and Function Summary**

Mode	Function Name	LED State and Description
16-19	Reserved	Reserved
20	Force LED Off	1: De-asserts the LED.
21	Force LED On	0: Asserts the LED. LED pulsing is disabled in this mode.
22	Fast Link Fail	1: Enable fast link fail on the LED pin 0: Disable

3.12.5 LED Port Swapping

For additional hardware configurations, the VSC8502 device can have its LED port order swapped. This is a useful feature to help simplify PCB layout design. Register 25G bit 0 controls the LED port swapping mode. LED port swapping only applies to the direct-drive LEDs and not to any serial LED output modes.

3.12.6 LED Behavior

Several LED behaviors can be programmed into the VSC8502 device. Use the settings in register 30 and 19E1 to program LED behavior, which includes the following:

3.12.6.1 LED Combine

Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 1000BASE-T mode and activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display when the combine feature is disabled.

3.12.6.2 LED Blink or Pulse-Stretch

This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin. Activity and collision events can occur randomly and intermittently throughout the link-up period. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin. Pulse-stretch guarantees that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

3.12.6.3 Rate of LED Blink or Pulse-Stretch

This behavior controls the LED blink rate or pulse-stretch length when blink/pulse-stretch is enabled on an LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.

3.12.6.4 LED Pulsing Enable

To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz, 20% duty cycle.

3.12.6.5 LED Blink After Reset

The LEDs will blink for one second after COMA_MODE is de-asserted (as described in Configuration, page 23) or a software reset is applied.

This feature can be enabled by setting register 19E1, bit 11 = 1.

3.12.6.6 Fast Link Failure

For more information about this feature, see Fast Link Failure Indication, page 18.

3.13 Fast Link Failure Indication

To aid Synchronous Ethernet applications, the VSC8502 device can indicate the onset of a link failure in less than 1 ms (<3 ms, worst case). In comparison, the IEEE 802.3 standard establishes a delay of up to 750 ms before indicating that a 1000BASE-T link is no longer present. A fast link failure indication is critical to support ports used in a synchronization timing link application. The fast link failure indication works for all copper media speeds. Fast link failure is supported for each PHY port through the FASTLINK-FAIL pin. Fast link failure is supported through the MDINT (active low) pin only in 1000BASE-T and 100BASE-TX modes. It is not supported through the MDINT pin and interrupt status register 26, bit 7 in 10BASE-T mode.

Note: For all links except 1000BASE-T, the fast link failure indication matches the link status register (address 1, bit 2). For 1000BASE-T links, the link failure is based on a circuit that analyzes the integrity of the link, and will assert at the indication of failure. The MDINT pin is not reset until register 26 is cleared.

Note: A system can later confirm the fast link down indication for system management purposes by actively polling the link status bit to determine if a link has failed.

Note: FLF indication should not be used when EEE is enabled on a link.

3.14 Testing Features

The VSC8502 device includes several testing features designed to facilitate performing system-level debugging and in-system production testing. This section describes the available features.

3.14.1 Ethernet Packet Generator

The Ethernet packet generator (EPG) can be used at each of the 10/100/1000BASE-T speed settings for copper Cat5 media to isolate problems between the MAC and the VSC8502 device, or between a locally connected PHY and its remote link partner. Enabling the EPG feature disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface. This feature is not used when the SerDes media is set to pass-through mode.

Important The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the VSC8502 device is connected to a live network.

To enable the EPG feature, set the device register bit 29E1.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output pins to the MAC are still active when the EPG is enabled. When it is necessary to disable the MAC receive pins as well, set the register bit 0.10 to 1.

When the device register bit 29E1.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E1 and 30E1. These registers set:

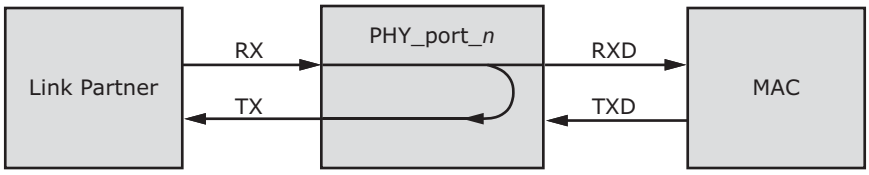
- Source and destination addresses for each packet
- Packet size
- Interpacket gap
- FCS state
- Transmit duration
- Payload pattern

When register bit 29E1.13 is set to 0, register bit 29E1.14 is cleared automatically after 30,000,000 packets are transmitted.

3.14.2 Far-End Loopback

The far-end loopback testing feature is enabled by setting register bit 23.3 to 1. When enabled, it forces incoming data from a link partner on the current media interface into the MAC interface of the PHY where it is retransmitted back to the link partner on the media interface as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

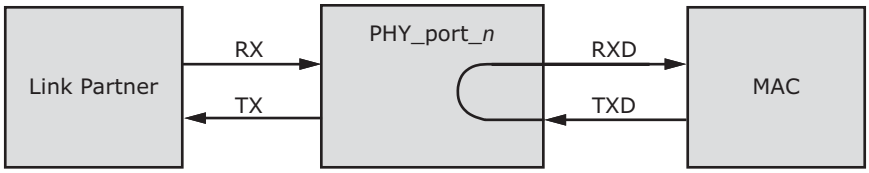
Figure 13 • **Far-End Loopback Diagram**



3.14.3 Near-End Loopback

When the near-end loopback testing feature is enabled, transmitted data (TXD) is looped back in the PCS block onto the receive data signals (RXD), as shown in the following illustration. When using this testing feature, no data is transmitted over the network. To enable near-end loopback, set the device register bit 0.14 to 1.

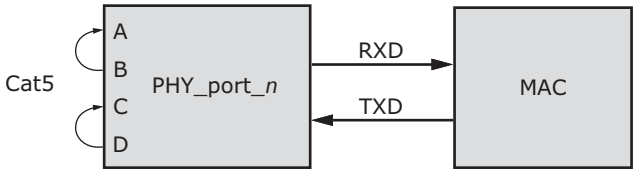
Figure 14 • **Near-End Loopback Diagram**



3.14.4 Connector Loopback

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Connect pair A to pair B, and pair C to pair D, as shown in the following illustration. The connector loopback feature functions at all available interface speeds.

Figure 15 • **Connector Loopback Diagram**



When using the connector loopback testing feature, the device auto-negotiation, speed, and duplex configuration is set using device registers 0, 4, and 9.

For 1000BASE-T connector loopback, additional writes are required in the following order:

1. Enable the 1000BASE-T connector loopback. Set register bit 24.0 to 1.
2. Disable pair swap correction. Set register bit 18.5 to 1.

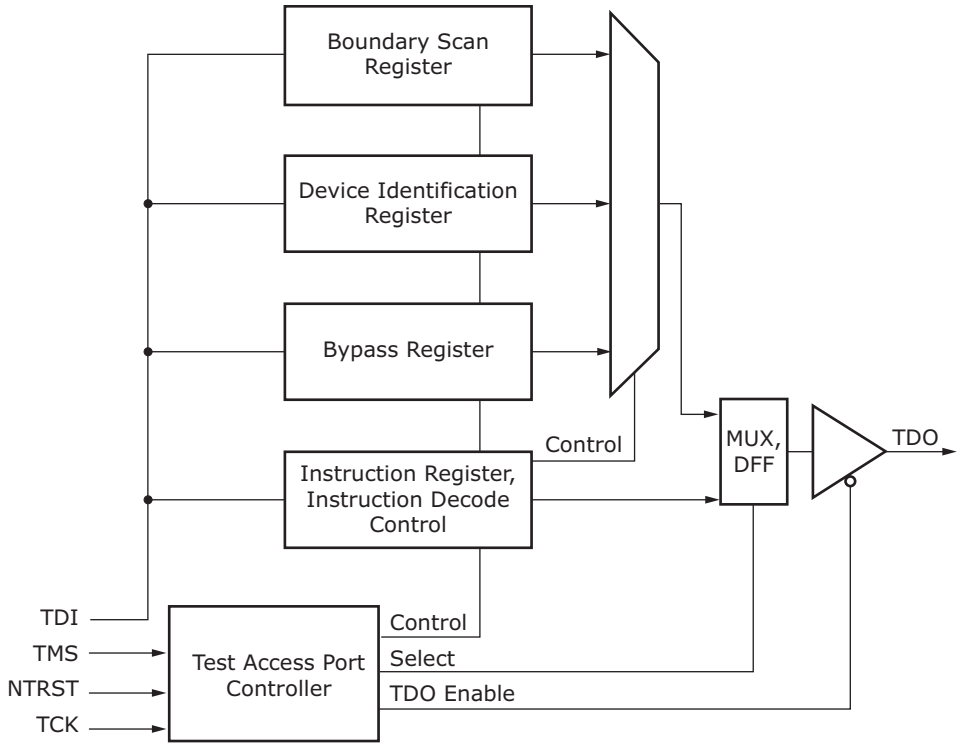
3.14.5 JTAG Boundary Scan

The VSC8502 device supports the test access port (TAP) and boundary scan architecture described in IEEE 1149.1. The device includes an IEEE 1149.1-compliant test interface, referred to as a JTAG TAP interface.

The JTAG boundary scan logic on the VSC8502 device, accessed using its TAP interface, consists of a boundary scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal TRST. The following illustration shows the TAP and boundary scan architecture.

Important When JTAG is not in use, the TRST pin must be tied to ground with a pull-down resistor for normal operation.

Figure 16 • **Test Access Port and Boundary Scan Architecture**



After a TAP reset, the device identification register is serially connected between TDI and TDO by default. The TAP instruction register is loaded from a shift register when a new instruction is shifted in, or, if there is no new instruction in the shift register, a default value of 6'b100000 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

3.14.5.1 JTAG Instruction Codes

The following table shows the supported JTAG instruction codes.

Table 8 • **JTAG Instruction Codes**

Instruction Code	Description
BYPASS	The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.
CLAMP	Allows the state of the signals driven from the component pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins do not change.
EXTEST	Allows tests of the off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary scan cells, which have to be updated with valid values, with the PRELOAD instruction, prior to the EXTEST instruction.

Table 8 • **JTAG Instruction Codes *(continued)***

Instruction Code	Description
HIGHZ	Places the component in a state in which all of its system logic outputs are placed in a high-impedance state. In this state, an in-circuit test system can drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.
IDCODE	Provides the version number (bits 31:28), device family ID (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.
SAMPLE/PRELOAD	Allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary scan cells prior to the selection of other boundary scan test instructions.
USERCODE	Provides the version number (bits 31:28), part number (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.

The following tables provide information about the IDCODE and USERCODE binary values stored in the device JTAG registers.

Table 9 • **IDCODE JTAG Device Identification Register Descriptions**

Description	Device Version	Family ID	Manufacturing Identity	LSB
Bit field	31–28	27–12	11–1	0
Binary value	0000	1000 0101 0000 0010	000 0111 0100	1

Table 10 • **USERCODE JTAG Device Identification Register Descriptions**

Description	Device Version	Model Number	Manufacturing Identity	LSB
Bit field	31–28	27–12	11–1	0
Binary value	0000	1000 0101 0000 0010	000 0111 0100	1

The following table provides information about the location and IEEE compliance of the JTAG instruction codes used in the VSC8502 device. Instructions not explicitly listed in the table are reserved. For more information about these IEEE specifications, visit the IEEE Web site at www.IEEE.org.

Table 11 • **JTAG Instruction Code IEEE Compliance**

Instruction	Code	Selected Register	Register Width	IEEE 1149.1
EXTEST	000000	Boundary Scan	139	Mandatory
SAMPLE/PRELOAD	000001	Boundary Scan	139	Mandatory
IDCODE	100000	Device Identification	32	Optional
USERCODE	100001	Device Identification	32	Optional
HIGHZ	000101	Bypass Register	1	Optional
BYPASS	11111	Bypass Register	1	Mandatory

3.14.5.2 Boundary Scan Register Cell Order

All inputs and outputs are observed in the boundary scan register cells. All outputs are additionally driven by the contents of boundary scan register cells. Bidirectional pins have all three related boundary scan register cells: input, output, and control.

The complete boundary scan cell order is available as a BSDL file format on the Microsemi Web site at www.microsemi.com.

3.15 On-Chip Voltage Regulators

The VSC8502 device includes dual on-chip voltage regulators that generate 2.5 V and 1.0 V supplies from 3.3 V. The voltage regulators are designed to supply the current needed by the device itself. These regulators should not be used to power any other device in the system. Each voltage regulator can be enabled independently, and together they allow the device to operate from a single 3.3 V power supply.

Note: The 2.5 V voltage regulator is designed to supply the VDD25A supply of the VSC8502 device. When operating from a 3.3 V power supply, all the other interfaces must be operated at 3.3 V and directly connected to that power supply.

The following illustrations show the block diagrams of the two voltage regulators and highlight the off-chip components and connections needed with each regulator.

Figure 17 • **3.3 V to 1.0 V Voltage Regulator**

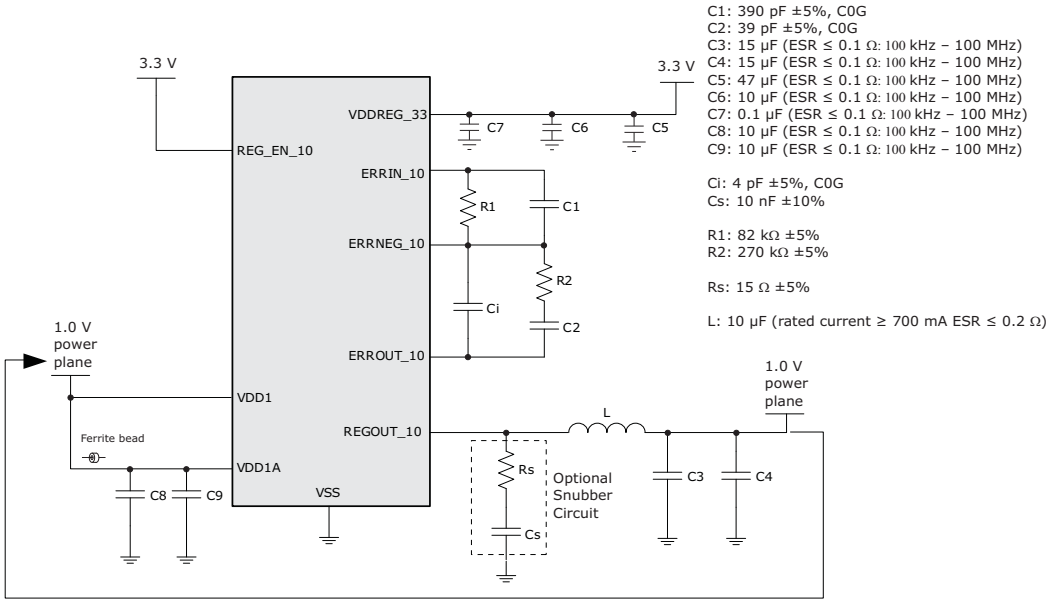
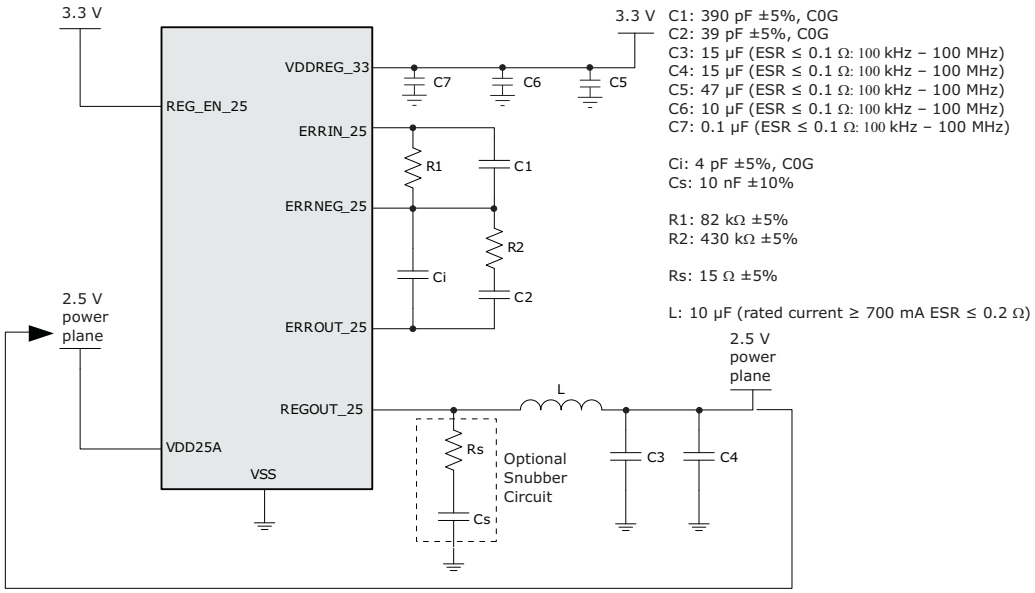


Figure 18 • **3.3 V to 2.5 V Voltage Regulator**



3.16 Configuration

The VSC8502 device can be configured by setting internal memory registers using the management interface. To configure the device, perform the following steps:

1. COMA_MODE active, drive high (optional).
2. Apply power.
3. Apply RefClk.
4. Release reset, drive high. Power and clock must be high before releasing reset.
5. Wait 120 ms minimum.
6. Apply patch from PHY_API (required for production release, optional for board testing).
7. Configure register 23 for MAC interface mode. Read register 23 (to access register 23, register 31 must be 0). Set bit 12, MAC configuration as follows:
   0: GMII/MII
   1: RGMII
8. Write new register 23.
9. Software reset. Read register 0 (to access register 0, register 31 must be 0). Set bit 15 to 1.
10. Write new register 0.
11. Read register 0 until bit 15 equals to 0.
12. For RGMII mode: Configure register 20E2 (to access register 20E2, register 31 must be set to 2). Set bit 11 to 0 and set RX_CLK delay and GTX_CLK delay accordingly through bit [6:4] and/or bit [2:0] respectively.
13. Release the COMA_MODE pin, drive low (only necessary if COMA_MODE pin is driven high or unconnected).

3.16.1 Initialization

The COMA_MODE pin provides an optional feature that may be used to control when the PHYs become active. The typical usage is to keep the PHYs from becoming active before they have been fully initialized. For more information, see Configuration, page 23. Alternatively the COMA_MODE pin may be connected low (ground) and the PHYs will be fully active once out of reset.

4 Registers

This section provides information about how to configure the VSC8502 device using its internal memory registers and the management interface. The registers marked reserved should not be read or written to, because doing so may produce undesired effects.

The default value documented for registers is based on the value at reset; however, in some cases, that value may change immediately after reset.

The access type for each register is shown using the following abbreviations:

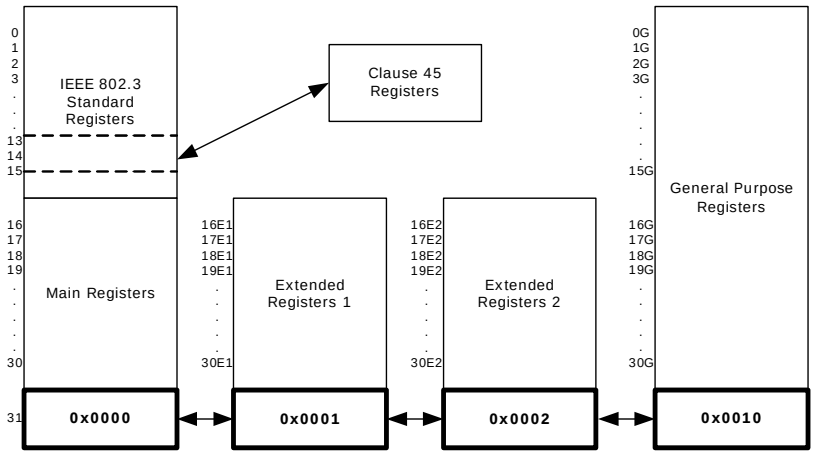
- RO: Read Only
- ROCR: Read Only, Clear on Read
- RO/LH: Read Only, Latch High
- RO/LL: Read Only, Latch Low
- R/W: Read and Write
- RWSC: Read Write Self Clearing

The VSC8502 device uses several different types of registers:

- IEEE Clause 22 device registers with addresses from 0 to 31
- Two pages of extended registers with addresses from 17E1–30E1 and 16E2–30E2
- General-purpose registers with addresses from 0G to 30G
- IEEE Clause 45 devices registers accessible through the Clause 22 registers 13 and 14 to support IEEE 802.3az-2010 energy efficient Ethernet registers and IEEE 802.3bf-2011 registers

The following illustration shows the relationship between the device registers and their address spaces.

Figure 18 • **Register Space Diagram**



Reserved Registers

For main registers 16–31, extended registers 17E1–30E1, 16E2–30E2, and general purpose registers 0G–30G, any bits marked as Reserved should be processed as read-only and their states as undefined.

Reserved Bits

In writing to registers with reserved bits, use a read-modify-then-write technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and their read state cannot be considered static or unchanging.

4.1 Register and Bit Conventions

This document refers to registers by their address and bit number in decimal notation. A range of bits is indicated with a colon. For example, a reference to address 26, bits 15 through 14 is shown as 26.15:14.

A register with an E and a number attached (example 27E1) means it is a register contained within extended register page number 1. A register with a G attached (example 13G) means it is a GPIO page register.

Bit numbering follows the IEEE standard with bit 15 being the most significant bit and bit 0 being the least significant bit.

4.2 IEEE 802.3 and Main Registers

In the VSC8502 device, the page space of the standard registers consists of the IEEE 802.3 standard registers and the Microsemi standard registers. The following table lists the names of the registers associated with the addresses as specified by IEEE 802.3.

Table 12 • **IEEE 802.3 Registers**

Address	Name
0	Mode Control
1	Mode Status
2	PHY Identifier 1
3	PHY Identifier 2
4	Auto-negotiation Advertisement
5	Auto-negotiation Link Partner Ability
6	Auto-negotiation Expansion
7	Auto-negotiation Next-Page Transmit
8	Auto-negotiation Link Partner Next-Page Receive
9	1000BASE-T Control
10	1000BASE-T Status
11–12	Reserved
13	Clause 45 Access Registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D
14	Clause 45 Access Registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D
15	1000BASE-T Status Extension 1

The following table lists the names of the registers in the main page space of the device. These registers are accessible only when register address 31 is set to 0x0000.

Table 13 • **Main Registers**

Address	Name
16	100BASE-TX status extension
17	1000BASE-T status extension 2
18	Bypass control
19	Error Counter 1
20	Error Counter 2
21	Error Counter 3
22	Extended control and status
23	Extended PHY control 1

Table 13 • **Main Registers *(continued)***

Address	Name
24	Extended PHY control 2
25	Interrupt mask
26	Interrupt status
27	Reserved
28	Auxiliary control and status
29	LED mode select
30	LED behavior
31	Extended register page access

4.2.1 Mode Control

The device register at memory address 0 controls several aspects of the VSC8502 device functionality. The following table shows the available bit settings in this register and what they control.

Table 14 • **Mode Control, Address 0 (0x00)**

Bit	Name	Access	Description	Default
15	Software reset	R/W	Self-clearing. Restores all serial management interface (SMI) registers to default state, except for sticky and super-sticky bits. 1: Reset asserted. 0: Reset de-asserted. Wait 1 µs after setting this bit to initiate another SMI register access.	0
14	Loopback	R/W	1: Loopback enabled. 0: Loopback disabled. When loop back is enabled, the device functions at the current speed setting and with the current duplex mode setting (bits 6, 8, and 13 of this register).	0
13	Forced speed selection LSB	R/W	Least significant bit. MSB is bit 6. 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	0
12	Autonegotiation enable	R/W	1: Autonegotiation enabled. 0: Autonegotiation disabled.	1
11	Power-down	R/W	1: Power-down enabled.	0
10	Isolate	R/W	1: Disable MAC interface outputs and ignore MAC interface inputs.	0
9	Restart autonegotiation	R/W	Self-clearing bit. 1: Restart autonegotiation on media interface.	0
8	Duplex	R/W	1: Full-duplex. 0: Half-duplex.	0
7	Collision test enable	R/W	1: Collision test enabled.	0
6	Forced speed selection MSB	R/W	Most significant bit. LSB is bit 13.(1) 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	10

Table 14 • **Mode Control, Address 0 (0x00) *(continued)***

Bit	Name	Access	Description	Default
5:0	Reserved		Reserved.	00000

1. Before selecting the 1000 Mbps forced speed mode, manually configure the PHY as master or slave by setting bit 11 in register 9 (1000BASE-T Control). Each time the link drops, the PHY needs to be powered down manually to enable it to link up again using the master/slave setting specified in register 9.11.

4.2.2 Mode Status

The register at address 1 in the device main registers space enables reading the currently enabled mode setting. The following table shows possible readouts of this register.

Table 15 • **Mode Status, Address 1 (0x01)**

Bit	Name	Access	Description	Default
15	100BASE-T4 capability	RO	1: 100BASE-T4 capable.	0
14	100BASE-TX FDX capability	RO	1: 100BASE-TX FDX capable.	1
13	100BASE-TX HDX capability	RO	1: 100BASE-TX HDX capable.	1
12	10BASE-T FDX capability	RO	1: 10BASE-T FDX capable.	1
11	10BASE-T HDX capability	RO	1: 10BASE-T HDX capable.	1
10	100BASE-T2 FDX capability	RO	1: 100BASE-T2 FDX capable.	0
9	100BASE-T2 HDX capability	RO	1: 100BASE-T2 HDX capable.	0
8	Extended status enable	RO	1: Extended status information present in register 15.	1
7	Reserved	RO	Reserved.	1
6	Preamble suppression capability	RO	1: MF preamble can be suppressed. 0: MF required.	1
5	Autonegotiation complete	RO	1: Auto-negotiation complete.	0
4	Remote fault	RO	Latches high. 1: Far-end fault detected.	0
3	Autonegotiation capability	RO	1: Auto-negotiation capable.	1
2	Link status	RO	Latches low. 1: Link is up.	0
1	Jabber detect	RO	Latches high. 1: Jabber condition detected.	0
0	Extended capability	RO	1: Extended register capable.	1

4.2.3 Device Identification

All 16 bits in both register 2 and register 3 in the VSC8502 device are used to provide information associated with aspects of the device identification. The following tables list the expected readouts.

Table 16 • **Identifier 1, Address 2 (0x02)**

Bit	Name	Access	Description	Default
15:0	Organizationally unique identifier (OUI)	RO	OUI most significant bits (3:18)	0×0007

Table 17 • **Identifier 2, Address 3 (0x03)**

Bit	Name	Access	Description	Default
15:10	OUI	RO	OUI least significant bits (19:24)	000001
9:4	Microsemi model number	RO	0x12	100011
3:0	Device revision number	RO	Revision A	0000

4.2.4 Auto-Negotiation Advertisement

The bits in address 4 in the main registers space control the ability to notify other devices of the status of its auto-negotiation feature. The following table shows the available settings and readouts.

Table 18 • **Device Auto-Negotiation Advertisement, Address 4 (0x04)**

Bit	Name	Access	Description	Default
15	Next page transmission request	R/W	1: Request enabled	0
14	Reserved	RO	Reserved	0
13	Transmit remote fault	R/W	1: Enabled	0
12	Reserved	R/W	Reserved	0
11	Advertise asymmetric pause	R/W	1: Advertises asymmetric pause	0
10	Advertise symmetric pause	R/W	1: Advertises symmetric pause	0
9	Advertise100BASE-T4	R/W	1: Advertises 100BASE-T4	0
8	Advertise100BASE-TX FDX	R/W	1: Advertise 100BASE-TX FDX	1
7	Advertise100BASE-TX HDX	R/W	1: Advertises 100BASE-TX HDX	1
6	Advertise10BASE-T FDX	R/W	1: Advertises 10BASE-T FDX	1
5	Advertise10BASE-T HDX	R/W	1: Advertises 10BASE-T HDX	1
4:0	Advertise selector	R/W		00001

4.2.5 Link Partner Auto-Negotiation Capability

The bits in main register 5 can be used to determine if the Cat5 link partner (LP) used with the VSC8502 device is compatible with the auto-negotiation functionality.

Table 19 • **Auto-Negotiation Link Partner Ability, Address 5 (0x05)**

Bit	Name	Access	Description	Default
15	LP next page transmission request	RO	1: Requested	0
14	LP acknowledge	RO	1: Acknowledge	0
13	LP remote fault	RO	1: Remote fault	0
12	Reserved	RO	Reserved	0
11	LP advertise asymmetric pause	RO	1: Capable of asymmetric pause	0
10	LP advertise symmetric pause	RO	1: Capable of symmetric pause	0
9	LP advertise 100BASE-T4	RO	1: Capable of 100BASE-T4	0
8	LP advertise 100BASE-TX FDX	RO	1: Capable of 100BASE-TX FDX	0
7	LP advertise 100BASE-TX HDX	RO	1: Capable of 100BASE-TX HDX	0
6	LP advertise 10BASE-T FDX	RO	1: Capable of 10BASE-T FDX	0

Table 19 • **Auto-Negotiation Link Partner Ability, Address 5 (0x05) *(continued)***

Bit	Name	Access	Description	Default
5	LP advertise 10BASE-T HDX	RO	1: Capable of 10BASE-T HDX	0
4:0	LP advertise selector	RO		00000

4.2.6 Auto-Negotiation Expansion

The bits in main register 6 work together with those in register 5 to indicate the status of the LP auto-negotiation functioning. The following table shows the available settings and readouts.

Table 20 • **Auto-Negotiation Expansion, Address 6 (0x06)**

Bit	Name	Access	Description	Default
15:5	Reserved	RO	Reserved.	All zeros
4	Parallel detection fault	RO	This bit latches high. 1: Parallel detection fault.	0
3	LP next page capable	RO	1: LP is next page capable.	0
2	Local PHY next page capable	RO	1: Local PHY is next page capable.	1
1	Page received	RO	This bit latches low. 1: New page is received.	0
0	LP is autonegotiation capable	RO	1: LP is capable of auto-negotiation.	0

4.2.7 Transmit Auto-Negotiation Next Page

The settings in register 7 in the main registers space provide information about the number of pages in an auto-negotiation sequence. The following table shows the settings available.

Table 21 • **Auto-Negotiation Next Page Transmit, Address 7 (0x07)**

Bit	Name	Access	Description	Default
15	Next page	R/W	1: More pages follow	0
14	Reserved	RO	Reserved	0
13	Message page	R/W	1: Message page 0: Unformatted page	1
12	Acknowledge 2	R/W	1: Complies with request 0: Cannot comply with request	0
11	Toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	Message/unformatted code	R/W		00000000001

4.2.8 Auto-Negotiation Link Partner Next Page Receive

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP auto-negotiation. The following table shows the possible readouts.

Table 22 • **Auto-Negotiation LP Next Page Receive, Address 8 (0x08)**

Bit	Name	Access	Description	Default
15	LP next page	RO	1: More pages follow	0
14	Acknowledge	RO	1: LP acknowledge	0

Table 22 • **Auto-Negotiation LP Next Page Receive, Address 8 (0x08) *(continued)***

Bit	Name	Access	Description	Default
13	LP message page	RO	1: Message page 0: Unformatted page	0
12	LP acknowledge 2	RO	1: LP complies with request	0
11	LP toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	LP message/unformatted code	RO		All zeros

4.2.9 1000BASE-T Control

The 1000BASE-T functionality is controlled by the bits in register 9 of the main register space. The following table shows the settings and readouts available.

Table 23 • **1000BASE-T Control, Address 9 (0x09)**

Bit	Name	Access	Description	Default
15:13	Transmitter test mode	R/W	000: Normal 001: Mode 1: Transmit waveform test 010: Mode 2: Transmit jitter test as master 011: Mode 3: Transmit jitter test as slave 100: Mode 4: Transmitter distortion test 101–111: Reserved	000
12	Master/slave manual configuration	R/W	1: Master/slave manual configuration enabled	0
11	Master/slave value	R/W	This register is only valid when bit 9.12 is set to 1. 1: Configure PHY as master during negotiation 0: Configure PHY as slave during negotiation	0
10	Port type	R/W	1: Multi-port device 0: Single-port device	1
9	1000BASE-T FDX capability	R/W	1: PHY is 1000BASE-T FDX capable	1
8	1000BASE-T HDX capability	R/W	1: PHY is 1000BASE-T HDX capable	1
7:0	Reserved	R/W	Reserved	0x00

Note: Transmitter test mode (bits 15:13) operates in the manner described in IEEE 802.3 section 40.6.1.1.2.

4.2.10 1000BASE-T Status

The bits in register 10 of the main register space can be read to obtain the status of the 1000BASE-T communications enabled in the device. The following table shows the readouts.

Table 24 • **1000BASE-T Status, Address 10 (0x0A)**

Bit	Name	Access	Description	Default
15	Master/slave configuration fault	RO	This bit latches high. 1: Master/slave configuration fault detected 0: No master/slave configuration fault detected	0

Table 24 • **1000BASE-T Status, Address 10 (0x0A) *(continued)***

Bit	Name	Access	Description	Default
14	Master/slave configuration resolution	RO	1: Local PHY configuration resolved to master 0: Local PHY configuration resolved to slave	1
13	Local receiver status	RO	1: Local receiver is operating normally	0
12	Remote receiver status	RO	1: Remote receiver OK	0
11	LP 1000BASE-T FDX capability	RO	1: LP 1000BASE-T FDX capable	0
10	LP 1000BASE-T HDX capability	RO	1: LP 1000BASE-T HDX capable	0
9:8	Reserved	RO	Reserved	00
7:0	Idle error count	RO	Self-clearing register	0x00

4.2.11 MMD Access Control Register

The bits in register 13 of the main register space are a window to the EEE registers as defined in IEEE 802.3az-2010 Clause 45.

Table 25 • **MMD EEE Access, Address 13 (0x0D)**

Bit	Name	Access	Description
15:14	Function	R/W	00: Address 01: Data, no post increment 10: Data, post increment for read and write 11: Data, post increment for write only
13:5	Reserved	R/W	Reserved
4:0	DVAD	R/W	Device address as defined in IEEE 802.3az-2010 table 45–1

4.2.12 MMD Address or Data Register

The bits in register 14 of the main register space are a window to the EEE registers as defined in IEEE 802.3az-2010 Clause 45.

Table 26 • **MMD Address or Data Register, Address 14 (0x0E)**

Bit	Name	Access	Description
15:0	Register Address/Data	R/W	When register 13.15:14 = 2'b00, address of register of the device that is specified by 13.4:0. Otherwise, the data to be written to or read from the register.

4.2.13 1000BASE-T Status Extension 1

Register 15 provides additional information about the operation of the device 1000BASE-T communications. The following table shows the readouts available.

Table 27 • **1000BASE-T Status Extension 1, Address 15 (0x0F)**

Bit	Name	Access	Description	Default
15	Reserved	RO	Reserved	0
14	1000BASE-X HDX capability	RO	1: PHY is 1000BASE-X HDX capable	0
13	1000BASE-T FDX capability	RO	1: PHY is 1000BASE-T FDX capable	1

Table 27 • **1000BASE-T Status Extension 1, Address 15 (0x0F) *(continued)***

Bit	Name	Access	Description	Default
12	1000BASE-T HDX capability	RO	1: PHY is 1000BASE-T HDX capable	1
11:0	Reserved	RO	Reserved	0x000

4.2.14 100BASE-TX/FX Status Extension

Register 16 in the main registers page space provides additional information about the status of the 100BASE-TX/100BASE-FX operation.

Table 28 • **100BASE-TX/FX Status Extension, Address 16 (0x10)**

Bit	Name	Access	Description	Default
15	100BASE-TX Descrambler	RO	1: Descrambler locked	0
14	100BASE-TX lock error	RO	Self-clearing bit. 1: Lock error detected	0
13	100BASE-TX disconnect state	RO	Self-clearing bit. 1: PHY 100BASE-TX link disconnect detected	0
12	100BASE-TX current link status	RO	1: PHY 100BASE-TX link active	0
11	100BASE-TX receive error	RO	Self-clearing bit. 1: Receive error detected	0
10	100BASE-TX transmit error	RO	Self-clearing bit. 1: Transmit error detected	0
9	100BASE-TX SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected	0
8	100BASE-TX ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected	0
7:0	Reserved	RO	Reserved	

4.2.15 1000BASE-T Status Extension 2

The second status extension register is at address 17 in the device main registers space. It provides information about another set of parameters associated with 1000BASE-T communications. For information about the first status extension register, see Table 27, page 31.

Table 29 • **1000BASE-T Status Extension 2, Address 17 (0x11)**

Bit	Name	Access	Description	Default
15	1000BASE-T descrambler	RO	1: Descrambler locked.	0
14	1000BASE-T lock error	RO	Self-clearing bit. 1: Lock error detected	0
13	1000BASE-T disconnect state	RO	Self-clearing bit. 1: PHY 1000BASE-T link disconnect detected	0
12	1000BASE-T current link status	RO	1: PHY 1000BASE-T link active	0
11	1000BASE-T receive error	RO	Self-clearing bit. 1: Receive error detected	0

Table 29 • **1000BASE-T Status Extension 2, Address 17 (0x11) *(continued)***

Bit	Name	Access	Description	Default
10	1000BASE-T transmit error	RO	Self-clearing bit. 1: Transmit error detected	0
9	1000BASE-T SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected	0
8	1000BASE-T ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected	0
7	1000BASE-T carrier extension error	RO	Self-clearing bit. 1: Carrier extension error detected	0
6	Non-compliant BCM5400 detected	RO	1: Non-compliant BCM5400 link partner detected	0
5	MDI crossover error	RO	1: MDI crossover error was detected	0
4:0	Reserved	RO	Reserved	

4.2.16 Bypass Control

The bits in this register control aspects of functionality in effect when the device is disabled for the purpose of traffic bypass. The following table shows the settings available.

Table 30 • **Bypass Control, Address 18 (0x12)**

Bit	Name	Access	Description	Default
15	Transmit disable	R/W	1: PHY transmitter disabled	0
14	4B5B encoder/decoder	R/W	1: Bypass 4B/5B encoder/decoder	0
13	Scrambler	R/W	1: Bypass scrambler	0
12	Descrambler	R/W	1: Bypass descrambler	0
11	PCS receive	R/W	1: Bypass PCS receiver	0
10	PCS transmit	R/W	1: Bypass PCS transmit	0
9	LFI timer	R/W	1: Bypass Link Fail Inhibit (LFI) timer	0
8	Reserved	RO	Reserved	
7	HP Auto-MDIX at forced 10/100	R/W	Sticky bit. 1: Disable HP Auto-MDIX at forced 10/100 speeds	1
6	Non-compliant BCM5400 detect disable	R/W	Sticky bit. 1: Disable non-compliant BCM5400 detection	0
5	Disable pair swap correction (HP Auto-MDIX when autonegotiation enabled)	R/W	Sticky bit. 1: Disable the automatic pair swap correction	0
4	Disable polarity correction	R/W	Sticky bit. 1: Disable polarity inversion correction on each subchannel	0
3	Parallel detect control	R/W	Sticky bit. 1: Do not ignore advertised ability 0: Ignore advertised ability	1
2	Pulse shaping filter	R/W	1: Disable pulse shaping filter	0

Table 30 • **Bypass Control, Address 18 (0x12) *(continued)***

Bit	Name	Access	Description	Default
1	Disable automatic 1000BASE-T next page exchange	R/W	Sticky bit. 1: Disable automatic 1000BASE T next page exchanges	0
0	Reserved	RO	Reserved	

Note: If bit 18.1 is set to 1 in this register, automatic exchange of next pages is disabled, and control is returned to the user through the SMI after the base page is exchanged. The user then must send the correct sequence of next pages to the link partner, determine the common capabilities, and force the device into the correct configuration following the successful exchange of pages.

4.2.17 Error Counter 1

The bits in register 19 provide an error counter. The following table shows the settings available.

Table 31 • **Extended Control and Status, Address 19 (0x13)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	100/1000 receive error counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

4.2.18 Error Counter 2

The bits in register 20 provide an error counter. The following table shows the settings available.

Table 32 • **Extended Control and Status, Address 20 (0x14)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	100/1000 false carrier counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

4.2.19 Error Counter 3

The bits in register 21 provide an error counter. The following table shows the settings available.

Table 33 • **Extended Control and Status, Address 21 (0x15)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	Copper media link disconnect counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

4.2.20 Extended Control and Status

The bits in register 22 provide additional device control and readouts. The following table shows the settings available.

Table 34 • **Extended Control and Status, Address 22 (0x16)**

Bit	Name	Access	Description	Default
15	Force 10BASE-T link high	R/W	Sticky bit. 1: Bypass link integrity test 0: Enable link integrity test	0
14	Jabber detect disable	R/W	Sticky bit. 1: Disable jabber detect	0
13	Disable 10BASE-T echo	R/W	Sticky bit. 1: Disable 10BASE-T echo	1
12	Disable SQE mode	R/W	Sticky bit. 1: Disable SQE mode	1
11:10	10BASE-T squelch control	R/W	Sticky bit. 00: Normal squelch 01: Low squelch 10: High squelch 11: Reserved	00
9	Sticky reset enable	R/W	Super-sticky bit. 1: Enabled	1
8	EOF Error	RO	This bit is self-clearing. 1: EOF error detected	0
7	10BASE-T disconnect state	RO	This bit is self-clearing. 1: 10BASE-T link disconnect detected	0
6	10BASE-T link status	RO	1: 10BASE-T link active	0
5:1	Reserved	RO	Reserved	
0	SMI broadcast write	R/W	Sticky bit. 1: Enabled	0

The following information applies to the extended control and status bits:

- When bit 22.15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.
- When bits 22.11:10 are set to 00, the squelch threshold levels are based on the IEEE standard for 10BASE-T. When set to 01, the squelch level is decreased, which can improve the bit error rate performance on long loops. When set to 10, the squelch level is increased and can improve the bit error rate in high-noise environments.
- When bit 22.9 is set, all sticky register bits retain their values during a software reset. Clearing this bit causes all sticky register bits to change to their default values upon software reset. Super-sticky bits retain their values upon software reset regardless of the setting of bit 22.9.
- When bit 22.0 is set, if a write to any PHY register (registers 0–31, including extended registers), the same write is broadcast to all PHYs. For example, if bit 22.0 is set to 1 and a write to PHY0 is executed (register 0 is set to 0x1040), all PHYs' register 0s are set to 0x1040. Disabling this bit restores normal PHY write operation. Reads are still possible when this bit is set, but the value that is read corresponds only to the particular PHY being addressed.

4.2.21 Extended PHY Control 1

The following table shows the settings available.

Table 35 • **Extended PHY Control 1, Address 23 (0x17)**

Bit	Name	Access	Description	Default
15:13[1]	Reserved	R/W	Reserved	001
12	MAC interface selection	R/W	MAC interface mode. 0: GMII/MII 1: RGMII **Note:** This bit may be changed during COMA mode or written prior to a soft-reset after which it takes effect.	0
11:4	Reserved	RO	Reserved.	0000
3	Far-end loopback mode	R/W	1: Enabled.	0
2:0	Reserved	RO	Reserved.	00

1. Reserved bit 13 remains set for correct operation.

Note: After changing bit 12 of the extended PHY control register set 1, a software reset (register 0, bit 15) must be written to change the device operating mode. On read, these bits only indicate the actual operating mode and not the pending operating mode setting before a software reset has taken place.

4.2.22 Extended PHY Control 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table shows the settings and readouts available.

Table 36 • **Extended PHY Control 2, Address 24 (0x18)**

Bit	Name	Access	Description	Default
15:13	100BASE-TX edge rate control	R/W	Sticky bit. 011: +5 edge rate (slowest) 010: +4 edge rate 001: +3 edge rate 000: +2 edge rate 111: +1 edge rate 110: Default edge rate 101: –1 edge rate 100: –2 edge rate (fastest)	000
12	PICMG 2.16 reduced power mode	R/W	Sticky bit. 1: Enabled	0
11:6	Reserved	RO	Reserved	
5:4	Jumbo packet mode	R/W	Sticky bit. 00: Normal IEEE 1.5 kB packet length 01: 9 kB jumbo packet length (12 kB with 60 ppm or better reference clock) 10: 12 kB jumbo packet length (16 kB with 70 ppm or better reference clock) 11: Reserved	00
3:1	Reserved	RO	Reserved	

Table 36 • **Extended PHY Control 2, Address 24 (0x18) *(continued)***

Bit	Name	Access	Description	Default
0	1000BASE-T connector loopback	R/W	1: Enabled	0

Note: When bits 5:4 are set to jumbo packet mode, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the bit description results in a higher jumbo packet length.

4.2.23 Interrupt Mask

These bits control the device interrupt mask. The following table shows the settings available.

Table 37 • **Interrupt Mask, Address 25 (0x19)**

Bit	Name	Access	Description	Default
15	MDINT interrupt status enable	R/W	Sticky bit. 1: Enabled.	0
14	Speed state change mask	R/W	Sticky bit. 1: Enabled.	0
13	Link state change mask	R/W	Sticky bit. 1: Enabled.	0
12	FDX state change mask	R/W	Sticky bit. 1: Enabled.	0
11	Autonegotiation error mask	R/W	Sticky bit. 1: Enabled.	0
10	Autonegotiation complete mask	R/W	Sticky bit. 1: Enabled.	0
9	Inline-powered device (PoE) detect mask	R/W	Sticky bit. 1: Enabled.	0
8	Symbol error interrupt mask	R/W	Sticky bit. 1: Enabled.	0
7	Fast link failure interrupt mask	R/W	Sticky bit. 1: Enabled.	0
6	Wake-on-LAN event interrupt mask	R/W	Sticky bit. 1: Enabled.	0
5	Extended interrupt mask	R/W	Sticky bit. 1: Enabled	0
4	Reserved	R/W	Reserved	0
3	False carrier interrupt mask	R/W	Sticky bit. 1: Enabled.	0
2	Link speed downshift detect mask	R/W	Sticky bit. 1: Enabled.	0
1	Master/Slave resolution error mask	R/W	Sticky bit. 1: Enabled.	0
0	RX_ER interrupt mask	R/W	Sticky bit. 1: Enabled.	0

Note: When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted. Also, before enabling this bit, read register 26 to clear any previously inactive interrupts pending that will cause bit 25.15 to be set.

4.2.24 Interrupt Status

The status of interrupts already written to the device is available for reading from register 26 in the main registers space. The following table shows the expected readouts.

Table 38 • **Interrupt Status, Address 26 (0x1A)**

Bit	Name	Access	Description	Default
15	Interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
14	Speed state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
13	Link state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
12	FDX state change status	RO	Self-clearing bit. 1: Interrupt pending.	0

Table 38 • **Interrupt Status, Address 26 (0x1A) *(continued)***

Bit	Name	Access	Description	Default
11	Autonegotiation error status	RO	Self-clearing bit. 1: Interrupt pending.	0
10	Autonegotiation complete status	RO	Self-clearing bit. 1: Interrupt pending.	0
9	Inline powered device detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
8	Symbol error status	RO	Self-clearing bit. 1: Interrupt pending.	0
7	Fast link failure detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
6	Wake-on-LAN event status	RO	Self-clearing bit. 1: Interrupt pending.	0
5	Extended interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
4	Reserved	RO	Reserved	0
3	False carrier interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
2	Link speed downshift detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
1	Master/Slave resolution error status	RO	Self-clearing bit. 1: Interrupt pending.	0
0	RX_ER interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.2, bits 4.8:5 must be set for this interrupt to assert.
- For bit 26.0, this interrupt will not occur when RX_ER is used for carrier-extension decoding of a link partner's data transmission.
- If bit 5 is set, register 29E2 must be read to determine the source of the interrupt.

4.2.25 Device Auxiliary Control and Status

Register 28 provides control and status information for several device functions not controlled or monitored by other device registers. The following table shows the settings available and the expected readouts.

Table 39 • **Auxiliary Control and Status, Address 28 (0x1C)**

Bit	Name	Access	Description	Default
15	Autonegotiation complete	RO	Duplicate of bit 1.5 when auto-negotiation is enabled, otherwise this is the current link status	0
14	Autonegotiation disabled	RO	Inverted duplicate of bit 0.12	0
13	HP Auto-MDIX crossover indication	RO	1: HP Auto-MDIX crossover performed internally	0
12	CD pair swap	RO	1: CD pairs are swapped	0
11	A polarity inversion	RO	1: Polarity swap on pair A	0
10	B polarity inversion	RO	1: Polarity swap on pair B	0
9	C polarity inversion	RO	1: Polarity swap on pair C	0
8	D polarity inversion	RO	1: Polarity swap on pair D	0

Table 39 • **Auxiliary Control and Status, Address 28 (0x1C) *(continued)***

Bit	Name	Access	Description	Default
7	ActiPHY link status time-out control [1]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 2.3 seconds 01: 3.3 seconds 10: 4.3 seconds 11: 5.3 seconds	0
6	ActiPHY mode enable	R/W	Sticky bit. 1: Enabled	0
5	FDX status	RO	1: Full-duplex 0: Half-duplex	00
4:3	Speed status	RO	00: Speed is 10BASE-T 01: Speed is 100BASE-TX 10: Speed is 1000BASE-T 11: Reserved	0
2	ActiPHY link status time-out control [0]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 2.3 seconds 01: 3.3 seconds 10: 4.3 seconds 11: 5.3 seconds	1
1:0	Media mode status	RO	00: No media selected 01: Copper media selected 10: Reserved 11: Reserved	00

4.2.26 LED Mode Select

The device LED outputs are controlled using the bits in register 29 of the main register space. The following table shows the information needed to access the functionality of each of the outputs. For more information about LED modes, see Table 5, page 14. For information about enabling the extended LED mode bits in Register 19E1 bits 13 to 12, see Table 7, page 17.

Table 40 • **LED Mode Select, Address 29 (0x1D)**

Bit	Name	Access	Description	Default
15:12	LED3 mode select	R/W	Sticky bit. Select from LED modes 0–15.	1000
11:8	LED2 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0000
7:4	LED1 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0010
3:0	LED0 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0001

4.2.27 LED Behavior

The bits in register 30 control and enable you to read the status of the pulse or blink rate of the device LEDs. The following table shows the settings you can write to the register or read from the register.

Table 41 • **LED Behavior, Address 30 (0x1E)**

Bit	Name	Access	Description	Default
15:14	Reserved	R/W	Reserved	0

Table 41 • **LED Behavior, Address 30 (0x1E)** ***(continued)***

Bit	Name	Access	Description	Default
13	Reserved	RO	Reserved	
12	LED pulsing enable	R/W	Sticky bit 0: Normal operation 1: LEDs pulse with a 5 kHz, programmable duty cycle when active	0
11:10	LED blink/pulse-stretch rate	R/W	Sticky bit 00: 2.5 Hz blink rate/400 ms pulse-stretch 01: 5 Hz blink rate/200 ms pulse-stretch 10: 10 Hz blink rate/100 ms pulse-stretch 11: 20 Hz blink rate/50 ms pulse-stretch The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports	01
9	Reserved	RO	Reserved	
8	LED3 pulse-stretch/blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
7	LED2 pulse-stretch/blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
6	LED1 pulse-stretch/blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
5	LED0 pulse-stretch/blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
4	Reserved	RO	Reserved	
3	LED3 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0
2	LED2 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0
1	LED1 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0
0	LED0 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0

Note: Bits 30.11:10 are active only in port 0 and affect the behavior of LEDs for all the ports.

4.2.28 Extended Page Access

To provide functionality beyond the IEEE 802.3-specified registers and main device registers, an extended set of registers provide an additional 15 register spaces.

The register at address 31 controls access to the extended registers. Accessing the GPIO page register space is similar to accessing the extended page registers. The following table shows the settings available.

Table 42 • **Extended/GPIO Register Page Access, Address 31 (0x1F)**

Bit	Name	Access	Description	Default
15:0	Extended/GPIO page register access	R/W	0x0000: Register 16–30 accesses main register space. Writing 0x0000 to register 31 restores the main register access. 0x0001: Registers 16–30 access extended register space 1 0x0002: Registers 16–30 access extended register space 2 0x0003: Registers 16–30 access extended register space 3 0x0010: Registers 0–30 access GPIO register space 0x0004: Registers 16-30 access extended register space 4	0x0000

4.3 Extended Page 1 Registers

To access the extended page 1 registers (17E1–30E1), enable extended register access by writing 0x0001 to register 31. Writing 0x0000 to register 31 restores the main register access.

When extended page 1 register access is enabled, reads and writes to registers 16–30 affect the extended registers 17E1–30E1 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Table 43 • **Extended Registers Page 1 Space**

Address	Name
17E1	Reserved
18E1	Cu Media CRC good counter
19E1	Extended mode control
20E1	Extended PHY control 3 (ActiPHY)
21E1–22E1	Reserved
23E1	Extended PHY control 4 (PoE and CRC error counter)
27E1–28E1	Reserved
29E1	Ethernet packet generator (EPG) 1
30E1	EPG 2

4.3.1 Cu Media CRC Good Counter

Register 18E1 makes it possible to read the contents of the CRC good counter for packets that are received on the Cu media interface; the number of CRC routines that have executed successfully. The following table shows the expected readouts.

Table 44 • **Cu Media CRC Good Counter, Address 18E1 (0x12)**

Bit	Name	Access	Description	Default
15	Packet since last read	RO	Self-clearing bit. 1: Packet received since last read.	0

Table 44 • **Cu Media CRC Good Counter, Address 18E1 (0x12) *(continued)***

Bit	Name	Access	Description	Default
14	Reserved	RO	Reserved.	
13:0	Cu Media CRC good counter contents	RO	Self-clearing bit. Counter containing the number of packets with valid CRCs modulo 10,000; this counter does not saturate and will roll over to zero on the next good packet received after 9,999.	0x000

4.3.2 Extended Mode Control

Register 19E1 controls the extended LED and other chip modes. The following table shows the settings available.

Table 45 • **Extended Mode Control, Address 19E1 (0x13)**

Bit	Name	Access	Description	Default
15	LED3 Extended Mode	R/W	Sticky bit. 1: See Basic Serial LED Mode, page 15	0
14	LED2 Extended Mode	R/W	Sticky bit. 1: See Basic Serial LED Mode, page 15	0
13	LED1 Extended Mode	R/W	Sticky bit. 1: See Basic Serial LED Mode, page 15	0
12	LED0 Extended Mode	R/W	Sticky bit. 1: See Basic Serial LED Mode, page 15	0
11	LED Reset Blink Suppress	R/W	Sticky bit. 1: Blink LEDs after COMA_MODE is de-asserted 0: Suppress LED blink after COMA_MODE is de-asserted	0
10:5	Reserved	RO	Reserved	0
4	Fast link failure	R/W	Sticky bit. Enable fast link failure pin. This must be done from PHY0 only. 1: Enabled 0: Disabled	0
3:2	Force MDI crossover	R/W	Sticky bit. 00: Normal HP Auto-MDIX operation 01: Reserved 10: Copper media forced to MDI 11: Copper media forced MDI-X	00
1	Reserved	RO	Reserved	
0	Reserved	R/W	Reserved	0

4.3.3 ActiPHY Control

Register 20E1 controls the device ActiPHY sleep timer, its wake-up timer, and its link speed downshifting feature. The following table shows the settings available.

Table 46 • **Extended PHY Control 3, Address 20E1 (0x14)**

Bit	Name	Access	Description	Default
15	Disable carrier extension	R/W	1: Disable carrier extension in 1000BASE-T copper links	1
14:13	ActiPHY sleep timer	R/W	Sticky bit. 00: 1 second 01: 2 seconds 10: 3 seconds 11: 4 seconds	01
12:11	ActiPHY wake-up timer	R/W	Sticky bit. 00: 160 ms 01: 400 ms 10: 800 ms 11: 2 seconds	00
10	Slow MDC	R/W	Sticky bit. 1: Indicates that MDC runs at less than 10 MHz (use of this bit is optional and indicated when MDC runs at less than 1 MHz)	0
9	PHY address reversal	R/W	Sticky bit. Reverse PHY address Enabling causes physical PHY 0 to have address of 1, and PHY 1 address of 0. Changing this bit to 1 should initially be done from PHY 0 and changing to 0 from PHY1 1: Enabled 0: Disabled Valid only on PHY0	0
8	Reserved	RO	Reserved	
7:6	Media mode status	RO	00: No media selected 01: Copper media selected 10: Reserved 11: Reserved	00
5	Enable 10BASE-T no preamble mode	R/W	Sticky bit. 1: 10BASE-T will assert RX_DV indication when data is presented to the receiver even without a preamble preceding it	0
4	Enable link speed autodownshift feature	R/W	Sticky bit. 1: Enable auto link speed downshift from 1000BASE-T	0

Table 46 • **Extended PHY Control 3, Address 20E1 (0x14) *(continued)***

Bit	Name	Access	Description	Default
3:2	Link speed auto downshift control	R/W	Sticky bit. 00: Downshift after 2 failed 1000BASE-T auto-negotiation attempts 01: Downshift after 3 failed 1000BASE-T auto-negotiation attempts 10: Downshift after 4 failed 1000BASE-T auto-negotiation attempts 11: Downshift after 5 failed 1000BASE-T auto-negotiation attempts	01
1:0	Reserved	RO	Reserved	0

4.3.4 Ethernet Packet Generator Control 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two separate EPG control registers. The following table shows the settings available in the first register.

Table 47 • **EPG Control Register 1, Address 29E1 (0x1D)**

Bit	Name	Access	Description	Default
15	EPG enable(1)	R/W	1: Enable EPG	0
14	EPG run or stop	R/W	1: Run EPG	0
13	Transmission duration	R/W	1: Continuous (sends in 10,000-packet increments) 0: Send 30,000,000 packets and stop	0
12:11	Packet length	R/W	00: 125 bytes 01: 64 bytes 10: 1518 bytes 11: 10,000 bytes (jumbo packet)	0
10	Interpacket gap	R/W	1: 8,192 ns 0: 96 ns	0
9:6	Destination address	R/W	Lowest nibble of the 6-byte destination address	0001
5:2	Source address	R/W	Lowest nibble of the 6-byte destination address	0000
1	Payload type	R/W	1: Randomly generated payload pattern 0: Fixed based on payload pattern	0
0	Bad frame check sequence (FCS) generation	R/W	1: Generate packets with bad FCS 0: Generate packets with good FCS	0

1. To end forced transmission of EEE LPIs from the PHY, clear the force EEE LPI bit (17E2.4) first before clearing the EPG enable bit (29E1.15).

The following information applies to the EPG control number 1:

- Do not run the EPG when the VSC8502 device is connected to a live network.
- bit 29E1.13 (continuous EPG mode control): When enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.
- The 6-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.

- The 6-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.3.5 Ethernet Packet Generator Control 2

Register 30E1 consists of the second set of bits that provide access to and control over the various aspects of the EPG testing feature. The following table shows the settings available.

Table 48 • **EPG Control Register 2, Address 30E1 (0x1E)**

Bit	Name	Access	Description	Default
15:0	EPG packet payload	R/W	Data pattern repeated in the payload of packets generated by the EPG	0x00

Note: If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E1 is set to 1), that bit (29E1.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.4 Extended Page 2 Registers

To access the extended page 2 registers (16E2–30E2), enable extended register access by writing 0x0002 to register 31. For more information, see Table 42, page 41.

When extended page 2 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E2–30E2 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 2 space. These registers are accessible only when the device register 31 is set to 0x0002.

Table 49 • **Extended Registers Page 2 Space**

Address	Name
16E2	Cu PMD Transmit Control
17E2	EEE Control
18E2	Extended Chip ID
19E2	Reserved
20E2	RGMII Control
21E2	Wake-on-LAN MAC Address [15:0]
22E2	Wake-on-LAN MAC Address [31:16]
23E2	Wake-on-LAN MAC Address [47:32]
24E2	Secure-On Password [15:0]
25E2	Secure-On Password [31:16]
26E2	Secure-On Password [47:32]
27E2	Wake-on-LAN and MDINT Control
28E2	Extended Interrupt Mask
29E2	Extended Interrupt Status
30E2	Ring Resiliency Control

4.4.1 Cu PMD Transmit Control

The register at address 16E2 consists of the bits that provide control over the amplitude settings for the transmit side Cu PMD interface. These bits provide the ability to make small adjustments in the signal amplitude to compensate for minor variations in the magnetics from different vendors. Extreme caution must be exercised when changing these settings from the default values as they have a direct impact on the signal quality. Changing these settings also affects the linearity and harmonic distortion of the transmitted signals. For help with changing these values, contact your Microsemi representative.

Table 50 • **Cu PMD Transmit Control, Address 16E2 (0x10)**

Bit	Name	Access	Description	Default
15:12	1000BASE-T signal amplitude trim(1)	R/W	Sticky bit. 1000BASE-T signal amplitude 1111: -1.7% 1110: -2.6% 1101: -3.5% 1100: -4.4% 1011: -5.3% 1010: -7% 1001: -8.8% 1000: -10.6% 0111: 5.5% 0110: 4.6% 0101: 3.7% 0100: 2.8% 0011: 1.9% 0010: 1% 0001: 0.1% 0000: -0.8%	0000
11:8	100BASE-TX signal amplitude trim(2)	R/W	Sticky bit. 100BASE-TX signal amplitude 1111: -1.7% 1110: -2.6% 1101: -3.5% 1100: -4.4% 1011: -5.3% 1010: -7% 1001: -8.8% 1000: -10.6% 0111 5.5% 0110: 4.6% 0101: 3.7% 0100: 2.8% 0011: 1.9% 0010: 1% 0001: 0.1% 0000: -0.8%	0010

Table 50 • **Cu PMD Transmit Control, Address 16E2 (0x10) *(continued)***

Bit	Name	Access	Description	Default
7:4	10BASE-T signal amplitude trim(3)	R/W	Sticky bit. 10BASE-T signal amplitude 1111: -7% 1110: -7.9% 1101: -8.8% 1100: -9.7% 1011: -10.6% 1010: -11.5% 1001: -12.4% 1000: -13.3% 0111: 0% 0110: -0.7% 0101: -1.6% 0100: -2.5% 0011: -3.4% 0010: -4.3% 0001: -5.2% 0000: -6.1%	1011
3:0	10BASE-Te signal amplitude trim	R/W	Sticky bit. 10BASE-Te signal amplitude 1111: -30.45% 1110: -31.1% 1101: -31.75% 1100: -32.4% 1011: -33.05% 1010: -33.7% 1001: -34.35% 1000: -35% 0111: -25.25% 0110: -25.9% 0101: -26.55% 0100: -27.2% 0011: -27.85% 0010: -28.5% 0001: -29.15% 0000: -29.8%	1110

1. Changes to 1000BASE-T amplitude may result in unpredictable side effects.
2. Adjust 100BASE-TX to specific magnetics.
3. Amplitude is limited by V_{CC} (2.5 V).

4.4.2 EEE Control

The register at address 17E2 consists of the bits that provide additional control over the chip behavior in energy efficient Ethernet (IEEE 802.3az-2010) mode for debug.

Table 51 • **EEE Control, Address 17E2 (0x11)**

Bit	Name	Access	Description	Default
15	Enable 10BASE-Te	R/W	Sticky bit. Enable energy efficient (IEEE 802.3az-2010) 10BASE-Te operating mode.	0
14	Reserved	R/W	Reserved	0

Table 51 • **EEE Control, Address 17E2 (0x11) *(continued)***

Bit	Name	Access	Description	Default
13:10	Invert LED polarity	R/W	Sticky bit. Invert polarity of LED[3:0]_PHY[1:0] signals. Default is to drive an active low signal on the LED pins. This also applies to enhanced serial LED mode. For more information, see Enhanced Serial LED Mode, page 16.	0000
9	Reserved	RO	Reserved.	
8	Link status	RO	1: Link is up.	0
7	1000BASE-T EEE enable	RO	1: EEE is enabled for 1000BASE-T.	0
6	100BASE-TX EEE enable	RO	1: EEE is enabled for 100BASE-TX.	0
5	Enable 1000BASE-T force mode	R/W	Sticky bit. 1: Enable 1000BASE-T force mode to allow PHY to link-up in 1000BASE-T mode without forcing master/slave when register 0, bits 6 and 13 are set to 2'b10.	0
4	Force transmit LPI (1, 2)	R/W	Sticky bit. 1: Enable the EPG to transmit LPI on the MDI, ignore data from the MAC interface. 0: Transmit idles being received from the MAC.	0
3	Inhibit 100BASE-TX transmit EEE LPI	R/W	Sticky bit. 1: Disable transmission of EEE LPI on transmit path MDI in 100BASE-TX mode when receiving LPI from MAC.	0
2	Inhibit 100BASE-TX receive EEE LPI	R/W	Sticky bit. 1: Disable transmission of EEE LPI on receive path MAC interface in 100BASE-TX mode when receiving LPI from the MDI.	0
1	Inhibit 1000BASE-T transmit EEE LPI	R/W	Sticky bit. 1: Disable transmission of EEE LPI on transmit path MDI in 1000BASE-T mode when receiving LPI from MAC.	0
0	Inhibit 1000BASE-T receive EEE LPI	R/W	Sticky bit. 1: Disable transmission of EEE LPI on receive path MAC interface in 1000BASE-T mode when receiving LPI from the MDI.	0

1. To end forced transmission of EEE LPIs from the PHY, clear this bit first before clearing the EPG enable bit (29E1.15).
2. 17E2 bits 4:0 are for debugging purposes only, not for operational use.

4.4.3 Extended Chip ID

The following table shows the register settings for the extended chip ID at address 18E2.

Table 52 • **Extended Chip ID, Address 18E2 (0x12)**

Bit	Name	Access	Description	Default
15	Industrial temperature capable	RO	1: Industrial temperature capable 0: Commercial temperature capable	

Table 52 • **Extended Chip ID, Address 18E2 (0x12) *(continued)***

Bit	Name	Access	Description	Default
14	Reserved	RO	Reserved	1
13:10	Reserved	RO	Reserved	0
	Reserved	RO	Reserved	0
7:0	Extended chip ID	RO	Dash number of the device in BCD	

4.4.4 RGMII Control

The following table shows the register settings for the RGMII controls at address 20E2.

Table 53 • **RGMII Control, Address 20E2 (0x14)**

Bit	Name	Access	Description	Default
15:12	Reserved	RO	Reserved	0
11	RX_CLK output disable	R/W	Sticky bit. 0: Normal RX_CLK behavior 1: RXCLK driven low	1
10:8	Reserved	RO	Reserved	0
7	RGMII/GMII RXD bit reversal	R/W	Sticky bit. When set to 1 makes the following reversed mapping internally. **RGMII mode** RXD3_[1:0] maps to RXD0_[1:0] RXD2_[1:0] maps to RXD1_[1:0] RXD1_[1:0] maps to RXD2_[1:0] RXD0_[1:0] maps to RXD3_[1:0] **GMII/MII mode** RXD7_[1:0] maps to RXD0_[1:0] RXD6_[1:0] maps to RXD1_[1:0] RXD5_[1:0] maps to RXD2_[1:0] RXD4_[1:0] maps to RXD3_[1:0] RXD3_[1:0] maps to RXD4_[1:0] RXD2_[1:0] maps to RXD5_[1:0] RXD1_[1:0] maps to RXD6_[1:0] RXD0_[1:0] maps to RXD7_[1:0]	0
6:4	RX_CLK_[1:0] delay	R/W	Sticky bit. 000: 0.2 ns delay 001: 0.8 ns delay 010: 1.1 ns delay 011: 1.7 ns delay 100: 2.0 ns delay 101: 2.3 ns delay 110: 2.6 ns delay 111: 3.4 ns delay	000

Table 53 • **RGMII Control, Address 20E2 (0x14) *(continued)***

Bit	Name	Access	Description	Default
3	RGMII/GMII TXD bit reversal	R/W	Sticky bit. When set to 1 makes the following reversed mapping internally. **RGMII mode** TXD3_[1:0] maps to TXD0_[1:0] TXD2_[1:0] maps to TXD1_[1:0] TXD1_[1:0] maps to TXD2_[1:0] TXD0_[1:0] maps to TXD3_[1:0] **GMII/MII mode** TXD7_[1:0] maps to TXD0_[1:0] TXD6_[1:0] maps to TXD1_[1:0] TXD5_[1:0] maps to TXD2_[1:0] TXD4_[1:0] maps to TXD3_[1:0] TXD3_[1:0] maps to TXD4_[1:0] TXD2_[1:0] maps to TXD5_[1:0] TXD1__[1:0] maps to TXD6_[1:0] TXD0_[1:0] maps to TXD7_[1:0]	0
2:0	GTX_CLK_[1:0] delay	R/W	Sticky bit. 000: 0.2 ns delay 001: 0.8 ns delay 010: 1.1 ns delay 011: 1.7 ns delay 100: 2.0 ns delay 101: 2.3 ns delay 110: 2.6 ns delay 110: 3.4 ns delay	000

4.4.5 Wake-on-LAN MAC Address [15:0]

The following table shows the register settings for the Wake-on-LAN MAC address at 21E2.

Table 54 • **Wake-on-LAN MAC Address, 21E2 (0x15)**

Bit	Name	Access	Description	Default
15:0	WoL MAC address [15:0]	RW	Sticky bit. WoL MAC address lower two bytes	00

4.4.6 Wake-on-LAN MAC Address [31:16]

The following table shows the register settings for the Wake-on-LAN MAC address at 22E2.

Table 55 • **Wake-on-LAN MAC Address, 22E2 (0x16)**

Bit	Name	Access	Description	Default
15:0	WoL MAC address [31:16]	RW	Sticky bit. WoL MAC address middle two bytes	00

4.4.7 Wake-on-LAN MAC Address [47:32]

The following table shows the register settings for the Wake-on-LAN MAC address at 23E2.

Table 56 • **Wake-on-LAN MAC Address, 23E2 (0x17)**

Bit	Name	Access	Description	Default
15:0	WoL MAC address [47:32]	RW	Sticky bit. WoL MAC address upper two bytes	00

4.4.8 Secure-On Password [15:0]

The following table shows the register settings for the Secure-On password used for WoL at 24E2.

Table 57 • **Secure-On Password, 24E2 (0x18)**

Bit	Name	Access	Description	Default
15:0	Secure-On password [15:0]	RW	Sticky bit. Secure-On password for WoL lower two bytes	00

4.4.9 Secure-On Password [31:16]

The following table shows the register settings for the Secure-On password used for WoL at 25E2.

Table 58 • **Secure-On Password, 25E2 (0x19)**

Bit	Name	Access	Description	Default
15:0	Secure-On password [31:16]	RW	Sticky bit. Secure-On password for WoL middle two bytes	00

4.4.10 Secure-On Password [47:32]

The following table shows the register settings for the Secure-On password used for WoL at 26E2.

Table 59 • **Secure-On Password, 26E2 (0x1A)**

Bit	Name	Access	Description	Default
15:0	Secure-On password [47:32]	RW	Sticky bit. Secure-On password for WoL upper two bytes	00

4.4.11 Wake-on-LAN and MDINT Control

The following table shows the register settings for the Wake-on-LAN and MDINT control at address 27E2.

Table 60 • **WoL and MDINT Control, Address 27E2 (0x1B)**

Bit	Name	Access	Description	Default
15	Secure-On enable	R/W	Sticky bit. 0: Disabled 1: Enabled	0
14	Secure-On password length	R/W	Sticky bit. 0: 6 byte password 1: 4 byte password	0

Table 60 • **WoL and MDINT Control, Address 27E2 (0x1B) *(continued)***

Bit	Name	Access	Description	Default
11:8	Address repetition count in Magic packet	R/W	Sticky bit. Count value 0000: 1 0001: 2 0010: 3 0011: 4 0100: 5 0101: 6 0110: 7 0111: 8 1000: 9 1001: 10 1010: 11 1011: 12 1100: 13 1101: 14 1110: 15 1111: 16	1111
7:2	Reserved	RO	Reserved	000000
1	MDINT signal control	R/W	Sticky bit. 0: interrupt signals from both ports are combined and then driven onto both MDINT pins 1: interrupt signals from Port 0 are indicated on MDINT_0 and interrupt signals from Port 1 are indicated on MDINT_1	0
0	Reserved	R/W	Reserved	0

4.4.12 Extended Interrupt Mask

The following table shows the register settings for the extended interrupt mask at address 28E2.

Table 61 • **Extended Interrupt Mask, Address 28E2 (0x1C)**

Bit	Name	Access	Description	Default
15:14	Reserved	RO	Reserved.	00
13	Rx FIFO overflow/underflow interrupt mask	R/W	Sticky bit. 1: Enabled.	0
12	Tx FIFO overflow/underflow interrupt mask	R/W	Sticky bit. 1: Enabled.	0
11:5	Reserved	RO	Reserved.	0
4	RR switchover complete interrupt mask	R/W	Sticky bit. 1: Enabled.	0
3	EEE link fail interrupt mask	R/W	Sticky bit. 1: Enabled.	0
2	EEE Rx TQ timer interrupt mask	R/W	Sticky bit. 1: Enabled.	0
1	EEE wait quiet/Rx TS timer interrupt mask	R/W	Sticky bit. 1: Enabled.	0
0	EEE wake error interrupt mask	R/W	Sticky bit. 1: Enabled.	0

4.4.13 Extended Interrupt Status

The following table shows the register settings for the extended interrupt status at address 29E2.

Table 62 • **Extended Interrupt Status, Address 29E2 (0x1D)**

Bit	Name	Access	Description	Default
15:14	Reserved	RO	Reserved.	00000
13	Rx FIFO overflow/underflow interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
12	Tx FIFO overflow/underflow interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
11:5	Reserved	RO	Reserved.	0
4	RR switchover complete interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
3	EEE link fail interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
2	EEE Rx TQ timer interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
1	EEE wait quiet/Rx TS timer interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
0	EEE wake error interrupt mask	RO	Self-clearing bit. 1: Interrupt pending.	0

4.4.14 Ring Resiliency Control

The following table shows the register settings for the ring resiliency controls at address 30E2.

Table 63 • **Ring Resiliency, Address 30E2 (0x1E)**

Bit	Name	Access	Description	Default
15	Ring resiliency startup enable (master TR enable)	R/W	Sticky	0
14	Advertise ring resiliency	R/W	Sticky	0
13	LP ring resiliency advertisement	RO		0
12	Force ring resiliency enable (override autoneg)	R/W	Sticky	0
11:6	Reserved	RO	Reserved	000000
5:4	Ring resiliency status	RO	Ring resiliency status (from r1000 DSP SM) 00: Timing slave(1) 10: Timing slave becoming master 11: Timing master(1) 01: Timing master becoming slave	00
3:1	Reserved	RO	Reserved	000
0	Start switchover (only when not in progress)	RWSC		0

1. Reflects autoneg master/slave at initial link-up.

4.5 General Purpose Registers

Accessing the general purpose register space is similar to accessing the extended page registers. Set register 31 to 0x0010. This sets all 32 registers to the general purpose register space.

To restore main register page access, write 0x0000 to register 31. All general purpose register bits are super-sticky.

4.5.1 Reserved General Purpose Address Space

The bits in registers 0G to 13G, 15G to 18G, and 30G of the general purpose register space are reserved.

4.5.2 GPIO Control 2

The GPIO control 2 register configures the functionality of the COMA_MODE input pins, and provides control for possible GPIO pin options.

Table 64 • **GPIO Control 2, Address 14G (0x0E)**

Bit	Name	Access	Description	Default
15:14	Reserved	R/W	Reserved.	00
13	COMA_MODE output enable (active low)	R/W	1: COMA_MODE pin is an input. 0: COMA_MODE pin is an output.	1
12	COMA_MODE output data	R/W	Value to output on the COMA_MODE pin when it is configured as an output.	0
11	COMA_MODE input data	RO	Data read from the COMA_MODE pin.	
10	Reserved	RO	Reserved.	0
9	Tri-state enable for LEDs	R/W	1: Tri-state LED output signals instead of driving them high. This allows the signals to be pulled above V_{VDDIO} using an external pull-up resistor. 0: Drive LED bus output signals to high and low values.	1
8:0	Reserved	RO	Reserved.	0

4.5.3 MAC Configuration and Fast Link

Register 19G in the GPIO register space controls the selection of the source PHY for the fast link failure indication. The following table shows the settings available for the FASTLINK_FAIL pin.

Table 65 • **MAC Configuration and Fast Link Register, Address 19G (0x13)**

Bit	Name	Access	Description	Default
15:2	Reserved	RO	Reserved	
1:0	Fast link failure port setting	R/W	Select fast link failure PHY source 00: Port0 01: Port1 10–11: Output disabled	11

4.5.4 Recovered Clock 1 Control

Register 23G in the extended register space controls the functionality of the recovered clock 1 output signal.

Table 66 • **Recovered Clock 1 Control, Address 23G (0x17)**

Bit	Name	Access	Description	Default
15	Enable RCVRDCLK1	R/W	1: Enable recovered clock 1 output 0: Disable recovered clock 1 output	0
14:11	Clock source select	R/W	Select bits for source PHY for recovered clock: 0000: PHY0 0001: PHY1 0100–1111: Reserved	0000
10:8	Clock frequency select	R/W	Select output clock frequency: 000: 25 MHz output clock 001: 125 MHz output clock 010: 31.25 MHz output clock 011–111: Reserved	000
7:6	Reserved	RO	Reserved.	
5:4	Clock squelch level	R/W	Select clock squelch level 00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave). 01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE. 10: Squelch only when the link is not up. 11: Disable clock squelch. **Note:** A clock from the Cu PHY will be output on the recovered clock output in this mode when the link is down. When the CLK_SQUELCH_IN pin is set high, it squelches the recovered clocks regardless of bit settings.	
3	Reserved	RO	Reserved.	000
2:0	Clock selection for specified PHY	R/W	001: Copper PHY recovered clock 010: Copper PHY transmitter TCLK 011–111: Reserved	

4.5.5 Recovered Clock 2 Control

Register 24G in the extended register space controls the functionality of the recovered clock 2 output signal.

Table 67 • **Recovered Clock 2 Control, Address 24G (0x18)**

Bit	Name	Access	Description	Default
15	Enable RCVRDCLK2	R/W	1: Enable recovered clock 2 output 0: Disable recovered clock 2 output	0
14:11	Clock source select	R/W	Select bits for source PHY for recovered clock: 0000: PHY0 0001: PHY1 0010–1111: Reserved	0000
10:8	Clock frequency select	R/W	Select output clock frequency: 000: 25 MHz output clock 001: 125 MHz output clock 010: 31.25 MHz output clock 011–111: Reserved	000
7:6	Reserved	RO	Reserved	
5:4	Clock squelch level	R/W	Select clock squelch level: 00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave). 01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE 10: Squelch only when the link is not up 11: Disable clock squelch. **Note:** A clock from the Cu PHY will be output on the recovered clock output in this mode when the link is down. When the CLK_SQUELCH_IN pin is set high, it squelches the recovered clocks regardless of bit settings.	
3	Reserved	RO	Reserved	
2:0	Clock selection for specified PHY	R/W	000: Reserved 001: Copper PHY recovered clock 010–111: Reserved	000

4.5.6 Enhanced LED Control

The following table contains the bits to control advanced functionality of the parallel and serial LED signals.

Table 68 • **Enhanced LED Control, Address 25G (0x19)**

Bit	Name	Access	Description	Default
15:8	LED pulsing duty cycle control	R/W	Programmable control for LED pulsing duty cycle when bit 30.12 is set to 1. Valid settings are between 0 and 198. A setting of 0 corresponds to a 0.5% duty cycle and 198 corresponds to a 99.5% duty cycle. Intermediate values change the duty cycle in 0.5% increments	00
7	Port 1 enhanced serial LED output enable	R/W	Enable the enhanced serial LED output functionality for port 1 LED pins. 1: Enhanced serial LED outputs 0: Normal function	0
6	Port 0 enhanced serial LED output enable	R/W	Enable the enhanced serial LED output functionality for port 0 LED pins. 1: Enhanced serial LED outputs 0: Normal function	0
5:3	Serial LED frame rate selection	R/W	Select frame rate of serial LED stream 000: 2500 Hz frame rate 001: 1000 Hz frame rate 010: 500 Hz frame rate 011: 250 Hz frame rate 100: 200 Hz frame rate 101: 125 Hz frame rate 110: 40 Hz frame rate 111: Output basic serial LED stream See Table 6, page 16.	
2:1	Serial LED select	R/W	Select which LEDs from each PHY to enable on the serial stream 00: Enable all four LEDs of each PHY 01: Enable LEDs 2, 1 and 0 of each PHY 10: Enable LEDs 1 and 0 of each PHY 11: Enable LED 0 of each PHY	00
0	LED port swapping	R/W	0: LED port swapping disabled 1: LED port swapping enabled	0

4.5.7 Global Interrupt Status

The following table contains the interrupt status from the various sources to indicate which one caused that last interrupt on the pin.

Table 69 • **Global Interrupt Status, Address 29G (0x1D)**

Bit	Name	Access	Description
15:2	Reserved	RO	Reserved
1	PHY1 interrupt source	RO	PHY1 interrupt source indication 0: PHY1 caused the interrupt 1: PHY1 did not cause the interrupt

Table 69 • **Global Interrupt Status, Address 29G (0x1D) *(continued)***

Bit	Name	Access	Description
0	PHY0 interrupt source	RO	PHY0 interrupt source indication 0: PHY0 caused the interrupt 1: PHY0 did not cause the interrupt

4.6 Clause 45 Registers to Support Energy Efficient Ethernet and 802.3bf

This section describes the Clause 45 registers that are required to support energy efficient Ethernet. Access to these registers is through the IEEE standard registers 13 and 14 (MMD access control and MMD data or address registers) as described in section 4.2.11 and 4.2.12.

The following table lists the addresses and register names in the Clause 45 register page space. When the link is down, 0 is the value returned for the x.180x addresses.

Table 70 • **Clause 45 Registers Page Space**

Address	Name
1.1	PMA/PMD status 1
3.1	PCS status 1
3.20	EEE capability
3.22	EEE wake error counter
4.1800	TimeSync PHY XS Capability
4.1801	Tx maximum delay through xMII (GMII, RGMII, including FIFO variations)
4.1803	Tx minimum delay through xMII (GMII, RGMII, including FIFO variations)
4.1805	Rx maximum delay through xMII (GMII, RGMII, including FIFO variations)
4.1807	Rx minimum delay through xMII (GMII, RGMII, including FIFO variations)
7.60	EEE advertisement
7.61	EEE link partner advertisement

4.6.1 PMA/PMD Status 1

The following table shows the bit descriptions for the PMA/PMD Status 1 register.

Table 71 • **PMA/PMD Status 1**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	PMD/PMA receive link status	RO/LL	1: PMA/PMD receive link up 0: PMA/PMD receive link down
1:0	Reserved	RO	Reserved

4.6.2 PCS Status 1

The bits in the PCS Status 1 register provide a status of the EEE operation from the PCS for the link that is currently active.

Table 72 • **PCS Status 1, Address 3.1**

Bit	Name	Access	Description
15:12	Reserved	RO	Reserved
11	Tx LPI received	RO/LH	1: Tx PCS has received LPI 0: LPI not received
10	Rx LPI received	RO/LH	1: Rx PCS has received LPI 0: LPI not received
9	Tx LPI indication	RO	1: Tx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
8	Rx LPI indication	RO	1: Rx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
7:3	Reserved	RO	Reserved
2	PCS receive link status	RO/LL	1: PCS receive link up 0: PCS receive link down
1:0	Reserved	RO	Reserved

4.6.3 EEE Capability

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The following table shows the bit assignments for the EEE capability register.

Table 73 • **EEE Capability, Address 3.20**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	1000BASE-T EEE	RO	1: EEE is supported for 1000BASE-T 0: EEE is not supported for 1000BASE-T
1	100BASE-TX EEE	RO	1: EEE is supported for 100BASE-TX 0: EEE is not supported for 100BASE-TX
0	Reserved	RO	Reserved

4.6.4 EEE Wake Error Counter

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and can occur during a refresh or a wakeup as defined by the PHY. This 16-bit counter is reset to all zeros when the EEE wake error counter is read or when the PHY undergoes hardware or software reset.

Table 74 • **EEE Wake Error Counter, Address 3.22**

Bit	Name	Access	Description
15:0	Wake error counter	RO	Count of wake time faults for a PHY

4.6.5 EEE Advertisement

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code. The following table shows the bit assignments for the EEE advertisement register.

Table 75 • **EEE Advertisement, Address 7.60**

Bit	Name	Access	Description	Default
15:3	Reserved	RO	Reserved	
2	1000BASE-T EEE	R/W	1: Advertise that the 1000BASE-T has EEE capability 0: Do not advertise that the 1000BASE-T has EEE capability	0
1	100BASE-TX EEE	R/W	1: Advertise that the 100BASE-TX has EEE capability 0: Do not advertise that the 100BASE-TX has EEE capability	0
0	Reserved	RO	Reserved	

4.6.6 EEE Link Partner Advertisement

All the bits in the EEE LP Advertisement register are read only. A write to the EEE LP advertisement register has no effect. When the AN process has been completed, this register will reflect the contents of the link partner's EEE advertisement register. The following table shows the bit assignments for the EEE advertisement register.

Table 76 • **EEE Advertisement, Address 7.61**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	1000BASE-T EEE	RO	1: Link partner is advertising EEE capability for 1000BASE-T 0: Link partner is not advertising EEE capability for 1000BASE-T
1	100BASE-TX EEE	RO	1: Link partner is advertising EEE capability for 100BASE-TX 0: Link partner is not advertising EEE capability for 100BASE-TX
0	Reserved	RO	Reserved

The following table shows the bit assignments for the 802.3bf registers. When the link is down, 0 is the value returned. cl45reg1_1801 would be device address of 1 and register address of 1801.

Table 77 • **802.3bf Registers**

Register	Name	Function
1.1800	PMA/PMD Time Sync capable	1: PMA/PMD Time Sync Tx capable 0: PMA/PMD Time Sync Rx capable
1.1801	cl45reg1_1801_val[15:0]	Tx maximum delay through PHY (PMA/PMD/PCS)
1.1803	cl45reg1_1803_val[15:0]	Tx minimum delay through PHY (PMA/PMD/PCS)
1.1805	cl45reg1_1805_val[15:0]	Rx maximum delay through PHY (PMA/PMD/PCS)
1.1807	cl45reg1_1807_val[15:0]	Rx minimum delay through PHY (PMA/PMD/PCS)

For information about PHY latency specifications between the media interface and the MAC interface, see PHY Latency Specifications, page 64.

5 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8502 device.

5.1 DC Characteristics

This section contains the DC specifications for the VSC8502 device.

5.1.1 VDDMAC0, VDDMAC1, VDDIO, and VDDMDIO (2.5 V)

The following table shows the DC specifications for the pins referenced to VDDMAC0, VDDMAC1, VDDIO, and VDDMDIO when it is set to 2.5 V. The specifications listed in the following table are valid only when V_{DD1} = 1.0 V, V_{DD1A} = 1.0 V, and V_{DD25A} = 2.5 V.

Table 68 • **VDDMAC0, VDDMAC1, VDDIO, and VDDMDIO (2.5 V) DC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.0		V	I_{OH} = –1.0 mA
Output low voltage	V_{OL}		0.4	V	I_{OL} = 1.0 mA
Input high voltage	V_{IH}	1.85	3.6	V	
Input low voltage	V_{IL}	–0.3	0.7	V	
Input leakage current	I_{ILEAK}	–85	85	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–85	85	µA	Internal resistor included
Output low current drive strength	I_{OL}	6		mA	
Output high current drive strength	I_{OH}		–6	mA	

5.1.2 VDDMAC0, VDDMAC1, VDDIO, and VDDMDIO (3.3 V)

The following table shows the DC specifications for the pins referenced to VDDMAC0, VDDMAC1, VDDIO, and VDDMDIO when it is set to 3.3 V. The specifications listed in the following table are valid only when V_{DD1} = 1.0 V, V_{DD1A} = 1.0 V, and V_{DD25A} = 2.5 V.

Table 69 • **VDDMAC0, VDDMAC1, VDDIO, and VDDMDIO (3.3 V) DC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.6		V	I_{OH} = –1.0 mA
Output low voltage	V_{OL}		0.4	V	I_{OL} = 1.0 mA
Input high voltage	V_{IH}	2.25	3.6	V	
Input low voltage	V_{IL}	–0.3	0.8	V	
Input leakage current	I_{ILEAK}	–125	125	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–125	125	µA	Internal resistor included
Output low current drive strength	I_{OL}	6		mA	
Output high current drive strength	I_{OH}		–6	mA	

5.1.3 VDDMDIO (1.2 V)

The following table shows the DC specifications for the pins referenced to VDDMDIO when it is set to 1.2 V. The specifications listed in the following table are valid only when V_{DD1} = 1.0 V, V_{DD1A} = 1.0 V, and V_{DD25A} = 2.5 V.

Table 70 • **VDDMDIO DC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	0.95		V	I_{OH} = –100 µA
Output low voltage	V_{OL}		0.2	V	I_{OL} = 100 µA
Input high voltage	V_{IH}	0.9	1.5	V	
Input low voltage	V_{IL}	–0.3	0.36	V	
Input leakage current	I_{ILEAK}	–32	32	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–32	32	µA	Internal resistor included
Output low current drive strength	I_{OL}	4		mA	V_{OL} = 0.2 V
Output high current drive strength	I_{OH}		–4	mA	V_{OH} = 1.0 V

5.1.4 LED

The following table shows the DC specifications for the LED pins.

Table 71 • **LED DC Characteristics**

Pin	Symbol	Minimum	Maximum	Unit
LED	I_{OH}		–24	mA
LED	I_{OL}	24		mA

5.1.5 Internal Pull-Up or Pull-Down Resistors

Internal pull-up or pull-down resistors are specified in the following table. For more information about signals with internal pull-up or pull-down resistors, see Pins by Function, page 68.

All internal pull-up resistors are connected to their respective I/O supply.

Table 72 • **Internal Pull-Up or Pull-Down Resistors**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Internal pull-up resistor, all others	R_{PU}	26	39	64	kΩ	3.3 V
Internal pull-down resistor	R_{PD}	26	45	79	kΩ	3.3 V
Internal pull-up resistor, all others	R_{PU}	33	53	93	kΩ	2.5 V
Internal pull-down resistor	R_{PD}	34	58	108	kΩ	2.5 V

5.1.6 Power Consumption

The following tables show the power consumption values. Add significant margin for sizing power supplies. Add values to calculate total power on each power supply with those functions enabled.

Table 73 • **RGMII/GMII/MII Mode, Regulator Enabled**

	Typical				Maximum			
Mode	**VDDMAC0/1 (mA) at 3.3 V**	**VDDIO (mA) at 3.3 V**	**VDD33 (mA) at 3.3 V**	**Power (mW)**	**VDDMAC0/1 (mA) at 3.465 V**	**VDDIO (mA) at 3.465 V**	**VDD33 (mA) at 3.465 V**	**Power (mW)**
NRESET asserted	1	1	36	125				
Power down, COMA mode	1	1	56	191				
ActiPHY	1	1	66	224				
10BASE-Te idle	5	1	96	337	5	1	146	527
10BASE-Te traffic	5	1	151	518	5	1	201	717
10BASE-T idle	5	1	96	337	5	1	146	527
10BASE-T traffic	5	1	151	518	5	1	206	735
100BASE-TX idle	20	1	206	749	10	1	206	752
100BASE-TX traffic	30	1	206	782	30	1	266	1029
100BASE-TX EEE, LP idle	15	1	131	485				
1000BASE-T idle	80	1	346	1409	85	1	426	1774
1000BASE-T traffic	140	1	351	1624	150	1	426	1999
1000BASE-T EEE, LP idle	80	1	136	716				

Table 74 • **RGMII/GMII/MII Mode, Regulator Disabled**

	Typical					Maximum				
Mode	**VDD1 (mA) at 1.0 V**	**VDD1A (mA) at 1.0 V**	**VDD25 (mA) at 2.5 V**	**VDD25A (mA) at 2.5 V**	**Power (mW)**	**VDD1 (mA) at 1.05 V**	**VDD1A (mA) at 1.05 V**	**VDD25 (mA) at 2.625 V**	**VDD25A (mA) at 2.625 V**	**Power (mW)**
NRESET asserted	38	11	1	3	59					
Power down, COMA mode	48	30	1	20	131					
ActiPHY	53	30	1	30	161					
10BASE-Te idle	58	35	1	65	258	180	65	2	70	446

Table 74 • **RGMII/GMII/MII Mode, Regulator Disabled *(continued)***

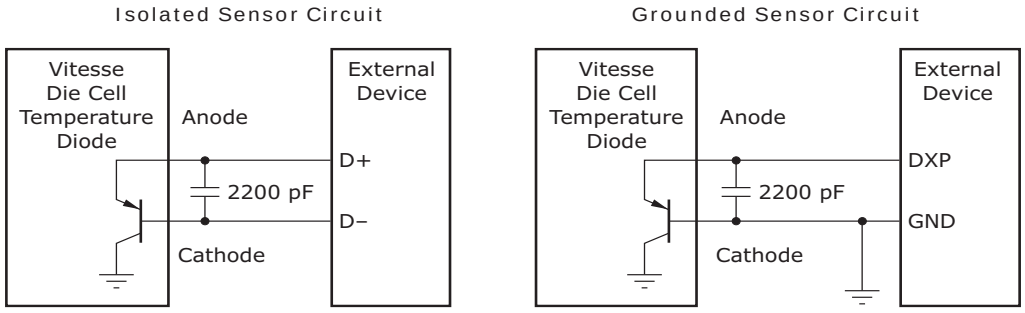
	Typical					Maximum				
Mode	VDD1 (mA) at 1.0 V	VDD1A (mA) at 1.0 V	VDD25 (mA) at 2.5 V	VDD25A (mA) at 2.5 V	Power (mW)	VDD1 (mA) at 1.05 V	VDD1A (mA) at 1.05 V	VDD25 (mA) at 2.625 V	VDD25A (mA) at 2.625 V	Power (mW)
10BASE-Te traffic	58	35	2	125	411	180	65	2	135	617
10BASE-T idle	58	35	1	65	258	180	65	2	70	446
10BASE-T traffic	58	35	1	135	433	180	65	2	140	630
100BASE-TX idle	83	35	15	185	618	205	65	15	200	848
100BASE-TX traffic	83	35	20	185	631	205	65	20	200	861
100BASE-TX EEE, LP idle	58	30	10	105	376					
1000BASE-T idle	168	45	60	290	1088	310	70	60	285	1305
1000BASE-T traffic	178	45	100	290	1198	315	75	110	295	1473
1000BASE-T EEE, LP idle	63	30	60	105	506					

5.1.7 Thermal Diode

The device includes an on-die diode and internal circuitry for monitoring die temperature (junction temperature). The operation and accuracy of the diode is not guaranteed and should only be used as a reference.

The on-die thermal diode requires an external thermal sensor, located on the board or in a stand-alone measurement kit. Temperature measurement using a thermal diode is very sensitive to noise. The following illustration shows a generic application design.

Figure 19 • **Thermal Diode**



Note: Microsemi does not support or recommend operation of the thermal diode under reverse bias.

The following table provides the diode parameter and interface specifications with the pins connected internally to VSS in the device.

Table 75 • **Thermal Diode Parameters**

Parameter	Symbol	Typical	Maximum	Unit
Forward bias current	I_{FW}	See note(1)	1	mA
Diode ideality factor	n	1.008		

1. Typical value is device dependent.

The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

$$I_{FW} = I_S(e^{(qV_D)/(nkT)} - 1)$$

where, I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann constant, and T = absolute temperature (Kelvin).

5.2 AC Characteristics

This section provides the AC specifications for the VSC8502 device.

5.2.1 Reference Clock

The following table lists the AC specifications for the REFCLK reference clock.

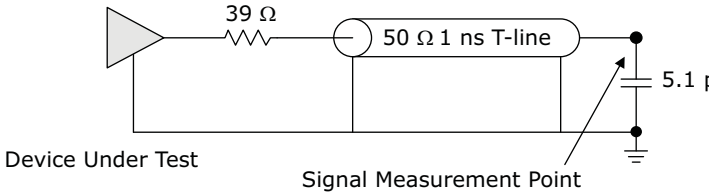
Table 76 • **RefClk**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
REFCLK frequency, REFCLK_SEL= 0	*f*	–100 ppm	125	100 ppm	MHz	
REFCLK frequency, REFCLK_SEL = 1	*f*	–100 ppm	25	100 ppm	MHz	
Rise time and fall time	t_R, t_F			1.5	ns	20% to 80%, 5.1 pF load
Duty cycle		45		55	%	
Phase jitter				4	ps_{RMS}	Bandwidth from 10 kHz to 10 MHz

5.2.2 Recovered Clock

This section provides the AC characteristics for the recovered clock output signals. The following illustration shows the test circuit for the recovered clock output signals.

Figure 20 • **Test Circuit for Recovered Clock Output Signals**



The following table shows the AC specifications for the RCVRDCLK1 and RCVRDCLK2 outputs.

Table 77 • **Recovered Clock AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Recovered clock frequency	*f*		125.00		MHz	
Recovered clock frequency	*f*		31.25		MHz	
Recovered clock frequency	*f*		25.00		MHz	

Table 77 • **Recovered Clock AC Characteristics *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Recovered clock cycle time	t_{RCYC}		8.0		ns	
Recovered clock cycle time	t_{RCYC}		32.0		ns	
Recovered clock cycle time	t_{RCYC}		40.0		ns	
Frequency stability	$f_{STABILITY}$			50	ppm	
Duty cycle	DC	45	50	55	%	
Clock rise time and fall time	t_R, t_F			1.1	ns	20% to 80%
Peak-to-peak jitter, copper media interface, 1000BASE-T	JPP_{CLK_Cu}			400	ps	10k samples. On-chip regulator disabled
Peak-to-peak jitter, copper media interface, 1000BASE-T	JPP_{CLK_Cu}			1020	ps	10k samples. On-chip regulator enabled

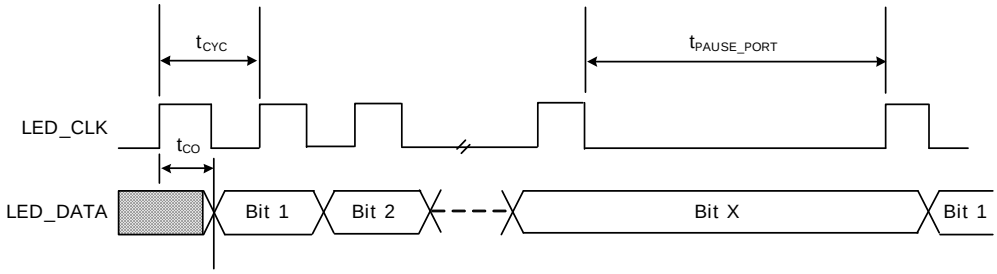
5.2.3 Basic Serial LEDs

This section contains the AC specifications for the basic serial LEDs.

Table 78 • **Basic Serial LEDs AC Characteristics**

Parameter	Symbol	Typical	Unit
LED_CLK cycle time	t_{CYC}	1024	ns
Pause between LED port sequences	t_{PAUSE_PORT}	3072	ns
Pause between LED bit sequences	t_{PAUSE_BIT}	25.541632	ms
LED_CLK to LED_DATA	t_{CO}	1	ns

Figure 21 • **Basic Serial LED Timing**



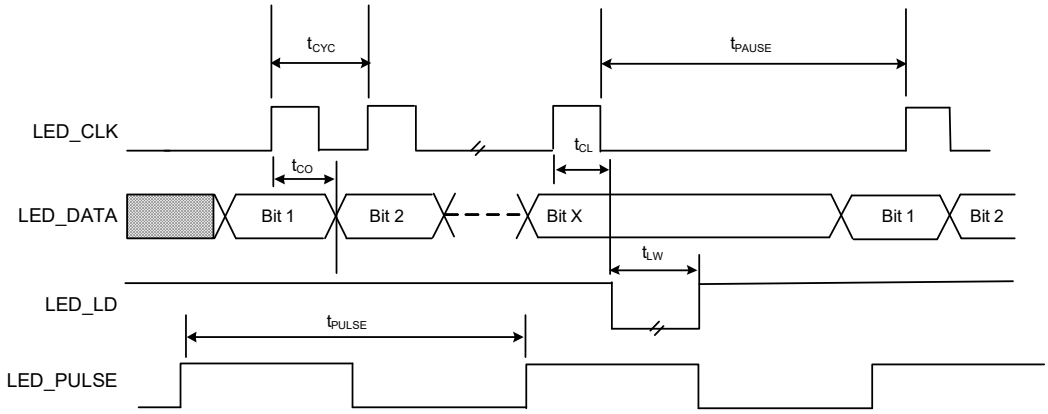
5.2.4 Enhanced Serial LEDs

This section contains the AC specifications for the enhanced serial LEDs. The duty cycle of the LED_PULSE signal is programmable and can be varied between 0.5% and 99.5%.

Table 79 • **Enhanced Serial LEDs AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
LED_CLK cycle time	t_{CYC}		256		ns
Pause between LED_DATA bit sequences	t_{PAUSE}	0.396		24.996	ms
LED_CLK to LED_DATA	t_{CO}		127		ns
LED_CLK to LED_LD	t_{CL}		256		ns
LED_LD pulse width	t_{LW}		128		ns
LED_PULSE cycle time	t_{PULSE}	199		201	µs

Figure 22 • **Enhanced Serial LED Timing**



5.2.5 JTAG Interface

This section provides the AC specifications for the JTAG interface. The specifications meet or exceed the requirements of IEEE 1149.1-2001. The JTAG receive signal requirements are requested at the pin of the device. The JTAG_TRST signal is asynchronous to the clock, and does not have a setup or hold time requirement.

Table 80 • **JTAG Interface AC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TCK frequency	f		10	MHz	
TCK cycle time	t_C	100		ns	
TCK high time	$t_{W(CH)}$	40		ns	
TCK low time	$t_{W(CL)}$	40		ns	
Setup time to TCK rising	t_{SU}	10		ns	
Hold time from TCK rising	t_H	10		ns	
TDO valid after TCK falling	$t_{V(C)}$		28	ns	C_L = 10 pF
TDO hold time from TCK falling	$t_{H(TDO)}$	0		ns	C_L = 0 pF
TDO disable time(1)	t_{DIS}		30	ns	See Figure 23, page 62.

Table 80 • **JTAG Interface AC Characteristics *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TRST time low	$t_{W(TL)}$	30		ns	

1. The pin begins to float when a 300 mV change from the actual V_{OH}/V_{OL} level occurs.

Figure 23 • **JTAG Interface Timing Diagram**

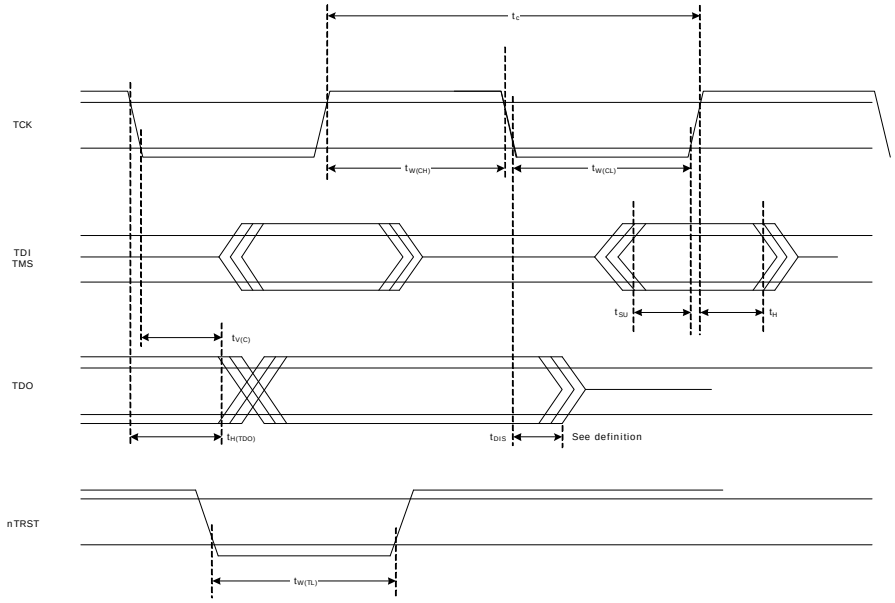
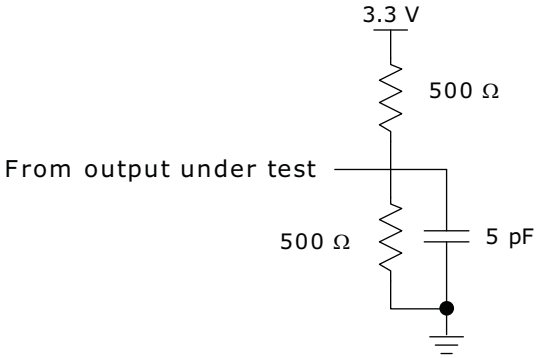


Figure 24 • **Test Circuit for TDO Disable Time**



5.2.6 GMII Transmit

The following table lists the characteristics when using the device in GMII transmit mode. For information about the GMII transmit timing, see Figure 24, page 63.

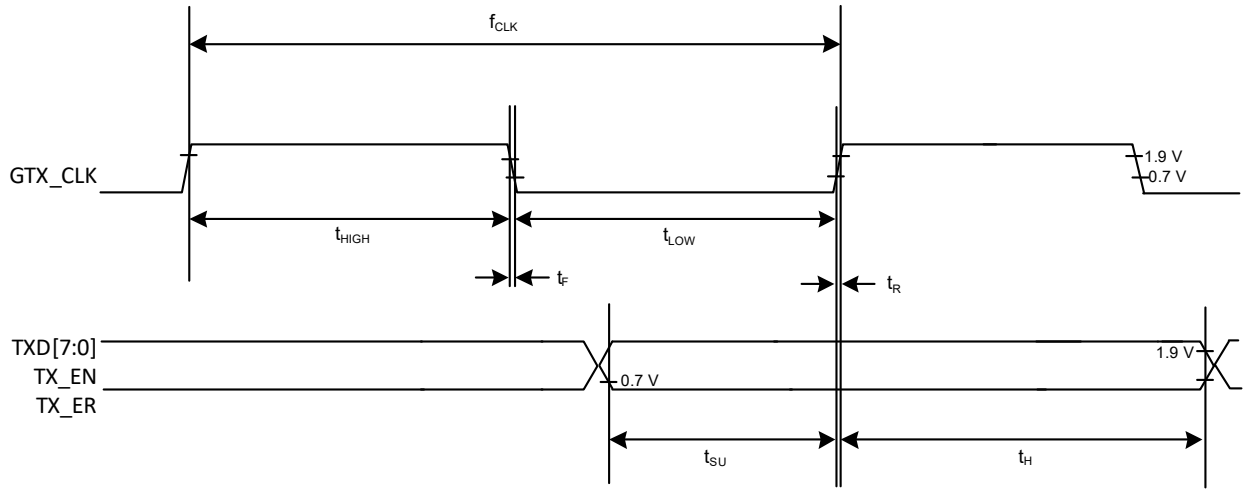
Table 81 • **GMII Transmit AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Clock frequency	f_{CLK}		125		MHz	
Frequency offset tolerance	f_{TOL}	–100		100	ppm	
Pulse width high	t_{HIGH}	2.5			ns	
Pulse width low	t_{LOW}	2.5			ns	

Table 81 • **GMII Transmit *(continued)*AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Setup to GTX_CLK rising	t_{SU}	2.0			ns	
Hold from GTX_CLK rising	t_H	0			ns	
GTX_CLK rise and fall times	t_R and t_F			1.0	ns	Measured from 0.7 V to 1.9 V

Figure 25 • **GMII Transmit Timing**



5.2.7 Uncompensated RGMII

The following table lists the characteristics when using the device in RGMII uncompensated mode. For more information about the RGMII uncompensated timing, see Figure 27, page 74.

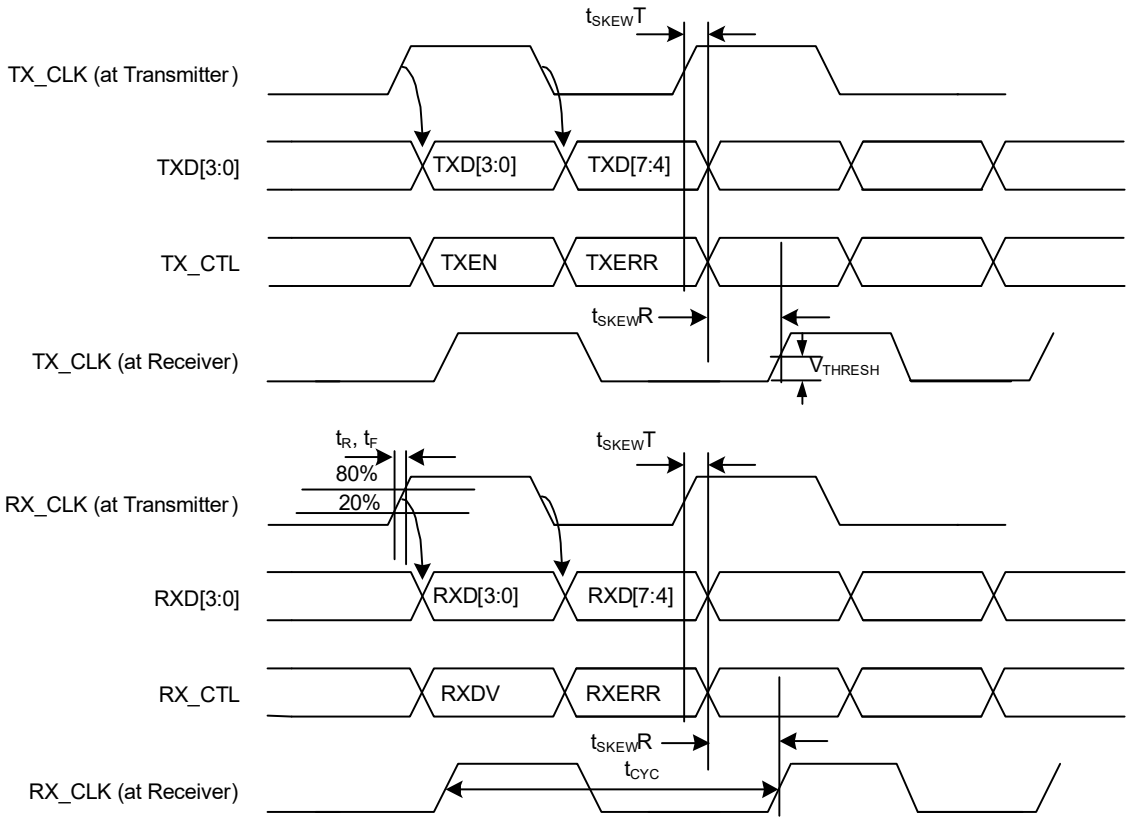
Table 82 • **Uncompensated RGMII AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Clock frequency	f_{CLK}		125 25 2.5		MHz	1000BASE-T operation 100BASE-TX operation 10BASE-T operation
1000BASE-T duty cycle	$t_{DUTY1000}$	40	50	60	%	Register 20E.6:4 = 000
10/100BASE-T duty cycle	$t_{DUTY10/100}$	35 40	38 50	65 60	%	10BASE-T 100BASE-TX
Data to clock output skew (at PHY)	$t_{SKEW}T$	–500		500	ps	
Data to clock output skew (at receiver)	$t_{SKEW}R$	1	1.8	2.6	ns	
TX_CLK switching threshold	V_{THRESH}		1.25 1.65		V	V_{DDMAC} = 2.5 V V_{DDMAC} = 3.3 V

Table 82 • **Uncompensated RGMII AC Characteristics *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Clock/data output rise and fall times	t_R, t_F	0.55 0.52 0.48		0.73 0.78 0.72	ns	1000BASE-T 100BASE-TX 10BASE-T

Figure 26 • **Uncompensated RGMII Timing**



5.2.8 Compensated RGMII

The following table lists the characteristics when using the device in RGMII compensated mode. For more information about the RGMII compensated timing, see Figure 28, page 75.

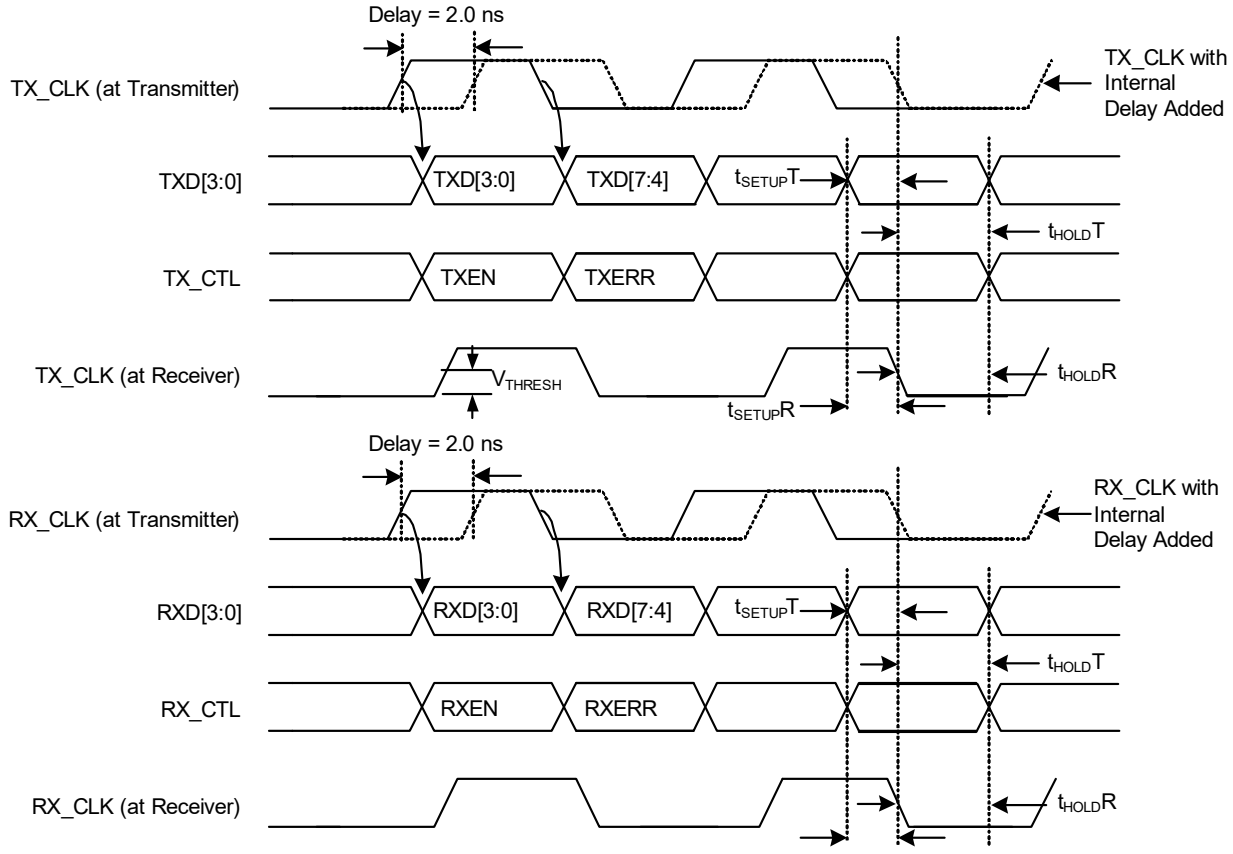
Table 83 • **Compensated RGMII AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Data to clock output setup (at PHY integrated delay)	$t_{SETUP}T$	1.11	2.0	3.1	ns	Min: 20E2.6:4 = 011 Max: 20E2.6:4 = 110
Data to clock output setup (at receiver integrated delay)	$t_{SETUP}R$	1.0	2.0	3.0	ns	System-level routing considerations apply
Data to clock output hold (at transmitter integrated delay)	$t_{HOLD}T$	0.6		3.1	ns	Min: 20E2.6:4 = 110 Max: 20E2.6:4 = 011

Table 83 • **Compensated RGMII AC Characteristics *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Data to clock output hold (at PHY integrated delay)	$t_{HOLD}R$	1.0	2.0	3.0	ns	System-level routing considerations apply
TX_CLK switching threshold	v_{THRESH}		1.25 1.65		V	V_{DDMAC} = 2.5 V V_{DDMAC} = 3.3 V

Figure 27 • **Compensated RGMII Timing**



5.2.9 Serial Management Interface

This section contains the AC specifications for the serial management interface (SMI).

Table 84 • **Serial Management Interface AC Characteristics**

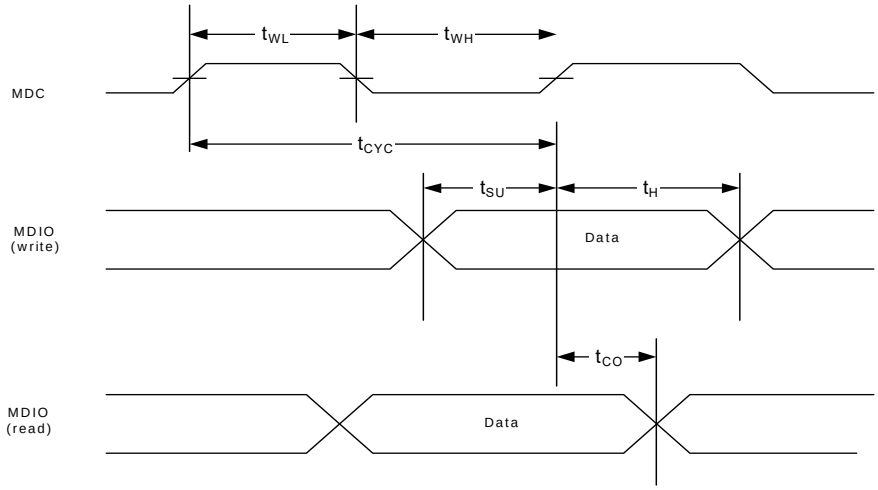
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC frequency(1)	f_{CLK}		2.5	12.5	MHz	
MDC cycle time	t_{CYC}	80	400		ns	
MDC time high	t_{WH}	20	50		ns	
MDC time low	t_{WL}	20	50		ns	
Setup to MDC rising	t_{SU}	10			ns	

Table 84 • **Serial Management Interface AC Characteristics *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Hold from MDC rising	t_H	10			ns	
MDC rise time	t_R			100 t_{CYC} × 10%(1)	ns	MDC = 0: 1 MHz MDC = 1: MHz – f_{CLK} maximum
MDC fall time	t_F			100 t_{CYC} × 10%(1)		
MDC to MDIO valid	t_{CO}		10	300	ns	Time-dependant on the value of the external pull-up resistor on the MDIO pin

1. For f_{CLK} above 1 MHz, the minimum rise time and fall time is in relation to the frequency of the MDC clock period. For example, if f_{CLK} is 2 MHz, the minimum clock rise time and fall time is 50 ns.

Figure 28 • **Serial Management Interface Timing**



5.2.10 Reset Timing

This section contains the AC specifications that apply to device reset functionality. The signal applied to the NRESET input must comply with the specifications listed in the following table.

Table 85 • **Reset Timing AC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit
NRESET assertion time after power supplies and clock stabilize	t_W	2		ms
Recovery time from reset inactive to device fully active	t_{REC}		105	ms
NRESET pulse width	$t_{W(RL)}$	100		ns
Wait time between NRESET de-assert and access of the SMI interface	t_{WAIT}	105		ms

5.2.11 PHY Latency Specifications

The following table shows the PHY latency, measured between the media interface and RGMII MAC interface pins.

Table 86 • **PHY Latency in RGMII Mode**

Mode	Transmit (egress)			Receive (ingress)			
	Minimum	Typical	Maximum	Minimum	Typical	Maximum	Unit
1000BASE-T	92 – 8	92	92 + 8	247 – 4	247	247 + 4	ns
100BASE-TX	354 – 20	354	354 + 20	351 – 24	351	351 + 24	ns
10BASE-T	3828 – 16	3828	3828 + 16	2560 – 290	2560	2560 + 290	ns

The following table shows the PHY latency, measured between the media interface and GMII/MII MAC interface pins.

Table 87 • **PHY Latency in GMII and MII Modes**

Mode	Transmit (egress)			Receive (ingress)			
	Minimum	Typical	Maximum	Minimum	Typical	Maximum	Unit
1000BASE-T	70 – 4	70	70 + 4	240 – 4	240	240 + 4	ns
100BASE-TX	111 – 20	111	111 + 20	360 – 24	360	360 + 24	ns
10BASE-T	1452 – 16	1452	1452 + 16	2495 – 115	2495	2495 + 115	ns

5.3 Operating Conditions

The following table shows the recommended operating conditions for the VSC8502 device.

Table 88 • **Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for core supply	V_{DD1}	0.95	1.00	1.05	V
Power supply voltage for analog circuits	V_{DD1A}	0.95	1.00	1.05	V
Power supply voltage for regulator	V_{DDREG_33}	3.135	3.30	3.465	V
2.5 V power supply voltage for analog circuits	V_{DD25A}	2.38	2.50	2.62	V
2.5 V power supply voltage for VDDMAC0, VDDMAC1, VDDIO, and VDDMDIO	V_{25}	2.38	2.50	2.62	V
3.3 V power supply voltage for VDDMAC0, VDDMAC1, VDDIO, and VDDMDIO	V_{33}	3.135	3.30	3.465	V
1.2 V power supply voltage for VDDMDIO	V_{DDMDIO}	1.14	1.20	1.26	V
VSC8502 operating temperature(1)	T	0		125	°C
VSC8502-03 operating temperature(1)	T	–40		125	°C

1. Minimum specification is ambient temperature, and the maximum is junction temperature.

5.4 Stress Ratings

This section contains the stress ratings for the VSC8502 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 89 • **Stress Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage for core supply	V_{DD1}	–0.3	1.10	V
Power supply voltage for analog circuits	V_{DD1A}	–0.3	1.10	V
Power supply voltage for analog circuits	V_{DD25A}	–0.3	2.75	V
Power supply voltage for digital I/O	V_{DDMAC0}, V_{DDMAC1}, V_{DDIO}, V_{DDMDIO}	–0.3	3.60	V
Input voltage for digital I/O (3.3 V)			3.60	V
Input voltage for digital I/O (2.5 V)			3.30	V
Storage temperature	T_S	–55	125	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–500	500	V
Electrostatic discharge voltage, human body model, REF_FILT pin	V_{ESD_HBM}	–1500	1500	V
Electrostatic discharge voltage, human body model, all pins except the REF_FILT pin	V_{ESD_HBM}	See note(1)		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Microsemi recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

6 Pin Descriptions

The VSC8502 device has 135 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file so that you can copy it electronically. In Acrobat, double-click the attachment icon.

6.1 Pin Identifications

This section contains the pin descriptions for the VSC8502 device. The following table provides notations for definitions of the various pin types.

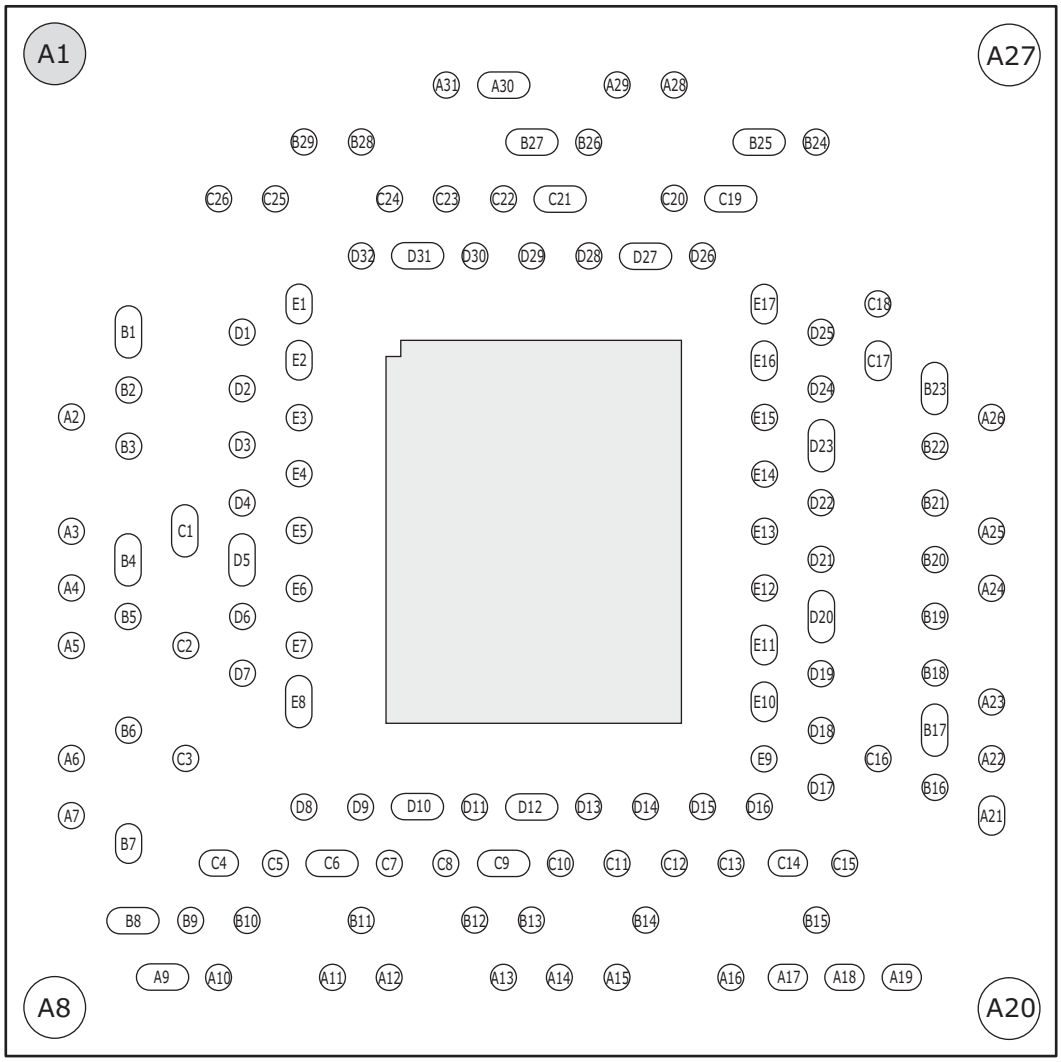
Table 85 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
ADIFF	Analog differential	Analog differential signal pair.
I	Input	Input without on-chip pull-up or pull-down resistor.
I/O	Bidirectional	Bidirectional input or output signal.
NC	No connect	No connect pins must be left floating.
O	Output	Output signal.
OD	Open drain	Open drain output.
PD	Pull-down	On-chip pull-down resistor to VSS.
PU	Pull-up	On-chip pull-up resistor.

6.2 Pin Diagram

The following illustration shows the pin diagram for the VSC8502 device, as seen looking through the package from the top of it. Note that the exposed pad connects to the package ground.

Figure 26 • **Pin Diagram**



6.3 Pins by Function

This section contains the functional pin descriptions for the VSC8502 device.

6.3.1 Copper PHY Media

The following table lists the copper PHY media pins.

Table 86 • **Copper PHY Media Pins**

Name	Pin	Type	I/O Domain	Description
P0_D0N	B26	ADIFF	VDD25A	PHY 0 Tx/Rx channel A negative signal
P0_D0P	B27	ADIFF	VDD25A	PHY 0 Tx/Rx channel A positive signal
P0_D1N	A28	ADIFF	VDD25A	PHY 0 Tx/Rx channel B negative signal
P0_D1P	A29	ADIFF	VDD25A	PHY 0 Tx/Rx channel B positive signal
P0_D2N	C19	ADIFF	VDD25A	PHY 0 Tx/Rx channel C negative signal
P0_D2P	C20	ADIFF	VDD25A	PHY 0 Tx/Rx channel C positive signal
P0_D3N	B24	ADIFF	VDD25A	PHY 0 Tx/Rx channel D negative signal

Table 86 • **Copper PHY Media Pins *(continued)***

Name	Pin	Type	I/O Domain	Description
P0_D3P	B25	ADIFF	VDD25A	PHY 0 Tx/Rx channel D positive signal
P1_D0N	C25	ADIFF	VDD25A	PHY 1 Tx/Rx channel A negative signal
P1_D0P	C26	ADIFF	VDD25A	PHY 1 Tx/Rx channel A positive signal
P1_D1N	B28	ADIFF	VDD25A	PHY 1 Tx/Rx channel B negative signal
P1_D1P	B29	ADIFF	VDD25A	PHY 1 Tx/Rx channel B positive signal
P1_D2N	C23	ADIFF	VDD25A	PHY 1 Tx/Rx channel C negative signal
P1_D2P	C24	ADIFF	VDD25A	PHY 1 Tx/Rx channel C positive signal
P1_D3N	A30	ADIFF	VDD25A	PHY 1 Tx/Rx channel D negative signal
P1_D3P	A31	ADIFF	VDD25A	PHY 1 Tx/Rx channel D positive signal

6.3.2 JTAG

The following table lists the JTAG test pins.

Table 87 • **JTAG Pins**

Name	Pin	Type	I/O Domain	Description
JTAG_CLK	B4	I, PU	VDDIO	JTAG clock
JTAG_DI	A3	I, PU	VDDIO	JTAG test serial data input
JTAG_DO	C1	O	VDDIO	JTAG test serial data output
JTAG_TMS	E5	I, PU	VDDIO	JTAG test mode select
JTAG_TRST	D4	I, PU	VDDIO	JTAG reset **Important** When JTAG is not in use, this pin must be tied to ground with a pull-down resistor

6.3.3 Miscellaneous

The following table lists the miscellaneous pins.

Table 88 • **Miscellaneous Pins**

Name	Pin	Type	Description
LED[0:3]_PHY[0:1]	E13, E6, B21, C2, A25, A5, B20, B5	O	LED direct-drive outputs. All LEDs pins are active-low. A serial LED stream can also be implemented.
NC_[1:4]	A1, A8, A20, A27	NC	No connect.
REF_FILT	C21	A	Reference filter connects to an external 1 µF capacitor to analog ground.
REF_REXT	C22	A	Reference external connects to an external 2 kΩ (1%) resistor to analog ground.
THERMDA	B2	A	Thermal diode anode.
THERMDC_VSS	D3	A	Thermal diode cathode connected to device ground. Temperature sensor must be chosen accordingly.

6.3.4 PHY Configuration

The following table lists the PHY configuration pins.

Table 89 • **PHY Configuration Pins**

Name	Pin	Type	I/O Domain	Description
CLK_SQUELCH_IN	A2	I, PD	VDDIO	Input control to squelch recovered clock.
COMA_MODE	B22	I/O, PU	VDDIO	When this pin is asserted high, all PHYs are held in a powered down state. When de-asserted low, all PHYs are powered up and resume normal operation. This signal is also used to synchronize the operation of multiple chips on the same PCB to provide visual synchronization for LEDs driven by separate chips.(1)
FASTLINK_FAIL	A4	O	VDDIO	Fast link failure indication signal.
NRESET	E14	I, PD	VDDIO	Device reset. Active low input that powers down the device and sets all register bits to their default state.
RCVRDCLK1/PHYADD1	A26	I/O, PD	VDDIO	Clock output, can be enabled or disabled. Output a clock based on the selected active media with programmable frequency. This pin is not active when NRESET is asserted. When disabled, the pin is held low. Also functions as device SMI address bit 1 that is latched when NRESET is deasserted.(2)
RCVRDCLK2/PHYADD2	B23	I/O, PD	VDDIO	Clock output, can be enabled or disabled. Output a clock based on the selected active media with programmable frequency. This pin is not active when NRESET is asserted. When disabled, the pin is held low. Also functions as device SMI address bit 2 that is latched when NRESET is deasserted.(2)
PHYADD3	D23	I, PD	VDDIO	Device SMI address bit 3.(2)
PHYADD4	C17	I, PD	VDDIO	Device SMI address bit 4.(2)
REFCLK	B3	I	VDDIO	Reference clock.
REFCLK_SEL	E4	I, PU	VDDIO	Reference clock frequency select signal.

1. For more information, see Initialization, page 23. For information about a typical bring-up example, see Configuration, page 23.
2. When pulled high to 3.3 V VDDIO, the pull-up must be composed of a 2.4 kΩ from VDDIO to PHYADD, and 10 kΩ from PHYADD to VSS.

6.3.5 Power Supply and Ground

The following table lists the power supply pins and associated functional pins. All power supply pins must be connected to their respective voltage input, even if certain functions are not used for a specific application. No power supply sequencing is required. However, clock and power must be stable before releasing Reset.

Table 90 • **Power Supply and Ground Pins**

Name	Pin	Description
VDD1	D6, D7, D18, D20	1.0 V digital core power supply
VDD1A	D26, D28, D30, D32	1.0 V analog power requiring additional PCB power supply filtering

Table 90 • **Power Supply and Ground Pins *(continued)***

Name	Pin	Description
VDD25A	D27, D29, D31	2.5 V analog power requiring additional PCB power supply filtering
VDDIO	D5, D21, D22	2.5 V or 3.3 V general I/O power supply
VDDMAC0	C12, E10, E11	2.5 V or 3.3 V RGMII/GMII MAC power supply for PHY0
VDDMAC1	C3, C9, D10	2.5 V or 3.3 V RGMII/GMII MAC power supply for PHY1[1]
VDDMDIO	D13	1.2 V, 2.5 V, or 3.3 V power for SMI pins
VDDREG_33	E2, E16	3.3 V power for regulator
VSS_CASE	Exposed pad, E7	Common device ground

1. This pin shall be connected to the same external supply rail as VDDMAC0. It is a required supply input even if PHY1 is unused on the dual-port device.

6.3.6 Regulator

The following table lists the regulator pins.

Table 91 • **Regulator Pins**

Name	Pin	Type	I/O Domain	Description
ERRIN_10	D24	A	VDDREG_33	Off-chip compensation for regulator
ERRIN_25	B1	A	VDDREG_33	Off-chip compensation for regulator
ERRNEG_10	E15	A	VDDREG_33	Off-chip compensation for regulator
ERRNEG_25	E3	A	VDDREG_33	Off-chip compensation for regulator
ERROUT_10	D25	A	VDDREG_33	Off-chip compensation for regulator
ERROUT_25	D1	A	VDDREG_33	Off-chip compensation for regulator
REG_EN_10	C18	A	VDDREG_33	1.0 V Regulator enable
REG_EN_25	D2	A	VDDREG_33	2.5 V Regulator enable
REG_OUT_10	E17	A	VDDREG_33	1.0 V Regulator output
REG_OUT_25	E1	A	VDDREG_33	2.5 V Regulator output

6.3.7 RGMII/GMII/MII Interface

The following table lists the RGMII/GMII/MII interface pins.

Table 92 • **RGMII/GMII/MII Interface Pins**

Name	Pin	Type	I/O Domain	Description
COL_0	E9	O	VDDMAC0	GMII/MII collision output for PHY0
CRS_0	C15	O	VDDMAC0	GMII/MII carrier sense output for PHY0
GTX_CLK_0/TXC_0	B16	I, PD	VDDMAC0	GMII/RGMII transmit clock input for PHY0
RX_CLK_0	D16	O	VDDMAC0	GMII/MII receive clock output for PHY0
RX_DV_0/RX_CTL_0	D15	O	VDDMAC0	GMII/MII receive data valid output/RGMII receive control output for PHY0
RX_ER_0	C14	O	VDDMAC0	GMII/MII receive data error output for PHY0

Table 92 • **RGMII/GMII/MII Interface Pins *(continued)***

Name	Pin	Type	I/O Domain	Description
RXD[0:3]_0	A19, B15, A18, D14	O	VDDMAC0	RGMII/GMII/MII data output for PHY0
RXD[4:7]_0	C13, A17, A16, B14	O	VDDMAC0	GMII data output for PHY0
TX_CLK_0	D17	O	VDDMAC0	MII transmit clock output for PHY0
TX_EN_0/TX_CTL_0	C16	I, PD	VDDMAC0	GMII/MII transmit data enable input/RGMII transmit data control input for PHY0
TX_ER_0	A21	I, PD	VDDMAC0	GMII/MII transmit data error input for PHY0
TXD[0:3]_0	A22, B17, D19, A23	I, PD	VDDMAC0	RGMII/GMII/MII data input for PHY0
TXD[4:7]_0	B18, B19, E12, A24	I, PD	VDDMAC0	GMII data input for PHY0
COL_1	C5	O	VDDMAC1	GMII/MII collision output for PHY1
CRS_1	B11	O	VDDMAC1	GMII/MII carrier sense output for PHY1
GTX_CLK_1/TXC_1	C6	I, PD	VDDMAC1	GMII/RGMII transmit clock input for PHY1
RX_CLK_1	C7	O	VDDMAC1	GMII/MII receive clock output for PHY1
RX_DV_1_CTL_1	B8	O	VDDMAC1	GMII/MII receive data valid output/RGMII receive control output for PHY1
RX_ER_1	B9	O	VDDMAC1	GMII/MII receive data error output for PHY1
RXD[0:3]_1	C4, D9, B7, D8	O	VDDMAC1	RGMII/GMII/MII data output for PHY1
RXD[4:7]_1	A7, A6, E8, B6	O	VDDMAC1	GMII data output for PHY1
TX_CLK_1	A9	O	VDDMAC1	MII transmit clock output for PHY1
TX_EN_1/TX_CTL_1	B10	I, PD	VDDMAC1	GMII/MII transmit data enable input/RGMII transmit data control input for PHY1
TX_ER_1	D11	I, PD	VDDMAC1	GMII/MII transmit data error input for PHY1
TXD[0:3]_1	A10, A11, D12, C8	I, PD	VDDMAC1	RGMII/GMII/MII data input for PHY1
TXD[4:7]_1	A12, B12, B13, A13	I, PD	VDDMAC1	GMII data input for PHY1

6.3.8 Serial Management Interface

The following table lists the serial management interface (SMI) pins.

Table 93 • **SMI Pins**

Name	Pin	Type	I/O Domain	Description
MDC	C11	I	VDDMDIO	Management data clock. A 0 MHz to 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
MDINT_[0:1]	A14, C10	O, OD	VDDMDIO	Management interrupt signal. These pins can be tied together in a wired-OR configuration with only a single pull-up resistor.
MDIO	A15	I/O	VDDMDIO	Management data input/output pin. Serial data is written or read from this pin bidirectionally between the PHY and station manager, synchronously on the positive edge of MDC. One external pull-up resistor is required at the station manager.

7 Package Information

The VSC8502XML package is a lead-free (Pb-free), 135-pin, multi-row quad flat no-lead (QFN) package with an exposed pad, 12 mm × 12 mm body size, 0.65 mm pin pitch, and 0.85 mm maximum height.

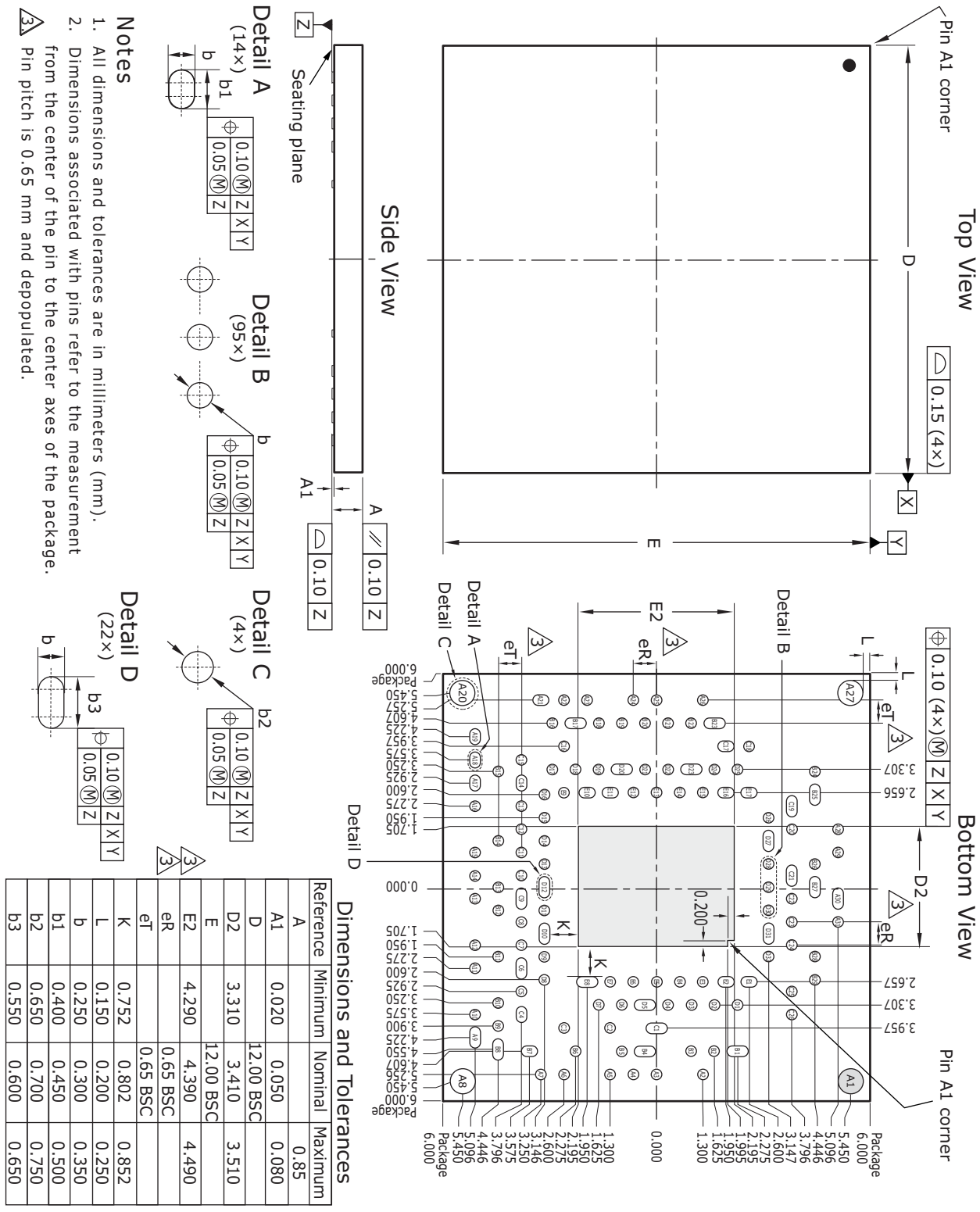
Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8502 device.

7.1 Package Drawing

The following illustration shows the package drawing for the VSC8502 device. The drawing contains the top view, bottom view, side view, dimensions, tolerances, and notes.

Figure 27 • **Package Drawing**



Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A			0.85
A1	0.020	0.050	0.080
D		12.00 BSC	
D2	3.310	3.410	3.510
E		12.00 BSC	
E2	4.290	4.390	4.490
eR		0.65 BSC	
eT		0.65 BSC	
K	0.752	0.802	0.852
L	0.150	0.200	0.250
b	0.250	0.300	0.350
b1	0.400	0.450	0.500
b2	0.650	0.700	0.750
b3	0.550	0.600	0.650

7.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are

modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Table 94 • **Thermal Resistances**

Symbol	°C/W	Parameter
θ_{JCtop}	26.03	Die junction to package case top
θ_{JB}	11.33	Die junction to printed circuit board
θ_{JA}	27.94	Die junction to ambient
θ_{JMA} at 1 m/s	22.29	Die junction to moving air measured at an air speed of 1 m/s
θ_{JMA} at 2 m/s	19.88	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using QFN packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

7.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

8 Design Considerations

This section provides information about design considerations for the VSC8502 device.

8.1 Rx clock duty cycle performance in MII mode

In MII mode, Rx clock duty cycle does not meet the MII standard.

Use the positive edge of RXCLK to capture the data.

8.2 1000BASE-T jitter

1000 BASE-T Jitter is not compliant with IEEE 802.3 Clause 40.6.1.2.5 when using either the 1.0 V or the 2.5 V on-chip voltage regulator.

8.3 10BASE-T signal amplitude

10BASE-T signal amplitude can be lower than the minimum specified in IEEE 802.3 paragraph 14.3.1.2.1 (2.2 V) if using an external 2.5V regulator at low supply voltage. Additionally, associated templates may be marginal or have failures.

This issue is not estimated to present any system level impact. Performance is not impaired with cables up to 130 m with various link partners.

8.4 TX_CLK is on in GMII 1000BASE-T mode

When operating a PHY port in 1000 Mbps mode with GMII MAC interface, the TX_CLK pin for the corresponding port will drive the TX_CLK output. TX_CLK should be ignored because it is not used in 1000 Mbps mode.

8.5 Data is driven on RXD[7:4] in RGMII 1000BASE-T mode

When operating a PHY port in 1000 Mbps mode with RGMII MAC interface, ingress data is driven on the RXD[4:7] output pins of the corresponding port. The RXD[4:7] pins should be ignored in that case because they are not specified for the RGMII interface.

8.6 Rx clock duty cycle performance in RGMII mode at 10 Mbps

In RGMII mode at 10 Mbps operation, Rx clock duty cycle does not meet the RGMII standard.

Use the positive edge of the RX_CLK pin to capture the data.

8.7 Anomalous PCS error indications in Energy Efficient Ethernet mode

When a port is processing traffic with EEE enabled on the link, certain PCS errors (such as false carriers, spurious start-of-stream detection, and idle errors) and EEE wake errors may occur. There is no effect on traffic bit error rate for cable lengths up to 75 meters, and minor packet loss may occur on links longer than 75 meters.

Regardless of cable length, some error indications should not be used while EEE is enabled. These error indications include false carrier interrupts (Interrupt Status, page 37, bit 3), receive error interrupts (Interrupt Status, page 37, bit 0), and EEE wake error interrupts.

Contact Microsemi for a script that needs to be applied during system initialization if EEE will be enabled.

8.8 RGMII interface may not generate even count of preamble nibbles at 10 Mbps

When operating in 10 Mbps mode, the PHY may generate either an even or an odd number of preamble nibbles. Certain third-party RGMII MAC hosts cannot process odd numbers of preamble nibbles and will drop those odd-count frames. The nibble count output from the PHY is random, depending on input copper signal characteristics.

There is no workaround for those MAC hosts that lack odd-or-even alignment capability for RGMII data streams received at their input pins.

8.9 MAC interface RX_CLK synchronization

The receive RX_CLK and its associated data outputs on the MAC interface are synchronized to the local REFCLK input of the device. RX_CLK and the associated RXD pins are not synchronized to the media-recovered clock.

8.10 Link status LED remains on while COMA_MODE pin is asserted high

When the COMA_MODE is asserted high, the link status LED may not deactivate unless the media cable is disconnected from the device.

While using COMA_MODE, link status should be verified using status registers rather than LED indicators.

8.11 LED pulse stretch enable turns off LED pins

Enabling the pulse stretch function for LED pins by setting register 30, bits 5:8 shuts off those LED pins.

Use the default blink function setting of LED0 and LED1 rather than pulse stretching. For more information, see LED Behavior, page 17.

8.12 Long link up times while in forced 100BASE-TX mode

While in forced 100BASE-TX operation and attempting to link up, the device may experience abnormally long link-up times.

This issue can only occur if the unified API is not used with the device. In those circumstances, the workaround for this issue is to clear all speed advertisements in the autonegotiation advertisement registers (register 4, bits 9:5 and register 9, bits 9:8), then toggle the auto-negotiation enable bit of the mode control register (register 0, bit 12) for a port upon detecting its link is down. Any advertisements temporarily cleared can then be restored once register 0, bit 12 is cleared.

9 Ordering Information

The VSC8502 device is offered with two operating temperature ranges. The range for VSC8502 is 0 °C ambient to 125 °C junction. The range for VSC8502-03 is –40 °C ambient to 125 °C junction.

The VSC8502XML package is a lead-free (Pb-free), 135-pin, multi-row plastic quad flat no-lead (QFN) package with an exposed pad, 12 mm × 12 mm body size, 0.65 mm pin pitch, and 0.85 mm maximum height.

Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8502 device.

Table 95 • **Ordering Information**

Part Order Number	Description
VSC8502XML	Lead-free, 135-pin, multi-row plastic QFN package with an exposed pad, 12 mm × 12 mm body size, 0.65 mm pin pitch, and 0.85 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction.
VSC8502XML-03	Lead-free, 135-pin, multi-row plastic QFN package with an exposed pad, 12 mm × 12 mm body size, 0.65 mm pin pitch, and 0.85 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction.

Looking for pricing, stock, or lifecycle information?

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