



**THE DATASHEET OF  
74AVCH16T245DGG,11**





# 74AVCH16T245

16-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 8 — 25 June 2024

Product data sheet

## 1. General description

The 74AVCH16T245 is a 16-bit transceiver with bidirectional level voltage translation and 3-state outputs. The device can be used as two 8-bit transceivers or as a 16-bit transceiver. It has dual supplies ( $V_{CC(A)}$  and  $V_{CC(B)}$ ) for voltage translation and four 8-bit input-output ports ( $nAn$ ,  $nBn$ ) each with its own output enable ( $nOE$ ) and send/receive ( $nDIR$ ) input for direction control.  $V_{CC(A)}$  and  $V_{CC(B)}$  can be independently supplied at any voltage between 0.8 V and 3.6 V making the device suitable for low voltage translation between any of the following voltages: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V. A HIGH on  $nDIR$  selects transmission from  $nAn$  to  $nBn$  while a LOW on  $nDIR$  selects transmission from  $nBn$  to  $nAn$ . A HIGH on  $nOE$  causes the outputs to assume a high-impedance OFF-state

The device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{CC(A)}$  or  $V_{CC(B)}$  are at GND level, both A and B outputs are in the high-impedance OFF-state. The bus-hold circuitry on the powered-up side always stays active.

The 74AVCH16T245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

## 2. Features and benefits

- Wide supply voltage range:  $V_{CC(A)}$ : 0.8 V to 3.6 V and  $V_{CC(B)}$ : 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- Maximum data rates:
  - 380 Mbit/s ( $\geq$  1.8 V to 3.3 V translation)
  - 200 Mbit/s ( $\geq$  1.1 V to 3.3 V translation)
  - 200 Mbit/s ( $\geq$  1.1 V to 2.5 V translation)
  - 200 Mbit/s ( $\geq$  1.1 V to 1.8 V translation)
  - 150 Mbit/s ( $\geq$  1.1 V to 1.5 V translation)
  - 100 Mbit/s ( $\geq$  1.1 V to 1.2 V translation)
- Suspend mode
- Bus hold on data inputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3B exceeds 8000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74AVCH16T245DGG</a>	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	<a href="#">SOT362-1</a>

### 4. Functional diagram

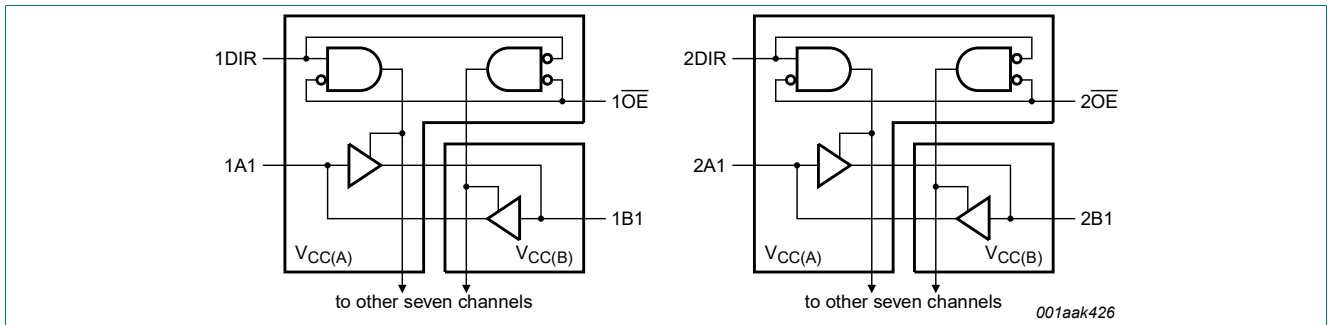


Fig. 1. Logic diagram

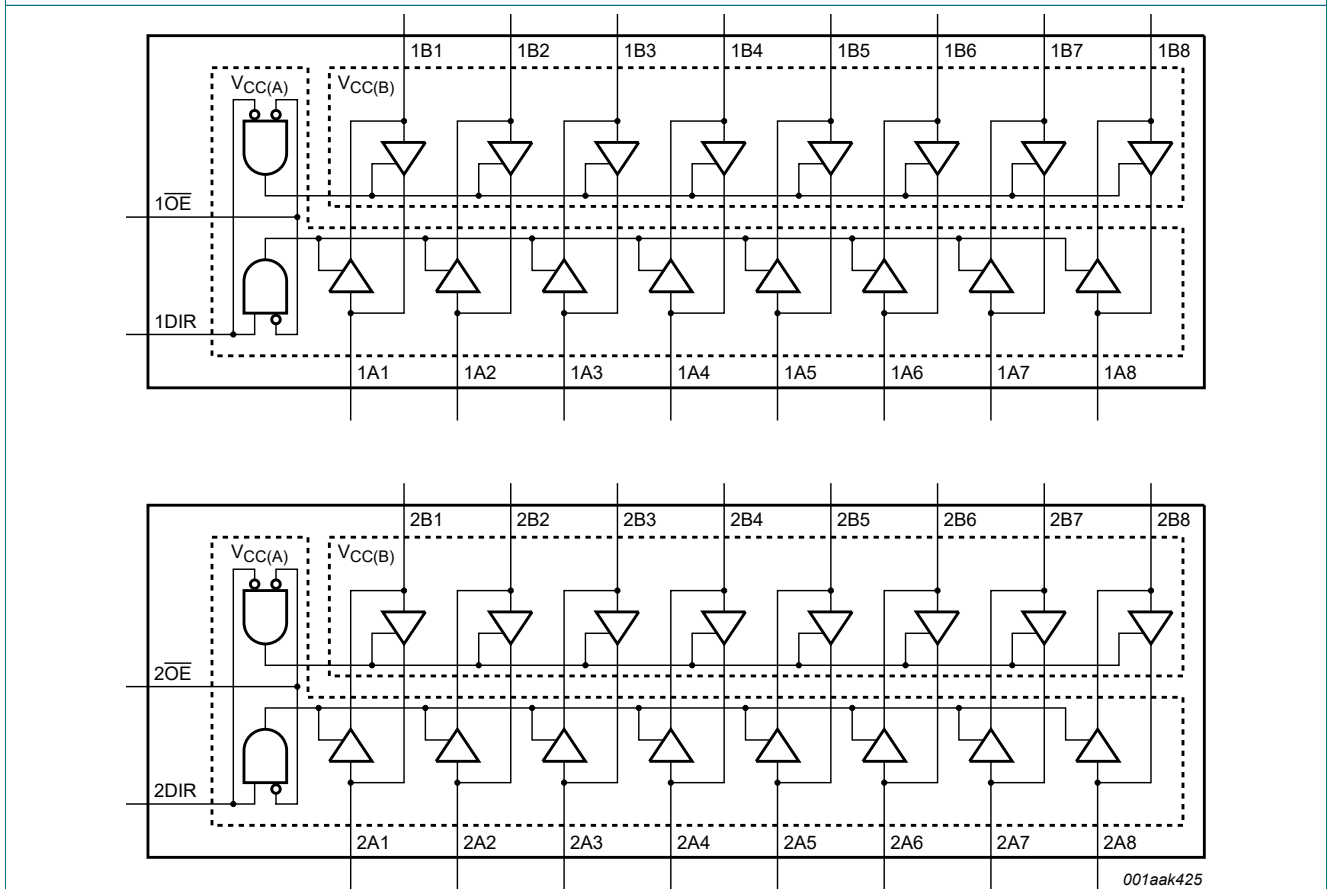
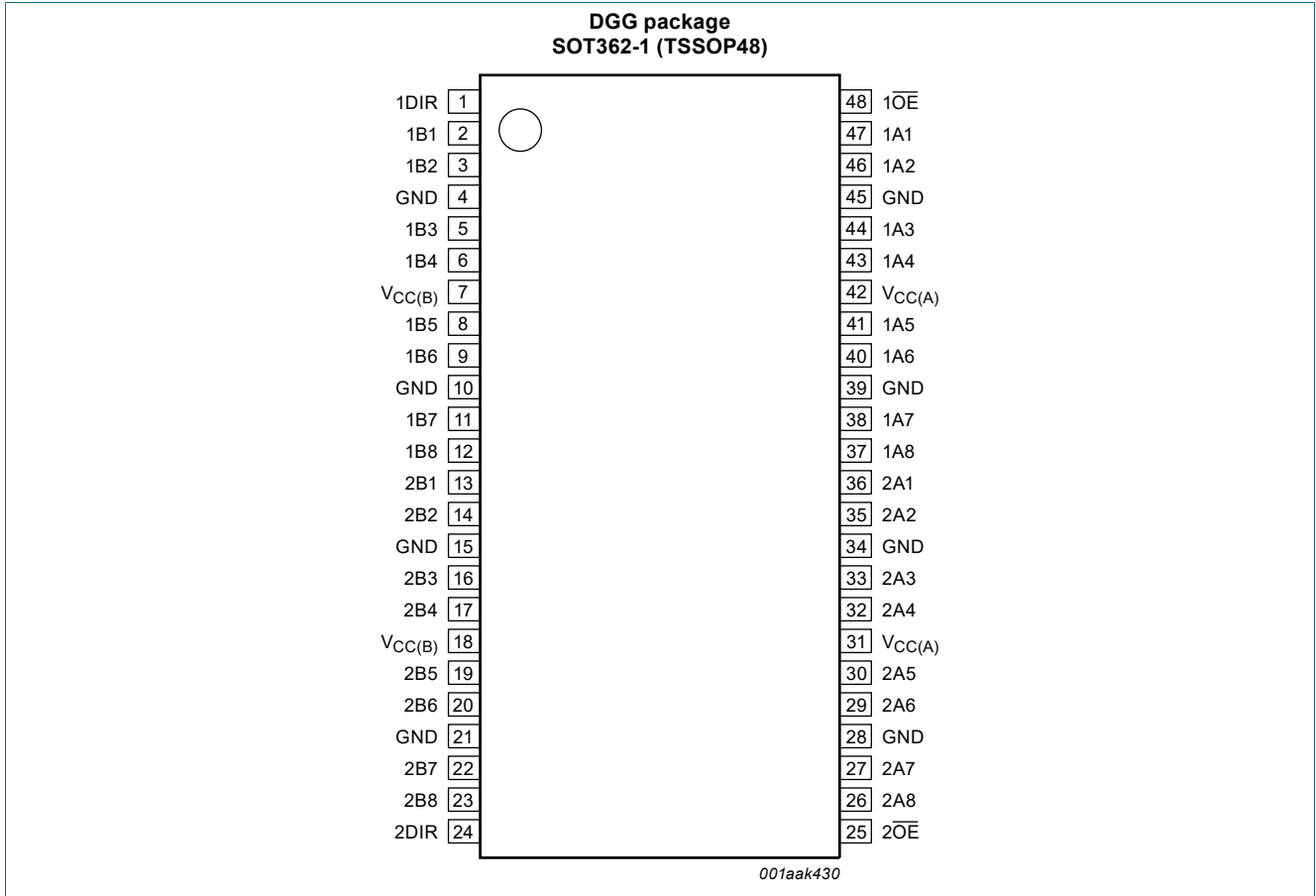


Fig. 2. Logic symbol

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

**Table 2. Pin description**

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control (referenced to V <sub>CC(A)</sub> )
1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7, 1B8	2, 3, 5, 6, 8, 9, 11, 12	data input or output (referenced to V <sub>CC(B)</sub> )
2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7, 2B8	13, 14, 16, 17, 19, 20, 22, 23	data input or output (referenced to V <sub>CC(B)</sub> )
GND [1]	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC(B)</sub>	7, 18	supply voltage B
1OE, 2OE	48, 25	output enable input (active LOW) (referenced to V <sub>CC(A)</sub> )
1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7, 1A8	47, 46, 44, 43, 41, 40, 38, 37	data input or output (referenced to V <sub>CC(A)</sub> )
2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7, 2A8	36, 35, 33, 32, 30, 29, 27, 26	data input or output (referenced to V <sub>CC(A)</sub> )
V <sub>CC(A)</sub>	31, 42	supply voltage A

[1] All GND pins must be connected to ground (0 V).

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Supply voltage	Input		Input/output [1]	
	nOE [2]	nDIR [2]	nAn [2]	nBn [2]
0.8 V to 3.6 V	L	L	nAn = nBn	input
0.8 V to 3.6 V	L	H	input	nBn = nAn
0.8 V to 3.6 V	H	X	Z	Z
GND [1]	X	X	Z	Z

[1] If at least one of  $V_{CC(A)}$  or  $V_{CC(B)}$  is at GND level, the device goes into suspend mode.

[2] The nAn, nDIR and nOE input circuit is referenced to  $V_{CC(A)}$ ; The nBn input circuit is referenced to  $V_{CC(B)}$ .

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$V_O$	output voltage	Active mode [1] [2] [3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode [1]	-0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$ [2]	-	$\pm 50$	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C; [4]	-	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

[3]  $V_{CCO} + 0.5$  V should not exceed 4.6 V.

[4] For SOT362-1 (TSSOP48) packages:  $P_{tot}$  derates linearly with 12.2 mW/K above 109 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	Active mode [1]	0	$V_{CCO}$	V
		Suspend or 3-state mode	0	3.6	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8 \text{ V to } 3.6 \text{ V}$ [2]	-	5	ns/V

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the input port.

## 9. Static characteristics

Table 6. Typical static characteristics at  $T_{amb} = 25 \text{ °C}$

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -1.5 \text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.69	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 1.5 \text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.07	-	V
$I_I$	input leakage current	nDIR, $\overline{nOE}$ input; $V_I = 0 \text{ V}$ or $3.6 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V to } 3.6 \text{ V}$	-	$\pm 0.025$	$\pm 0.25$	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	A or B port; $V_I = 0.42 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 1.2 \text{ V}$ [2]	-	26	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	A or B port; $V_I = 0.78 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 1.2 \text{ V}$ [3]	-	-24	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	A or B port; $V_{CC(A)} = V_{CC(B)} = 1.2 \text{ V}$ [4]	-	27	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	A or B port; $V_{CC(A)} = V_{CC(B)} = 1.2 \text{ V}$ [5]	-	-26	-	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0 \text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = V_{CC(B)} = 3.6 \text{ V}$ [6]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode A port; $V_O = 0 \text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 3.6 \text{ V}$ ; $V_{CC(B)} = 0 \text{ V}$ [6]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode B port; $V_O = 0 \text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 0 \text{ V}$ ; $V_{CC(B)} = 3.6 \text{ V}$ [6]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0 \text{ V to } 3.6 \text{ V}$ ; $V_{CC(A)} = 0 \text{ V}$ ; $V_{CC(B)} = 0.8 \text{ V to } 3.6 \text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0 \text{ V to } 3.6 \text{ V}$ ; $V_{CC(B)} = 0 \text{ V}$ ; $V_{CC(A)} = 0.8 \text{ V to } 3.6 \text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	nDIR, $\overline{nOE}$ input; $V_I = 0 \text{ V}$ or $3.3 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	2.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3 \text{ V}$ or $0 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	4.5	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2] The bus hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_I$  to GND and then raising it to  $V_{IL}$  max.

[3] The bus hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_I$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

[4] An external driver must source at least  $I_{BHLO}$  to switch this node from LOW to HIGH.

[5] An external driver must sink at least  $I_{BHHO}$  to switch this node from HIGH to LOW.

[6] For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

## 16-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	data input					
		V <sub>CCI</sub> = 0.8 V	0.70V <sub>CCI</sub>	-	0.70V <sub>CCI</sub>	-	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	0.65V <sub>CCI</sub>	-	0.65V <sub>CCI</sub>	-	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, n $\overline{\text{OE}}$ input					
		V <sub>CC(A)</sub> = 0.8 V	0.70V <sub>CC(A)</sub>	-	0.70V <sub>CC(A)</sub>	-	V
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	0.65V <sub>CC(A)</sub>	-	0.65V <sub>CC(A)</sub>	-	V
		V <sub>CC(A)</sub> = 2.3 V to 2.7 V	1.6	-	1.6	-	V
V <sub>CC(A)</sub> = 3.0 V to 3.6 V	2	-	2	-	V		
V <sub>IL</sub>	LOW-level input voltage	data input					
		V <sub>CCI</sub> = 0.8 V	-	0.30V <sub>CCI</sub>	-	0.30V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CCI</sub>	-	0.35V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, n $\overline{\text{OE}}$ input					
		V <sub>CC(A)</sub> = 0.8 V	-	0.30V <sub>CC(A)</sub>	-	0.30V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CC(A)</sub>	-	0.35V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V
V <sub>CC(A)</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V		
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -100 $\mu$ A; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	V <sub>CCO</sub> - 0.1	-	V <sub>CCO</sub> - 0.1	-	V
		I <sub>O</sub> = -3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	0.85	-	0.85	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	1.05	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	1.2	-	1.2	-	V
		I <sub>O</sub> = -9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	1.75	-	1.75	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	2.3	-	2.3	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 100 $\mu$ A; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	0.25	-	0.25	V
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	0.35	-	0.35	V
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	0.45	-	0.45	V
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	0.55	-	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	0.7	-	0.7	V
I <sub>I</sub>	input leakage current	nDIR, n $\overline{\text{OE}}$ input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	$\pm 1$	-	$\pm 5$	$\mu$ A

## 16-bit dual supply translating transceiver with configurable voltage translation; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>BHL</sub>	bus hold LOW current	A or B port [3]					
		$V_I = 0.49 \text{ V}; V_{CC(A)} = V_{CC(B)} = 1.4 \text{ V}$	15	-	15	-	μA
		$V_I = 0.58 \text{ V}; V_{CC(A)} = V_{CC(B)} = 1.65 \text{ V}$	25	-	25	-	μA
		$V_I = 0.70 \text{ V}; V_{CC(A)} = V_{CC(B)} = 2.3 \text{ V}$	45	-	45	-	μA
		$V_I = 0.80 \text{ V}; V_{CC(A)} = V_{CC(B)} = 3.0 \text{ V}$	100	-	90	-	μA
I <sub>BHH</sub>	bus hold HIGH current	A or B port [4]					
		$V_I = 0.91 \text{ V}; V_{CC(A)} = V_{CC(B)} = 1.4 \text{ V}$	-15	-	-15	-	μA
		$V_I = 1.07 \text{ V}; V_{CC(A)} = V_{CC(B)} = 1.65 \text{ V}$	-25	-	-25	-	μA
		$V_I = 1.60 \text{ V}; V_{CC(A)} = V_{CC(B)} = 2.3 \text{ V}$	-45	-	-45	-	μA
		$V_I = 2.00 \text{ V}; V_{CC(A)} = V_{CC(B)} = 3.0 \text{ V}$	-100	-	-100	-	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	A or B port [5]					
		$V_{CC(A)} = V_{CC(B)} = 1.6 \text{ V}$	125	-	125	-	μA
		$V_{CC(A)} = V_{CC(B)} = 1.95 \text{ V}$	200	-	200	-	μA
		$V_{CC(A)} = V_{CC(B)} = 2.7 \text{ V}$	300	-	300	-	μA
		$V_{CC(A)} = V_{CC(B)} = 3.6 \text{ V}$	500	-	500	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	A or B port [6]					
		$V_{CC(A)} = V_{CC(B)} = 1.6 \text{ V}$	-125	-	-125	-	μA
		$V_{CC(A)} = V_{CC(B)} = 1.95 \text{ V}$	-200	-	-200	-	μA
		$V_{CC(A)} = V_{CC(B)} = 2.7 \text{ V}$	-300	-	-300	-	μA
		$V_{CC(A)} = V_{CC(B)} = 3.6 \text{ V}$	-500	-	-500	-	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; $V_O = 0 \text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = V_{CC(B)} = 3.6 \text{ V}$ [7]	-	±5	-	±30	μA
		suspend mode A port; $V_O = 0 \text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 3.6 \text{ V}; V_{CC(B)} = 0 \text{ V}$ [7]	-	±5	-	±30	μA
		suspend mode B port; $V_O = 0 \text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 3.6 \text{ V}$ [7]	-	±5	-	±30	μA
I <sub>OFF</sub>	power-off leakage current	A port; $V_I$ or $V_O = 0 \text{ V}$ to $3.6 \text{ V}$ ; $V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 0.8 \text{ V}$ to $3.6 \text{ V}$	-	±5	-	±30	μA
		B port; $V_I$ or $V_O = 0 \text{ V}$ to $3.6 \text{ V}$ ; $V_{CC(B)} = 0 \text{ V}; V_{CC(A)} = 0.8 \text{ V}$ to $3.6 \text{ V}$	-	±5	-	±30	μA

16-bit dual supply translating transceiver with configurable voltage translation; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>CC</sub>	supply current	A port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	30	-	125	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	25	-	100	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	25	-	100	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-5	-	-20	-	μA
		B port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	30	-	125	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	25	-	100	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-5	-	-20	-	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-	25	-	100	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	55	-	185	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	45	-	150	μA

- [1] V<sub>CCO</sub> is the supply voltage associated with the output port.
- [2] V<sub>CCI</sub> is the supply voltage associated with the data input port.
- [3] The bus hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>I</sub> to GND and then raising it to V<sub>IL</sub> max.
- [4] The bus hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>I</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.
- [5] An external driver must source at least I<sub>BHLO</sub> to switch this node from LOW to HIGH.
- [6] An external driver must sink at least I<sub>BHHO</sub> to switch this node from HIGH to LOW.
- [7] For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

Table 8. Typical total supply current (I<sub>CC(A)</sub> + I<sub>CC(B)</sub>)

V <sub>CC(A)</sub>	V <sub>CC(B)</sub>							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

## 10. Dynamic characteristics

**Table 9. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25\text{ °C}$**

Voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$C_{PD}$	power dissipation capacitance	A port: (direction nAn to nBn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nAn to nBn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nBn to nAn); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		A port: (direction nBn to nAn); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction nAn to nBn); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		B port: (direction nAn to nBn); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction nBn to nAn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction nBn to nAn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[2]  $f_i = 10\text{ MHz}$ ;  $V_i = \text{GND to } V_{CC}$ ;  $t_r = t_f = 1\text{ ns}$ ;  $C_L = 0\text{ pF}$ ;  $R_L = \infty\ \Omega$ .

**Table 10. Typical dynamic characteristics at  $V_{CC(A)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		nBn to nAn	14.4	12.4	12.1	11.9	11.8	11.8	ns
$t_{dis}$	disable time	$\overline{nOE}$ to nAn	16.2	16.2	16.2	16.2	16.2	16.2	ns
		$\overline{nOE}$ to nBn	17.6	10.0	9.0	9.1	8.7	9.3	ns
$t_{en}$	enable time	$\overline{nOE}$ to nAn	21.9	21.9	21.9	21.9	21.9	21.9	ns
		$\overline{nOE}$ to nBn	22.2	11.1	9.8	9.4	9.4	9.6	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

**Table 11. Typical dynamic characteristics at  $V_{CC(B)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		nBn to nAn	14.4	7.0	6.2	6.0	5.9	6.0	ns
$t_{dis}$	disable time	$\overline{nOE}$ to nAn	16.2	5.9	4.4	4.2	3.1	3.5	ns
		$\overline{nOE}$ to nBn	17.6	14.2	13.7	13.6	13.3	13.1	ns
$t_{en}$	enable time	$\overline{nOE}$ to nAn	21.9	6.4	4.4	3.5	2.6	2.3	ns
		$\overline{nOE}$ to nBn	22.2	17.7	17.2	17.0	16.8	16.7	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

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Table 12. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.2	0.5	6.9	0.5	6.0	0.5	5.1	0.5	4.9	ns
		nBn to nAn	0.5	9.2	0.5	8.7	0.5	8.5	0.5	8.2	0.5	8.0	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.5	1.5	9.7	1.5	9.5	1.0	8.1	1.0	8.9	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	ns
		n $\overline{\text{OE}}$ to nBn	1.1	14.9	1.1	11.0	1.1	9.6	1.0	8.1	1.0	7.7	ns
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.7	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns
		nBn to nAn	0.5	6.9	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.4	1.5	8.7	1.5	7.5	1.0	6.5	1.0	6.3	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	ns
		n $\overline{\text{OE}}$ to nBn	1.0	13.5	1.0	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.5	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns
		nBn to nAn	0.5	6.0	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.1	1.5	8.4	1.5	7.1	1.0	5.9	1.0	5.7	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns
		n $\overline{\text{OE}}$ to nBn	1.0	13.0	1.0	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.2	0.5	5.6	0.5	4.6	0.5	3.3	0.5	2.8	ns
		nBn to nAn	0.5	5.1	0.5	4.1	0.5	3.7	0.5	3.4	0.5	3.2	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	ns
		n $\overline{\text{OE}}$ to nBn	1.0	10.6	1.0	7.9	1.0	6.6	1.0	6.1	1.0	5.2	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
		n $\overline{\text{OE}}$ to nBn	0.5	12.5	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.0	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns
		nBn to nAn	0.5	4.9	0.5	3.7	0.5	3.3	0.5	2.9	0.5	2.7	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	ns
		n $\overline{\text{OE}}$ to nBn	1.0	10.3	1.0	7.7	1.0	6.5	1.0	5.2	0.5	5.0	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.3	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4.0	ns
		n $\overline{\text{OE}}$ to nBn	0.5	12.4	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4.0	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

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Table 13. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	10.2	0.5	7.6	0.5	6.6	0.5	5.7	0.5	5.4	ns
		nBn to nAn	0.5	10.2	0.5	9.6	0.5	9.4	0.5	9.1	0.5	8.8	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	ns
		n $\overline{\text{OE}}$ to nBn	1.5	13.8	1.5	10.7	1.5	10.5	1.0	9.0	1.5	9.8	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	ns
		n $\overline{\text{OE}}$ to nBn	1.1	16.4	1.1	12.1	1.1	10.6	1.0	9.0	1.0	8.5	ns
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.6	0.5	6.9	0.5	5.8	0.5	4.6	0.5	4.1	ns
		nBn to nAn	0.5	7.6	0.5	6.9	0.5	6.5	0.5	6.2	0.5	6.1	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.6	1.5	9.6	1.5	8.3	1.0	7.2	1.0	7.0	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	ns
		n $\overline{\text{OE}}$ to nBn	1.0	14.9	1.0	11.2	0.5	9.0	0.5	6.5	0.5	5.8	ns
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.4	0.5	6.5	0.5	5.3	0.5	4.1	0.5	3.7	ns
		nBn to nAn	0.5	6.6	0.5	5.8	0.5	5.3	0.5	5.0	0.5	4.9	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.3	1.5	9.3	1.5	7.9	1.0	6.5	1.0	6.3	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	ns
		n $\overline{\text{OE}}$ to nBn	1.0	14.3	1.0	10.2	0.5	8.2	0.5	5.9	0.5	5.0	ns
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.1	0.5	6.2	0.5	5.1	0.5	3.7	0.5	3.1	ns
		nBn to nAn	0.5	5.7	0.5	4.6	0.5	4.1	0.5	3.8	0.5	3.6	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	ns
		n $\overline{\text{OE}}$ to nBn	1.0	11.7	1.0	8.7	1.0	7.3	1.0	6.8	1.0	5.8	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	ns
		n $\overline{\text{OE}}$ to nBn	0.5	13.8	0.5	10.4	0.5	8.1	0.5	5.7	0.5	5.0	ns
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.8	0.5	6.1	0.5	4.9	0.5	3.6	0.5	3.0	ns
		nBn to nAn	0.5	5.4	0.5	4.1	0.5	3.7	0.5	3.2	0.5	3.0	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	ns
		n $\overline{\text{OE}}$ to nBn	1.0	11.4	1.0	8.5	1.0	7.2	1.0	5.8	0.5	5.5	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.8	0.5	4.8	0.5	4.7	0.5	4.6	0.5	4.4	ns
		n $\overline{\text{OE}}$ to nBn	0.5	13.7	0.5	10.3	0.5	8.0	0.5	5.4	0.5	4.4	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

10.1. Waveforms and test circuit

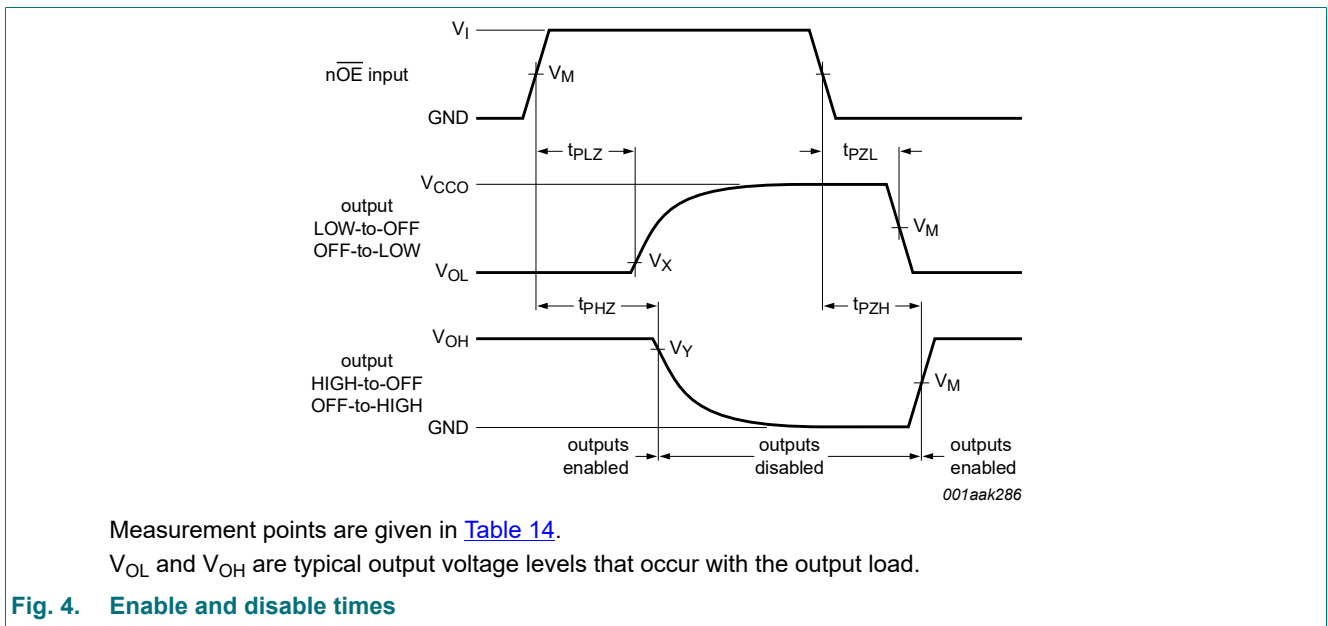
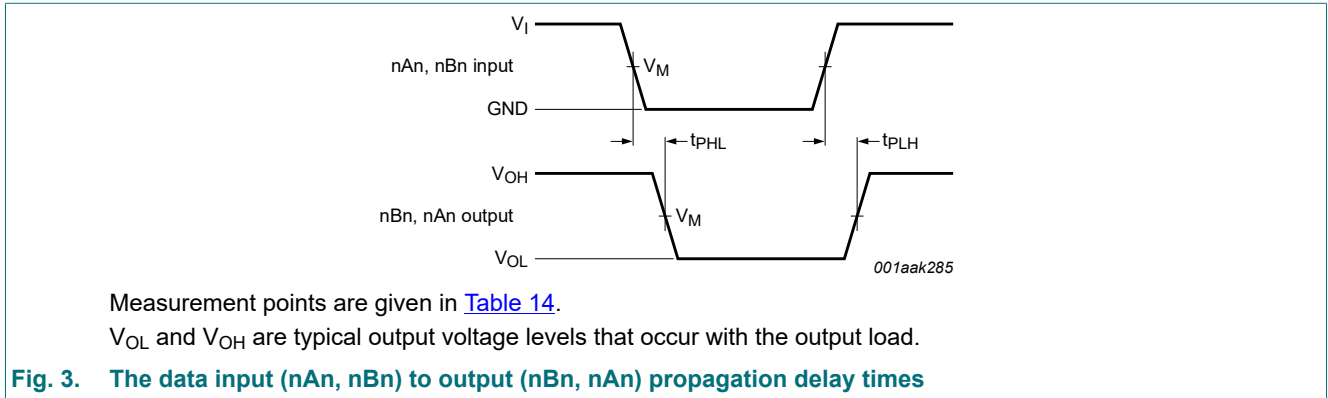
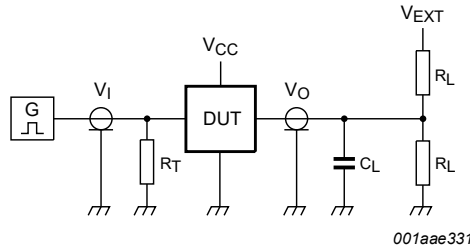
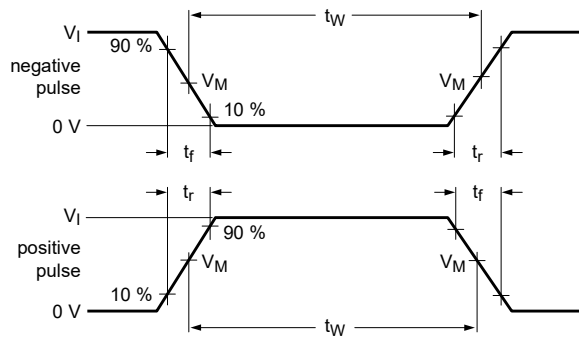


Table 14. Measurement points

Supply voltage	Input [1]	Output [2]		
$V_{CC(A)}, V_{CC(B)}$	$V_M$	$V_M$	$V_X$	$V_Y$
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.  
 [2]  $V_{CCO}$  is the supply voltage associated with the output port.

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Test data is given in [Table 15](#).

Definitions test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance;

$V_{EXT}$  = External voltage for measuring switching times

**Fig. 5. Test circuit for measuring switching times**

**Table 15. Test data**

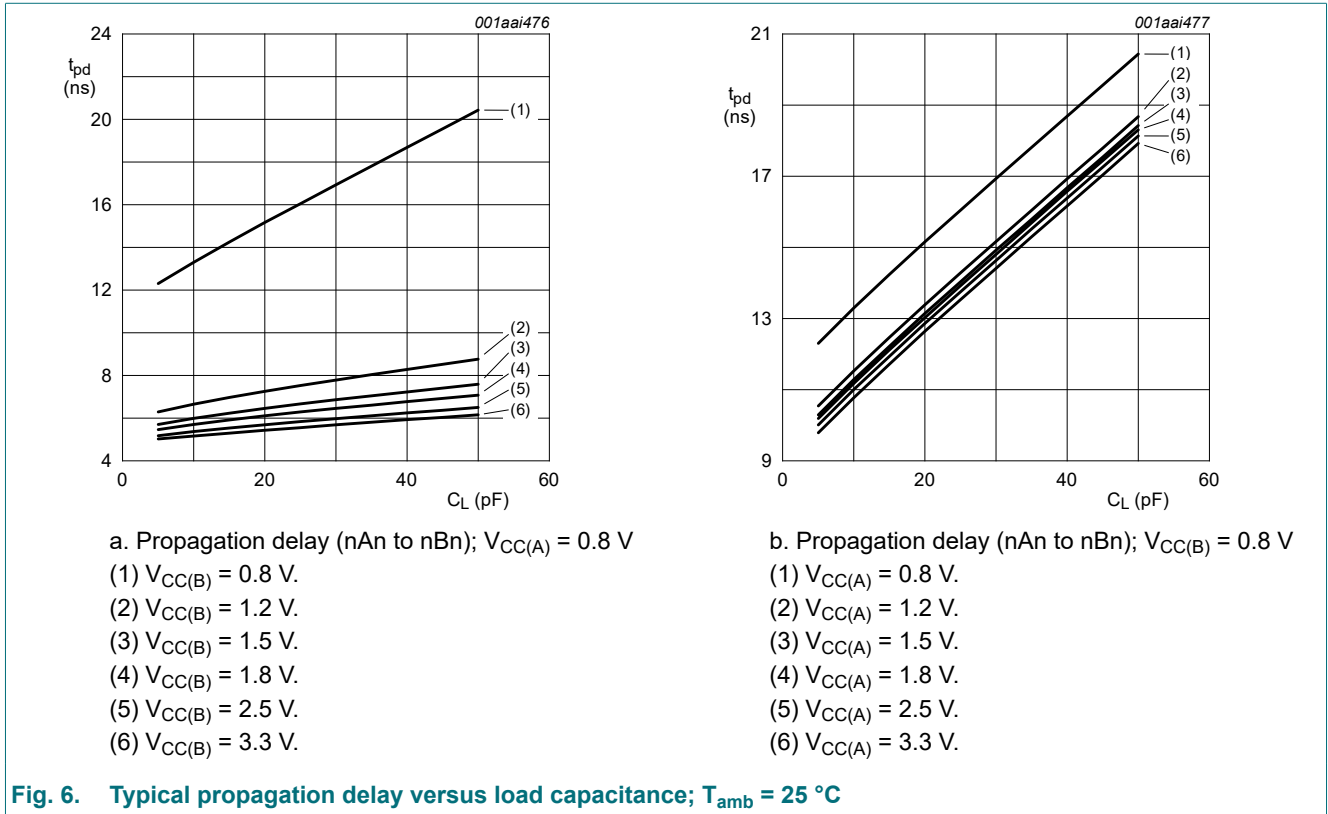
Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC(A)}, V_{CC(B)}$	$V_I$ [1]	$\Delta t/\Delta V$ [2]	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$ [3]
0.8 V to 1.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

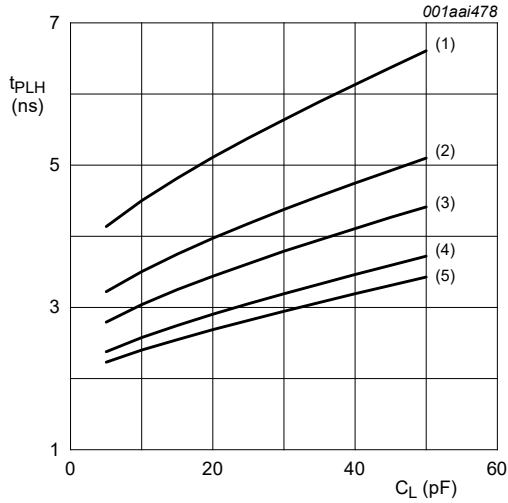
[2]  $dV/dt \geq 1.0$  V/ns

[3]  $V_{CCO}$  is the supply voltage associated with the output port.

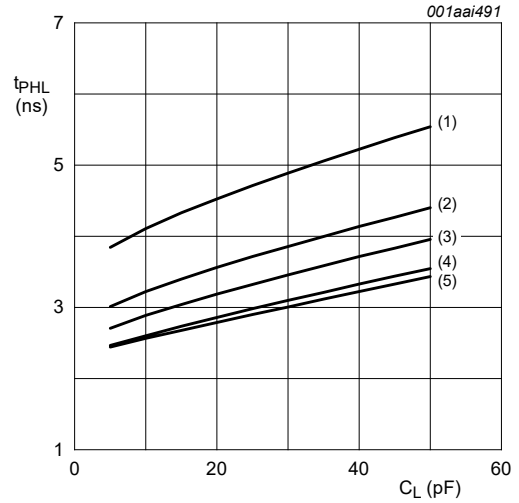
10.2. Typical propagation delay characteristics



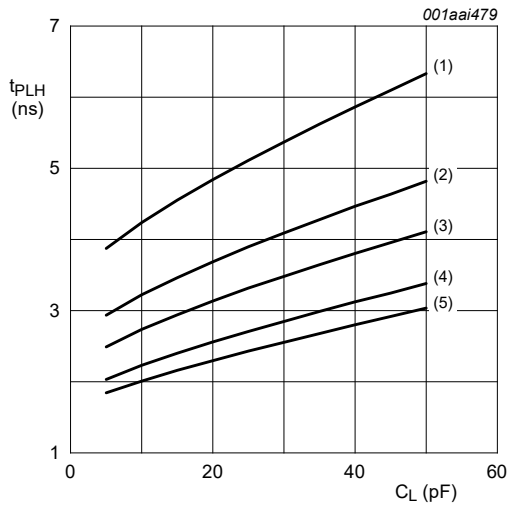
16-bit dual supply translating transceiver with configurable voltage translation; 3-state



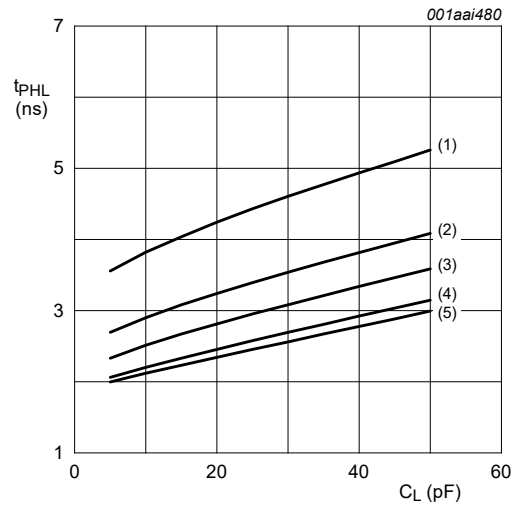
a. LOW to HIGH propagation delay (nAn to nBn);  $V_{CC(A)} = 1.2\text{ V}$



b. HIGH to LOW propagation delay (nAn to nBn);  $V_{CC(A)} = 1.2\text{ V}$



c. LOW to HIGH propagation delay (nAn to nBn);  $V_{CC(A)} = 1.5\text{ V}$

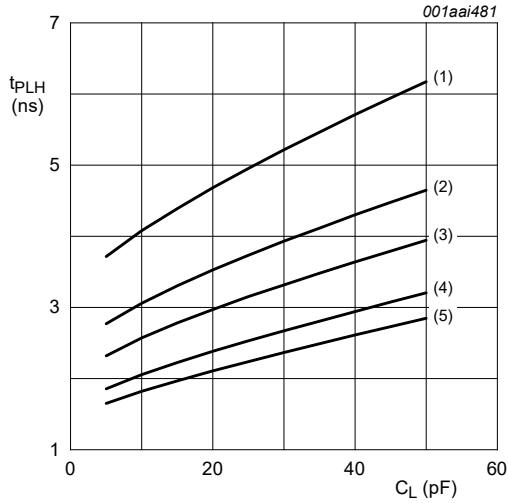


d. HIGH to LOW propagation delay (nAn to nBn);  $V_{CC(A)} = 1.5\text{ V}$

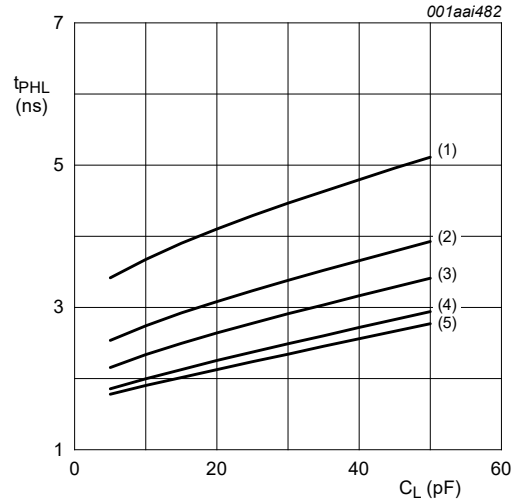
- (1)  $V_{CC(B)} = 1.2\text{ V}$ .
- (2)  $V_{CC(B)} = 1.5\text{ V}$ .
- (3)  $V_{CC(B)} = 1.8\text{ V}$ .
- (4)  $V_{CC(B)} = 2.5\text{ V}$ .
- (5)  $V_{CC(B)} = 3.3\text{ V}$ .

Fig. 7. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^\circ\text{C}$

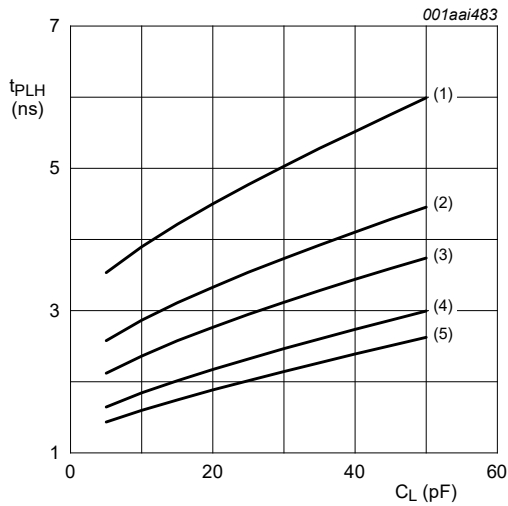
16-bit dual supply translating transceiver with configurable voltage translation; 3-state



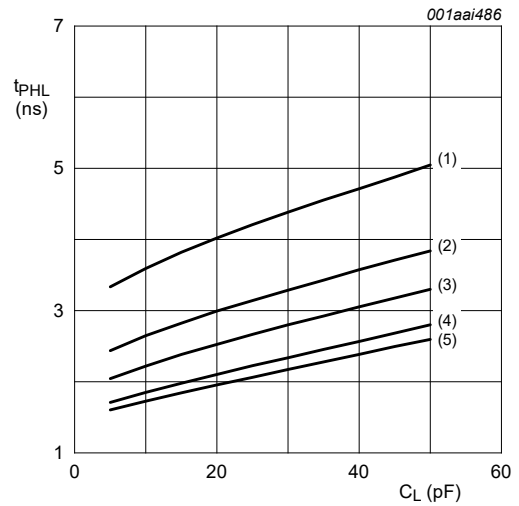
a. LOW to HIGH propagation delay (nAn to nBn);  $V_{CC(A)} = 1.8\text{ V}$



b. HIGH to LOW propagation delay (nAn to nBn);  $V_{CC(A)} = 1.8\text{ V}$



c. LOW to HIGH propagation delay (nAn to nBn);  $V_{CC(A)} = 2.5\text{ V}$

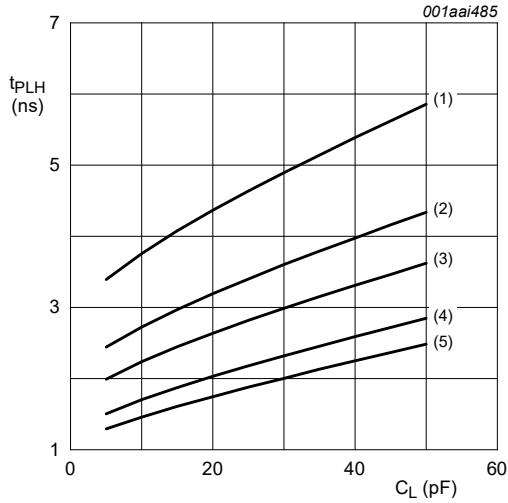


d. HIGH to LOW propagation delay (nAn to nBn);  $V_{CC(A)} = 2.5\text{ V}$

- (1)  $V_{CC(B)} = 1.2\text{ V}$ .
- (2)  $V_{CC(B)} = 1.5\text{ V}$ .
- (3)  $V_{CC(B)} = 1.8\text{ V}$ .
- (4)  $V_{CC(B)} = 2.5\text{ V}$ .
- (5)  $V_{CC(B)} = 3.3\text{ V}$ .

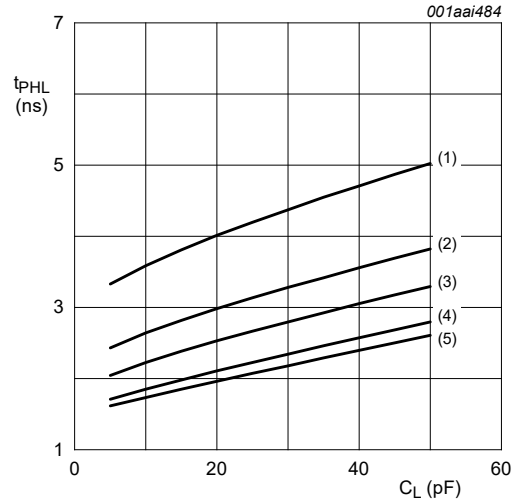
Fig. 8. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ °C}$

16-bit dual supply translating transceiver with configurable voltage translation; 3-state



a. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 3.3\text{ V}$

- (1)  $V_{CC(B)} = 1.2\text{ V}$ .
- (2)  $V_{CC(B)} = 1.5\text{ V}$ .
- (3)  $V_{CC(B)} = 1.8\text{ V}$ .
- (4)  $V_{CC(B)} = 2.5\text{ V}$ .
- (5)  $V_{CC(B)} = 3.3\text{ V}$ .



b. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 3.3\text{ V}$

Fig. 9. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ °C}$

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

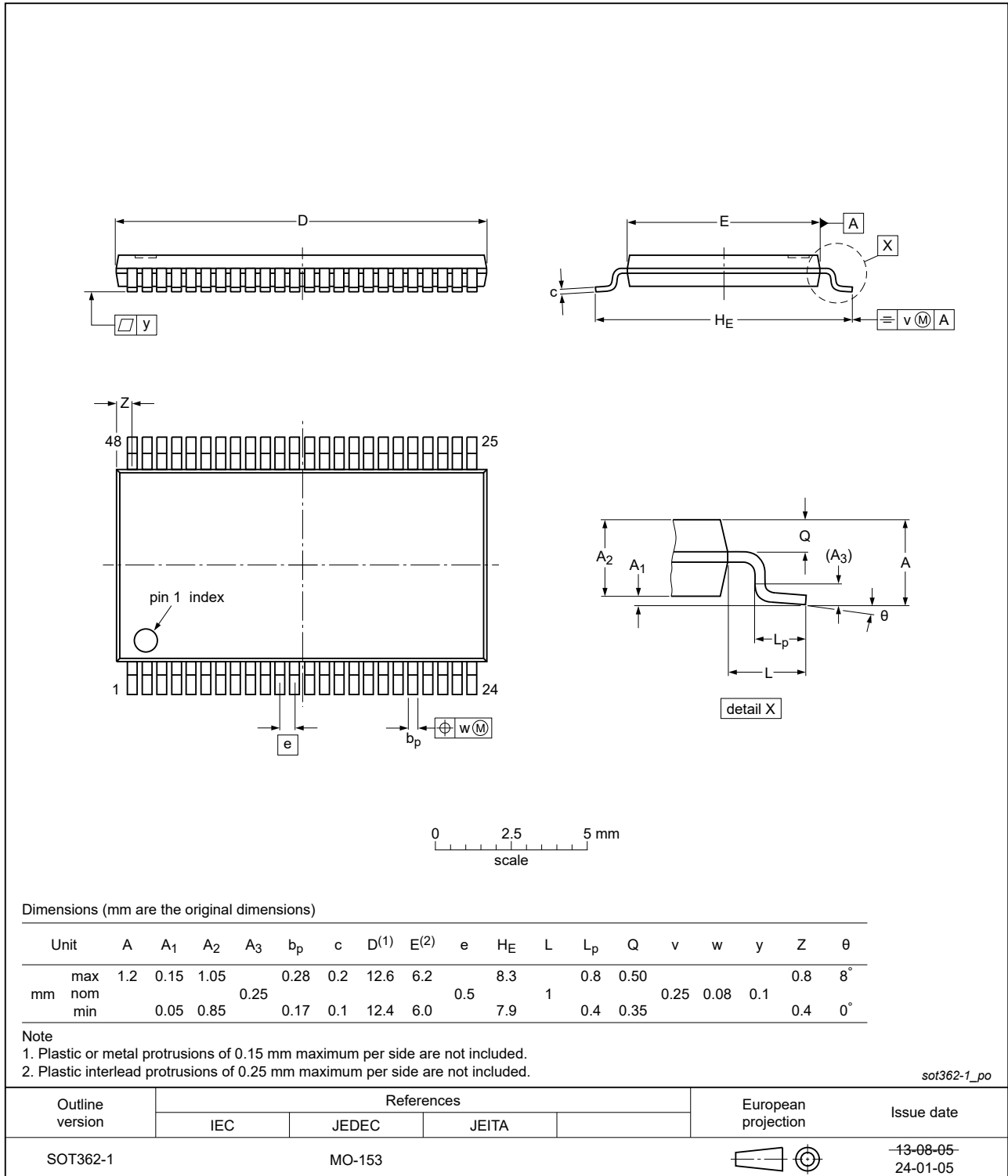


Fig. 10. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 16. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

## 13. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVCH16T245 v.8	20240625	Product data sheet	-	74AVCH16T245 v.7
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74AVCH16T245 v.7	20240426	Product data sheet	-	74AVCH16T245 v.6
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Fig. 10</a>: Updated package outline drawing SOT362-1 (TSSOP48).</li> </ul>			
74AVCH16T245 v.6	20190403	Product data sheet	-	74AVCH16T245 v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74AVCH16T245DGV (SOT480-1), 74AVCH16T245EV (SOT702-1) and 74AVCH16T245BX (SOT1134-2) removed.</li> <li>Package outline drawing <a href="#">SOT362-1</a> (TSSOP48) updated.</li> </ul>			
74AVCH16T245 v.5	20120301	Product data sheet	-	74AVCH16T245 v.4
Modifications:	<ul style="list-style-type: none"> <li>For type number 74AVCH16T245BX the SOT code has changed to SOT1134-2.</li> </ul>			
74AVCH16T245 v.4	20111207	Product data sheet	-	74AVCH16T245 v.3
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74AVCH16T245 v.3	20110616	Product data sheet	-	74AVCH16T245 v.2
74AVCH16T245 v.2	20100329	Product data sheet	-	74AVCH16T245 v.1
74AVCH16T245 v.1	20091014	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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