



**THE DATASHEET OF
74ABT244PW,112**



74ABT244

Octal buffer/line driver; 3-state

Rev. 5 — 24 June 2024

Product data sheet

1. General description

The 74ABT244 is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables ($1\overline{OE}$ and $2\overline{OE}$), each controlling four of the 3-state outputs. A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 4.5 to 5.5 V
- Octal bus interface
- 3-State buffers
- BiCMOS high speed and output drive
- Output capability: +64 mA/−32 mA
- Direct interface with TTL levels
- Power-up 3-State
- Live insertion capability
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from −40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT244D	−40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT244PW	−40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

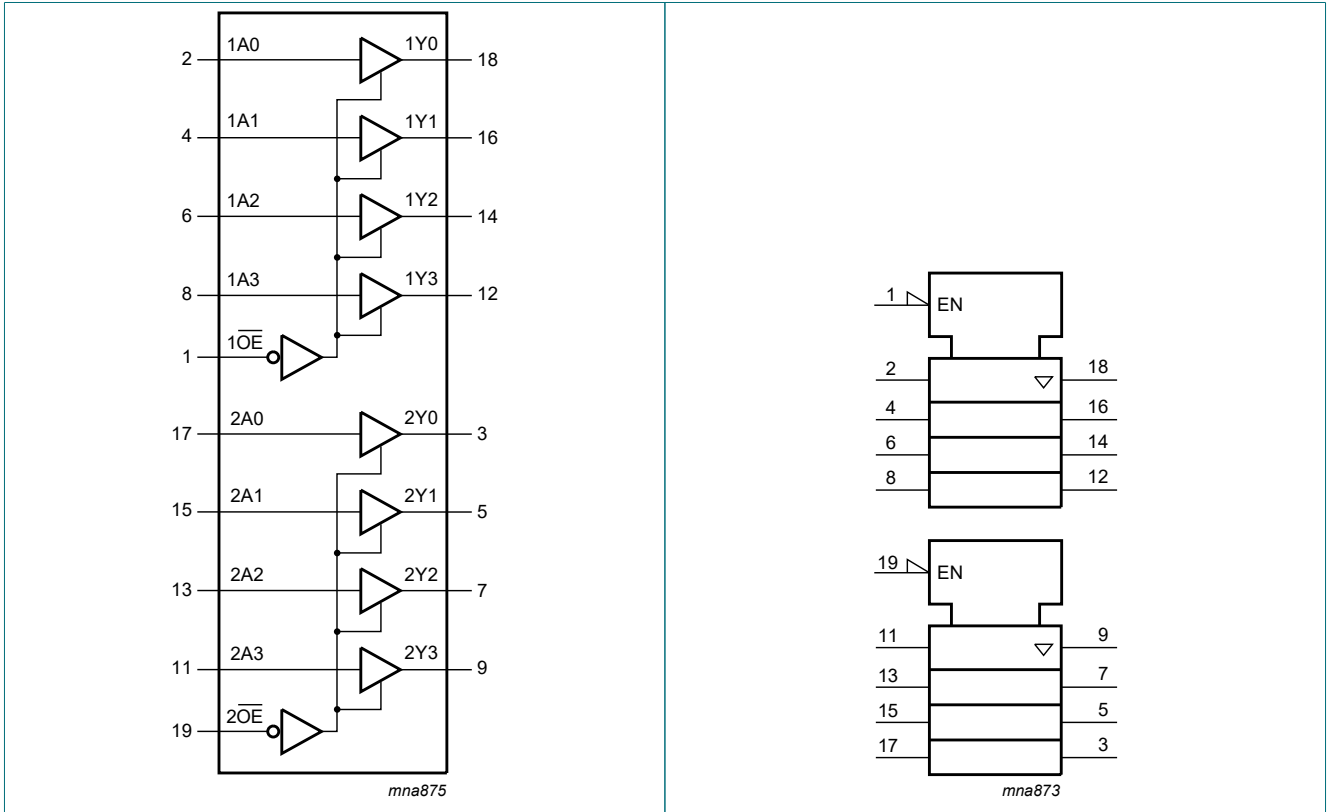


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

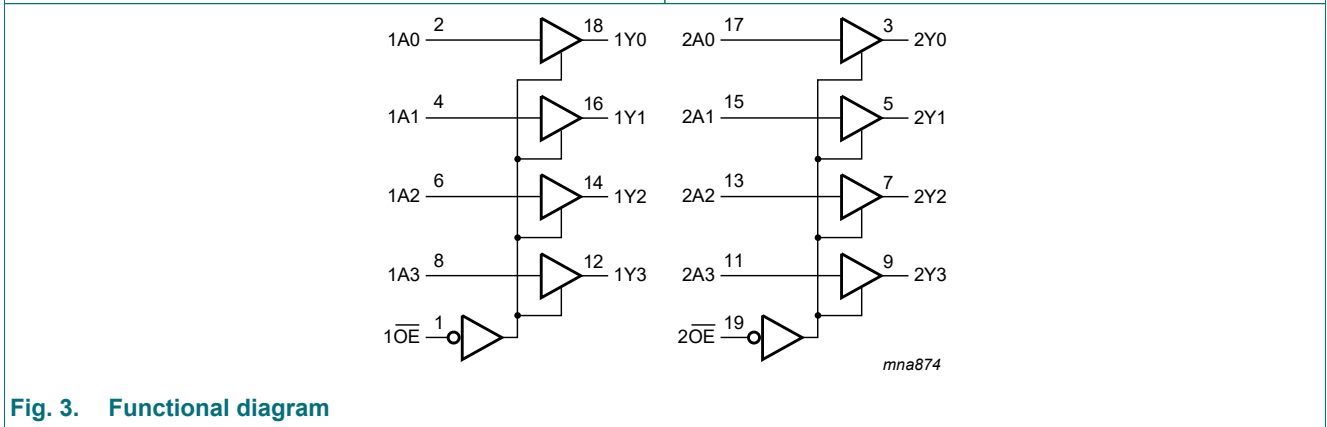
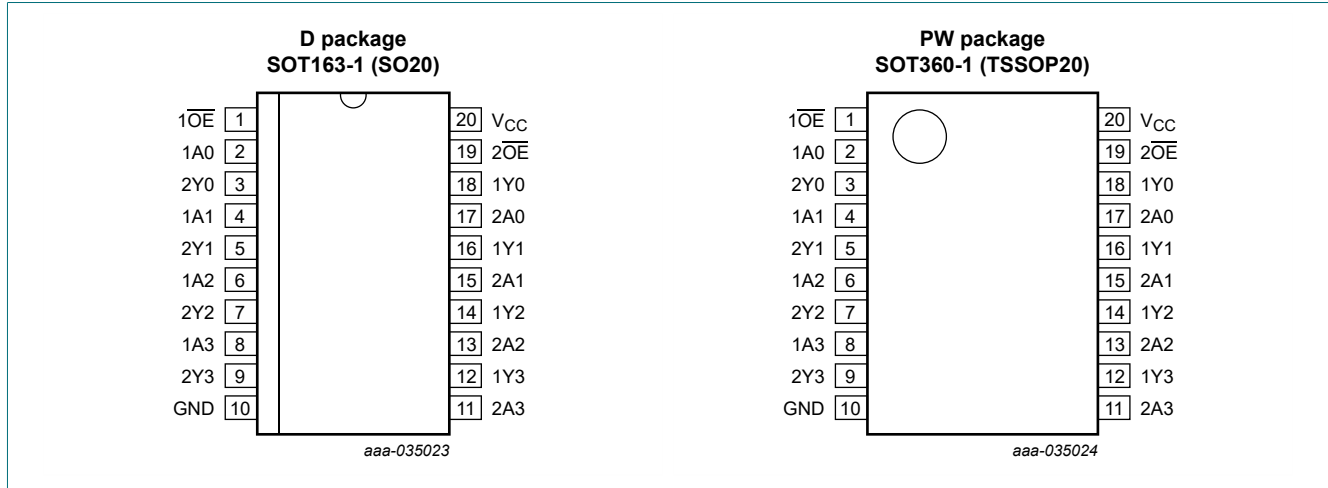


Fig. 3. Functional diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
1OE, 2OE	1, 19	output enable input (active LOW)
GND	10	ground (0 V)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
T_j	junction temperature	[2]	-	150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-45 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5$ V; $I_{IK} = -18$ mA	-1.2	-0.9	-	-1.2	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 4.5$ V; $V_I = V_{IL}$ or V_{IH}						
		$I_{OH} = -3$ mA	2.5	2.9	-	2.5	-	V
		$I_{OH} = -32$ mA	2.0	2.4	-	2.0	-	V
		$V_{CC} = 5.0$ V; $V_I = V_{IL}$ or V_{IH}						
		$I_{OH} = -3$ mA	3.0	3.4	-	3.0	-	V

Symbol	Parameter	Conditions	25 °C			-45 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; V _I = V _{IL} or V _{IH} ; I _{OL} = 64 mA	-	0.42	0.55	-	0.55	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _O or V _I ≤ 4.5 V	-	±5.0	±100	-	±100	µA
I _{O(pu/pd)}	power-up/ power-down output current	V _{CC} = 2.0 V; V _O = 0.5 V; V _I = GND or V _{CC} ; n \overline{OE} = don't care [1]	-	±5.0	±50	-	±50	µA
I _{OZ}	OFF-state output current	V _{CC} = 5.5 V; V _I = V _{IL} or V _{IH}						
		output HIGH-state at V _O = 2.7 V	-	5.0	50	-	50	µA
		output LOW-state at V _O = 0.5 V	-	-5.0	-50	-	-50	µA
I _{CEX}	output high leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}	-	5.0	50	-	50	µA
I _O	output current	V _{CC} = 5.5 V; V _O = 2.5 V [2]	-40	-100	-180	-40	-180	mA
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = GND or V _{CC}						
		outputs HIGH-state	-	50	250	-	250	µA
		outputs LOW-state	-	24	30	-	30	mA
		outputs disabled	-	50	250	-	250	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 5.5 V						
		outputs enabled; one data input at 3.4 V and other inputs at V _{CC} or GND [3]	-	0.5	1.5	-	1.5	mA
		outputs disabled; one data input at 3.4 V and other inputs at V _{CC} or GND [3]	-	50	250	-	250	µA
		outputs disabled; one enable input at 3.4 V and other inputs at V _{CC} or GND [3]	-	0.5	1.5	-	1.5	mA
C _I	input capacitance	V _I = 0 V or V _{CC}	-	4	-	-	-	pF
C _O	output capacitance	outputs disabled; V _O = 0 V or V _{CC}	-	7	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms.

From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 % a transition time of up to 100 µs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

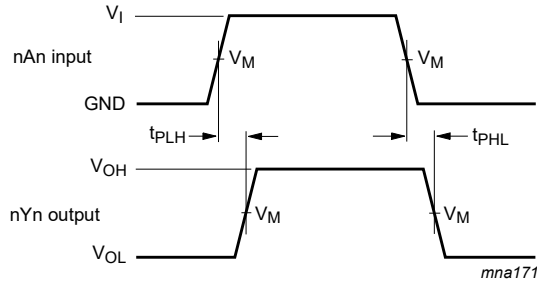
10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 6](#).

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			-40 °C to 85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Fig. 4	1.0	2.6	4.1	1.0	4.6	ns
t _{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Fig. 4	1.0	2.9	4.2	1.0	4.6	ns
t _{PZH}	OFF-state to HIGH propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 5	1.1	3.1	4.6	1.1	5.1	ns
t _{PZL}	OFF-state to LOW propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 5	2.1	4.1	5.6	2.1	6.1	ns
t _{PHZ}	HIGH to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 5	2.1	4.1	5.6	2.1	6.6	ns
t _{PLZ}	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 5	1.7	2.7	5.2	1.7	5.7	ns

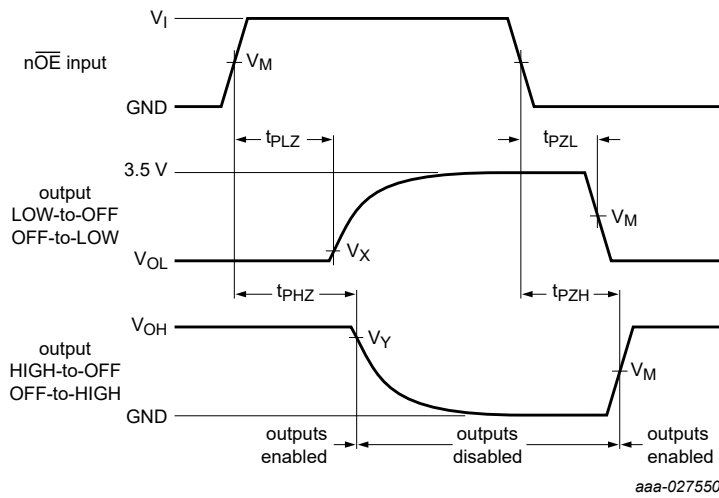
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Input (nAn) to output (nYn) propagation delays



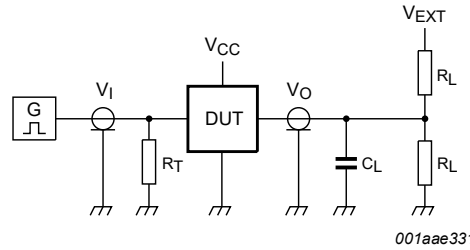
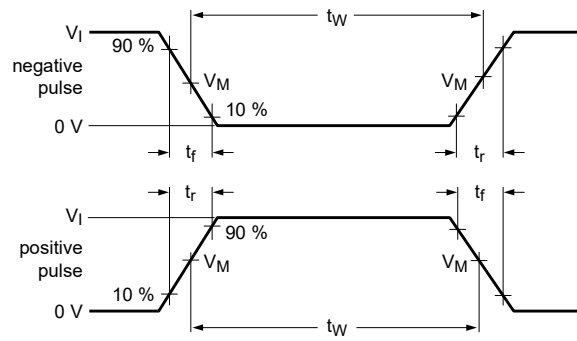
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. 3-state enable and disable propagation delays

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



001aae331

Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = Test voltage for switching times.

Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_w	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	≤ 1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	7 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

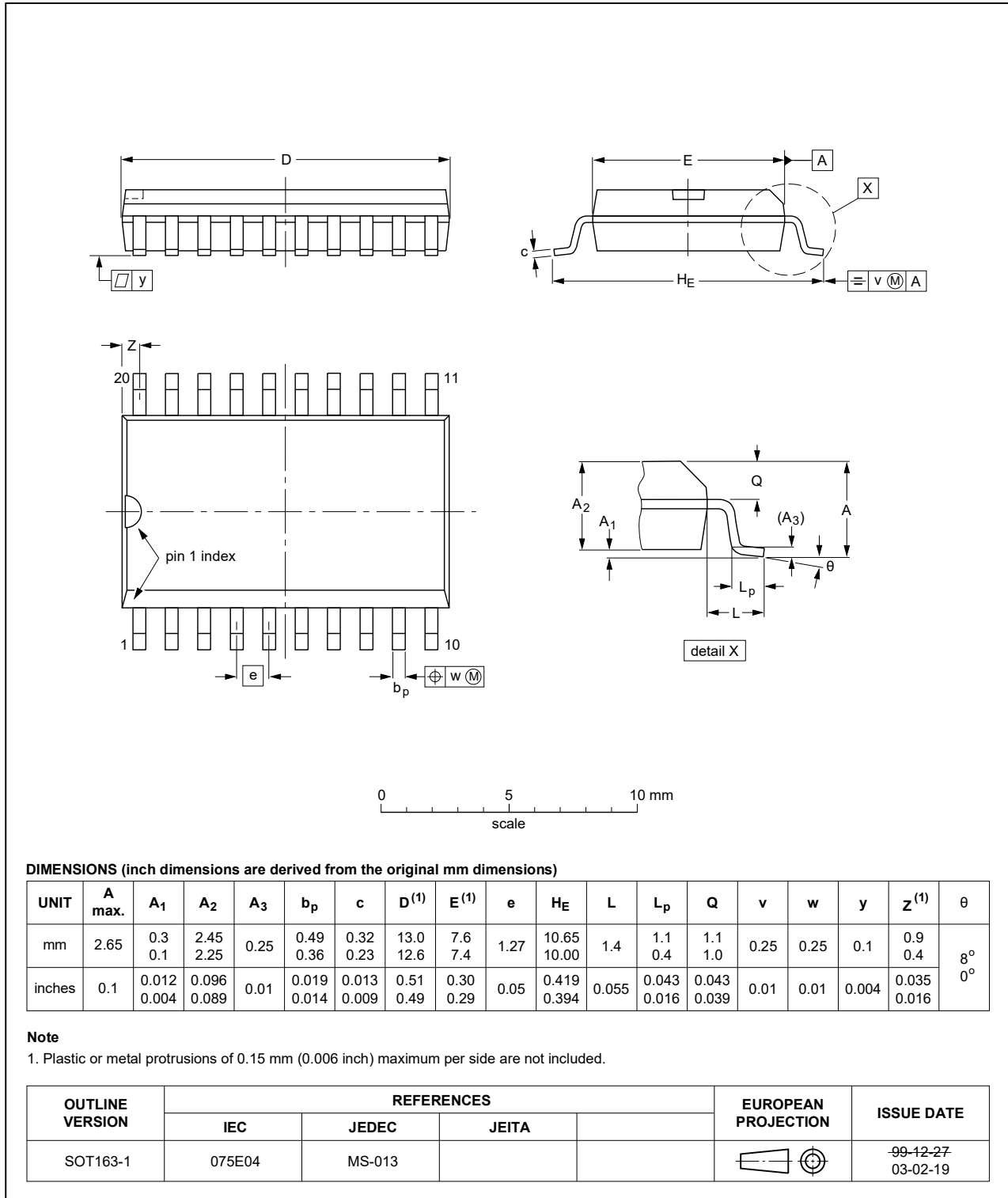


Fig. 7. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

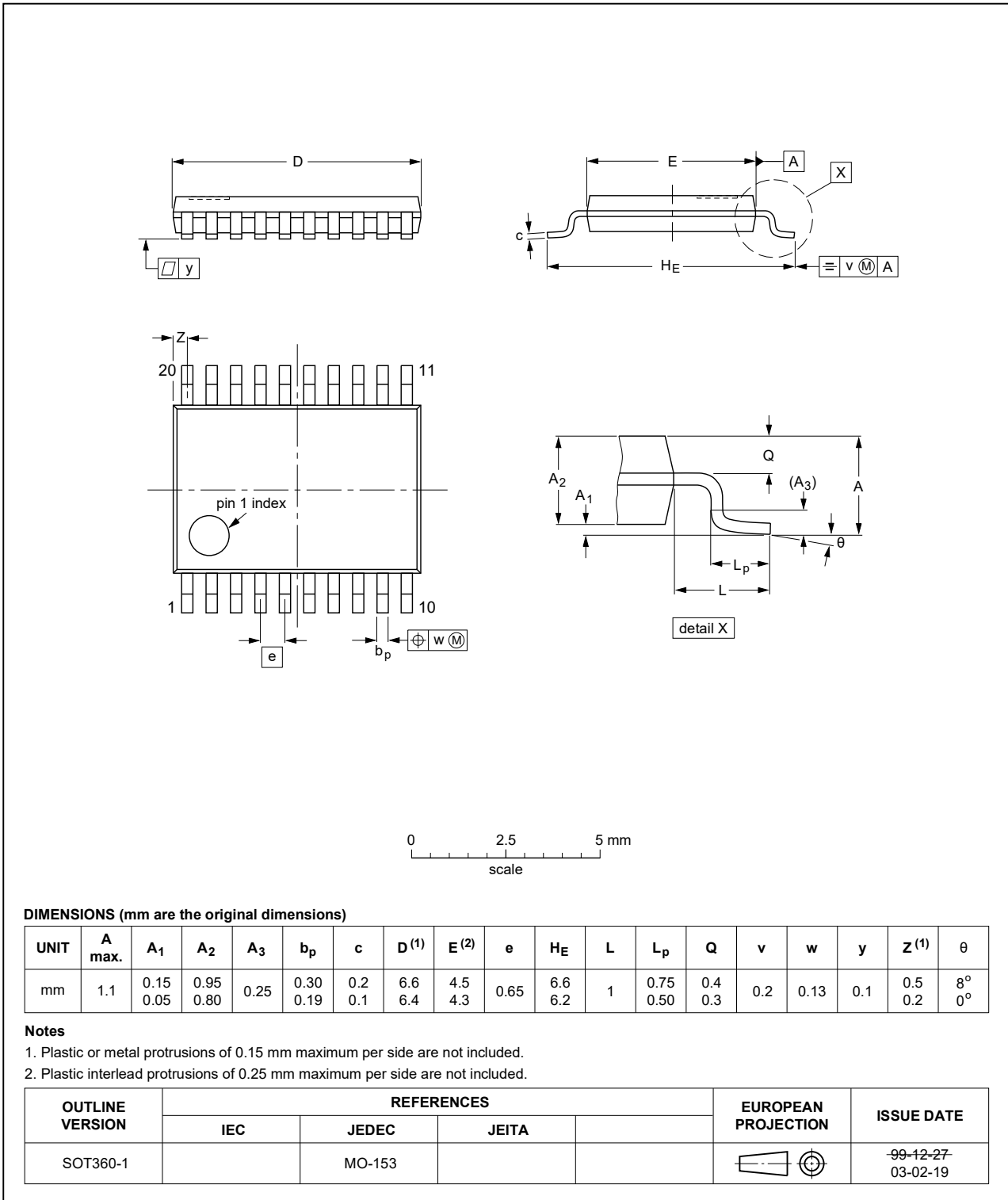


Fig. 8. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT244 v.5	20240624	Product data sheet	-	74ABT244 v.4
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74ABT244 v.4	20210708	Product data sheet	-	74ABT244 v.3
Modifications:	<ul style="list-style-type: none"> Section 1 and Section 2 updated. Type number 74ABT244DB (SOT339-1 / SSOP20) removed. 			
74ABT244 v.3	20171006	Product data sheet	-	74ABT244 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74ABT244N removed from data sheet. 			
74ABT244 v.2	19980116	Product specification	-	74ABT244 v.1
74ABT244 v.1	19950906	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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